Safety First

Meeting room locations

Welcome

HOUSEKEEPING ITEMS

- Lots of Information to share!

- Visit CHIPS.gov

  - Get the Notice of Funding Opportunity

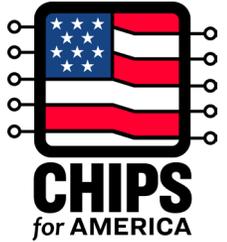 - Access additional resources for applicants and stakeholders: Frequently Asked Questions: CHIPS Manufacturing USA Institute Funding Opportunity | NIST is a living document

CHIPS for America QR Code:
CHIPS Manufacturing USA institute NOFO (full text)

Slido

You can change rooms any time using this dropdown menu

Toggle between functions, as needed

Scan the QR code or go to slido.com and enter code MFGUSA

Proposers Day Expectations
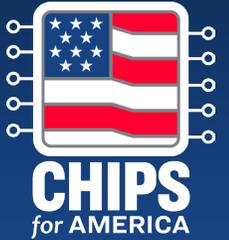
Agenda

- CHIPS Manufacturing USA
- Overview of Digital Twin Institute NOFO
- CHIPS R&D Policy Overview
- Grants Management Division
- Answers to Questions
- Natcast
- Manufacturing USA Network
- Interagency Panel
- Breakouts – Networking and Team Building
- Wrap Up

By the end, attendees should better understand:

- CHIPS Manufacturing USA Institute Description
- Requirements and stages/phases of the application process
- How to apply to the NOFO
- Prospective partnership opportunities

Morning Agenda (AM ET)
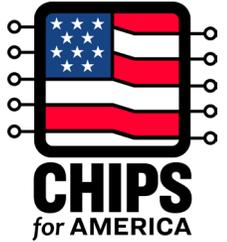
Time	Session	Speaker
8:30AM – **8:35**AM	Welcome	Under Secretary **Laurie Locascio**
8:35AM – **8:45**AM	Expectations for Day	**Mike McKittrick** Deputy Director, CHIPS Manufacturing USA
8:45AM – **9:40** AM	CHIPS Manufacturing USA institute NOFO Overview	**Eric Forsythe** Director, Manufacturing USA **Mike McKittrick** Deputy Director, CHIPS Manufacturing USA
9:40AM – **10:05**AM	Networking/Break	
10:05AM – **10:50**AM	CHIPS R&D Office Policy Overview	**Richard-Duane Chambers** Director of Policy and Integration **Greg Strouse** NIST Safeguarding Science Research Security Director
10:50AM – **11:00**AM	Ready, Set, Submit! Application, Preparation, and Submission	**Blase Etzel** Other Transaction Agreement Officer
11:00AM – **11:45**AM	Question and Answer Panel	**Moderator:** Christie Canaria **Panel:** Eric Forsythe, Richard-Duane Chambers, Greg Strouse, Mike McKittrick
11:45AM – **12:00**PM	Natcast Update	**Susan Feindt** Senior Vice President of Ecosystem Development, Natcast

Afternoon Agenda (PM ET)
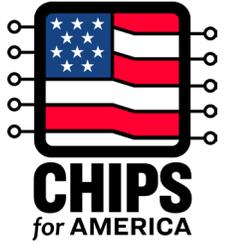
Time	Session	Speaker
12:00PM – **1:00**PM	Lunch (on own)	
1:00PM – **1:15**PM	Manufacturing USA Network	**Mojdeh Bahar** Associate Director, Innovation and Industry Services, NIST
1:15PM – **2:00**PM	Interagency Panel	**Moderator: Christie Canaria** Senior Policy Advisor, CHIPS R&D
2:00PM – **2:15**PM	Instructions/Move to Breakouts	**Mike McKittrick** Deputy Director, CHIPS Manufacturing USA
2:15PM – **4:25**PM	Breakout Sessions	*Networking*
4:25PM – **4:30**PM	Return to Plaza Ballroom	
4:30PM – **5:00**PM	Wrap Up	**Eric Forsythe** Director, CHIPS Manufacturing USA
5:00PM	Adjourn	

Disclaimers
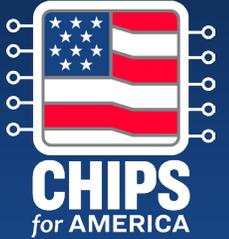
The Notice of Funding Opportunity (NOFO) 2024-NIST-CHIPS-MFGUSA-01 document is the official competition document. The following presentation is only a summary of the NOFO document. Please review the NOFO thoroughly prior to starting the application process. Any apparent or actual conflict between the NOFO and this presentation must be resolved in favor of the NOFO.

NIST cannot critique or provide feedback on any proposal ideas while the notice of funding opportunity is open.

CHIPS Manufacturing USA Program Leadership
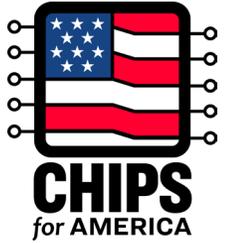
Eric Forsythe, Ph.D
Technical Director
CHIPS Manufacturing USA

Mike McKittrick, Ph.D
Deputy Director
CHIPS Manufacturing USA

Christie Canaria, Ph.D
Senior Advisor
CHIPS RD Office
Detail to Manufacturing USA

Office of Advanced Manufacturing CHIPS MFG USA Team
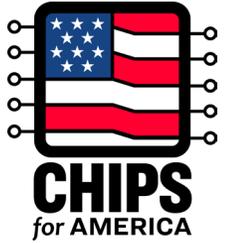
Mike Molnar
Director, OAM

Kelley Rogers
Division Chief, Program Operations

Robert Rudnitsky
Division Chief, Strategy and Planning

Zara Brunner
Division Chief, Partnerships & Outreach

Mahesh Mani
Competition & Technical PM

Cheryl Leonard
Competition Support

Susan Ipri-Brown
Strategic Partnerships

Nancy Stoffel
Strategic Initiatives

Shelly Pollard
Comms Specialist

Erin Rushing
Events and Outreach

Competition and Program Operations

CHIPS Program Alignment

Communications and Outreach

CHIPS R&D Programs

CHIPS Metrology Program
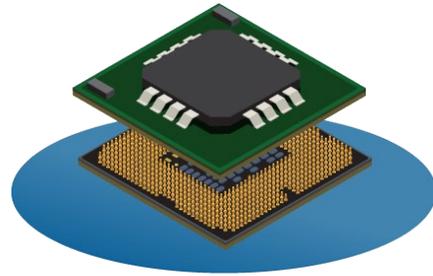
CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast is an independent nonprofit organization and operator of the NSTC consortium
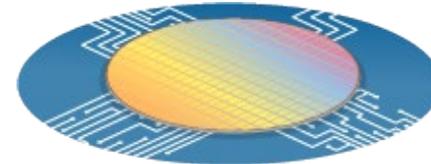
CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

CHIPS Manufacturing USA Program

Workforce Initiatives

What is a digital twin?

- A **virtual** representation or model that serves as the real-time digital counterpart of a physical object or process.
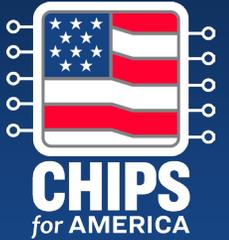
- *Benefits*
  - Innovate faster and at less expense
  - Access feasible for small and medium businesses
  - Shorten process design and validation times
  - Enhance training modalities
  - Improve facility performance

- *Challenges*
  - *Fragmentation* – Being able to produce and access the **data** needed to validate digital twins and power machine learning and AI tools
  - *Lack of Trust* – Strategic industry **collaboration**, which requires a neutral convener to build trust and bring together all parties to share the risks and rewards of working across boundaries
  - *High Barrier to Entry* – Significant **financial investment**, which is out of reach for small and medium-sized manufacturers to do themselves

Digital twin

AI analytics + decision making

Synchronization

Real-world object

Semiconductor Manufacturing Process Flow

Deposition	Inspection	Photoresist	Lithograph	Etch	Advanced Packaging
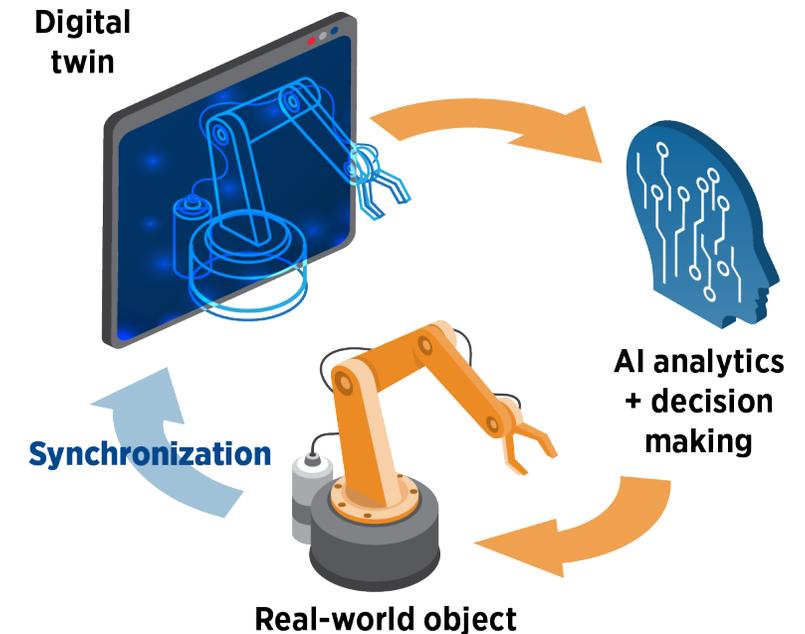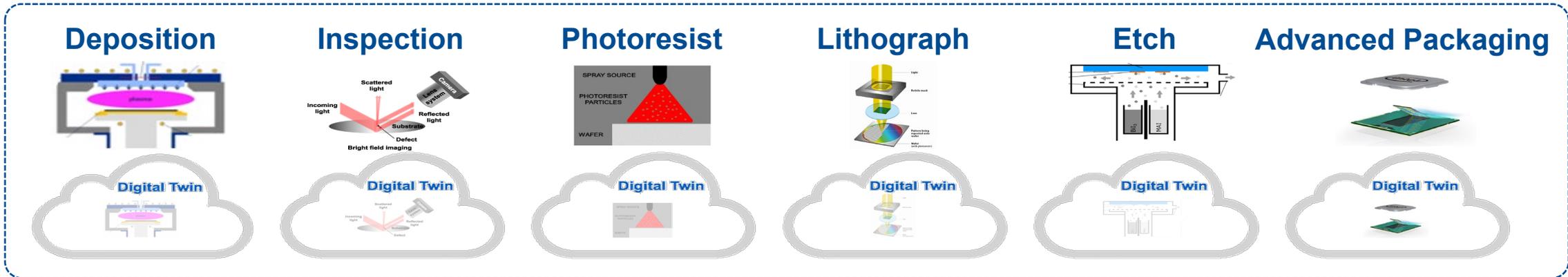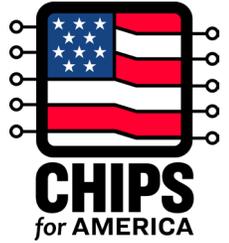
Complex Manufacturing

- Co-design: function, process, materials, tools
- 1000+ process steps
- 70+ masks
- Hundreds of materials
- Hundreds of different tools
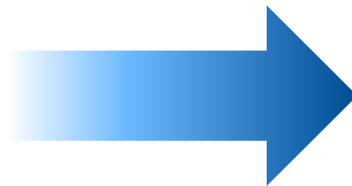
Digital twin:

- Enables collaborative development across the country, creating new opportunities for participation.
- Speeding innovation in new materials, tools, processes.
- Leverage emerging A.I. technology to help accelerate the innovation in manufacturing and co-optimization.
- Significantly reduce costs by improving capacity planning, production optimization.

Operational Areas
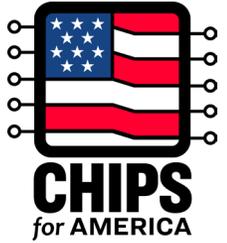
OA1
Institute Operations

OA2
Shared Capabilities

OA3
Industry Solutions

OA4
Workforce Training
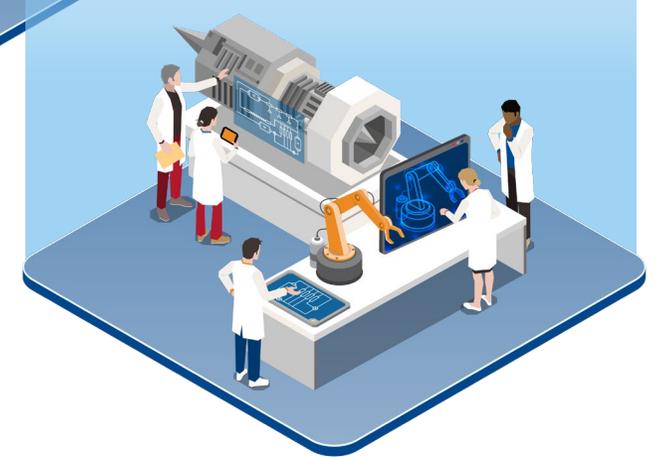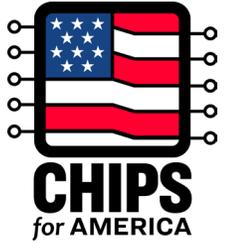
Collaboration is Critical for Success

Active Participation from a wide-range of organizations

Network of Manufacturing USA Institutes

CHIPS R&D Programs

Relevant Federally funded efforts

We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the CHIPS Manufacturing USA Institute

Collaboration CHIPS RD Programs
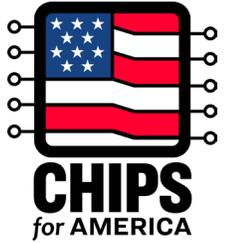
CHIPS National Semiconductor Technology Center (NSTC) Program
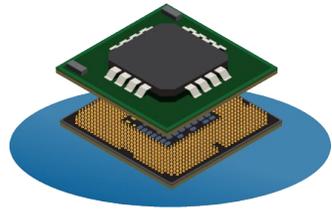
CHIPS National Advanced Packaging Manufacturing Program (NAPMP)
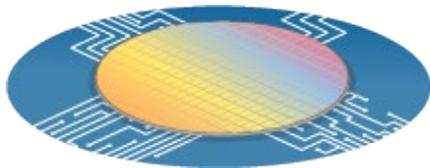
CHIPS Metrology Program

Visit the link for Grand Challenges

https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

Learn about METIS!

The Metrology Exchange to Innovate in Semiconductors, or METIS, is a data exchange ecosystem developed by NIST that will give stakeholders access to the CHIPS Metrology.

CHIPS R&D
Digital Twin Technical Standards Workshop

December 14–15, 2023
NIST National Cybersecurity Center of Excellence (NCCoE)

CHIPS R&D
Digital Twin Data Interoperability Standards Workshop

April 4–5, 2024
NIST National Cybersecurity Center of Excellence (NCCoE)

https://www.nist.gov/news-events/events/chips-rd-digital-twin-data-interoperability-standards-workshop
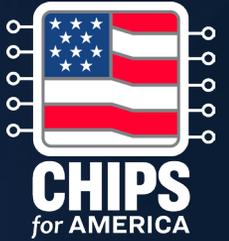
CHIPS for America Manufacturing USA Institute Notice of Funding Opportunity

CHIPS Manufacturing USA: Digital Twin Institute
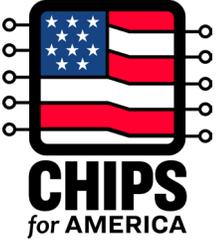
Vision

Enable seamless integration of digital twin models into the U.S. semiconductor manufacturing, advanced packaging, assembly, and test industry, enabling the rapid development and adoption of innovations and enhancing domestic competitiveness for decades.

Mission

The CHIPS Manufacturing USA Institute will foster a collaborative environment within the domestic semiconductor industry, enabled by shared facilities; support industry-led solutions through funded research projects; accelerate technology towards commercialization through significant co-investment; and enable digital-twin workforce training.

CHIPS Manufacturing USA Institute Objectives
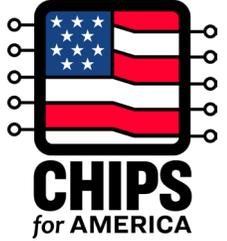
Convene stakeholders across the semiconductor production ecosystem

Improve the state of the art in manufacturing-relevant digital twins

Significantly reduce cost for U.S. chip development and manufacturing

Improve development cycle times of semiconductor product innovation

Advance digital twin-enabled curricula for training a domestic semiconductor workforce

Create a digital twin marketplace for industry to access digital models

Program Scope
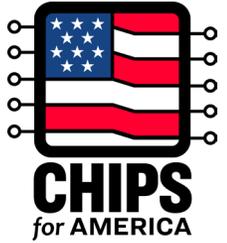
Institute-level targets

Applicants must propose specific Institute-level technical targets, representing significant improvements over the current state of the art for semiconductor-industry digital twins and real-world semiconductor manufacturing.

- Technical targets
- Non-technical targets

Operational Areas

Consistent with the mission and objectives, responsive applications to this NOFO must address each (of the 4) Operational Area (OA)

Activities

The applicant will develop activities for each operational area that will lead to the institute level targets.
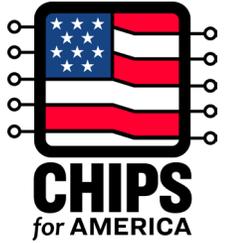
Example Institute-level targets

A substantial decrease in the time required to develop a specific new capability (e.g., a material, process, or tool) for semiconductor manufacturing, within two years of award.

A specific increase in the accuracy of a short loop of digital twins, leveraging artificial intelligence, within two years of award.

Establishing a production-representative digital twin of an end-to-end flow between semiconductor fabrication and advanced packaging, consisting of multiple interoperable digital twins validated with a pre-determined test vehicle, within five years of award.

Demonstrate applicability of one digital twin to another end-to-end flow, leveraging standards, within five years of award.

Achieving cost-share and co-investment commitments of more than three times the level of Federal investment, within two years of award.

Enabling the hiring or reskilling of a specific number of semiconductor industry workers, via EWD projects focused on credentialing, within the five-year Institute period of performance.

Applications are asked to propose Institute-level targets – these are provided as examples

CHIPS MFG USA – Approach
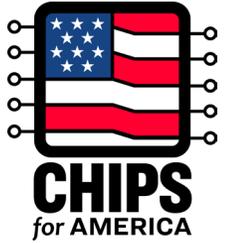
CHIPS R&D will invest up to $285M in Federal funds into four operational areas

	Phase 1. Stand up	Phase 2. Initial Performance	Phase 3: Advanced Performance	Phase 4: Transition Planning
5-yr Timeline	6 – 18 mos	6 – 18 mos	6 – 18 mos	6 – 18 mos
OA 1: Institute Operations	Establishing an Institute management and governance strategy, to include plans for outreach to a broad group of potential members			
OA 2: Shared Capabilities	Operating or providing member access to physical and virtual facilities, as appropriate.			
OA 3: Industry Solutions	Developing and supporting an Institute-funded portfolio of projects, to either improve the capabilities of digital twins or to impact real-world operations.			
OA 4: Workforce Training	Projects to either train the workforce to use digital twins or to leverage digital twin technology to deliver EWD services to diverse audiences of trainees.			
Milestones	• Stand up institute • Enroll members; build partnerships • Establish Shared Capabilities • Release project call(s)	• Demonstrate <u>major</u> manufacturing advances with digital twins • Refined policies and plans • Release project call(s) • Make project awards	• Increase performance with Digital Twin Backbone • Refined policies and plans • Release project call(s) • Make project awards	• Submit final reports • Increase performance with Digital Twin Backbone • Close out final project awards

(Commercial Scale-Up)

▲ OA 1 Milestones   ▲ OA 2 Milestones   ▲ OA 3 Milestones   ▲ OA 4 Milestones   ★ Program Go/No-go decision

What might constitute non-Federal investment?

Member Dues	Tools/Equipment on loan	State matching
Software licenses	Staff time	State facilities
Facility access	Materials	Philanthropy / Foundations
Data	Supplies	Follow-on funds (MRL 7 – 9)
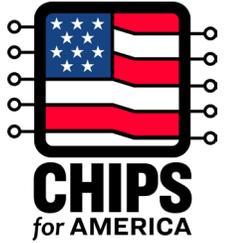
3.2 Cost Share Requirements

Highlight

- Non-federal cost share is required to at least equal the total amount of Federal funding over the lifetime of the award. CHIPS R&D will favorably consider applications with a well-supported ratio of at least 1:1 (cost share : federal funds).

- The cost share may include cash, services, contributions or donations of equipment or other property for use in the project, and third-party in-kind contributions, similar to those described at 2 C.F.R. § 200.306.

- The applicant may propose different types of cost share for evaluation other than those described at 2 C.F.R. § 200.306, provided the proposed cost share is allocable and necessary for the success of the project.

- Subrecipient cost share may be determined using Generally Acceptable Accounting Principles (GAAP).

Applicants should familiarize themselves thoroughly with the cost share requirements within the NOFO 2024-NIST-CHIPS-MFGUSA-01, Section 3

Manufacturing Readiness Levels Acceleration to Commercialization

Funding/Investment

High

Low

Co-investments

CHIPS Institute

Early-stage R&D

Manufacturing-Innovation Process

| Basic manufacturing research | Proof of concept | Production in laboratory | Capacity to produce prototype | Capacity in production environment | Demonstration of production rates |

A key goal of the CHIPS Manufacturing USA Institute is to have a significant impact on the semiconductor industry.

- Applicants should provide commitments from members to advance potential innovations from projects to higher MRLs.

- These commitments may involve late-stage technology development to commercialize digital twins or the application of digital twins to semiconductor manufacturing.

- Examples of co-investments may include those required to enable the scale-up, commercialization, and transition to domestic production of Institute-funded innovations.

Cost share and Optional co-investment

	Cost share (Section 3.2)	Optional Co-investment (Section 1.8)
Required/ Optional	Required – at least equal to the amount of the federal funds. Included in award budget.	Optional.
Description	Statutory requirement. Portion of the Institute costs not borne by the Federal Government.	Commitments by Institute members to transition Institute innovations to scale-up, commercialization and domestic production.
Evaluation	As part of Project Management, Resources, Budget criteria; • The extent to which the proposed non-Federal cost share provided to the Institute is rational in magnitude and nature, from specific known and anticipated sources, and will exceed the statutory requirement for the proposed Institute; • whether total support from non-Federal sources promotes a stable and sustainable business model for the Institute without the need for long-term Federal funding.	As part of Project Management, Resources, Budget criteria; • The extent to which the proposed non-Federal co-investment is rational in magnitude and nature, from specific known and anticipated sources, and will provide for significant investments into developing domestic digital twins or applying digital-twin innovations to the real world; • whether total support from non-Federal sources promotes a stable and sustainable business model for the Institute without the need for long-term Federal funding.
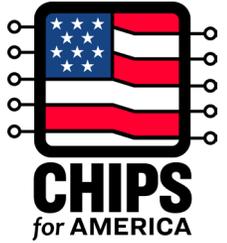
1.7 Broader Impacts

Commitment and Support to future investment in R&D Programs

- CHIPS R&D is committed to building strong communities that share in the prosperity of the semiconductor industry, as well as ensuring that taxpayer investments maximize benefits for the U.S. economy.

- CHIPS R&D also strongly supports inclusion, diversity, equity, and access, and firmly believes that the semiconductor industry cannot succeed unless all Americans have an equal opportunity to fully participate, including individuals from underserved communities.

- CHIPS R&D understands that semiconductor companies can reduce their environmental impact, improve the potential for domestic manufacturing, and further their competitive advantage by helping their customers meet environmental goals.

In its evaluation and selection processes, CHIPS R&D will consider how proposed Institutes will create broader impacts – see Section 1.7 for the full description.
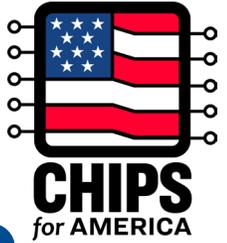
Eligibility

Eligible Applicants

- Non-profit organizations, Accredited institutions of higher education; State, local, and Tribal governments; and for-profit organizations that are domestic entities.

- Domestic entity is one incorporated within the United States (including U.S. territories) with its principal place of business in the United States (including U.S. territories).

Eligible Participants

- Organizations executing existing MFG USA institutes

- FFRDC as subrecipients or contractors with additional justifications

- Federal Entities as Subrecipients or contractors to extent allowed by law.

- Foreign organizations as members of project team, subrecipients or contractors, subject to CHIPS R&D review and approval

Additional Requirements

- Eligible Applicants may only submit one concept paper under this NOFO

- Entities may be included as subrecipients on multiple concept papers and applications

Applicants should familiarize themselves thoroughly with the eligibility requirements within the NOFO 2024-NIST-CHIPS-MFGUSA-01, Section 3
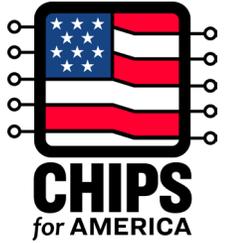
4.9 Funding Restrictions

Highlight

- Construction activities are not an allowable cost under this program. However, costs related to internal modifications of existing buildings that would be necessary to carry out the proposed research tasks may be allowed, at NIST discretion.

- In addition, recipients and subrecipients may not charge profits, fees, or other increments above cost to an award issued pursuant to this NOFO

CHIPS Manufacturing USA Application Process

| | 1 | Concept Paper | | 2 | Concept Paper Review | | 3 | Invited Full Application | | 4 | Full Application Review |
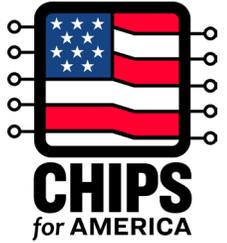
- Mandatory Concept Papers are due June 20, 2024.

- Following concept paper evaluation, applicants will be invited to submit full applications, which are due September 9, 2024.

  - CHIPS R&D may publicly release successful concept paper applicant names to facilitate re-teaming.

- Full applications will undergo evaluation.

4.5 Concept Paper Requirements
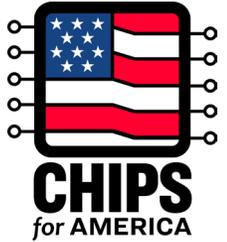
Key Forms and Documents	Brief Description
Executive Summary	Executive Summary is a two-page summary/abstract suitable for dissemination to the public. It should be a self-contained document that broadly describes Institute team, objectives, impacts, and education/workforce goals.
Concept Paper Narrative	A 20-page document that includes an Institute Impact Statement, Institute Management and Governance Strategy, and an Institute Investment Strategy containing an Education and Workforce Development Plan, Market Transformation Plan, and Shared Capabilities Infrastructure Plan.
Other	Table of Funded Participants and Unfunded Collaborators, Table of Required Cost Share and Optional Co-investment, Letters of Commitment.

Submission of concept papers is through grants.gov.
Applicants and recipients must have an active registration in SAM.gov.
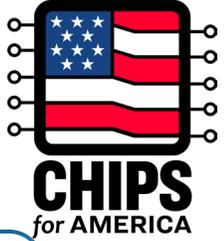
Concept Paper Evaluation Criteria

1 · **Relevance to Economic and National Security**
- This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals, as expressed in Section 1.1.1.

2 · **Project Management, Resources, and Budget**
- This criterion addresses the reasonableness, appropriateness, and cost-effectiveness of the proposed budget, management strategy, and resources, relative to the work and objectives of the CHIPS Manufacturing USA Program.

3 · **Overall Scientific and Technical Merit**
- This criterion addresses the quality, innovativeness, and feasibility of the Concept Paper Narrative and the potential for meeting the mission and objectives of the CHIPS Manufacturing USA Program, as expressed in Section 1.1.3.2.

4 · **Transition and Impact Strategy**
- This criterion addresses the project's potential for supporting the commercialization and domestic production of funded innovations, as well as beneficial impacts to the broader domestic research, development, and innovation ecosystem.

5 · **Education and Workforce Development**
- Concept papers will be evaluated for the quality, completeness, rationality, and feasibility of the proposed Institute's EWD models and plans.
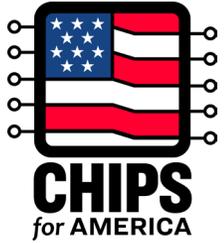
Concept Paper Review Process

1   **Initial Review**

- Concept papers and full applications received by the respective deadlines will be reviewed to determine eligibility, completeness, and responsiveness to this NOFO and stated program objectives.

2   **Review of Concept Papers**

- Merit Review, Evaluation Panel, Adjectival Rating.

3   **Selection of Successful Concept Papers**

- Selection of Successful Concept Papers and Invitations to Submit Full Applications.

Review of the concept papers, selection, and notification to applicants is expected to be complete on or about July 18, 2024.
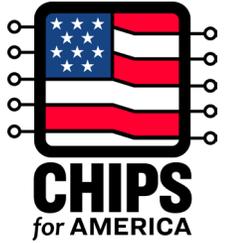
Full Applications

See Section 4.6 for the Full Requirements

- SF-424 (R&R), Research & Related Budget
- Institute Narrative
  - No more than 90 pages - note which elements count toward the page limit
- Table of Funded Participants and Unfunded Collaborators
- Table of Required Cost share and Optional Co-investments
- Budget Narrative
- Letters of Commitment and Interest

This is an abbreviated list of requirements.

*Applicants invited after concept paper stage will receive email instructions for submission of the full application. **Submission of full applications is through grants.gov. Applicants and recipients must have an active registration in SAM.gov.***
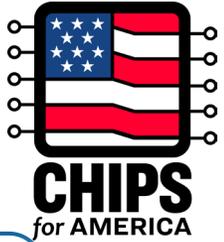
Full Application Evaluation Criteria

1	**Relevance to Economic and National Security**	• This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals, as expressed in Section 1.1.1.
2	**Project Management, Resources, and Budget**	• This criterion addresses the reasonableness, appropriateness, and cost-effectiveness of the proposed budget, management strategy, and resources, relative to the work and objectives of the CHIPS Manufacturing USA Program.
3	**Overall Scientific and Technical Merit**	• This criterion addresses the quality, innovativeness, and feasibility of the Institute Narrative and the potential for meeting the mission and objectives of the CHIPS Manufacturing USA Program, as expressed in Section 1.1.3.2.
4	**Transition and Impact Strategy**	• This criterion addresses the project's potential for supporting the commercialization and domestic production of funded innovations, as well as beneficial impacts to the broader domestic research, development, and innovation ecosystem.
5	**Education and Workforce Development**	• Concept papers will be evaluated for the quality, completeness, rationality, and feasibility of the proposed Institute's EWD models and plans.
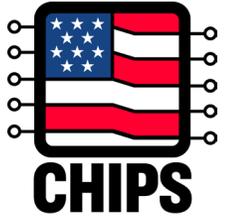
Full Application Review Process

1	**Merit Review**	• At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate professional and technical expertise relating to the topics covered in this NOFO.
2	**Evaluation Panel**	• Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate technical expertise will conduct a panel review of the ranked applications.
3	**Pre-Selection Interviews and Site Visits**	• At CHIPS R&D's discretion, applicants may be requested to participate in Pre-Selection Interviews and/or Site Visits during the evaluation panel phase, either at CHIPS R&D, the applicant's site, or a mutually agreed upon location, or via conference call or webinar.
4	**Adjectival Rating**	• The evaluation panel will provide a final adjectival rating and written evaluation of each full application to the Selecting Official for further deliberation.
5	**Selection and Federal Awarding Agency Review of Risk Posed by Applicants**	• The Selecting Official will make final award recommendations. NIST will also conduct the research security review described in Section 2.8.6 and the results will be provided to the Selecting Official.

Key Dates

May 6, 2024

Digital Twin Institute Funding Opportunity (Released)

To establish and operate a CHIPS Manufacturing USA Institute focused on digital twins to tackle important semiconductor-industry manufacturing challenges.

May 16, 2024

Proposers Day

Share detailed information on the NOFO, in a collaborative atmosphere

Due: June 20, 2024

Concept Papers Review

Mandatory concept papers submitted by teams

Teams invited to submit full application

September 9, 2024

Full Application Due

The full application from applicants due

CHIPS for America QR Code:
CHIPS Manufacturing USA institute NOFO (full text)

Networking / Break
9:45 – 10:05 AM
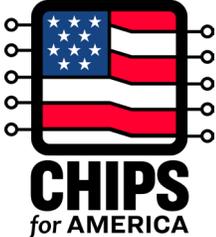
SCAN THE QR CODE AND SUBMIT A QUESTION TO SLIDO

Policy and Integration Speakers
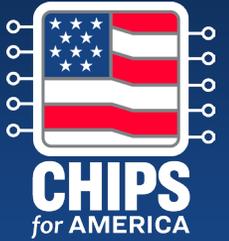
Richard-Duane Chambers
Director, Policy and Integration
CHIPS R&D Office

Greg Strouse
NIST Safeguarding Science
Research Security Director
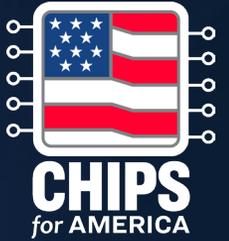
Policy Overview Agenda & Objectives
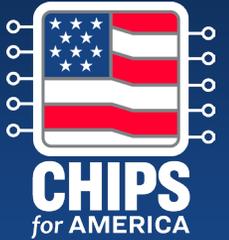
Agenda

- Unique Directives Informing Work

- Overview of CHIPS R&D Office Goals

- International Collaboration

- Key Requirements:

  - Domestic Control of Intellectual Property

  - Domestic Production

  - Research Security

By the end, attendees should better understand

- CHIPS R&D objectives and policy context

- CHIPS R&D domestic and international research requirements

- Key requirements for proposals

Policy and National Security Context
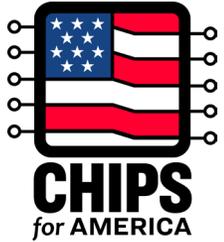
Unique or Emerging Directives

CHIPS and Science Act (2022)

- Prohibit malign foreign talent recruitment programs
- Research security training

CHIPS Act (2021)

- Domestic production requirements
- Domestic control requirements to protect intellectual property from foreign adversaries

National Security Policy Memorandum 33 (2021)

- Research security program requirements
- Disclosure of conflicts of interest / commitment
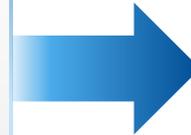
Application Requirements

- **Domestic research and development requirements**
- **Domestic control and Intellectual Property Rights Management Plan**
- **Market Transition Plan**
- **Research Security Plan**
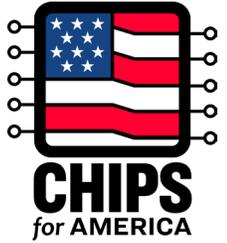
Overview of CHIPS R&D Office Goals

Vision

A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce, and leads the world in semiconductor research and innovation.

Mission

Accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic tools, resources, workers, and facilities.

2030 Goals

- **U.S. Technology Leadership:** The United States establishes the capacity to invent, develop, prototype, manufacture, and deploy the foundational semiconductor technologies of the future.
- **Accelerated Ideas to Market:** The best ideas achieve commercial scale as quickly and cost effectively as possible.
- **Robust Semiconductor Workforce:** Inventors, designers, researchers, developers, engineers, technicians, and staff sustainably meet evolving domestic government and commercial sector needs.
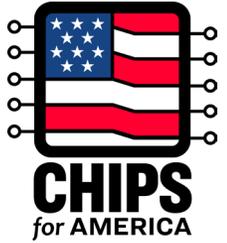
Domestic Control of Intellectual Property

> *15 U.S.C. 4656(g): "The head of any executive agency receiving funding under this section shall develop policies to require domestic production, to the extent possible, for any intellectual property (IP) resulting from microelectronics research and development conducted as a result of such funding and domestic control requirements to protect any such intellectual property from foreign adversaries."*

Key Requirements

- At least one domestic entity must own or co-own any IP from the funded R&D and must have full rights to enforce the applicable IP for a period of years determined prior to the final award.

- The domestic entity must notify NIST before selling, transferring, or assigning ownership of the IP to another entity.

- IP from the funded R&D cannot be sold, transferred, or assigned to a foreign adversary, to include FEOCs and foreign countries of concern. IP cannot be licensed (except in certain limited circumstances) to a foreign adversary.

IP Rights Management Considerations

- Describe:
  - Plans for Institute Member access to IP
  - **Existing or planned protocols to ensure domestic control and domestic production of the IP**
  - Any additional licensing provisions to protect IP rights

?
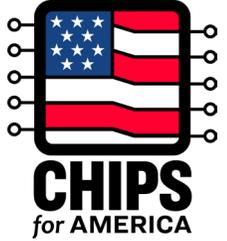
What is a foreign entity of concern?

Foreign entities of concern include entities owned by, controlled by, or subject to the jurisdiction or direction of the governments listed in 10 U.S.C 4872(d): China, Russia, North Korea, or Iran.

An entity is owned by, controlled by, or subject to the jurisdiction or direction of a government of a foreign country where:
(i) The entity is: a citizen, national, or resident of a foreign country listed in 10 U.S.C. 4872(d); and located in a foreign country listed in 10 U.S.C. 4872(d);
(ii) The entity is organized under the laws of or has its principal place of business in a foreign country listed in 10 U.S.C. 4872(d);
(iii) 25 percent or more of the entity's outstanding voting interest, board seats, or equity interest is held directly or indirectly by the government of a foreign country listed in 10 U.S.C. 4872(d); or
(iv) 25 percent or more of the entity's outstanding voting interest, board seats, or equity interest is held directly or indirectly by any combination of the persons who fall within subsections (i)–(iii).

Domestic & Int'l Research Requirements
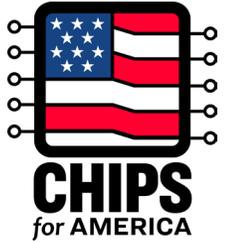
> *"NIST adheres to the principle that U.S. research leadership benefits from mutually beneficial international collaborations, including welcoming international scientists"*

- **The lead entity and funded collaborators on an Institute award application must be domestic entities;** foreign entities, excluding foreign entities of concern (FEOCs), can be unfunded collaborators.

- Foreign-owned entities, excluding FEOCs, can join the Institute as funded subrecipients post-award, subject to approval by CHIPS R&D.

- **Funded R&D activity should occur in the United States** but CHIPS R&D may approve the completion of certain tasks outside the United States.

- **Any disbursement of funds** outside the United States **must be approved by CHIPS R&D.**

Justification for Foreign Participants (excluding FEOCs):

- Foreign partner's involvement is essential to program objectives and doesn't jeopardize the project's pathway to domestic production.

- Applicant and foreign partner have adequate IP and data protection agreements in place.

- Foreign partner agrees to comply with laws and regulations and undergo a national security review.
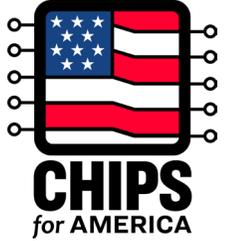
? What is a "domestic entity"? Can foreign entities apply for this award?

A domestic entity is one incorporated within the United States (including U.S. territories) with its principal place of business in the United States (including U.S. territories).

Foreign entities are eligible to join an institute team, a project team, or the membership of the institute, provided that they are not a foreign entity of concern, subject to CHIPS R&D review and approval. **However, foreign-owned or foreign-controlled entities cannot be the applicant entity.**

Note: CHIPS R&D expects funding recipients to exercise appropriate due diligence to determine whether a potential project partner may qualify as a foreign entity of concern or foreign country of concern and therefore be subject to prohibitions on participation.
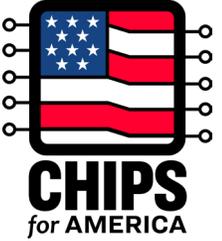
? The NOFO states that at least one domestic entity must own or co-own any IP resulting from R&D conducted under the NOFO and have full rights to enforce applicable IP rights for at least a period of years, to be determined prior to the final award. What is a "period of years"?

CHIPS R&D will determine the "period of years" for which domestic control requirements are in effect on a case-by-case basis.

Institute-level Market Transformation Plan

"Describe how the Institute will support advancing CHIPS-funded technologies towards commercialization and adoption with the goal of strengthening U.S. manufacturing competitiveness."

① **Market Analysis Topics**

② **Customer Analysis Topics**
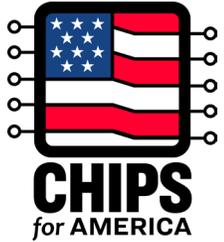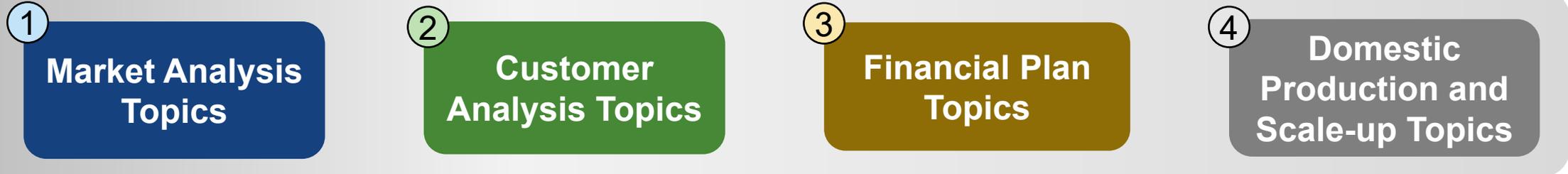
③ **Financial Plan Topics**

④ **Domestic Production and Scale-up Topics**

Key Components:

- **Market Analysis:** A clear description of the value proposition of the proposed technology or product and identification of competitors.

- **Customer Analysis:** An assessment of demand for the funded innovation by current and potential customers or categories of customers, at volumes necessary for commercial viability.

- **Financial Plan:** A realistic and sustainable business model that considers cost, revenue, and access to capital.

- **Consensus Building:** Plans to collaborate (e.g., with standards bodies) to promote technology adoption

Key Point: Plans are intended to be an "initial assessment" or an "overview", with updates occurring across the award period. Applicants should not feel compelled to have all the answers before the research is complete!

Key Point: Project-level Commercial Viability and Domestic Production Plans build on Institute Market Transformation Plans.

Institute-level Market Transformation Plan
(continued)

1 **Market Analysis Topics**	2 **Customer Analysis Topics**	3 **Financial Plan Topics**	④ **Domestic Production and Scale-up Topics**
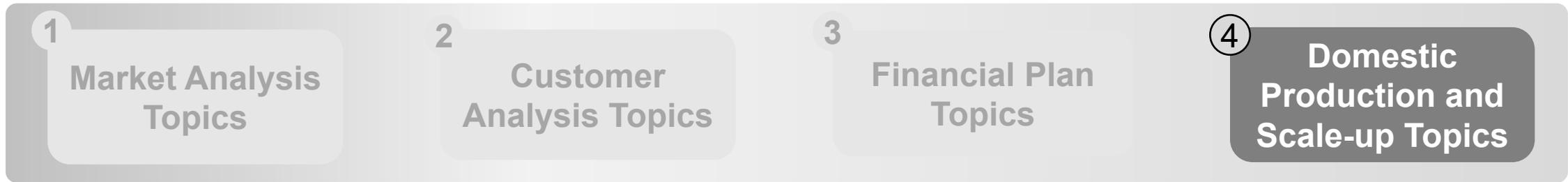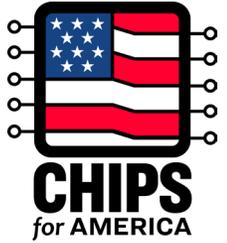
Key Component:

- **Member commitments:** Optional Co-investment to bring potential innovations to higher MRLs, including the commercialization of digital twins or the application of digital twins to semiconductor manufacturing

- **Domestic Production and Scale-up:** A pathway to transition the technology to domestic availability and to produce the technology within the United States

- **Non-Domestic Production:** Where relevant, applicants should explain what elements of production for the funded innovation are not feasible in the United States.

Key Point: Market Transformation Plans and Commercial Viability and Domestic Production plans do not require exclusive domestic production. Applicants are invited to address potential conflicts between domestic production and commercial viability.

Key Point: Applicants can therefore address viability and domestic production separately and update analyses during the award period.

?
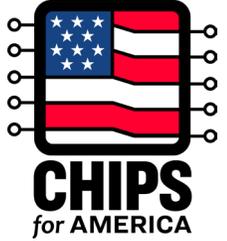
How do the Market Transformation Plan and a Commercial Viability and Domestic Production (CVDP) Plan differ?

CHIPS R&D requires applicants for an award to manage the CHIPS Manufacturing USA Institute to submit a Market Transformation Plan, describing how **the Institute** (including its project calls) will support technology commercialization and adoptions, leading to stronger U.S. manufacturing.

CHIPS R&D will further require applicants for Member-led or Institute-led projects to submit a CVDP Plan, describing how the **individual project** will support a realistic business model for the funded innovations (which may include software), include a technology transition plan, and pathways to benefitting national and economic security, such as through the domestic availability of the technology and successful adoption by commercial or defense partners.

CHIPS R&D has published a **Commercial Viability and Domestic Production Plan Guidebook**, which can inform the development of both Market Transformation Plans and CVDPs.

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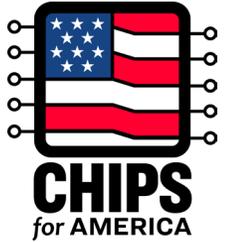
What factors might CHIPS R&D consider when evaluating applications that propose non-domestic production?

CHIPS R&D aims to improve the U.S. capacity to invent, develop, prototype, manufacture, and deploy the foundational semiconductor technologies of the future. However, consistent with 15 U.S.C. 4656(g), CHIPS R&D does not require exclusive domestic production, as this goal may be served by conducting activities overseas.

Where domestic production may not be possible, applicants should identify, as practicable at the time of application, factors driving overseas production, such as (CHIPS Mfg USA NOFO 2.9.1):

- Lack of domestic production capabilities

- Relative cost of domestic vs. foreign production, at relevant production volumes

- Potential economic or national security benefits from having distributed production among U.S. and overseas sites

- Potential risks of U.S.-based production such as market acceptance or changes to the value proposition

- Other factors the applicant deems relevant to the invention's success

Research Security Agenda & Objectives
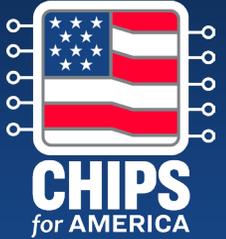
Agenda

- Safeguarding CHIPS Science through Research Security

- NIST IR 8484 – Research Security Framework

- Research Security Plan

- Research Security Reviews of Applications

- Selected FAQs

- Questions and Contact information

By the end, attendees should better understand

- What is Safeguarding Science and Research Security

- What is the NIST Research Security Framework

- What is a research security plan

- How will an application be reviewed

- Answers to the FAQs

- Who to contact regarding research security

Safeguarding CHIPS Research Science
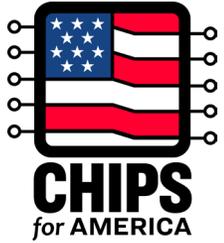
Safeguarding Science
facilitates open science and research security that values collaboration while protecting U.S. national security and economic security interests.

International Science — Research Security

Research Security
is protecting the means, know-how, and products of research until they are ready to be shared.

Risks to U.S. Scientific Research Advantages

- **National Security** – Transfer of research products accelerates foreign military applications
- **Economic Security** – Loss of technical advantages results in the loss of U.S. global market competitiveness
- **Intellectual Property** – Some governments violate core research integrity principles and facilitate the transfer of original ideas from the United States

NIST IR 8484 – Safeguarding International Science Research Security Framework
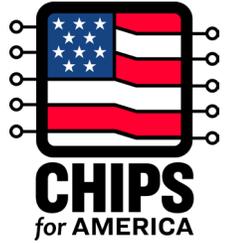
Framework Implementation

- Strikes a balance between scientific research security and fostering international collaboration

- Implements a methodology to review research and make risk balanced determinations

Research Security Program Implementation

- Strategic communication and training

- Composite multi-disciplined open-source analysis

- Risk-balanced determination and mitigation

- User friendly tools, checklists, and templates

NIST Internal Report
NIST IR 8484

Safeguarding International Science
Research Security Framework

Gregory F. Strouse
*Office of the Associate Director for
Laboratory Programs
Laboratory Programs*

Philip A. Bennett
*Research and Technology Protection
Commerce Office of Security*

Timothy R. Wood
*Research Protections Office
Laboratory Programs*

Mary Bedner
*CHIPS Research and Development Program
CHIPS Program Office*

Claire M. Saundry
*International and Academics Affairs Office
Director's Office*

This publication is available free of charge from:
https://doi.org/10.6028/NIST.IR.8484

August 2023

U.S. Department of Commerce
Gina M. Raimondo, Secretary

National Institute of Standards and Technology
Laurie E. Locascio, NIST Director and Under Secretary of Commerce for Standards and Technology

https://doi.org/10.6028/NIST.IR.8484

Research Security Plan: Key Components

"Provide a written plan that describes... internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity for both application team personnel and Institute members for the life of the Institute."

"Provide a point of contact on research security issues within the project leadership team."

Establishing a Research Security Team and Policies	**Scope of Program – Assessing At-risk Technologies and IP**	**Communication and Training Research Personnel and Staff**	**Reviews, Risk Determination and Mitigation**
Reviewing Personnel Appointments	**Reviewing Foreign Travel Requests**	**Reviewing Collaboration and Service Requests**	**Implementing Technology Control (e.g., Data Mgmt and Export Controls)**

Cybersecurity

Research Security Reviews of CHIPS Applications

- **Understanding the research and type**
  - Fundamental or Proprietary
- **Implementation**
  - Open-source analysis by multi-disciplined team
  - Risk Analysis (**RAFT**)
    - **R**ecruitment, **A**ffiliations, **F**unding, and **T**echnology
- **Risk Determination and Mitigation**
  - Does the Benefit Outweigh the Risk?
  - Consensus risk-balanced determination with countermeasures to mitigate levels of anticipated risk
- **Program Maintenance (if awarded)**
  - Recurring Case Review
  - Partnership Oversight

Low Risk Mitigation

- Fundamental Research
- No Foreign Affiliation
- Internal Source Funding
- Expand PI Threat Awareness/ OPSEC Training
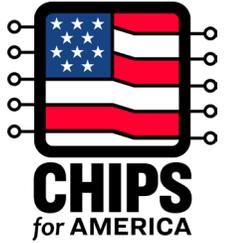
Medium Risk Mitigation

- Application Research
- Previous Foreign Affiliation
- Proximity to Critical Technology
- External Source Funding
- Enhanced Access Control/Disclosure Approval

High Risk Mitigation

- Critical Technology
- Mil/Civ Application
- Existing Foreign Affiliation
- USG/Proprietary Funding
- Program Reassignment or Request Denial
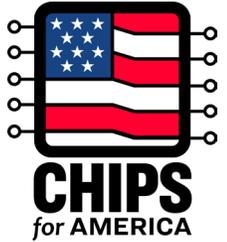
? Will CHIPS R&D provide funding or other resources to establish or improve a research security program or to the meet other CHIPS R&D research security requirements?

- To date, CHIPS R&D has not established any specific programs or set-asides to support the development of a research security program.

- However, limited funding may be available as part of the institute award to implement a Research Security Program, subject to the requirements of the NOFO and the approval of CHIPS R&D.

- For entities selected to receive funding, NIST may provide assistance to establish or improve research security activities consistent with NIST best practices (NIST IR 8484).
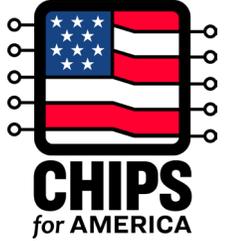
? Do entities applying for CHIPS R&D research funds need to demonstrate that they have a research security program in place before applying for a research award and/or before receiving research funding?

- At present, CHIPS R&D does not require applicants to demonstrate the existence of a research security program to apply for or receive funding.

- However, applicants must provide a written plan (i.e., a research security plan) to establish a Research Security Program, including describing internal processes or procedures for addressing foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity, as applicable.
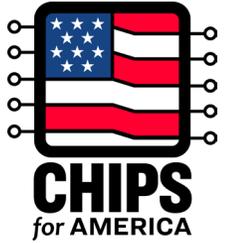
CHIPS Manufacturing USA Institute

Q&A during panel discussion

Contact Information

researchsecurity@nist.gov

NIST Internal Report
NIST IR 8484

Safeguarding International Science

Research Security Framework

Gregory F. Strouse
*Office of the Associate Director for
Laboratory Programs
Laboratory Programs*

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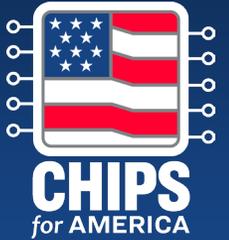
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National Institute of Standards and Technology
Laurie E. Locascio, NIST Director and Under Secretary of Commerce for Standards and Technology

https://doi.org/10.6028/NIST.IR.8484

Grants Management Division Speakers

Blase Etzel
NIST Grants Management

Agenda

PLAN AHEAD TO STAY AHEAD

- SAM.gov Registrations

- Grants.gov Registrations

- Tips for Success

SAM.gov

Link: https://sam.gov/content/home

**Help Desk: Monday - Friday from 8am - 8pm EST U.S. calls: 866-606-8220**

- 100% FREE to register

- Create an active account

- Get a Unique Entity ID

- Register to SAM.gov before Grants.gov

- Start Early: the process takes about 10 days but can take up to 6 weeks!

- Make sure Certifications and Representations are complete

Grants.gov

Link: https://www.grants.gov/applicants/applicant-registration
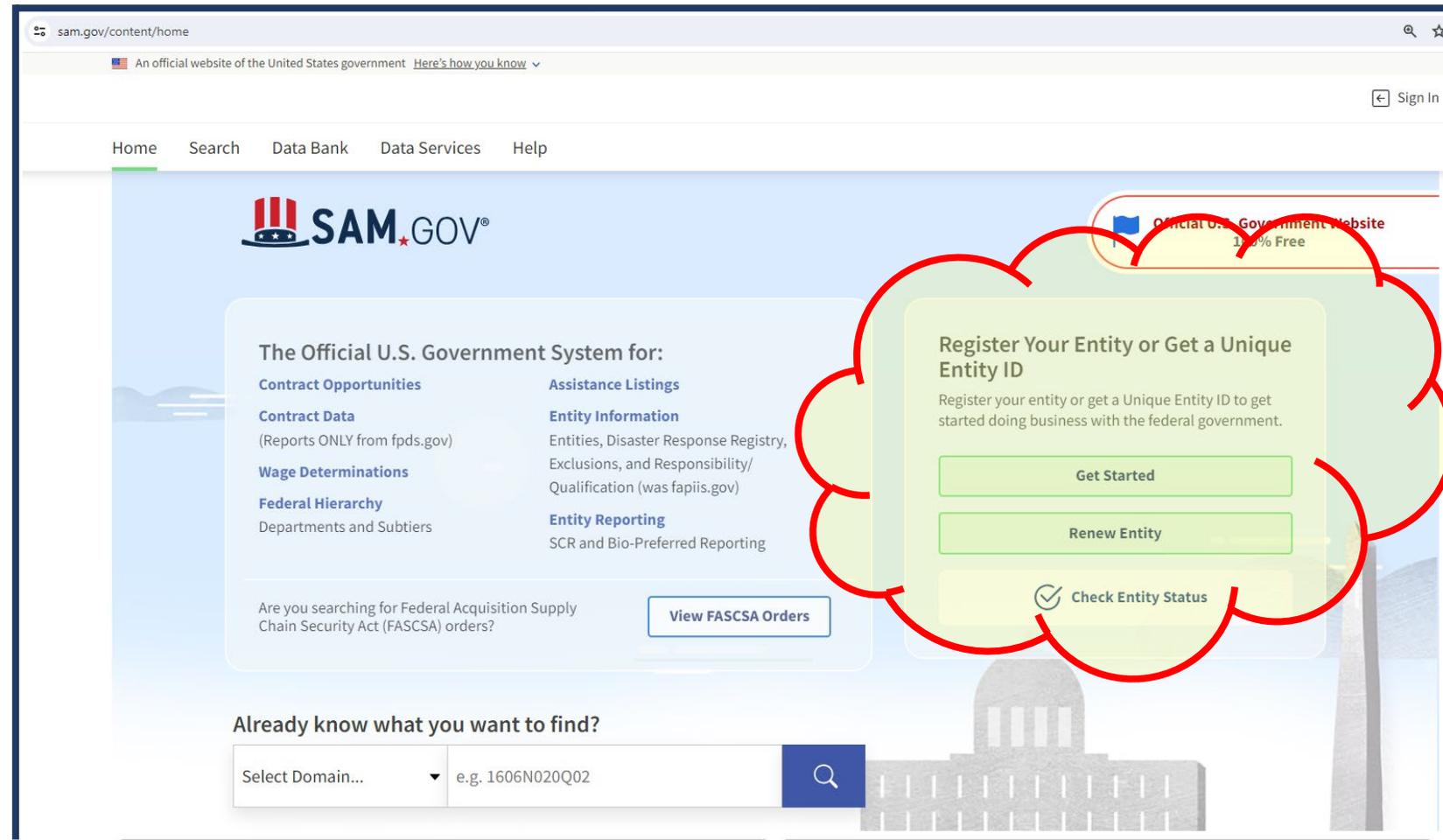
Help Desk: 1-800-518-4726 (24/7 excluding holidays) or support@grants.gov

- 100% FREE to register
- Grants.gov will be used for full applications only
- See NOFO for Concept Paper submission process
- User Guide
- Applicant FAQs

Grants.gov *(continued)*
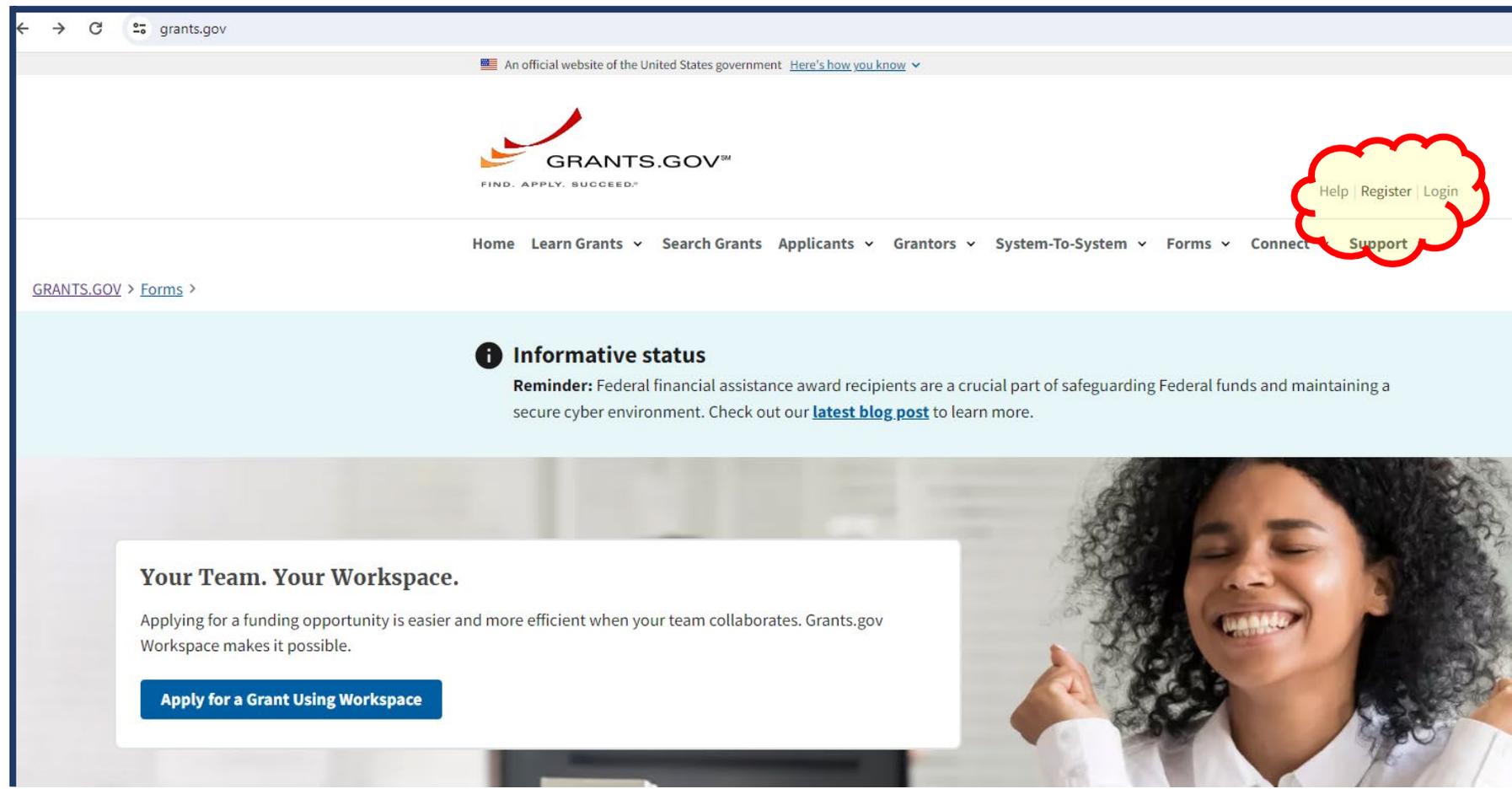
After obtaining the UEI for the organization from SAM.gov, you must return to Grants.gov to continue registration. There is no fee for registering with Grants.gov. Your organization's EBiz POC must:

1. Create a Grants.gov account with the same email address as used in SAM.gov for EBiz POC, and
2. Add a profile with Grants.gov using the UEI obtained from SAM.gov.

The EBiz POC can then delegate administrative roles to other users. Read the Help article, Manage Roles for Applicant for instructions.

Visit Learn Grants to find information about every phase of the grant management process, from applying and reporting to the award closeout.

On-Time Submission

All registrations including SAM.gov must be completed before the deadline

- **Concept Paper & Full Application must be free of Grants.gov errors; corrective submissions must be made BEFORE the submission deadline and will overwrite previous submissions**

  - Errors stop application processing and must be corrected

  - Warnings do not stop application processing and are corrected at your discretion based on your circumstances

- **Submit early to allow time to correct any unexpected errors or submission issues**

  - Depending on the size of the file, transmittal may take SEVERAL MINUTES to HOURS.

  - Don't wait until the deadline date to submit. The system may be slow due to last minute submissions.

Tips for Success

NIST

- **Do NOT apply with a full application in Grants.gov until invited**
- **Understand submission process in NOFO**
- **SAM.gov registration must be active to apply in Grants.gov (Concept Paper & Full Application)**
- **Use correct UEI and EIN**
- **Designate the proper roles in the systems (i.e. - Authorized Rep in Grants.gov)**
- **Utilize "workspace" feature in Grants.gov to draft applications**
- **Limit application to file size / character limits / page limits**
- **Make sure you are using compatible software (ex: Adobe Reader)**
- **Do not pay to create accounts**
- **Late applications will not be accepted**
- **Register to SAM.gov and Grants.gov early!**
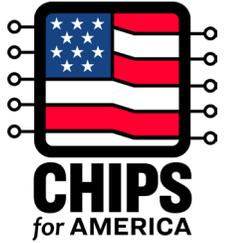
Questions?

NIST

Lisa Ko
Other Transaction Agreements Officer

E-mail: **Lisa.Ko@nist.gov** with "2024-NISTCHIPS-MFGUSA-01 Questions" in subject line

Panel Question & Answer

MODERATOR

Christie Canaria
Senior Advisor,
CHIPS R&D

PANELISTS

Eric Forsythe
Technical Director, CHIPS Manufacturing USA

Richard-Duane Chambers
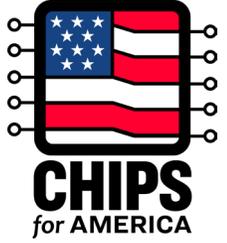Director, Policy and Integration, CHIPS R&D Office

Mike McKittrick
Deputy Director, CHIPS Manufacturing USA

Greg Strouse
NIST Safeguarding Science Research Security Director
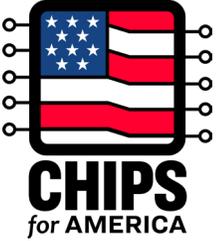
Slido

You can change rooms any time using this dropdown menu

Toggle between functions, as needed

Scan the QR code or go to slido.com and enter code MFGUSA

Lunch Options

- On your own
  - Olives restaurant in the hotel lobby
  - Olives restaurant "grab & go options" in the hotel lobby
  - Venture out to one of the local restaurants:
    - https://www.google.com/maps/d/edit?mid=1udE_t1I0vEh3adeRn9HtqTQkbSnd8KM&usp=sharing
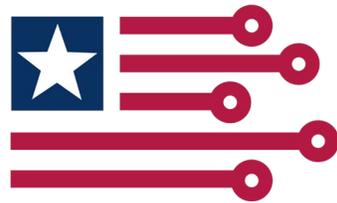   - QR code links to map of local eateries, may want to order ahead:

Natcast Speaker
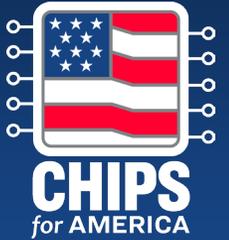
Susan Feindt
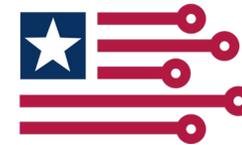SVP Ecosystem Development,
Natcast

The CHIPS & Science Act

$39B
Incentives

Invest in U.S. production of strategically important semiconductor chips, and assure a sufficient, sustainable, and secure supply of older and current generation chips for national security purposes and for critical manufacturing industries.

$11B
R&D

Strengthen U.S. semiconductor research and development (R&D) leadership to catalyze and capture the next set of critical technologies, applications, and industries.

$2B
DoD

The DoD Microelectronics Commons is a national network that will create direct pathways to commercialization for US microelectronics researchers and designers from "lab to fab."
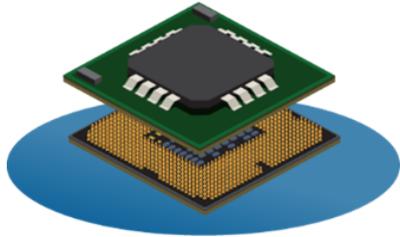
Workforce Initiatives

Natcast

CHIPS R&D Programs

CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is an independent nonprofit organization and operator of the NSTC consortium
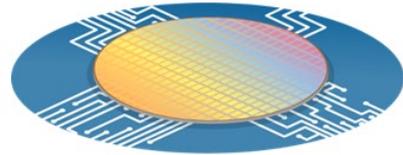
CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

Manufacturing USA

CHIPS Manufacturing USA Program

CHIPS Metrology Program

Workforce Initiatives

Focus Areas

Workforce Development

Technicians
Regional

Engineers

Researchers
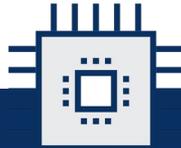
Lower Cost of Design

Design Enablement Gateway

Silicon Aggregation Services

Venture Fund

Research

Member-driven TAB

Development Projects

Prototyping

Technical Centers

Natcast

Community of Interest Survey

Academia 21%

Manufacturers 17%

Packaging/ assembly 2%

Equipment/ tools, materials suppliers 11%

Design 16%

Government Agencies, Labs Consortia 11%

Investors, incubators 7%

Non-technical organizations & service providers 6%

Other 8%

46%

Natcast
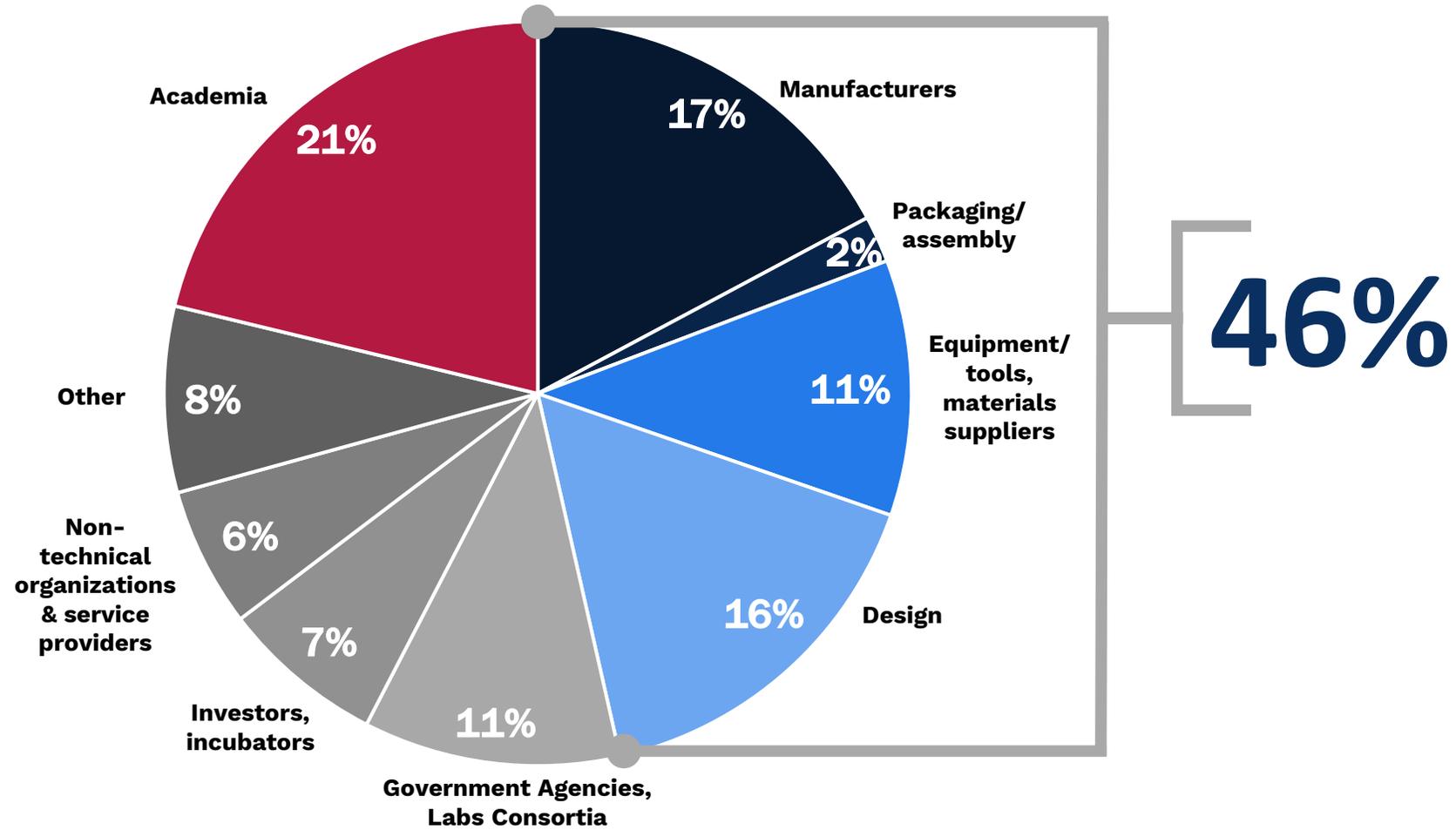
Top 10 Areas of Interest

1. Submit proposals for R&D funding
2. Participate in industry conferences
3. Access to prototyping facilities
4. Present technology to potential customers
5. Attend/present at symposiums/workshop
6. Submit proposals for WFD programs
7. Access to Advanced Packaging and HI
8. Access to metrology research, technology and IP
9. Access to test, measurement and analytic tools
10. Access to EDA design tools, flows, cloud and PDKs

Natcast

Community of Interest Survey
Enabling Technology Areas Natcast should invest
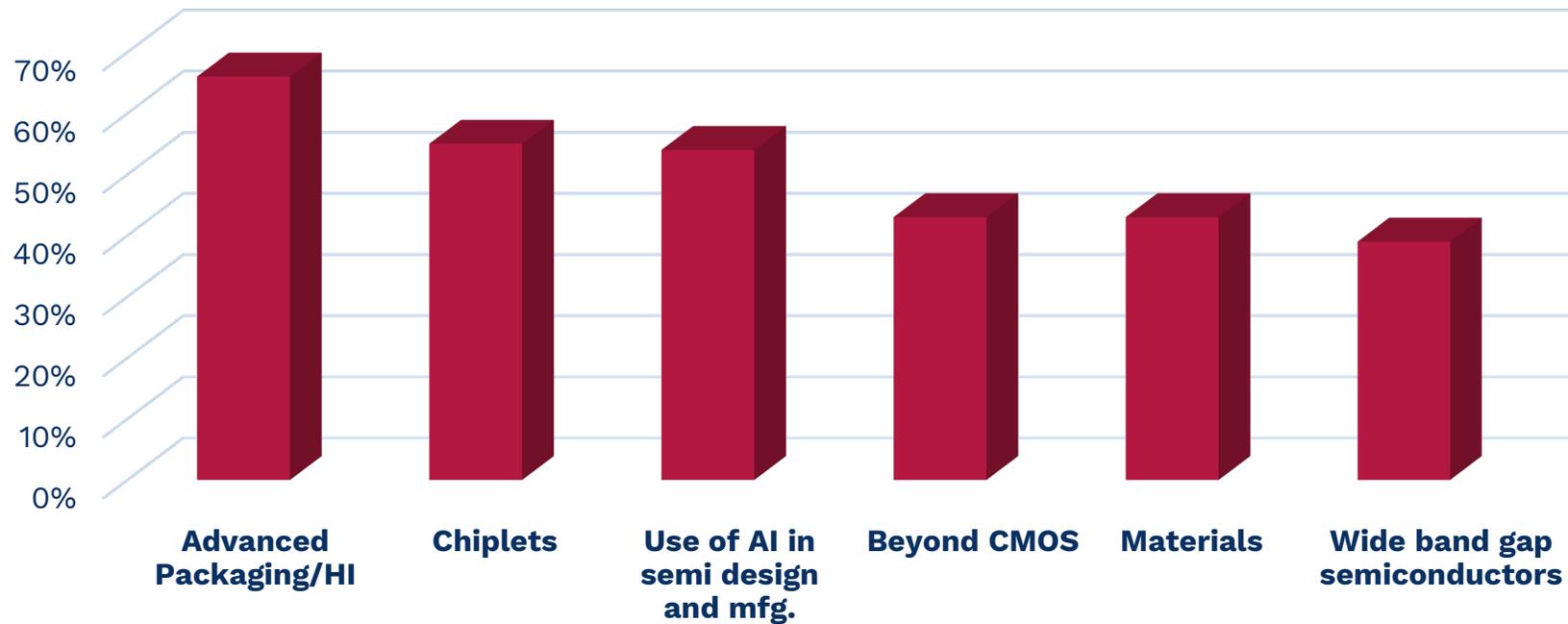
Prototyping Strategy: RFI Update

73 Respondents 25+ meetings

Excellent Participation

Wide Range of Inputs
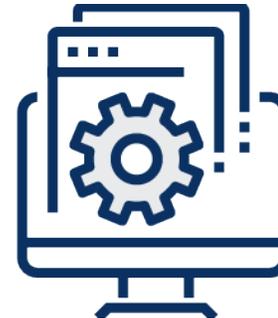
Diverse Set of Technologies and Topics

Natcast

Leveraging Insight
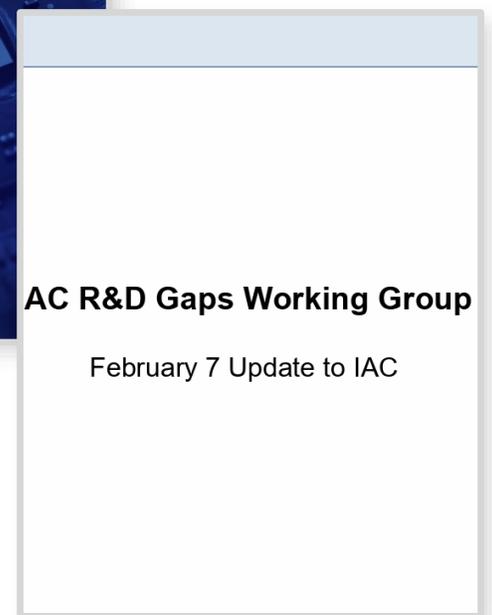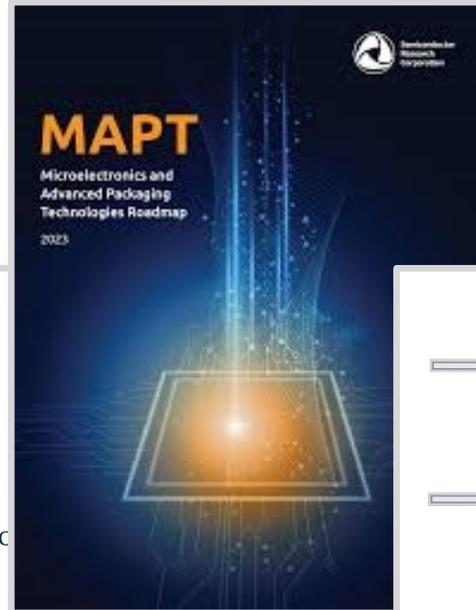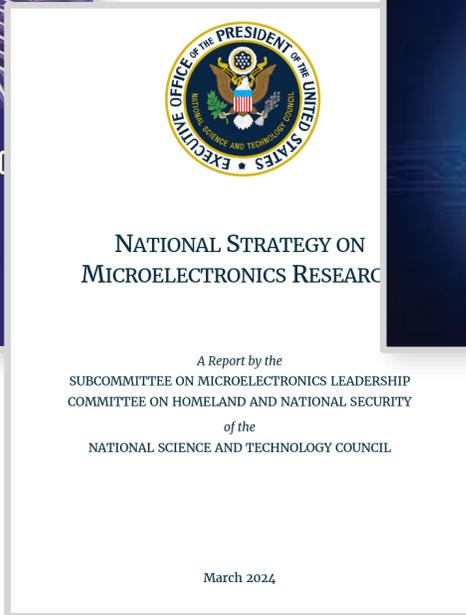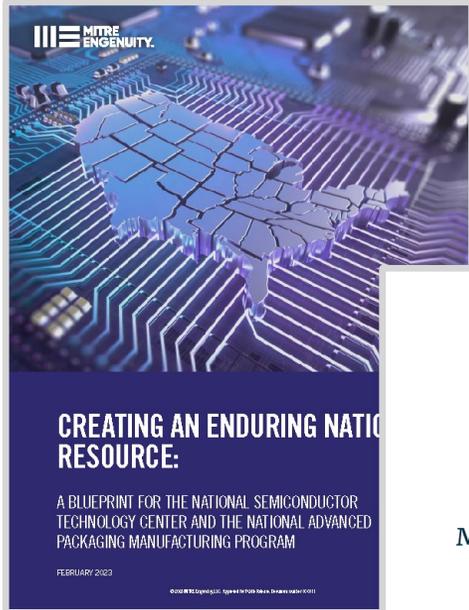
The Road Ahead
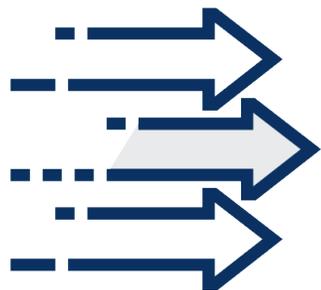
Jump Start Projects

Workforce Development

Membership Model

Facilities

Q & A
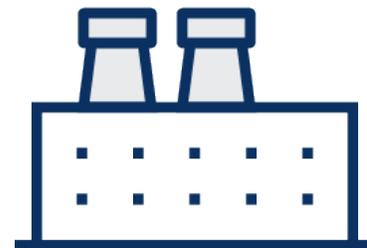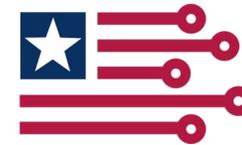
For more information, please contact:

Susan Feindt

SVP Ecosystem Development

info@natcast.org

Natcast
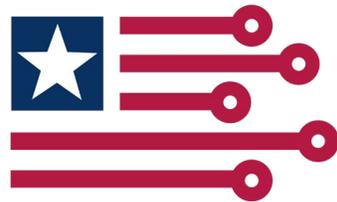
Lunch Options
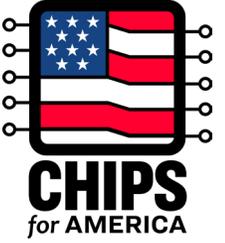
- On your own
  - Olives restaurant in the hotel lobby
  - Olives restaurant grab & go options in the hotel lobby
  - Venture out to one of the local nearby restaurants

Manufacturing USA Network Speaker
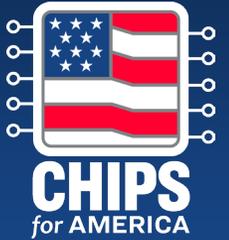
Mojdeh Bahar
Associate Director for Innovation
and Industry Services,
NIST
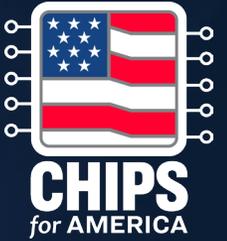
Manufacturing USA Network

Mojdeh Bahar
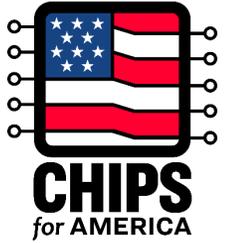
Disclaimer

- Statements and responses to questions about advanced microelectronics research and development programs in this webinar:
    - Are informational, pre-decisional, and preliminary in nature.
    - Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
    - Are subject in their entirety to any final action by NIST or the Department of Commerce.
- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity.

Manufacturing USA Vision and Mission

VISION: Securing U.S. Global Leadership in Advanced Manufacturing

MISSION: Connecting people, ideas, and technology to:
- solve industry-relevant advanced manufacturing challenges
- enhance industrial competitiveness and economic growth
- strengthen our economic and national security

Manufacturing USA Purpose: Accelerate Discovery to U.S. Production

Create an effective collaboration environment for applied industry research to "bridge the gap" from discovery to production.
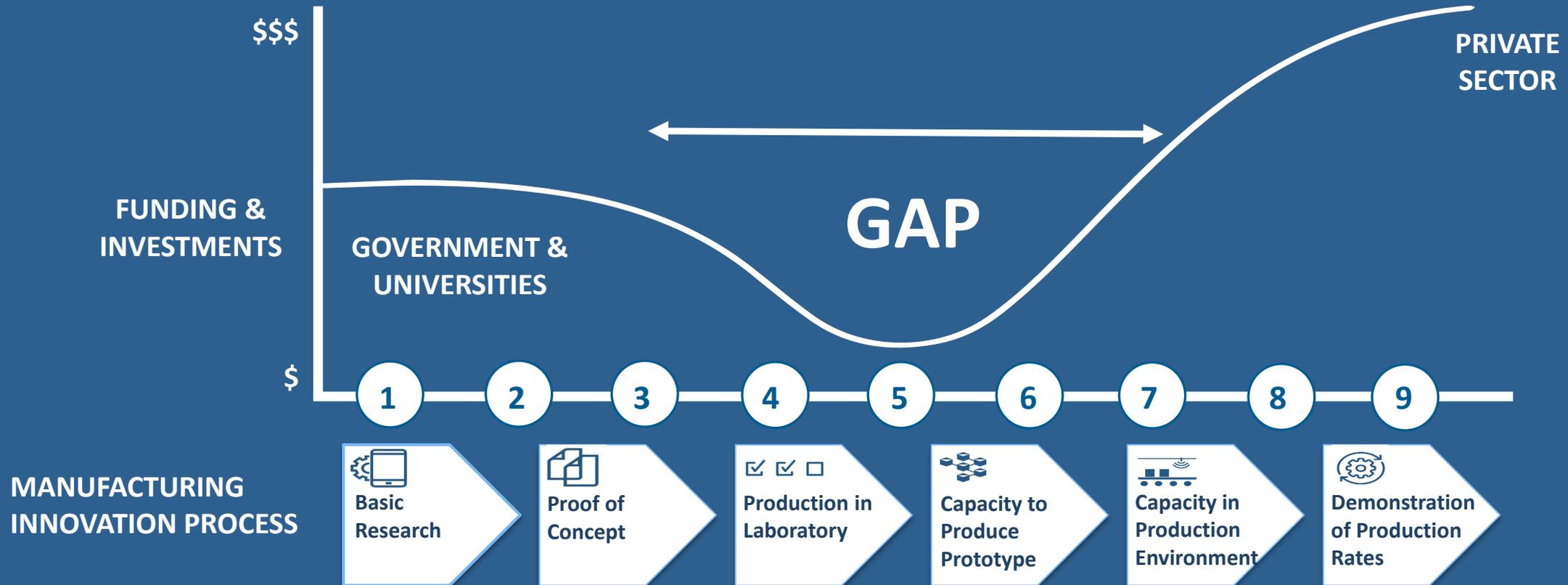
Institute Partnership Model

GOVERNMENT

FEDERAL LABS

ACADEMIA

MANUFACTURING USA INSTITUTE

+ Shared Use Facility
+ Testbeds
+ Equipment
+ Materials Prototyping

INDUSTRY

ManufacturingUSA

ManufacturingUSA
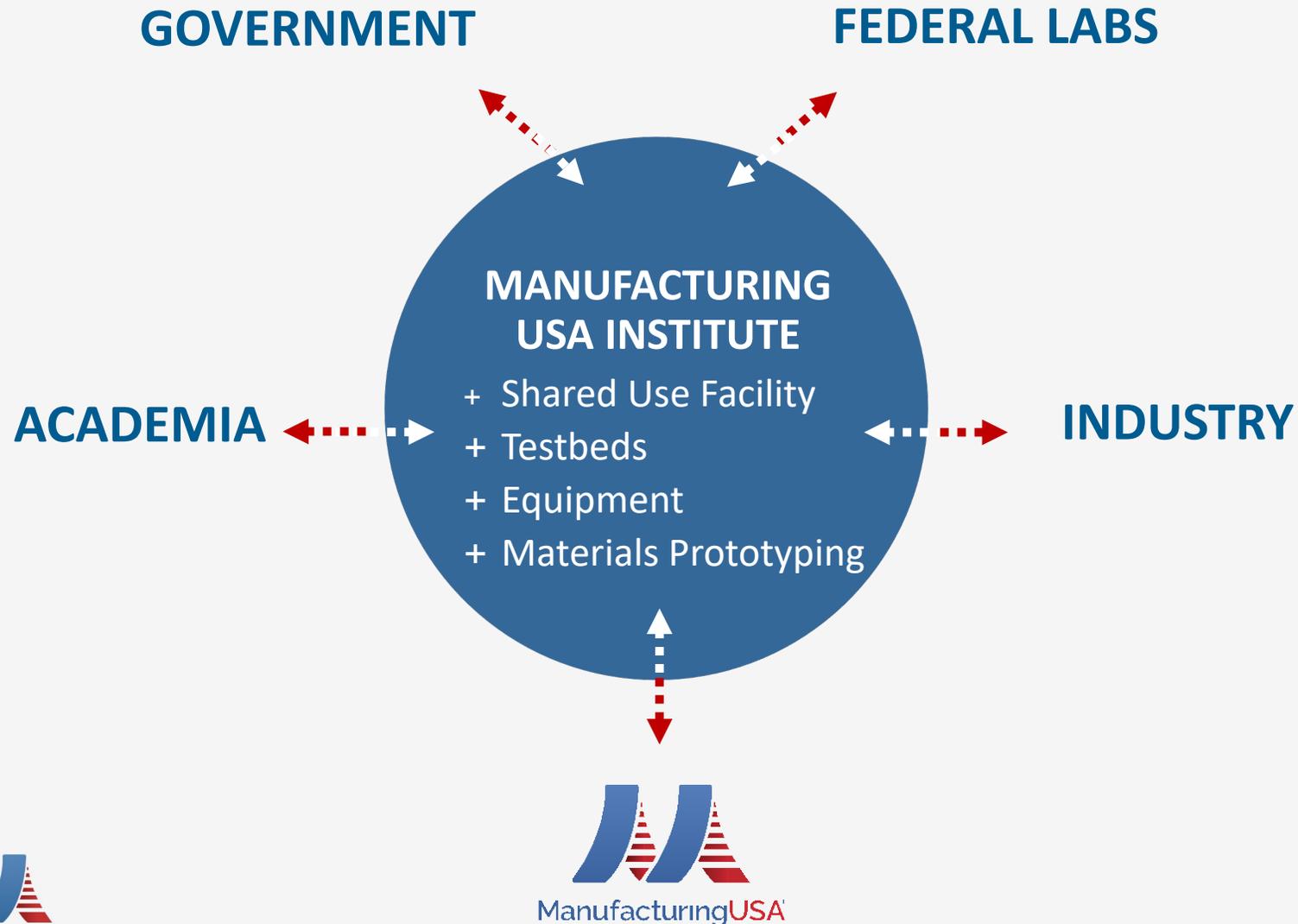
Common Institute Design:

- Industry-led public-private partnership
- Typically $70-120M federal investment
- At least 1:1 match with private funds
- Neutral convening for collaborations
- Each institute develops a unique technology
- Institutes address the education and workforce skills gap for their technologies

Manufacturing USA Network: 17 Institutes and Growing

ELECTRONICS

Integrated Photonics
Albany, NY
Rochester, NY

Flexible Hybrid Electronics
San Jose, CA

Wide Bandgap Semiconductors
Raleigh, NC

MATERIALS

Advanced Fibers and Textiles
Cambridge, MA

Advanced Composites
Knoxville, TN
Detroit, MI

Advanced Materials
Detroit, MI

ENERGY/ ENVIRONMENT

Modular Chemical Process Intensification
New York, NY

Sustainable Manufacturing
Rochester, NY

Smart Manufacturing
Los Angeles, CA

Industrial Process Decarbonization
Tempe, AZ

DIGITAL/ AUTOMATION

Additive Manufacturing
Youngstown, OH
El Paso, TX

Advanced Robotics & AI
Pittsburgh, PA

Digital Manufacturing & Cybersecurity
Chicago, IL

Cybersecurity in Manufacturing
San Antonio, TX

BIO- MANUFACTURING

Regenerative Manufacturing
Manchester, NH

Biopharmaceutical Manufacturing
Newark, DE

Bioindustrial Manufacturing
St. Paul, MN

Manufacturing USA Network

2022 Impacts

Work with
2,500+
Member Organizations

Collaborate on
670+
major applied research and development projects

Engage
106,000+
people with workforce knowledge and skills in advanced manufacturing

Invest
$416M
in these activities from state, industry, and federal funds

Our efforts help ensure **what's invented here is made here by a skilled American workforce.**

ManufacturingUSA

2023 Annual Report

Cyber Resource **Hub**

Roadmap for Automotive Smart Manufacturing

Military Service Members in Biopharma Manufacturing **Program**

National Partners

17 Institutes Members in **50 States + Puerto Rico**

9 Partner Federal Agencies

DOC sponsors 1 Institute Serves as **National Program Office**

DOE sponsors 7 Institutes

DOD sponsors 9 Institutes

NIST Program Office Role

Convene, Coordinate, Support Manufacturing USA

Public Service Award Funding

Cross-network coordination, including new Manufacturing USA Council

Advanced Manufacturing Education and Workforce Development

Shared resources and services

Triennial Strategic Plan + Annual Report to Congress

Information to the public, including ManufacturingUSA.com

NIST-Sponsored Manufacturing USA Institutes

Annual Network Meeting and 10th Anniversary

What's Ahead: Manufacturing USA Institute Competitions

CHIPS Manufacturing USA Digital Twins Institute

AI for Resilient Manufacturing Institute

Interagency Panel Moderator
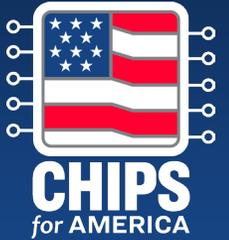
Christie Canaria
Senior Advisor,
CHIPS R&D

Disclaimer
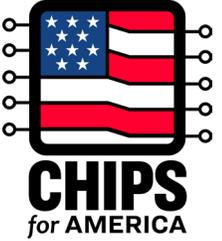
The Notice of Funding Opportunity (NOFO) 2024-NIST-CHIPS-MFGUSA-01 document is the official competition document. Potential applicants should follow the NOFO for guidance on pre-award and post-award interactions with the Federal Government.

The following presentation is for informational purposes only with an intent to familiarize potential applicants with some of the other government programs in technology areas related to the CHIPS Manufacturing USA Institute. These panelists represent only a subset of potentially relevant government programs.

Slido

You can change rooms any time using this dropdown menu

Toggle between functions, as needed

Scan the QR code or go to slido.com and enter code MFGUSA

Interagency Panel
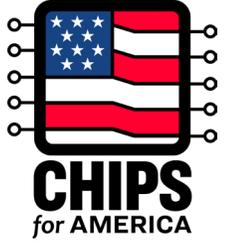
MODERATOR

Christie Canaria
Senior Advisor,
CHIPS R&D

PANELISTS

Bruce Kramer, Ph.D.
Senior Advisor, NSF

Devanand K. Shenoy, Ph.D.
Microelectronics Commons Executive Director, OUSD (R&D)/ASD(CT)

Stephen L. Luckowski
Program Manager, DoD MIIs, OUSD (R&E)

Tina Kaarsberg, Ph.D.
Deputy Program Manager, DOE/EERE

NSF Vision: A nation that leads the world in science and engineering innovation, to the benefit of all, without barriers to participation

11K
Number of awards NSF funds each year

$9.9B
FY 2023 Enacted

39K
Proposals evaluated

$1.6B
STEM education

1.8K
NSF-funded institutions

93%
Funds research, education and related activities

352K
People NSF supported

258
NSF-funded Nobel Prize winners
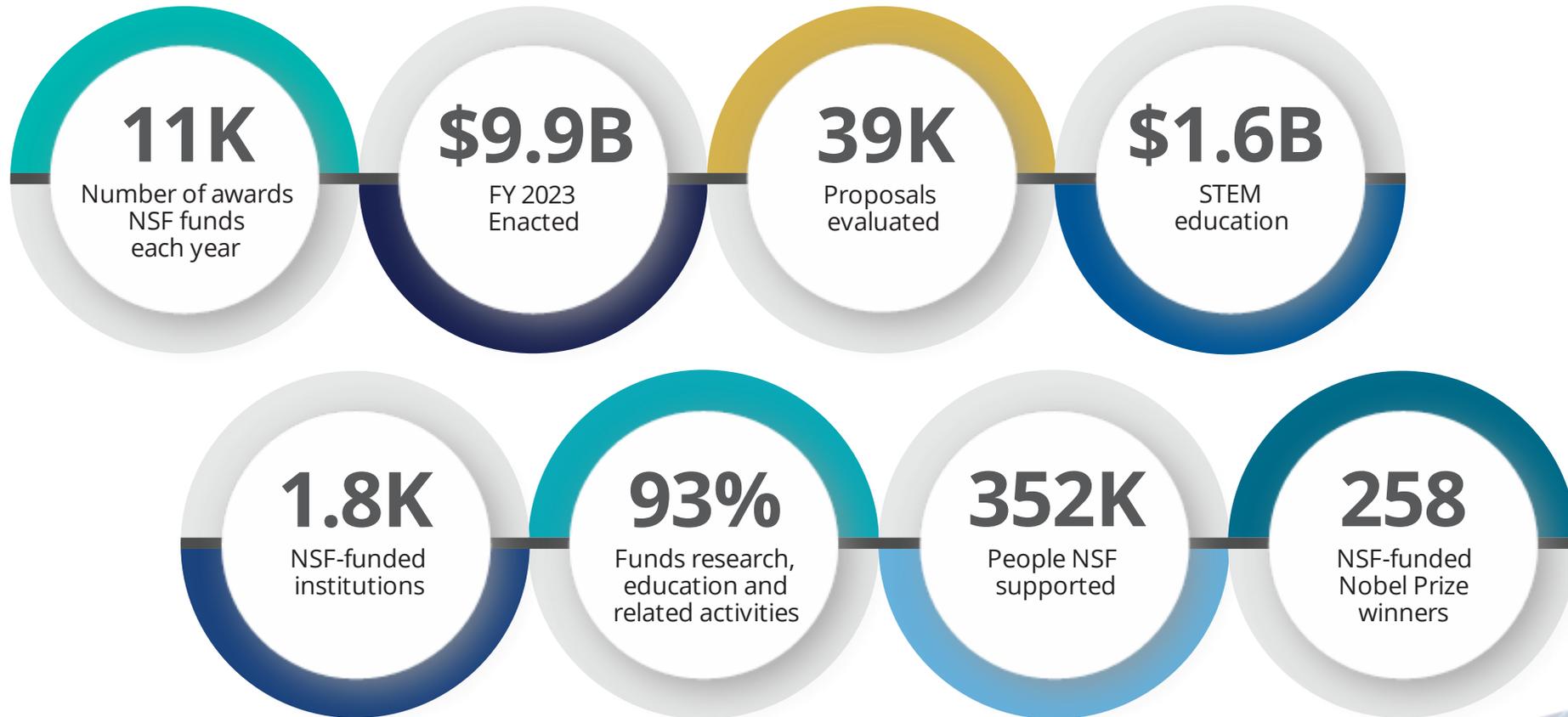
Leveraging NSF Programs

- We can competitively fund your long-term research.
  - Your partner universities know our programs.
  - Your future employees learn by researching your future technology needs.
- NSF 24-014 – DCL: Advancing Fundamental Research and Education in Advanced Manufacturing with the Objectives of the Manufacturing USA Institutes.
- NSF 21-598: Advanced Technological Education (ATE) Program – world class technician education.
- NSF 21-013: INTERN Program – Graduate-level internships in your member companies.

What to do

- Consider the benefits of accessing deep expertise from inside and outside your proposing team.
- Create a formal protocol for working with colleges and universities.
    - NSF 23-054 - DCL: Research on Integrated Photonics Utilizing AIM Photonics Capabilities
- Propose a National Artificial Intelligence Research Institute, NSF 23-610.
    - 25 exist, one in logistics, none in manufacturing
    - You have the data researchers need to create new methods.

DoD Microelectronics Commons

CHIPS Manufacturing USA Proposers Day, Panel Briefing
16 May 2024

Dr. Dev Shenoy
Principal Director for Microelectronics
Microelectronics Commons Executive Director
OUSD (R&E) Critical Technologies

CHIPS Offers a Whole of Government Approach

The NSTC and Microelectronics Commons will expand the number of concepts and ideas that can transition from proof-of-concept to the market.

NSF basic research
DMREF, RINGS, others

DOE basic/early-stage research
SC, NNSA, EERE, ARPA-E, others

DOD early stage
ERI 2.0, NGMM, SBIR, others

Other USG
Agency SBIR, NASA, NIH, others

Private capital

Commercial R&D

International programs

Pre-CHIPS

Microelectronics Commons

Commercial technology with defense implications

NSTC

Broad support for commercial technologies

USG scaling programs
NSF Fuse, DOE NNSA, other

Prototyping, scaling, and de-risking

Private capital

+ CHIPS Incentives

Commercial fabs, foundries

DARPA SHIP, DOD RAMP-C, DOE NNSA, others

Transition to market

Discovery and proof of concept

A VISION AND STRATEGY FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER
CHIPS Research and Development Office
April 25, 2023

Lab-to-Fab Transition of Microelectronics Technologies

Research Universities, **Start-ups** have facilities for Lab prototyping but face barriers to demonstrating manufacturability in a Fab.

Core Facilities or Foundries/Fabs provide access to early-stage Fab prototyping.

Microelectronics Commons aims to enable lab-to-fab prototyping– evolve microelectronics laboratory prototyping to foundry/fab prototyping – in domestic facilities

Microelectronics Commons Addresses the Valley of Death
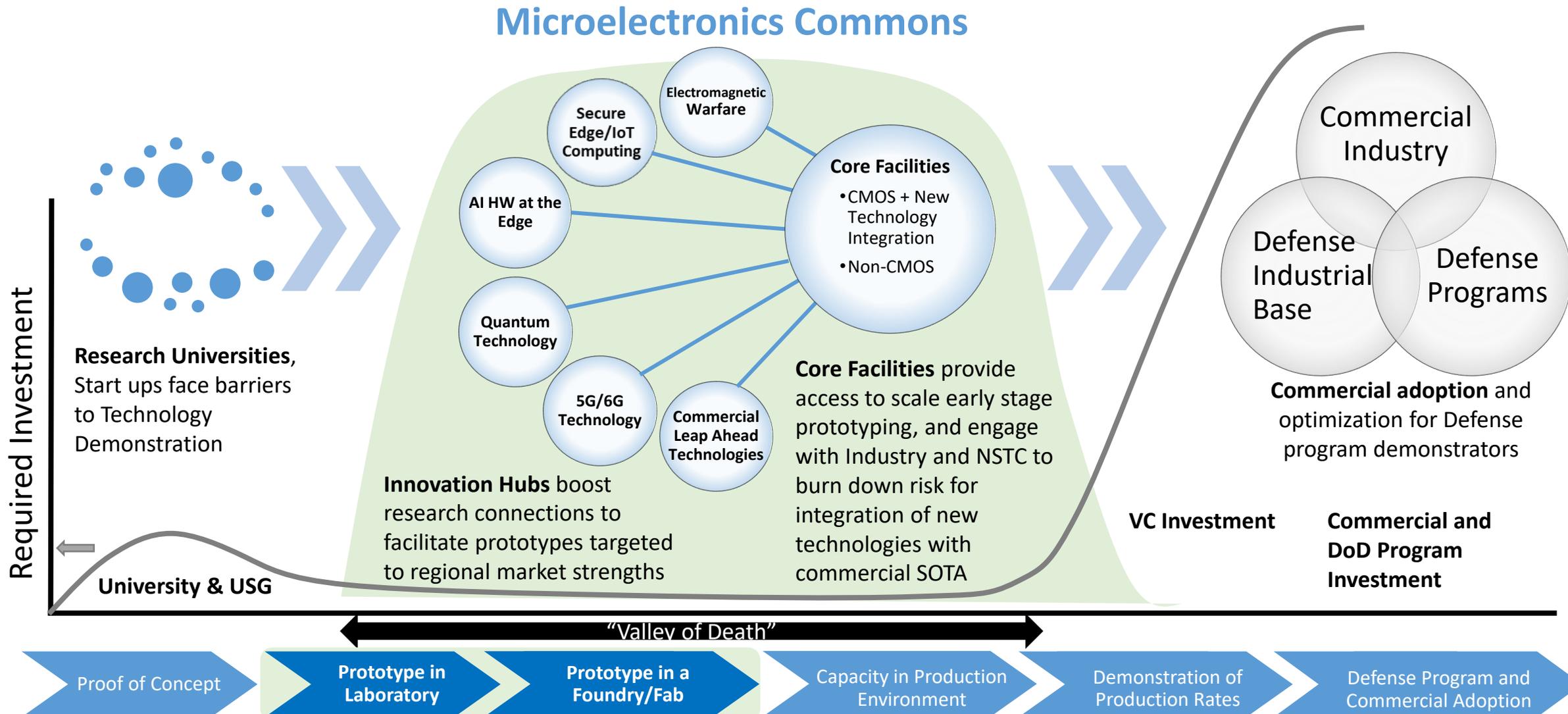
Commons Will Support Infrastructure

Human Infrastructure …
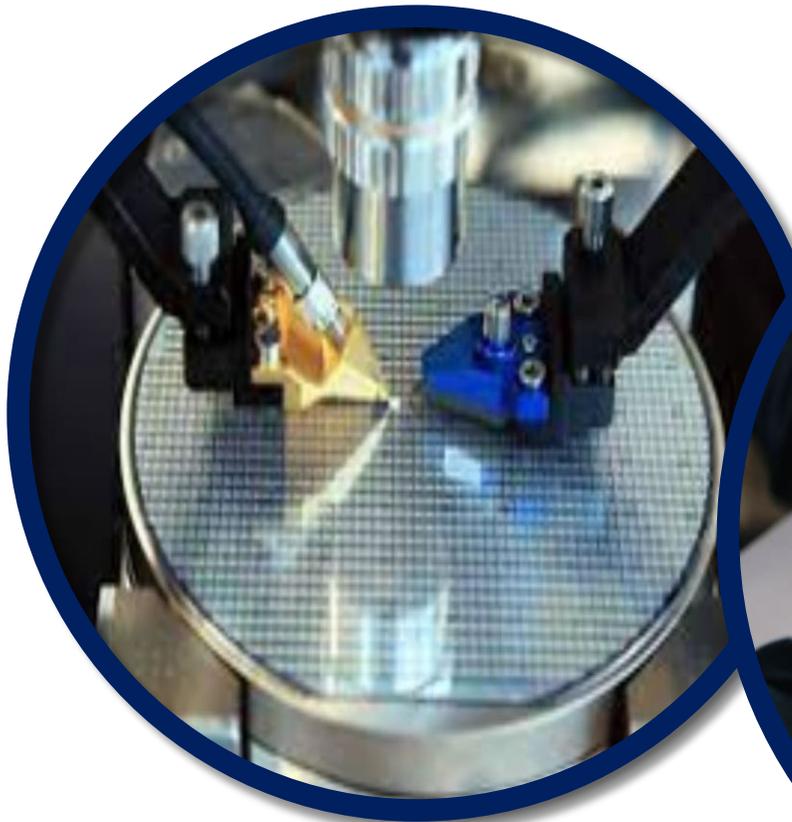
Physical Infrastructure …

Digital Infrastructure …

Infrastructure is foundational to the success of the Microelectronics Commons

Microelectronics Commons by the Numbers

8 Hub Leads

Microelectronics Commons

This map represents membership data provided to NSTXL by the Microelectronics Commons Hubs as of April 15, 2024.

Legend:
- Hub Lead
- Hub Member
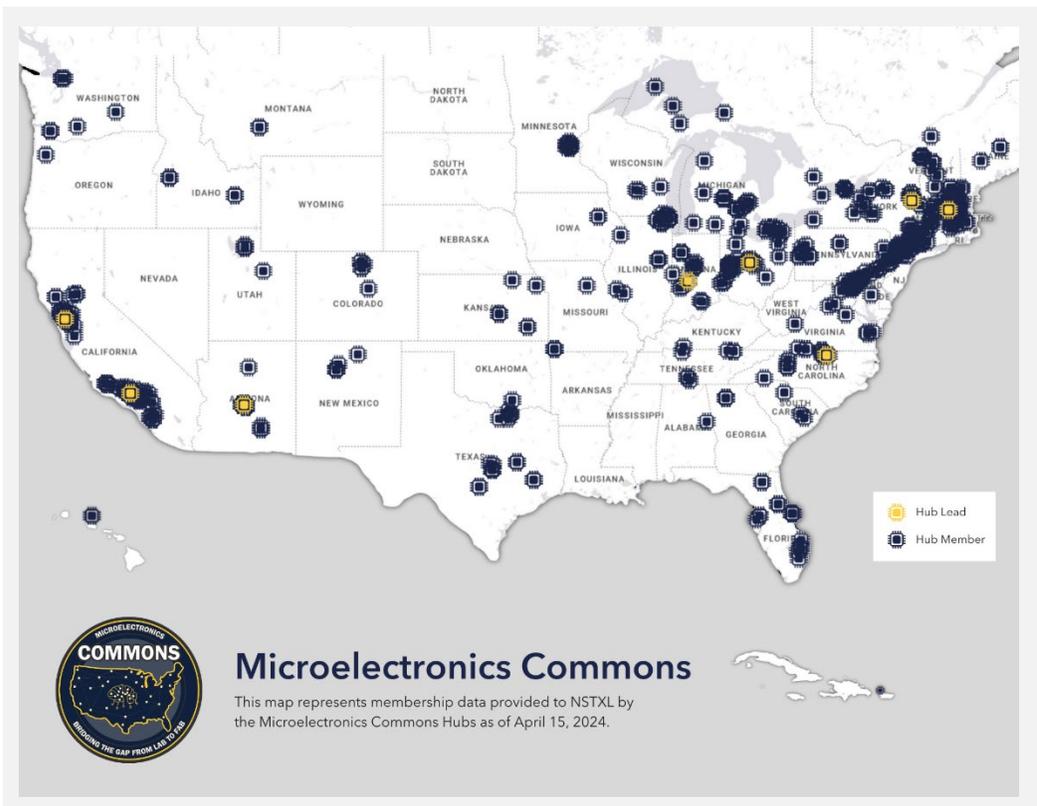
~$240M Funding to Hubs	Member Location 35 States +District of Columbia and Puerto Rico	642+ Hub Members
381 Unique Members	215+ Members Located Outside of Their Hub Lead's State	100+ Colleges & Universities

Progression from Concept to Capabilities

MICROELECTRONICS COMMONS PATHWAYS TO DEVELOP AND DELIVER NEW DEFENSE CAPABILITIES

Microelectronics Commons

- Electromagnetic Warfare
- Secure Edge/IoT Computing
- AI HW at the Edge
- Quantum Technology
- Commercial Leap Ahead Technologies

Commercial Dual Use Technologies

- Technologies sustained by commercial markets but optimized for DoD Needs
- Early access for DoD enables technology advantage for the warfighter
- Low cost, high reliability
- Leverages large commercial R&D budgets for continued innovation

DoD Unique Technologies

- High Performance niche technologies not sustained by commercial market
- Applications for Rugged operation
- Enhanced Security
- Low product volume ensures DoD control and protection of supply chain

Application Platforms

- Aircraft
- Submarines
- Ships
- Space Systems
- Ground Systems
- Missile Defense
- C4ISR

ENCRYPTION

POSITIONING, NAVIGATION, AND TIMING

WEAPON SYSTEMS

Artificial Intelligence

ENABLERS

COMMAND, CONTROL AND COMMUNICATIONS

The Cloud

Lab-to-fab prototyping bridges valley of death from laboratory research to foundry/fab prototyping

Department of Defense

Manufacturing Innovation Institutes

Steve Luckowski
Program Manager, DoD MIIs
Department of Defense Manufacturing Technology Program
Office of the Under Secretary of Defense
for Research and Engineering

May 16, 2024
www.CTO.mil
www.DoDManTech.mil

DoD ManTech Program

MISSION
Anticipate and close gaps in manufacturing capabilities for affordable, timely, and low-risk development, production, and sustainment of defense systems.

DoD ManTech carries out its mission through programs in the Military Departments, participating Defense Agencies, and OSD

DoD Manufacturing Innovation Institutes are executed out of OSD with support from the Services

DoD Manufacturing Innovation Institutes
Current Headquarters and Hubs

BioMADE
Bioindustrial Manufacturing
Minneapolis, MN
Emeryville, CA

M×D
Digital Manufacturing & Cybersecurity
Chicago, IL

NEXTFLEX
Hybrid Electronics
San Jose, CA

lift
Advanced Materials
Detroit, MI

biofabusa
Regenerative Manufacturing
Manchester, NH

afrva
Advanced Fibers & Textiles
Cambridge, MA

AIM PHOTONICS
Photonics
Albany, NY

ARM
Advanced Robotics
Pittsburgh, PA

America Makes
Additive Manufacturing
Youngstown, OH

LEGEND
○ Institute Headquarters
△ Institute Hubs

Since Launching in 2012…
- DoD's strategic commitment of $954 million has resulted in
  - ~$2 billion of committed non-federal cost share
  - Over $1.2 billion of committed federal project work
- 2,000+ companies, universities, and non-profit members or partners
- DoD MII members across 49 states, Washington DC, and Puerto Rico
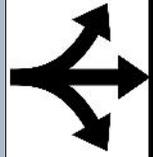
Data as of 31 March 2023

MIIs are a Unique Resource to Address DoD Challenges

MII responsiveness to COVID pandemic demonstrated value beyond their ecosystem-driven technology roadmaps.

1.4K MII members activated - DoD awarded > $60.7M for 20+ projects initiated within 5 weeks. Examples:
- Novel Drug Delivery
- PPE Design Database
- Pandemic Roadmap
- CleanSURFACES Mat

Hypersonics

- AM for high-temp metals ($2.1M, America Makes)
- Materials & Manufacturing for hypersonic vehicles ($3M, LIFT)

Project examples:
- Thermal Protective Coatings
- High Temperature Materials
- Integrated Computational Materials Engineering

Point of Need & Contested Logistics

- "Shark Tank" Challenge to deliver PoN solutions in austere climates (~$2.5M/6 projects/$700K cost share)
- 9 months later, projects demonstrated technologies at Cold Regions Research & Engineering Lab

Project examples:
- Zero-Trust Cyber Security Platform for Machines
- On-Demand Blood Program
- Additive Manufacturing and Repair platforms

Organic Industrial Base Modernization

- Shark Tank" Challenge to deliver dual-use technologies to meet OIB Modernization needs ($2.5M/5 projects/$1.1M cost share)
- Contract negotiations in progress with 6-mo PoP starting Jun 24

Partner OIB sites include:
- Marine Depot Maintenance Command
- Rock Island, IAAAP, Letterkenny, Picatinny, Watervliet
- Warner-Robins ALC
- …and many others

Advanced Materials Workshop

- Summit and workshop convene leaders from Gov, industry, and NPOs to identify and address greatest barriers to transitioning advanced materials

Identify	Advanced Materials
Design	ICME/M&S Tools
Prototype	Virtual or Actual Material
Demonstrate	Component on DOD System

Why partner with a DoD institute?

Experience operating an institute model

From contracting to governance, current MIIs have over 10 years of experience operating a public private partnership.
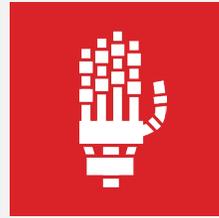
Leveraging an existing technology portfolio

MIIs have made Investments in digital twin technologies that have defined industry standards, practice, and framework.

MxD has over 150 technology design, production, and supply chain projects focused on digital thread, digital twin, AI/ML, and other technologies.

Leveraging existing EWD curriculum

Credentialed programs that are "shovel-ready".

MxD's Hiring Guides identify over 400 digital and cybersecurity manufacturing roles. CAPITAL program provides credentialed training modules focused on critical roles

NextFlex Manufacturing USA Institute

Mission: To create a strong U.S. industrial base for hybrid electronics manufacturing

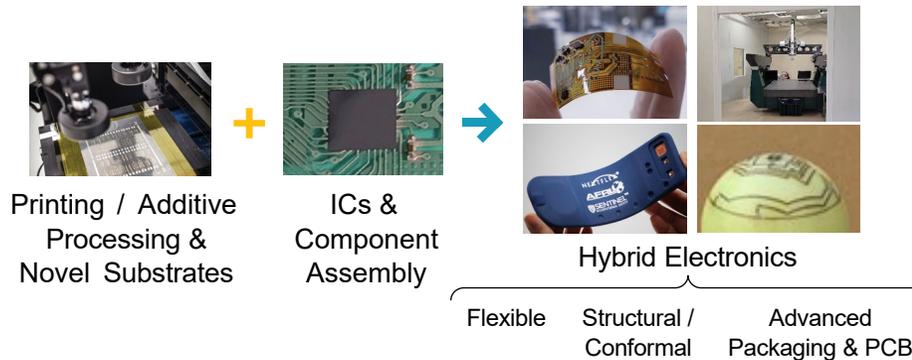
Printing / Additive Processing & Novel Substrates

+

ICs & Component Assembly

→

Hybrid Electronics

Flexible   Structural / Conformal   Advanced Packaging & PCB

11,000 ft² end-to-end pilot line fab

Institute assets relevant to digital twin institute

Technology

- Full pilot line for hybrid electronics developm't and manufacturing to generate data & validate models
- Library of project reports and data (including models)
- Data generation from member project calls; database built on NIST Configurable Data Curation System
- Technical working group & project call model, structure, operating mechanisms
- Roadmaps: 5-year outlook for technology and manufacturing

EWD Programs

- K-12 STEM Education (FlexFactor)
- Transitioning Service Members, Military Spouses, & Military Families (FlexMil)
- Pipeline and Skill-Based Programs for Untapped Talent
- Recruiting and Retaining Women in STEM, with Focus on Advanced Manufacturing and Engineering

NextFlex has identified topics for collaboration with digital twin institute – contact for more information.

For more information: Karen Savala, Director of Marketing & Membership, ksavala@nextflex.us

AIM Photonics Manufacturing Institute Mission and Capabilities

AIM Photonics Mission

Advance Photonic Integrated Circuit (PIC) technology providing PICS, EPD, and Packaging prototyping capability	Make the technology **Accessible** by Establishing & Growing a Manufacturing Ecosystem	Securing Human Capital through EWD Activities & Outcomes

Albany NanoTech 300mm

300mm Facility with >130K square feet of class-1 clean room

300mm Photonic Integrated Circuit Technologies → with customization possible

Base 300mm PIC MPW

SIN Sensor PIC MPW

Quantum PIC MPW

Efficient entangled photon source

PIC with III-V Lasers

Interposers, Heterogenous Integration

65nm Electronic Interposer

Electronic Photonic Interposer

Dense Bumping, Hybrid Bonding, 2.5D & 3D HI

Electronic Photonic Design Automation

PDKs for all PICs and Interposers and ADKs in development

DoD ManTech Program & Sponsored Institutes

www.DoDManTech.mil

The Manufacturing USA Program

www.manufacturingusa.com/

DOE Electronics Efforts of Potential Interest to NIST Digital Twin Institute NOFO Responders
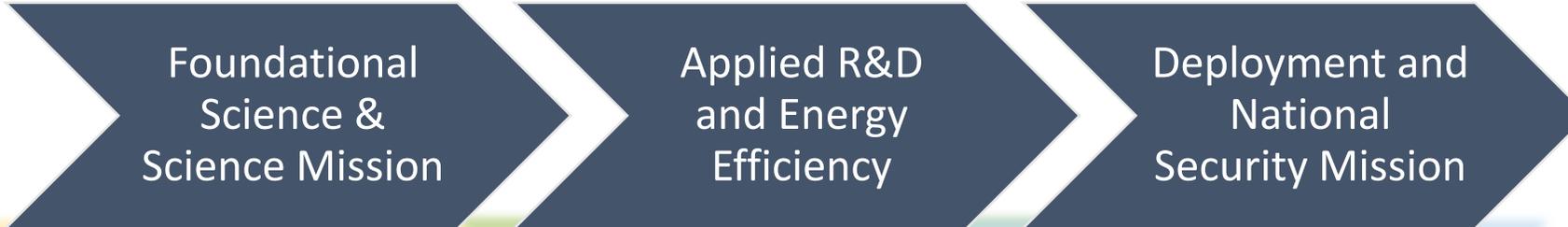
Tina Kaarsberg, PhD

May 16, 2024

Outline

- **DOE Microelectronics Overview**

- **EERE\AMMTO Efforts**
  - Power Electronics
  - Microelectronics EES2

- **DOE SC Efforts**
  - AI FOA Efficiency Topic
  - Microelectronics Centers for Efficiency and Extreme Environments

- **Other Thoughts: Digital Twin Definitions**

- **Active participation**

Three Major Microelectronics Equities at DOE

Foundational Science & Science Mission → Applied R&D and Energy Efficiency → Deployment and National Security Mission

U.S. DEPARTMENT OF ENERGY

Office of Science

U.S. DEPARTMENT OF ENERGY — Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

NNSA — National Nuclear Security Administration — DEFENSE PROGRAMS

Foundational Research (e.g. BES) but also Customer for R&D at accelerators (e.g. HEP) and high performance computing (e.g. ASCR)
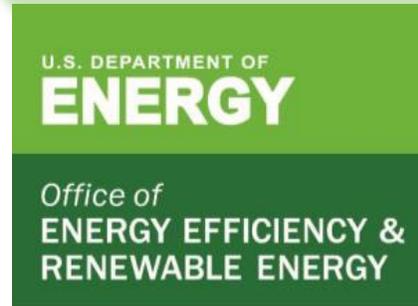
NOT its own customer

Customer for Rad-hard microelectronics and for high performance computing

DOE Power Electronics Innovation Ecosystem

Improving efficiency and performance of technologies that *create*, *distribute*, and *use* electricity through manufacturing R&D is foundational

Office of Science

Foundational and exploratory research

ARPA-E

High-risk, transformative PE technologies

Advanced Materials & Manufacturing Technologies Office

- Maturing (e.g., reducing costs) PE manufacturing processes and technologies
- Catalyzing domestic PE manufacturing
- Collaborating with DOE offices, national labs, SBIR across clean energy applications

Solar Energy Technologies Office

Wind Energy Technologies Office

Water Power Technologies Office

PowerAmerica

Office of Electricity

Industrial Efficiency and Decarbonization Office

Vehicle Technologies Office

Building Technologies Office

Early stage   *** Manufacturing platform development***   *Application-specific*

Climate goals drive DOE's work in energy **creation, distribution** and **use**

Power Electronics Materials & Manufacturing Roadmap: Goals & Principal Objectives

- Goal: Determine power electronics R&D advancements over the coming decade to achieve:
  - 50% cut in carbon emissions by 2030, net zero carbon power sector by 2035, and net zero carbon emissions by 2050

- Principal Objectives
  - Identify significant applications, trends, and challenges driving power electronics technology in the clean energy & decarbonization space.
  - Identify fundamental technology goals (e.g., cost, performance, efficiency), milestones, and timelines needed to meet decarbonization goals.
  - Quantitatively assess the potential impact and benefit-to-cost ratio (BCR) of advancements in power electronics on a clean energy economy.

Roadmap will cover 10-year time horizon (2025 - 2035)

➔ *Must anticipate needs of energy-related systems and power electronics solutions required to enable them*

2035

2025

Roadmap to identify PE RD&D and workforce targets, timelines, and convene key stakeholders

DOE Office of Science Efforts

- ASCR AI FOA Efficiency Topic

- Microelectronics Centers for Efficiency and Extreme Environments
  - Due May 30

Various Definitions

- A Digital Twin is a virtual representation of a connected physical asset - *DIGITAL TWIN: DEFINITION & VALUE | An AIAA and AIA Position Paper*

- A set of virtual information constructs that mimics the structure, context and behavior of an individual/ unique physical asset, or a group of physical assets, is dynamically updated with data from its physical twin throughout its life cycle and informs decisions that realize value.

- A digital twin is a set of virtual information constructs that mimics the structure, context, and behavior of a natural, engineered, or social system (or system-of-systems), is dynamically updated with data from its physical twin, has a predictive capability, and informs decisions that realize value. *Foundational Research Gaps and Future Directions for Digital Twins.* https://doi.org/10.17226/26894

- A DT is a virtual representation of real-world entities and processes, synchronized at specified frequency and fidelity, *Digital Twin Consortium, https://www.digitaltwinconsortium.org/2020/12/digital-twin-consortium-defines-digital-twin/* https://app.swapcard.com/event/iotswcdigitalsummit/planning/UGxhbm5pbmdfMjU3Mzcx

- **A Digital Twin is a representation of a real-world object, process, or system that changes over time as it is updated with data and models.** *https://nsf-gov-resources.nsf.gov/files/nsf24559.pdf?WT.mc_ev=click&WT.mc_id=&utm_medium=email&utm_source=govdelivery*

- A digital twin is an integrated multi-physics, multi-scale, probabilistic simulation of a vehicle or system that uses the best available physical models, sensor updates, fleet history, etc., to mirror the life of its flying twin - *Modeling, Simulation, Information Technology & Processing Roadmap Technology Area 11, NASA*

- "Digital twins" are software replicas of the dynamic function and failure of engineered products and processes. Digital twins describing infection and treatment require the development, validation, and integration of numerous component sub-models in the context of a rapidly developing scientific understanding of biological behaviors and continual generation of new experimental and clinical data. – *Science, 12 MARCH 2021 • VOL 371 ISSUE 6534*

- A digital twin is a virtual replica of a system's behavior in its operating environment. *Digital twins in manufacturing & product development | McKinsey*

- A digital twin is a dynamic virtual copy of a physical asset, process, system or environment that looks and behaves identically to its real-world counterpart - *https://unity.com/solutions/digital-twin-applications-and-use-cases*

Interagency Panel: Q&A Session

MODERATOR

Christie Canaria
Senior Advisor,
CHIPS R&D

PANELISTS

Bruce Kramer, Ph.D.
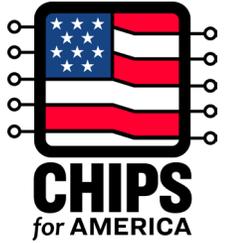Senior Advisor, NSF

Devanand K. Shenoy, Ph.D.
Microelectronics Commons Executive Director, OUSD (R&D)/ASD(CT)

Stephen L. Luckowski
Program Manager, DoD MIIs, OUSD (R&E)

Tina Kaarsberg, Ph.D.
Deputy Program Manager, DOE/EERE

Afternoon Breakout Sessions

- Successful outcomes are proposer's forming strong and diverse teams.

- There are identical sessions in three different rooms.
    - For Session 1: Self-select your room.
        - Madison, Regency, and Roosevelt
    - Following the break: Please try to network with a new group of people
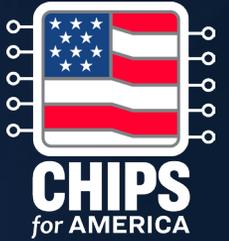
Time		
2:15 – 3:15 pm	Session 1	Networking/Facilitated Discussions
3:15 – 3:25 pm	Break	Consider switching rooms
3:30 – 4:25 pm	Session 2	Networking/Facilitated Discussions

- Virtual – virtual breakouts and discussions will follow the same schedule.

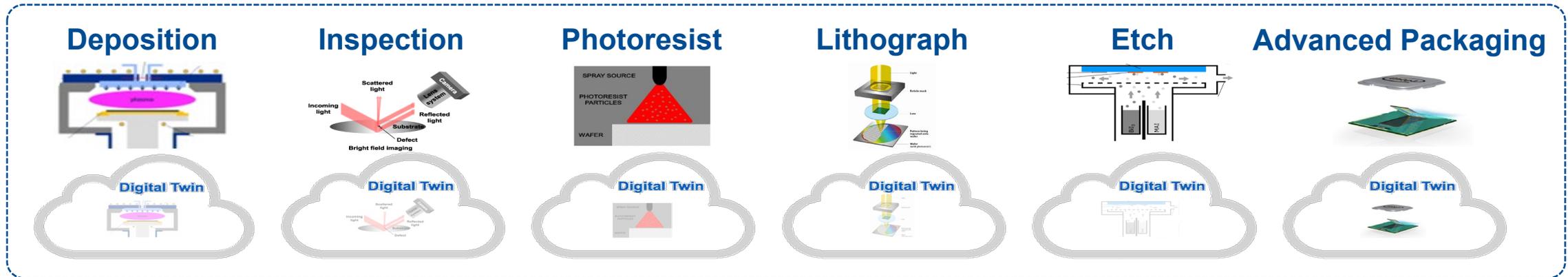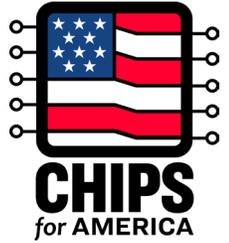**NIST staff in breakout rooms will not provide critique or provide feedback on any proposal ideas.**

Slido:
MFGUSA

Semiconductor Manufacturing Process Flow
(Recap)

Deposition   **Inspection**   **Photoresist**   **Lithograph**   **Etch**   **Advanced Packaging**

Institute Level Targets:

- Technical targets
- Non-technical targets

Operational Areas:

- Institute operations
- Shared Capabilities
- Industry Solutions
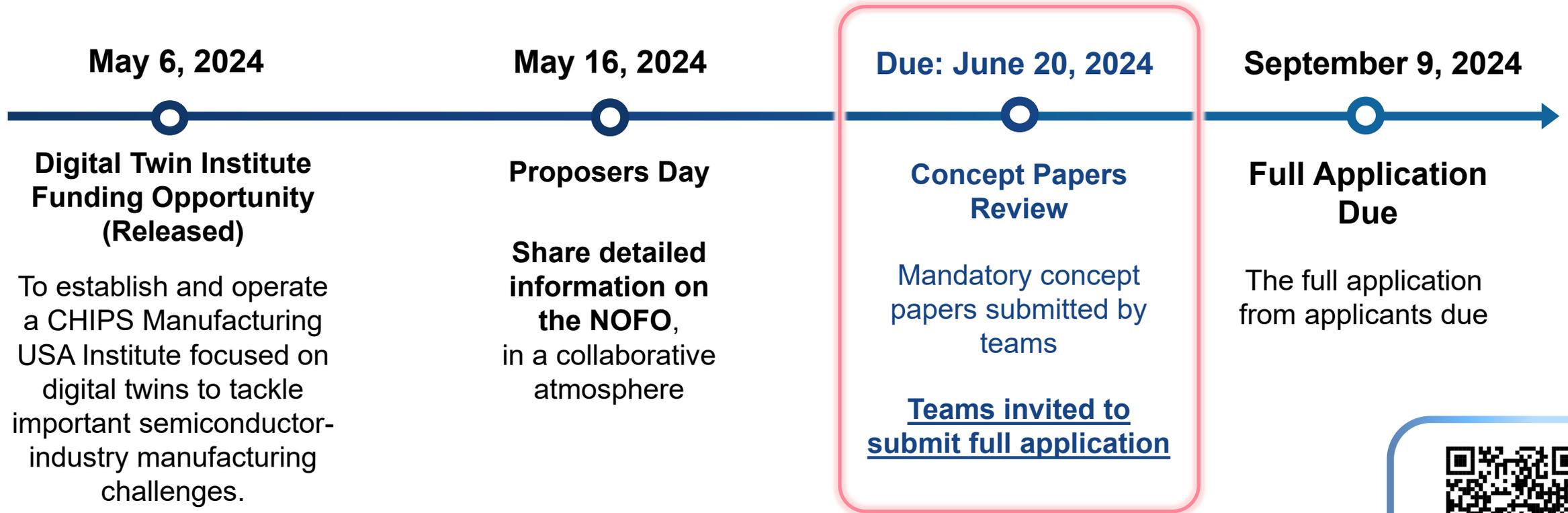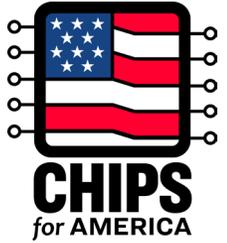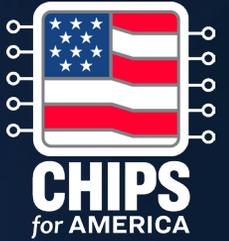- Workforce training

Digital twin:

- Enables collaborative development across the country, creating new opportunities for participation.
- Speeding innovation in new materials, tools, processes.
- Leverage emerging A.I. technology to help accelerate the innovation in manufacturing and co-optimization.
- Significantly reduce costs by improving capacity planning, production optimization.

Key Dates
(Reminder)

May 6, 2024

Digital Twin Institute Funding Opportunity (Released)

To establish and operate a CHIPS Manufacturing USA Institute focused on digital twins to tackle important semiconductor-industry manufacturing challenges.

May 16, 2024

Proposers Day

Share detailed information on the NOFO, in a collaborative atmosphere

Due: June 20, 2024

Concept Papers Review

Mandatory concept papers submitted by teams

Teams invited to submit full application

September 9, 2024

Full Application Due

The full application from applicants due

CHIPS for America QR Code:
CHIPS Manufacturing USA institute NOFO (full text)

Thank you for attending

Visit CHIPS.gov for future updates and additional information

askchips@chips.gov