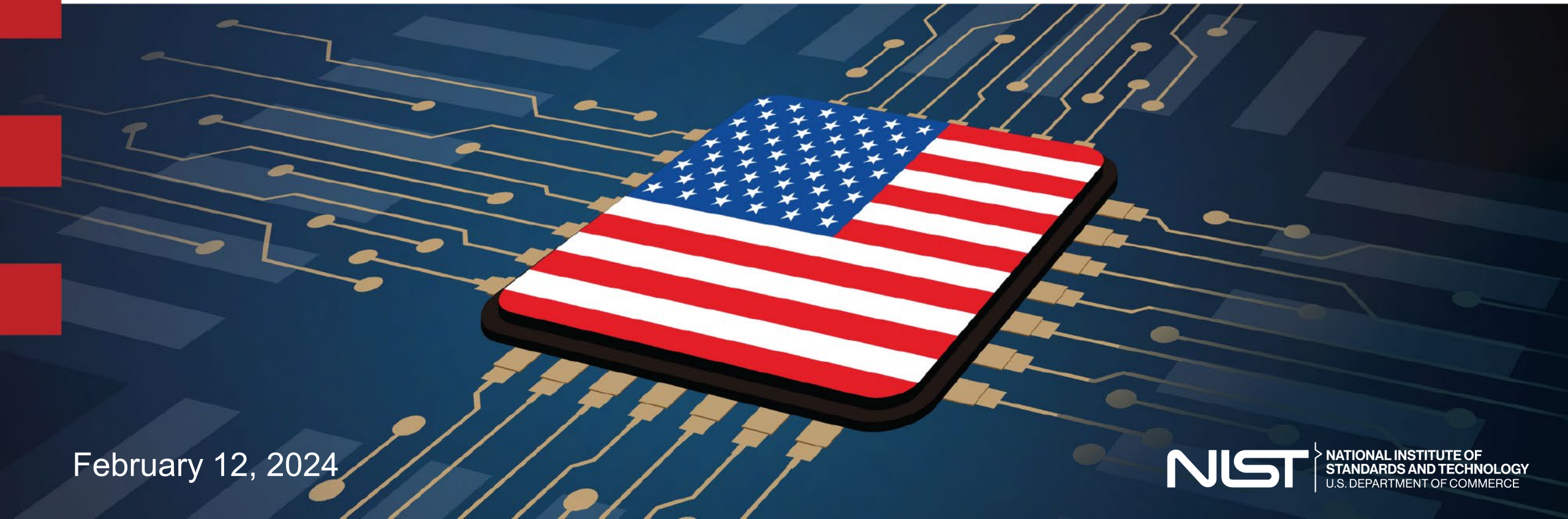
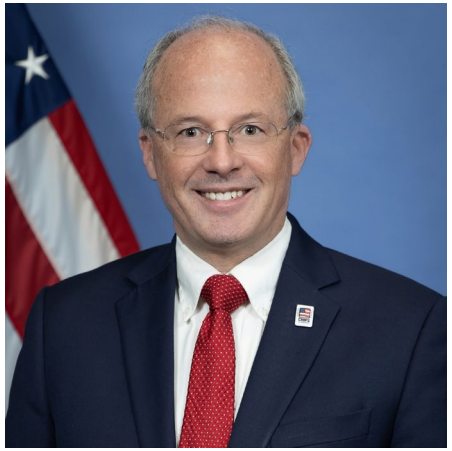
CHIPS Digital Twin Manufacturing USA Institute



February 12, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Today's Speakers



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Disclaimer

- Statements and responses to questions about advanced microelectronics research and development programs in this webinar:
  - Are informational, pre-decisional, and preliminary in nature.
  - Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
  - Are subject in their entirety to any final action by NIST or the Department of Commerce.
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Questions about this content?

•Email research@chips.gov

slido

In addition to workforce development, what is the biggest opportunity for digital twin technologies? (Pick 1)

ⓘ Start presenting to display the poll results on this slide.

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What are the biggest challenges that need to be solved to realize the full potential of digital twins for semiconductor manufacturing ? (Pick 2)

ⓘ Start presenting to display the poll results on this slide.

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What are the additional big challenges to developing digital twin technologies for semiconductor manufacturing?

ⓘ Start presenting to display the poll results on this slide.

CHIPS for America

$39 billion
for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

$11 billion
for R&D

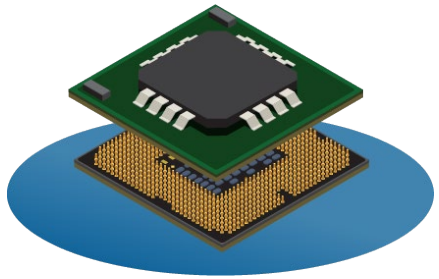
Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

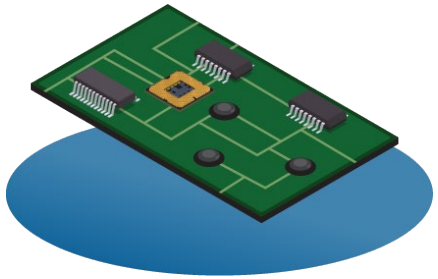
Plus CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

CHIPS R&D Programs

Metrology



National Semiconductor Technology Center



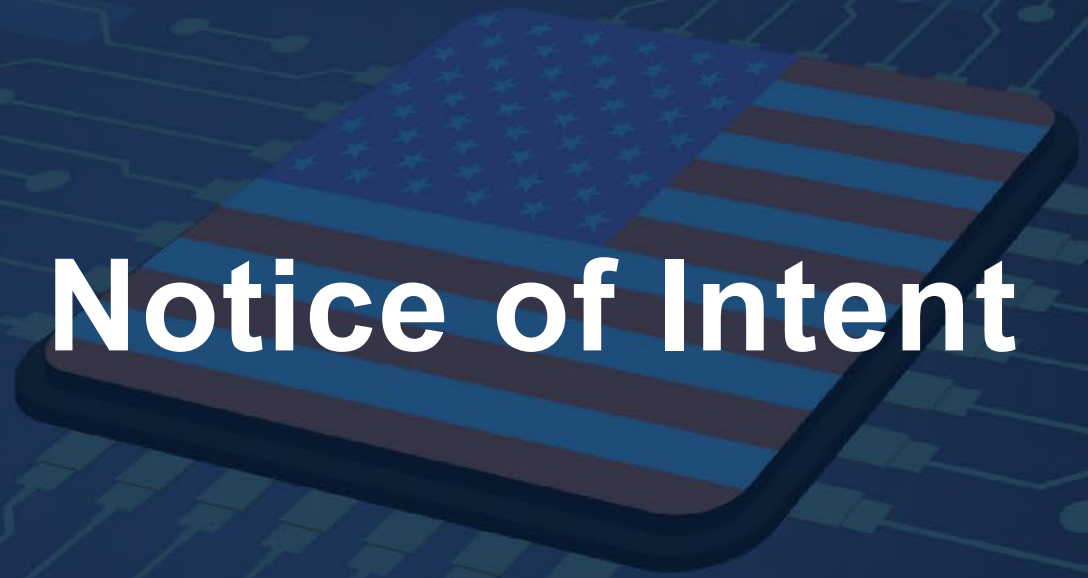
National Advanced Packaging Manufacturing Program

Manufacturing USA

Manufacturing USA Institute

Workforce Initiatives

Notice of Intent

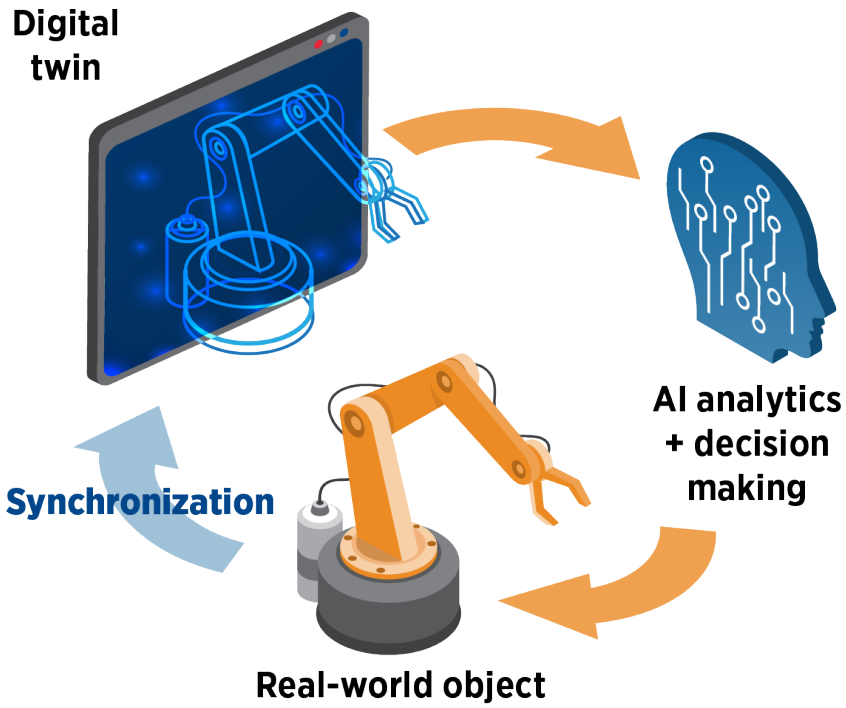


CHIPS Manufacturing USA Institute

- Establish one institute with the potential for significant impact on semiconductor manufacturing
- Topic: Digital twins
- Minimum expected NIST commitment ~$200 million over a five-year period
- Anticipate a greater than 1:1 cost share
- Analysis of RFI responses, industry feedback, listening sessions across 15+ engagements, and technology opportunities across the CHIPS R&D portfolio.

What is a digital twin?

- A **virtual** representation or model that serves as the real-time digital counterpart of a physical object or process.
- Benefits
  - Innovate faster and at less expense
  - Access feasible for small and medium businesses
  - Enhance training modalities
  - Shorten process design and validation times
  - Improve facility performance
- Challenges
  - Being able to produce and access the **data** needed to validate digital twins and power machine learning and AI tools
  - Strategic industry **collaboration**, which requires a neutral convener to build trust and bring together all parties to share the risks and rewards of working across boundaries
  - Significant **financial investment**, which is out of reach for small and medium-sized manufacturers to do themselves



Selection of Topic

CHIPS Manufacturing USA Institute on digital twins for manufacturing processes

Decision based on inputs from:

- Manufacturing USA – RFI for Semiconductor-Related Manufacturing USA Institutes
- CHIPS R&D Workshops
  - September 2023 Standards Summit
  - December 2023 Chiplet and Digital Twin Standards
- PCAST and CHIPS IAC recommendations
- Stakeholder meetings

Carol Handwerker

Digital Twins to Revolutionize Lab-to-Fab Transitions

Semiconductor Industry Needs

- CHIPS for America Industrial Advisory Committee
- SRC Roadmap for Microelectronics and Advanced Packaging Technologies
- NIST Semiconductor Metrology and Standards Workshops
- IPC Workshop on Advanced Packaging and Roadmap for Industry 4.0

Industrial Advisory Committee Recommendations

Establish five key capabilities aimed to lower the barriers to entry and success for innovators. These capabilities will rely on **a network of physical and virtual facilities.**

- Establish easily accessible prototyping capabilities in multiple facilities and enact the ability to rapidly try out CMOS+X at a scale that is relevant to industry
- Create a semiverse digital twin

Pervasive AI-enabled deep learning and model development applied to semiconductor R&D, design, and manufacturing

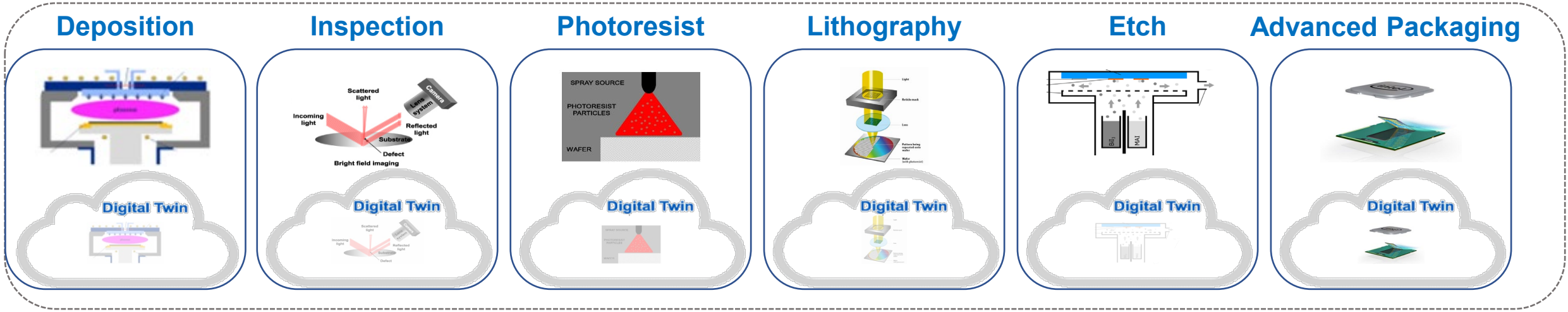
- Establish chiplets ecosystem and 3D heterogeneous integration platform for chiplet innovation and advanced packaging
- Build an accessible platform for chip design and enable new EDA tools that treat 3D (monolithic or stacked) as an intrinsic assumption
- Create a nurturing ecosystem for promising startups

Industrial Advisory Committee Recommendations

Identify a small number of application-driven grand challenges to inspire innovation across the computing stack and spans fundamental materials, equipment and process R&D; design and manufacturing.

- Improve computing energy efficiency by 1,000X in a decade including leveraging domain specific accelerators and architectures, and innovation in materials, process and equipment technologies.
- Develop and implement next-generation semiconductor manufacturing that is 10X more capital and human resource efficient and achieve net zero emissions with minimum waste and demonstrated sustainable materials in the next decade.
- CHIPS Act R&D programs to prioritize additional application grand challenges with advice from stakeholders

Semiconductor Manufacturing Process Flow



Ultimate product is a device:

- Co-design: function, process, materials, tools
- 1000+ process steps
- 70+ masks
- Hundreds of materials
- Hundreds of different tools

Digital twin: AI-enabled model development through an integrated system of tools, materials, processes, sensors, algorithms, data analytics

Use of AI at the Edge in a Smart Factory - Micron Example

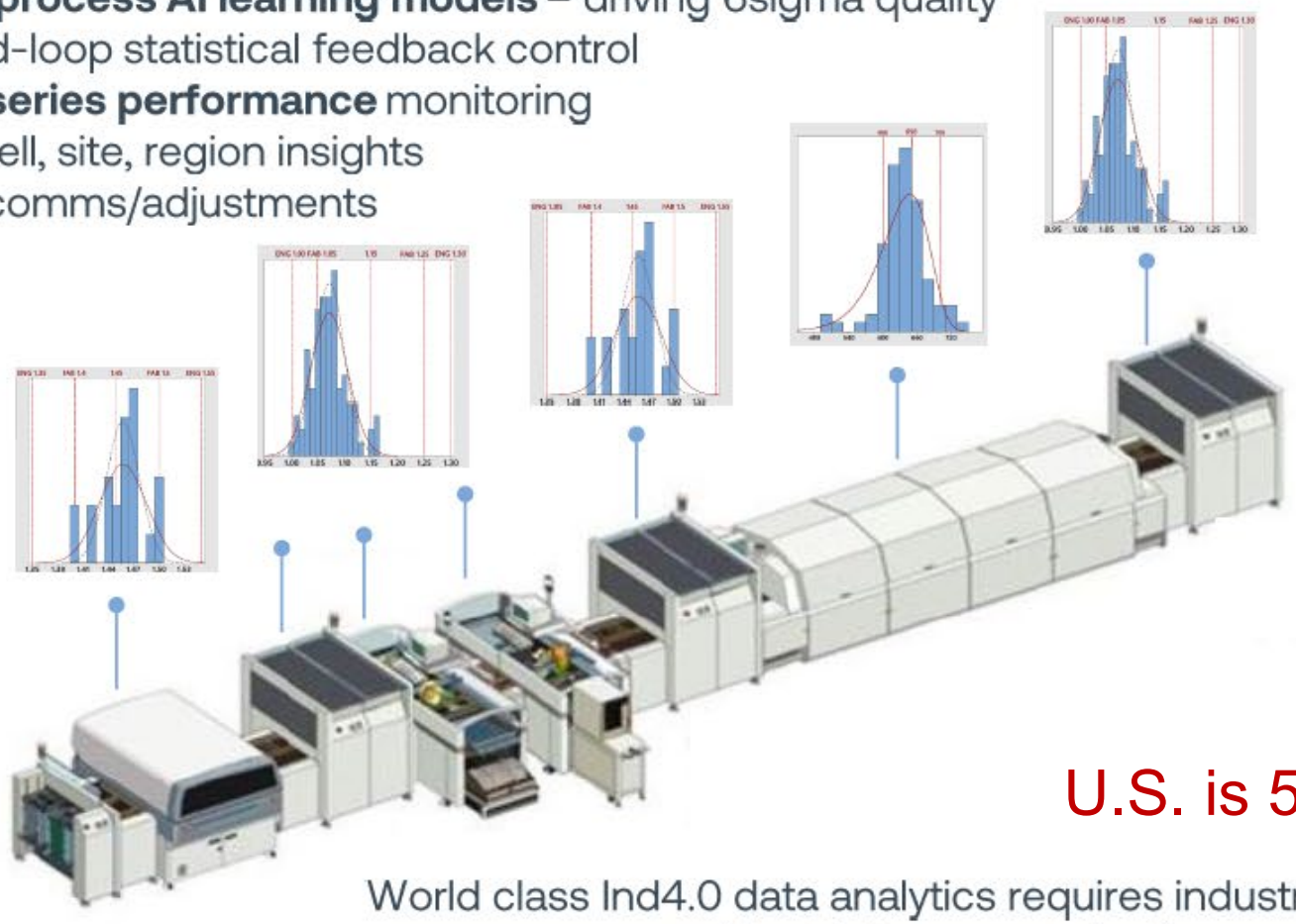
- **AI to improve factory efficiency**
  - Need data analysis locally, at the factory
- **Deploy IoT platform for early detection with IoT sensors (image, acoustic, video)**
  - Infrequent events, detect low-frequency, high-impact events
  - Automate root-cause analysis and prescribe action
  - Example: Detect dispense of nozzle tip and nearby area, time period of dispense (if irregular, stop tool)
  - Install on tools, such as photo tools
  - “Image analytics” detect deviation from standard to decrease variability
- **Large amount of data, visually examine**
  - 470,000 sensors
  - 13 terabytes of data
  - 15.6 million wafer images weekly
- **Automatically provide diagnostics**

J. Vardaman, 2022

Challenge #3: Achieve high quality, yield, throughput – Data Analytics

Manufacturing line – secure, real-time, big data sets (FEOL, BEOL)

- **Individual process control**, reports, Cp, Cpk, dashboards
- **Multi-process AI learning models** – driving 6sigma quality
- Closed-loop statistical feedback control
- **Time series performance** monitoring
- Line, cell, site, region insights
- M2M comms/adjustments



U.S. is 5-8 years behind Asia-Pacific

World class Ind4.0 data analytics requires industry-wide,
open-source machine data communication protocol eg) IPC-2591 CFX

IPC – Matt Kelly, 2021

300 mm

(1) Late-stage Prototyping
at Advanced Nodes
No Process Changes

(2) Mid/Late-stage Prototyping
CMOS+X
Changes: Mostly BEOL, some FEOL

(3) Pathfinding
New Materials/Process Dev
Process Experimentation

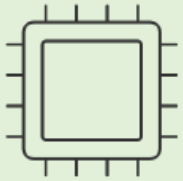
200 mm

(4) Mid/Late-stage Prototyping
CMOS + X
New Materials allowed

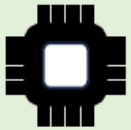
(5) Concept Hardening to
Mid-stage
Changes/New Materials allowed

(6) NSTC-enhanced
University Facilities
Coupons, 100/200 mm

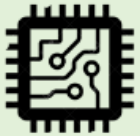
Packaging



(7a) Late-stage Prototyping
Standard Chiplet Interfaces
No or minimal changes



(7b) Pathfinding
Advanced + standard Packaging
Controlled changes allowed

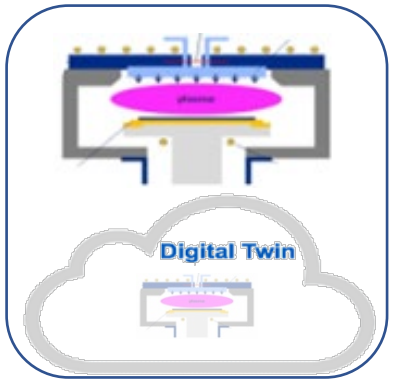


(7c)Early-Stage Proof-of-Concept
Process and tool development
Changes/New Materials allowed

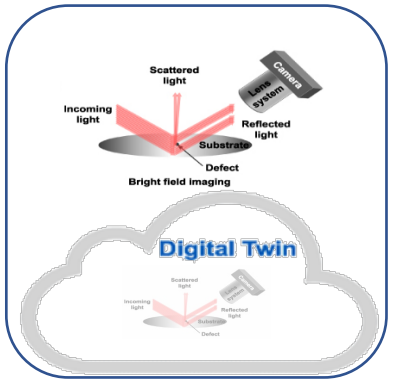
Innovation in Semiconductor Manufacturing

Development of digital twins for semiconductor prototyping and manufacturing: AI-based model development through integrated (materials, equipment, process) + metrology/sensors + AI/data analytics

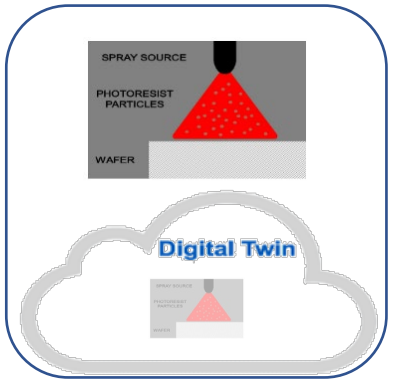
Deposition



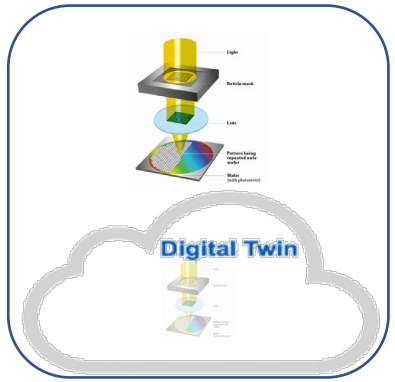
Inspection



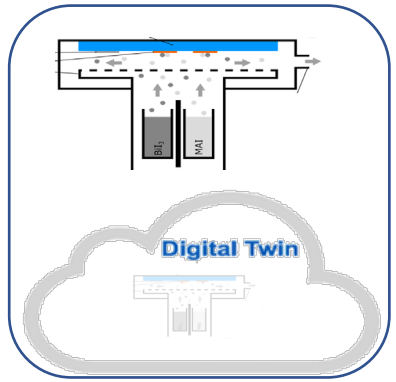
Photoresist



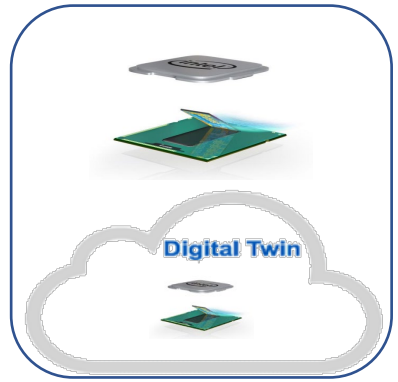
Lithography



Etch



Advanced Packaging



Level 1: Fixed Flow

- For innovations in chip design, process optimization, yield improvement …
- No new materials, equipment, or processes

Level 2: Modified Flow

- Introduce and optimize new materials, equipment, processes
- AI yields new models and interactions

Level 3: Integrated with Discovery

- Integrate manufacturing processes into discovery
- AI created new models and interactions to reduce time to manufacturing readiness

Eric Forsythe

CHIPS Digital Twin Manufacturing USA Institute

Digital Twin Institute

Vision

Enable **seamless integration of digital twin models** into the U.S. semiconductor manufacturing, advanced packaging, and assembly industries, enabling rapid adoption of innovations and enhancing domestic competitiveness for decades.

Mission

Foster a **collaborative environment** within the domestic semiconductor industry, enabled by the world's first **shared** semiconductor Digital Twin process **validation facility**, industry-relevant research projects, and digital-twin supported workforce training.

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For the shared facility to solve common industry challenges, what is the most important federal investment that will lead to private co-investment? (Pick 1)

ⓘ Start presenting to display the poll results on this slide.

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What other areas of this shared facility should receive federal investment?

ⓘ Start presenting to display the poll results on this slide.

Digital Twin Institute Objectives

Reduce the time and cost for chip development and manufacturing

Accelerate the adoption of semiconductor manufacturing innovations

Increase access to semiconductor manufacturing training through the adoption of digital twin-enabled tools

Expand access to digital twin tools, solutions and frameworks

Digital Twin Institute Approach

A physical facility and digital framework, integrated with industry-led research projects

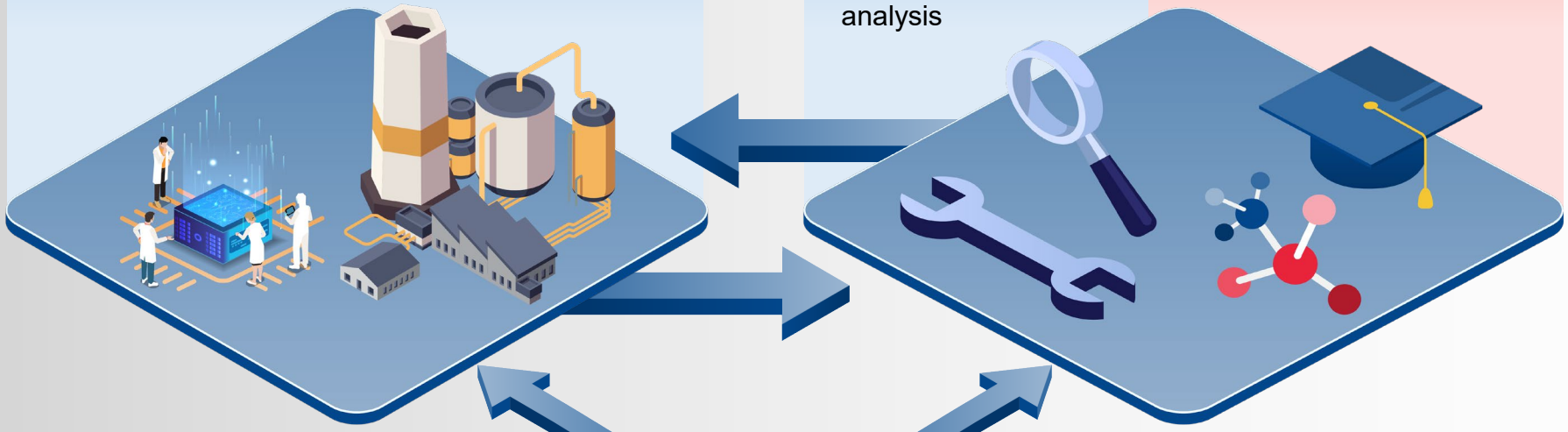
1 Establish a **shared physical facility**

Expected activities:
- Baseline facility testbed
- Digital emulation hardware
- Core technical & operations staff

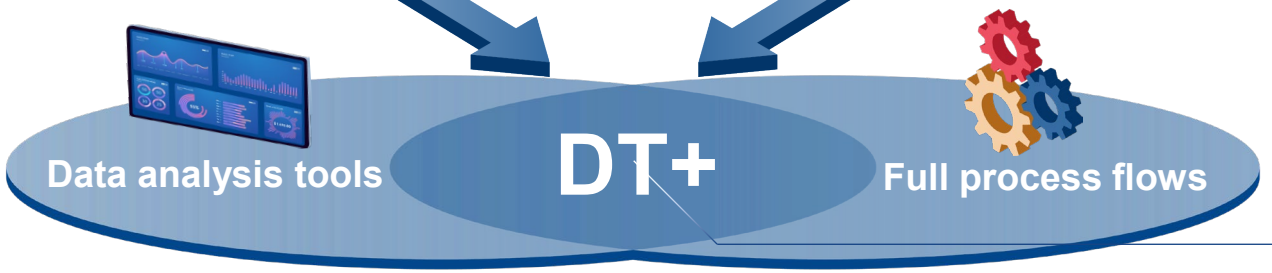
2 Competitively fund **industry-led technical and workforce development projects**

Deliver technical solutions, de-risk new tools, and conduct data analysis

Develop and test education & workforce development tools enabled by digital twins



3 **Digital framework** for interoperable data and models



4 Create a **shared marketplace** of digital twin models

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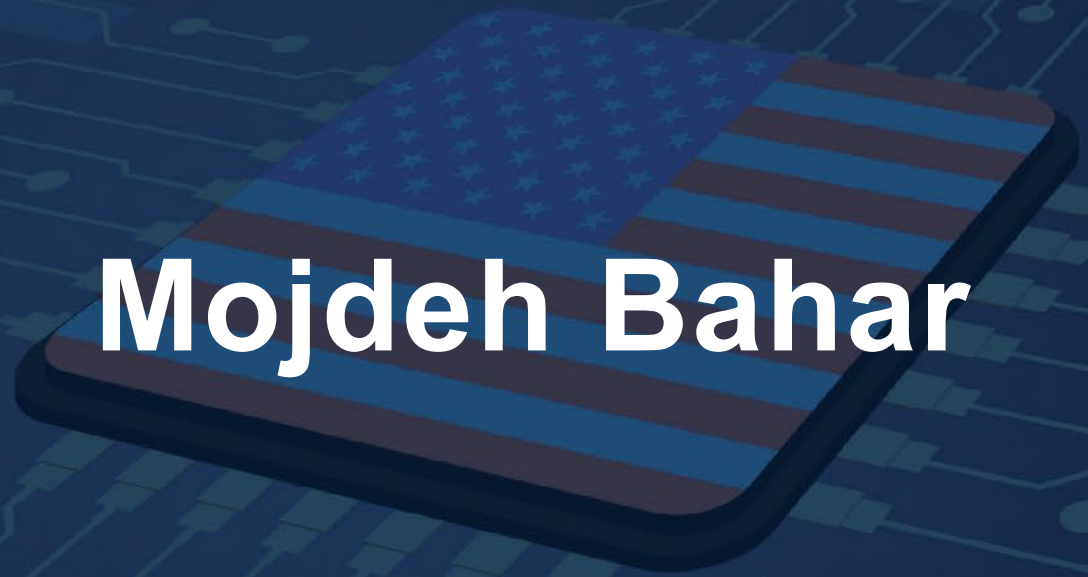
In addition to a shared facility, what institute-led technical project topics are most important to your organization? (Pick 3)

ⓘ Start presenting to display the poll results on this slide.

CHIPS for AMERICA



Mojdeh Bahar

Manufacturing USA

Manufacturing USA Vision and Mission

VISION: Securing U.S. Global Leadership in Advanced Manufacturing

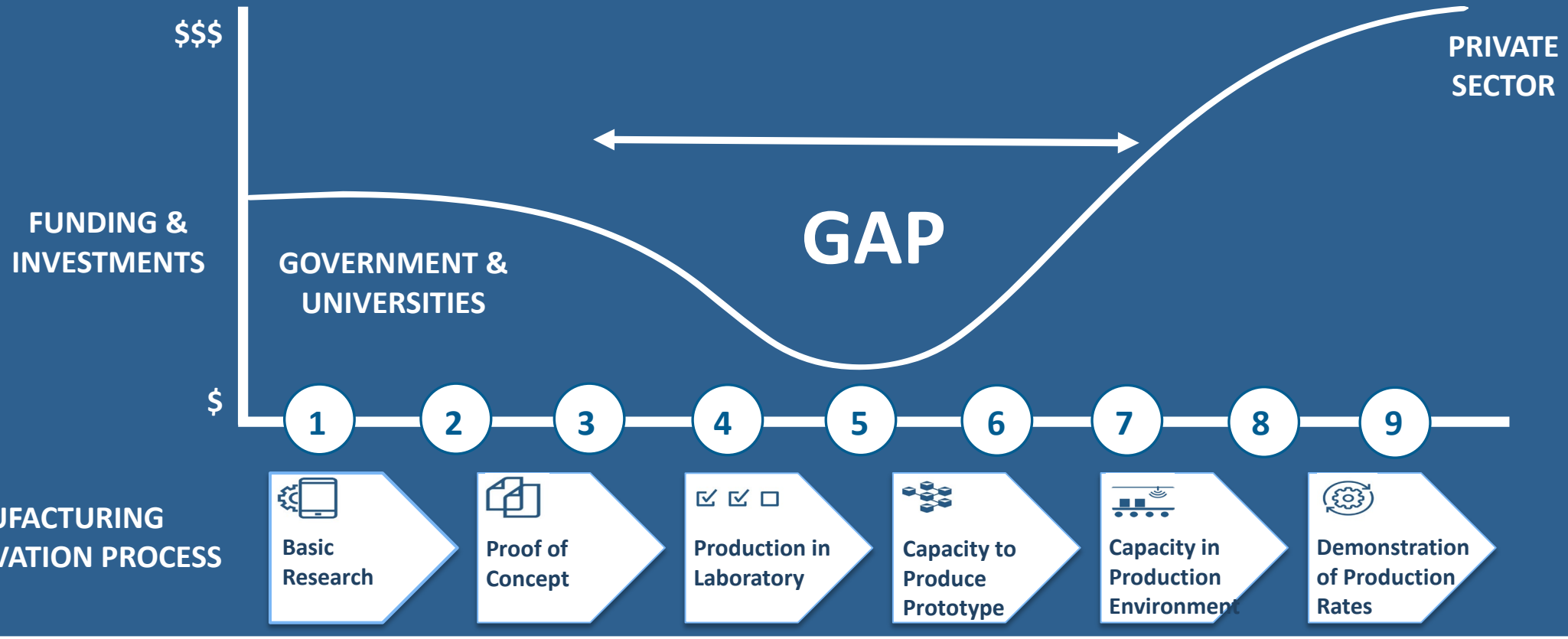
MISSION: Connecting people, ideas, and technology to:

- solve industry-relevant advanced manufacturing challenges
- enhance industrial competitiveness and economic growth
- strengthen our economic and national security

ManufacturingUSA

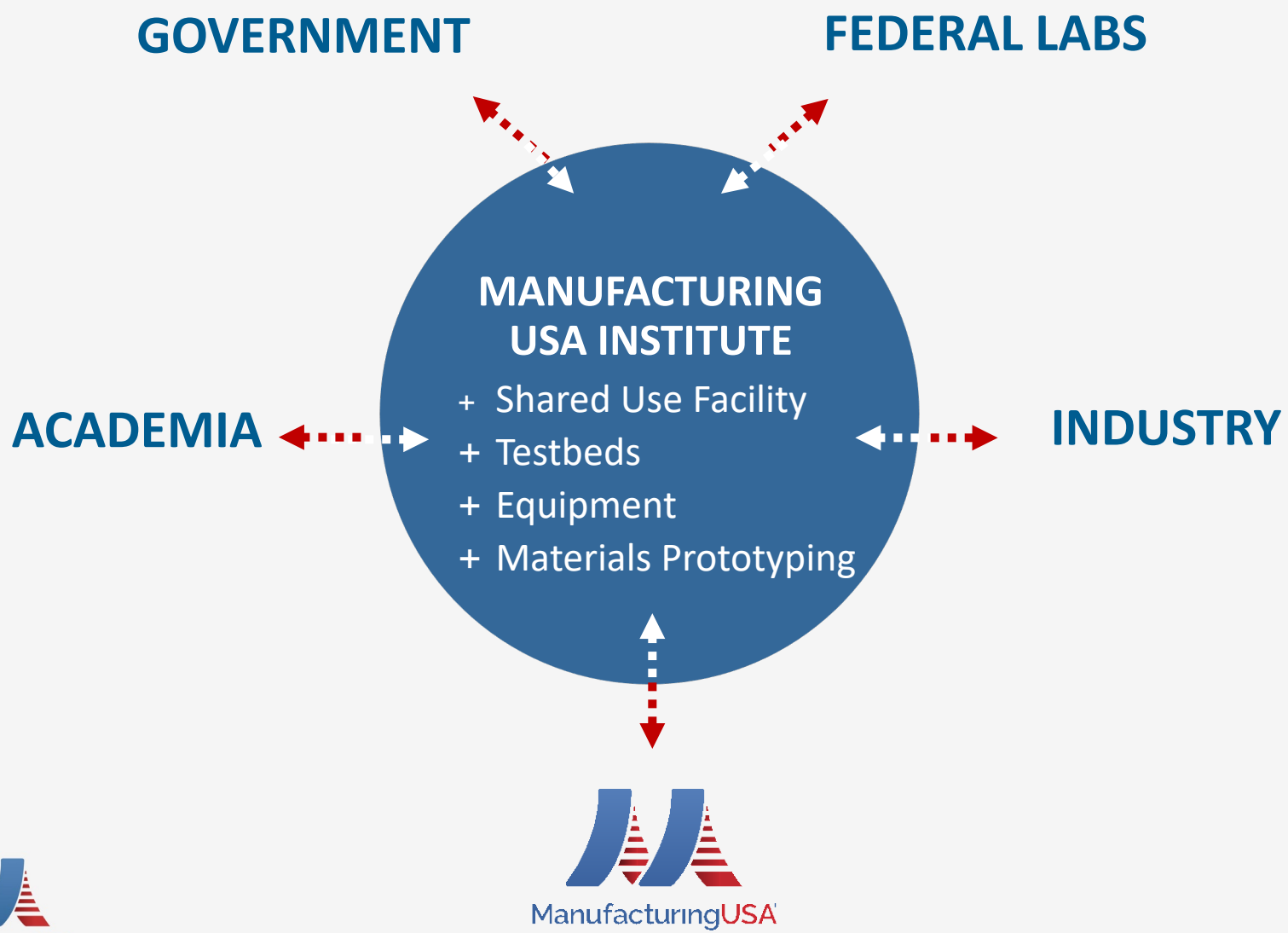
Manufacturing USA Purpose: Accelerate Discovery to U.S. Production

Create an effective collaboration environment for applied industry research to "bridge the gap" from discovery to production.



ManufacturingUSA

Institute Partnership Model



Common Institute Design:

- Industry-led public-private partnership
- Typically $70-120M federal investment
- At least 1:1 match with private funds
- Neutral convening for collaborations
- Each institute develops a unique technology
- Institutes address the education and workforce skills gap for their technologies

ManufacturingUSA

Manufacturing USA Network: 17 Institutes and Growing

ELECTRONICS

- AIM Photonics — Integrated Photonics — *Albany, NY; Rochester, NY*
- NextFlex — Flexible Hybrid Electronics — *San Jose, CA*
- PowerAmerica — Wide Bandgap Semiconductors — *Raleigh, NC*

MATERIALS

- AFFOA — Advanced Fibers and Textiles — *Cambridge, MA*
- IACMI — Advanced Composites — *Knoxville, TN; Detroit, MI*
- LIFT — Advanced Materials — *Detroit, MI*

ENERGY/ ENVIRONMENT

- RAPID — Modular Chemical Process Intensification — *New York, NY*
- REMADE — Sustainable Manufacturing — *Rochester, NY*
- CESMII — Smart Manufacturing — *Los Angeles, CA*
- EPIC — Industrial Process Decarbonization — *Tempe, AZ*

DIGITAL/ AUTOMATION

- America Makes — Additive Manufacturing — *Youngstown, OH; El Paso, TX*
- ARM Institute — Advanced Robotics & AI — *Pittsburgh, PA*
- MxD — Digital Manufacturing & Cybersecurity — *Chicago, IL*
- CyManII — Cybersecurity in Manufacturing — *San Antonio, TX*

BIO-MANUFACTURING

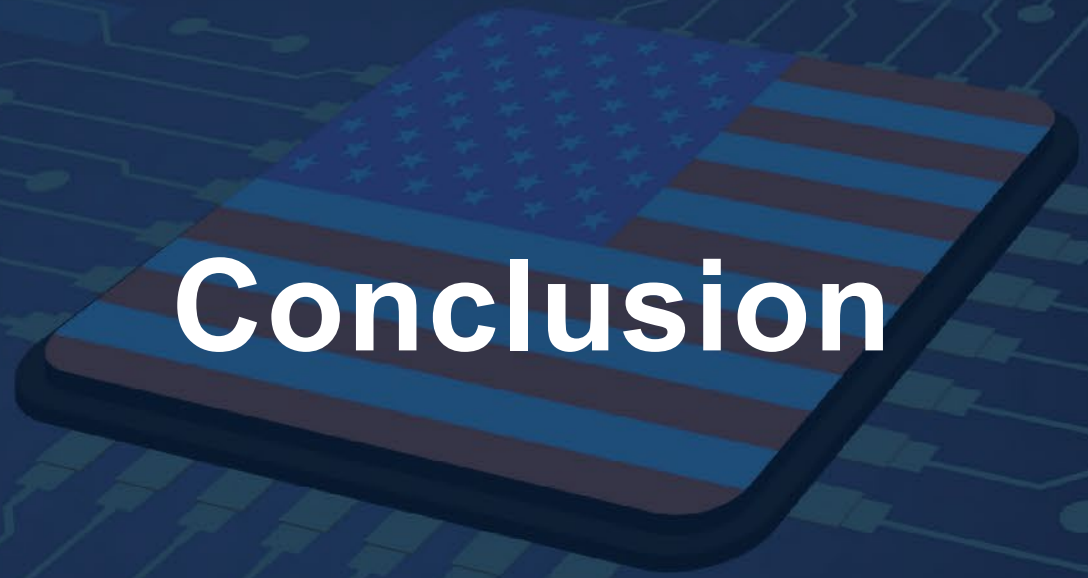
- BioFabUSA — Regenerative Manufacturing — *Manchester, NH*
- NIIMBL — Biopharmaceutical Manufacturing — *Newark, DE*
- BioMADE — Bioindustrial Manufacturing — *St. Paul, MN*

ManufacturingUSA

+ New CHIPS Manufacturing USA institute

Upcoming NIST competition for another new institute

ManufacturingUSA.com



Conclusion

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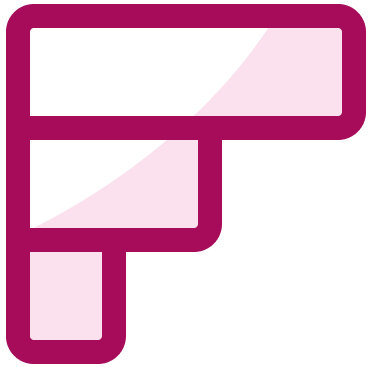


What areas would be most important for your organization to co-invest in, based on the value you expect to receive? (Ranking)

ⓘ Start presenting to display the poll results on this slide.

Next Steps

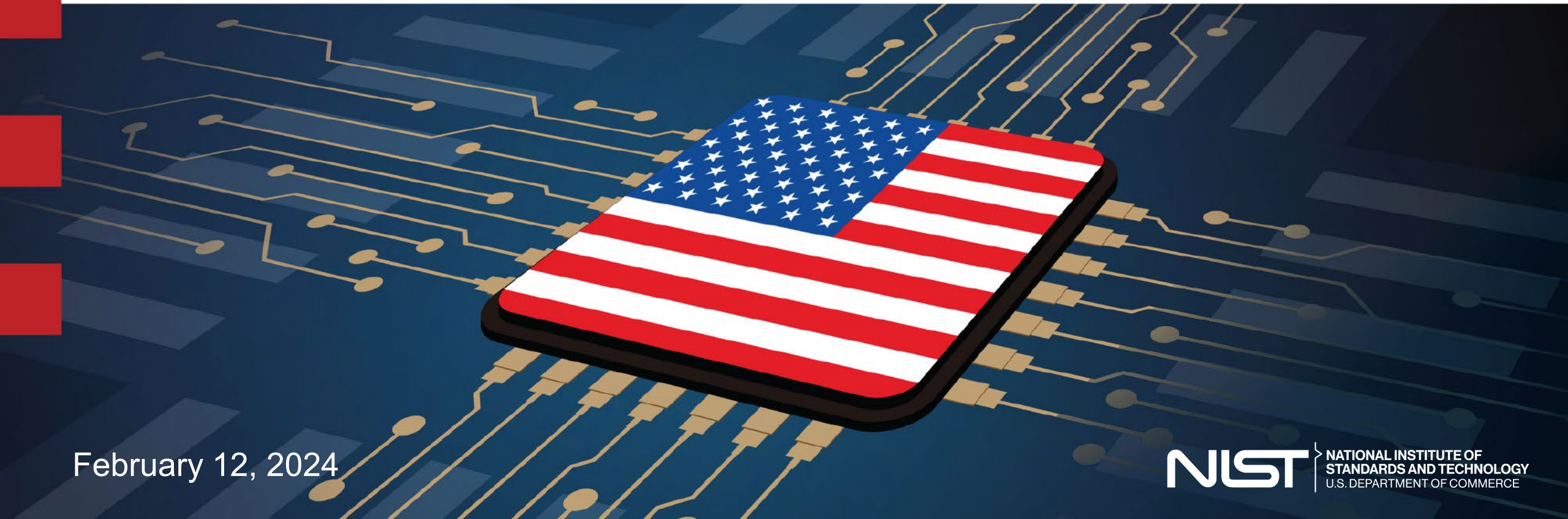
- Notice of Funding Opportunity — Spring of 2024
- Webinars and Proposer Days
- Sign up for emails from CHIPS.gov for details on webinars, events, and funding opportunities
- Send your outstanding questions to research@chips.gov

Thank you

CHIPS Manufacturing USA Institute

CHIPS Digital Twin Industry Day

Break Out Sessions



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Break Out Room Participants

- Please have your microphone muted when not speaking.
- Please use the raise hand feature to contribute. You will be called on in turn.
- Please list your name and affiliation in the participant list.
  - Select the three dots … on your image or next to your name in the participant list.
  - Select ‘rename’
  - Indicate your name and affiliation
- All additional comments can be sent to research@chips.gov

Breakout Session 1

Key Research Projects

1. In your opinion, what are the key research problems we need to solve to make digital twin tools that contribute to an accelerated innovation cycle?
2. In your opinion, what are the most impactful digital twin problems that member-led research projects in this institute should address?
    a. How should investments in member-led projects be distributed between manufacturing readiness levels 4-7 (where solutions are often shared) versus higher MRLs (where solutions are proprietary and only general outcomes are shared)?
    b. How should we balance investment between shared industry challenges and specific member-led projects?

Breakout Session 2

Physical Testbed

1. If we set up a Manufacturing USA digital twin shared facility, what are the most important gaps for federal funds to address that can maximize innovation and participation from a company like yours?
    a. In your opinion, what should the institute invest in for your sector to get the most benefit?
    b. What kind of participation do you imagine for your company?
    c. If your company were to participate in a shared facility, what co-investment might you provide? Under what terms?