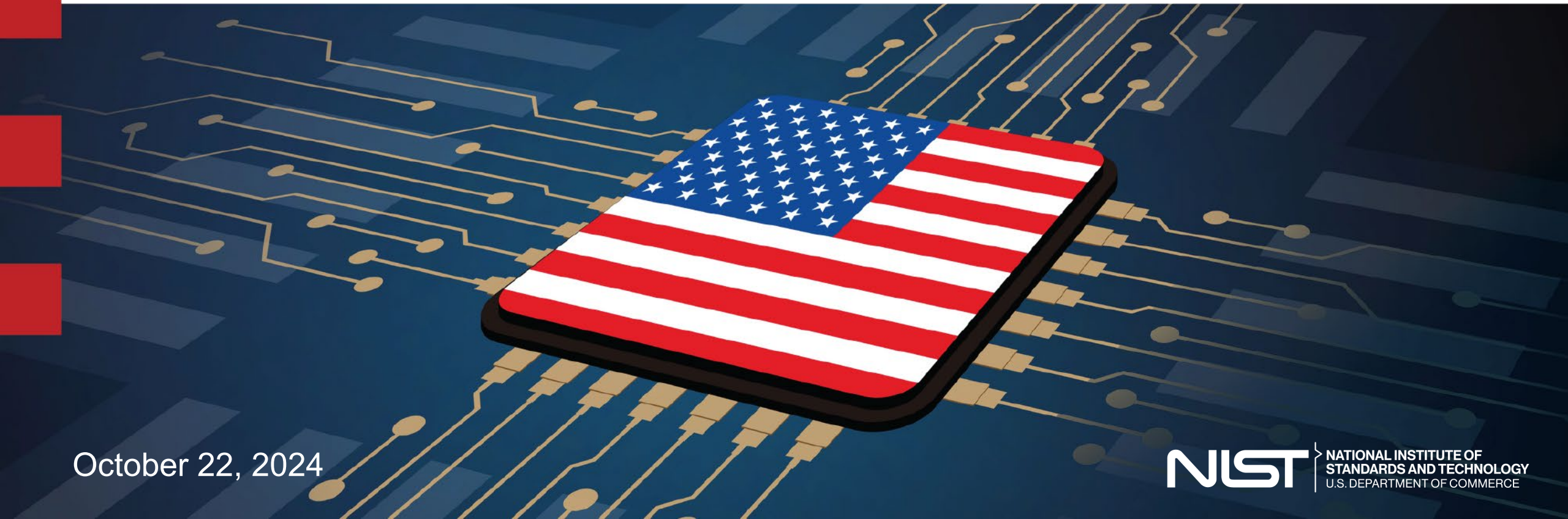
CHIPS for America

Advanced Packaging Research & Development Proposer's Day



October 22, 2024

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Disclaimer

- Statements and responses to questions about advanced packaging research and development programs in this presentation:
  - Are informational, pre-decisional, and preliminary in nature.
  - Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
  - Are subject in their entirety to any final action by NIST or the Department of Commerce.
- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity.

Morning Agenda (AM ET)

Time	Session	Speaker
7:30AM – 8:30AM	Check-in	
8:30AM – 8:40AM	Welcome Remarks	**Laurie Locascio** Director of NIST and the Under Secretary of Commerce for Standards and Technology
8:40AM – 8:45AM	Proposer's Day Expectations	**Dev Palmer** Director, CHIPS NAPMP
8:45AM – 9:00AM	NAPMP Program Overview	**Subu Iyer** Senior Technical Advisor, CHIPS NAPMP
9:00AM – 9:30AM	Advanced Packaging Research & Development (R&D) NOFO Overview	**Dev Palmer** Director, CHIPS NAPMP
9:30AM – 10:00AM	CHIPS R&D Office Policy Overview	**Richard-Duane Chambers** Director, Policy and Integration CHIPS R&D Office
10:00AM – 10:30AM	Networking/Break	
10:30AM – 10:45AM	Research Security	**Greg Strouse** NIST Safeguarding Science Research Security Director
10:45AM – 11:00PM	Application Preparation and Submission	**Shanell Williams** Other Transaction Agreements Officer
11:00AM – 12:00PM	Question and Answer Panel	**Panel:** Dev Palmer, Richard-Duane Chambers, Greg Strouse, Shanell Williams

Afternoon Agenda (PM ET)

Time	Session	Speaker
12:00PM – 1:30PM	Networking and Lunch (on own)	
1:30PM– 1:40PM	Afternoon Instructions	
	Research and Development Areas	
1:40PM – 1:50PM	Equipment, Tools, Processes, and Process Integration	**Bob Soave** Program Manager
1:50PM – 2:10PM	Facilitated Feedback	
2:10PM – 2:20PM	Power Delivery and Thermal Management	**David LaVan** Program Manager
2:20PM – 2:40PM	Facilitated Feedback	
2:40PM – 2:50PM	Connectors (Photonics & RF)	**Chris Myatt** Program Manager
2:50PM – 3:10PM	Facilitated Feedback	
3:10PM – 3:40PM	Networking/Break	
3:40PM – 3:50PM	Chiplets Ecosystem	**Bapi Vinnakota** Program Manager
3:50PM – 4:10PM	Facilitated Feedback	
4:10PM – 4:20PM	Co-design/Electronic Design Automation (EDA)	**Rob Aitken** Program Manager
4:20PM – 4:40PM	Facilitated Feedback	
4:40PM – 4:50PM	NAPMP Next Steps	**Dev Palmer** Director, CHIPS NAPMP
4:50PM – 5:10PM	Facilitated Feedback	
5:10PM – 5:15PM	Closing	

Proposer's Day Expectations

Dev Palmer

Proposer's Day Expectations

Agenda

- NAPMP Program Overview
- Advanced Packaging R&D Overview
- CHIPS R&D Policy Overview
- Application Process
- Answers to Questions
- R&D Area Overviews
- Next Steps for NAPMP

By the end, attendees should better understand

- Outcomes of the Advanced Packaging Program
- Requirements and Stages/Phases of the Advanced Packaging Program
- How to apply to Advanced Packaging NOFO
- The importance of teamwork!

CHIPS NAPMP Team

Dr. Dev Palmer
Director of NAPMP

Subu Iyer
Senior Technical Advisor

George Orji
Deputy Director

Dan Berger
Associate Director

Mike MacDonald
NAPPF Director

Bob Soave
Program Manager, Equipment, Tools, and Processes

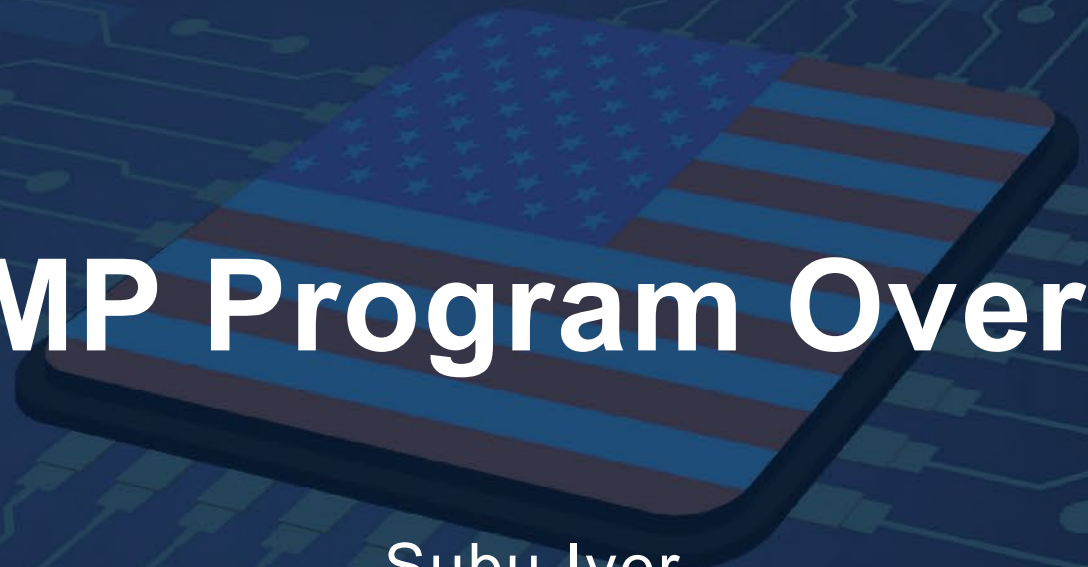
Aaron Forster
Program Manager, Materials and Substrates

Rob Aitken
Program Manager, Co-design and EDA

David LeVan
Program Manager, Thermal and Power

Bapi Vinnakota
Program Manager, Chiplets

Chris Myatt
Program Manager, Connectors



NAPMP Program Overview

Subu Iyer

Our Approach

1 Scale down: shrinking features on a package to near monolithic levels

- ✓ Making the features on the package approach those at the top level on a monolithic CMOS chip
- ✓ Connecting the dies to the package at pitches approaching the final via pitches on a chip
- ✓ Reducing the distance between dies that are assembled on a multi-chip package to approach the distance between IP blocks on a monolithic chip

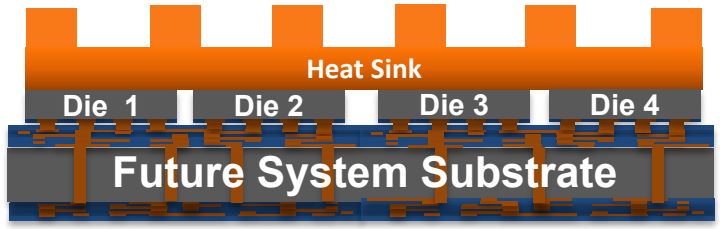
2 Scale out: increasing the number of intimately connected chips on a package

- ✓ Accommodate a larger number of closely packed heterogeneous die
- ✓ Address the power delivery, thermal dissipation and external connection challenges
- ✓ Develop standards and protocols to accommodate a large and diverse set of chips (Chiplets)

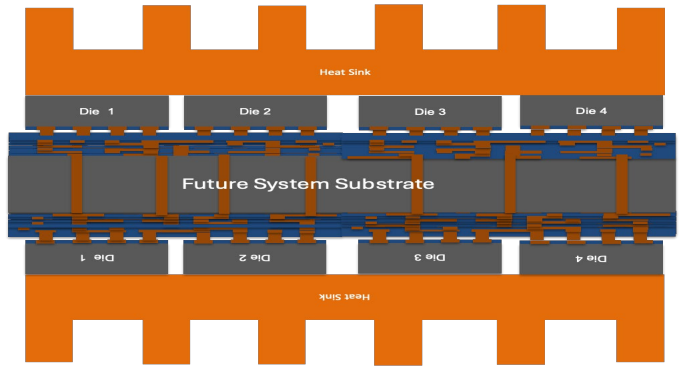
3 Blurring the boundary between monolithic chip and heterogeneous package

- ✓ Design chiplets and subassemblies similar to how we design monolithic chips
- ✓ But mix and match nodes, materials and technologies without limitations
- ✓ Use technologies developed in the NAPMP to achieve this

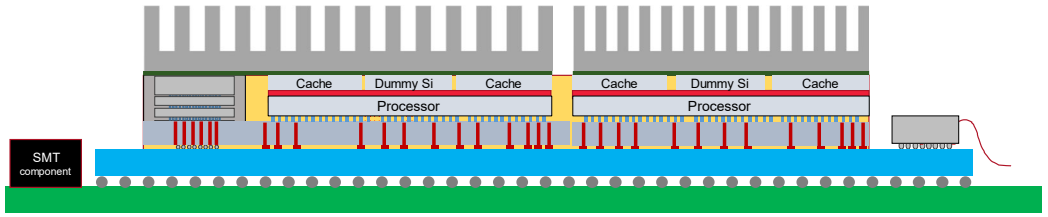
Scale-down by package simplification and modularity



Simple single level package built on a single substrate at sub 10μm bond pitch and CMOS-like wiring (wire abundance) with small (3DHI) chiplets



Double-sided package with integrated high capacity thermal and power delivery solutions and integrated EDA with built in test and repair

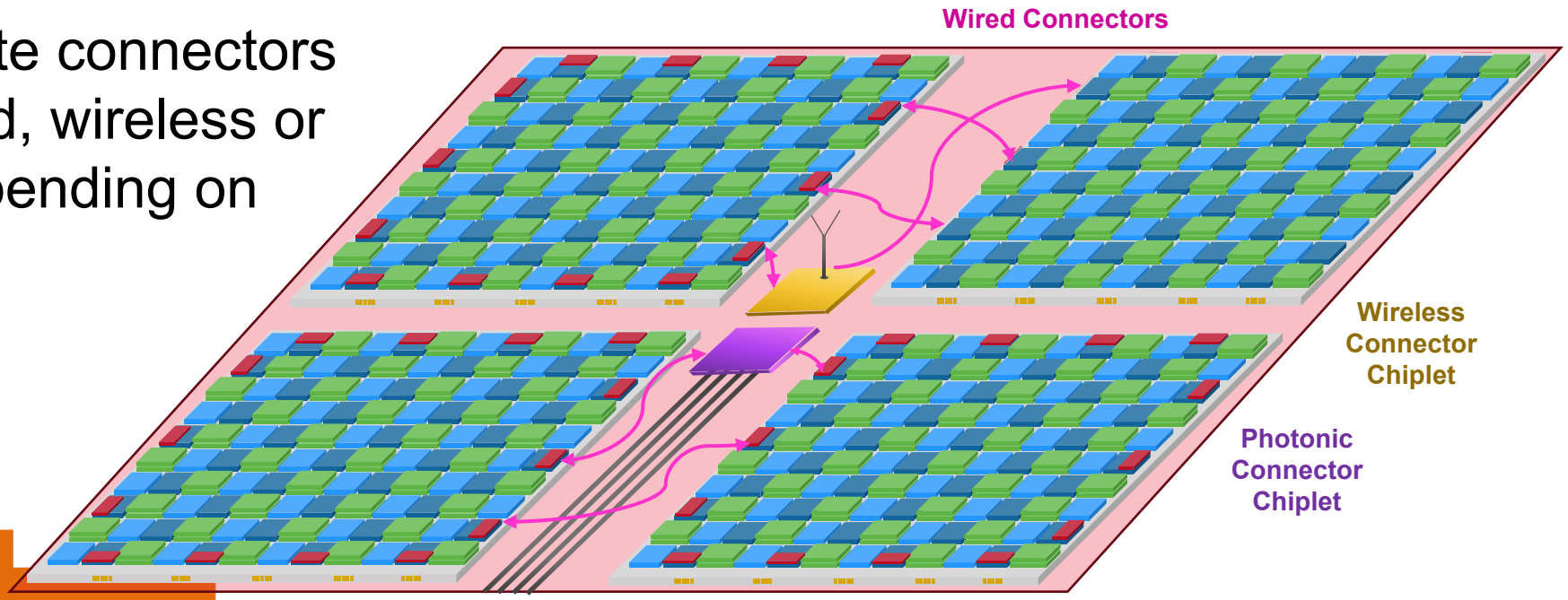


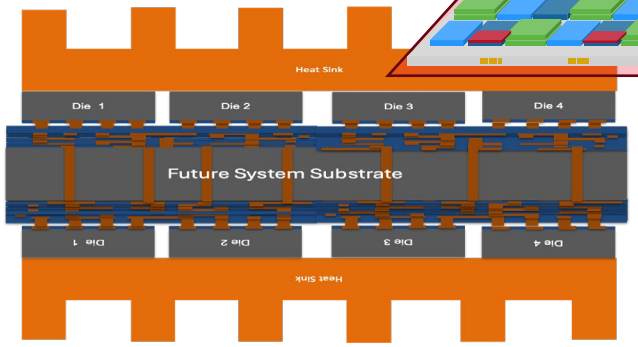
Today's complex multilevel package are adapted to legacy platforms

- Simpler automated processes
- Modular with easily customizable designs based on easily available chiplets that communicate using wire-based protocols
- Shorter times to market
- Adaptable to both high performance and low power

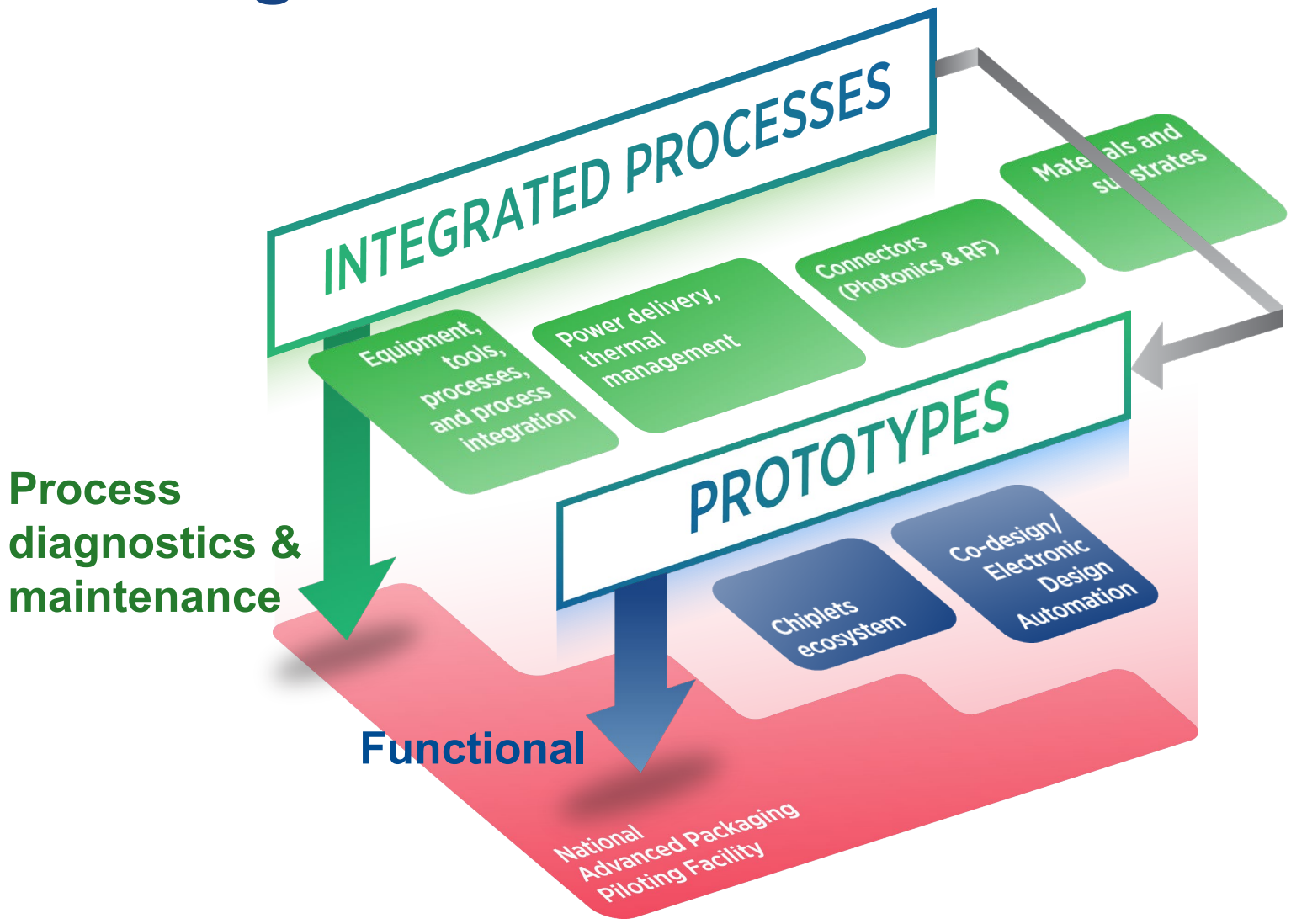
Scale out using many large area advanced substrates using connector technology

High data-rate connectors may be wired, wireless or photonic depending on length span





NAPMP Integration



Advanced Packaging Research & Development (R&D) Overview

Dev Palmer

NOFO Objectives

1. The NOFO sets out, across multiple R&D areas, key challenges and technology gaps in advanced packaging which must be addressed.

2. It provides for coordinated R&D efforts aligned through common technical targets so that results collectively contribute to composable and implementable advanced packaging flows.

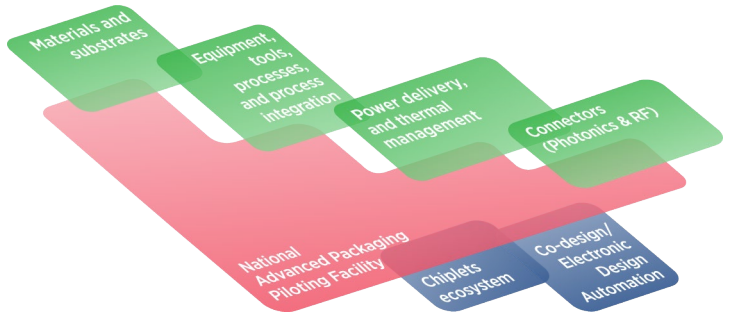
3. It provides for demonstrating the benefits of R&D results through a combination of prototypes and baseline packaging flows.

Program Drivers

Scale-Down and Scale-Out	Heterogeneous Integration Including Chiplets	End-to-End Advanced Packaging Flows	Prototypes for Demonstrating Functionality	Aligning R&D Efforts for Implementable Packaging Flows
Scaling-down refers to shrinking the size of the features on the package and increasing interconnect densities. Scaling out refers to increasing the number of chips assembled on the substrate and overall functional density in both two-dimensional (2D) and three-dimensional (3D) architectures	This driver focuses on the NAPMP vision for creating "an advanced packaging ecosystem based on heterogeneous chiplet technology to promote widespread and easy use of the technologies developed."	This driver addresses the NAPMP objective to "develop packaging platforms capable of both high-volume and customized manufacturing."	This driver addresses the NAPMP vision for enabling "successful advanced packaging development efforts to be validated and transitioned at scale to U.S. manufacturing."	The final program driver is aligning R&D efforts so that R&D results are not isolated or incompatible, but instead collectively contribute to implementable advanced packaging flows.

R&D Areas

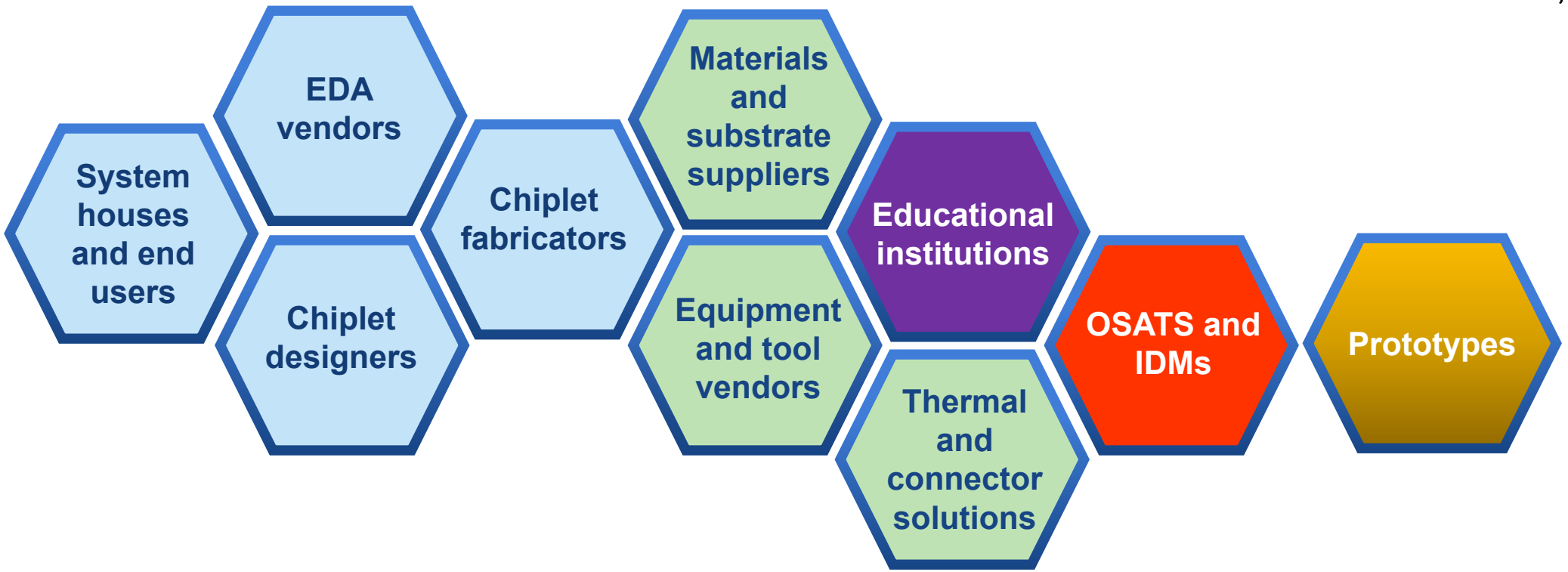
1. Equipment, Tools, Processes, and Process Integration
2. Power Delivery and Thermal Management
3. Connector Technology, Including Photonics and Radio Frequency (RF)
4. Chiplets Ecosystem
5. Co-design/Electronic Design Automation (EDA)



Funding Details

- **Total amount:** Up to ~$ 1.55 Billion covering five R&D areas plus prototypes with advanced packaging flows to be implement in the NAPPF
- Anticipated individual awards from a minimum of ~$10 Million to a maximum of ~$150 Million depending on scope, with a period of performance of up to 5 years per award
- Co-investment encouraged
- **Eligible:** Companies (profit & not-for-profit), accredited institutions of higher education, state and local governments, FFRDCs – applicants must be domestic entities
- Funding for the National Advanced Packaging Piloting Facility (NAPPF) is excluded from this NOFO; technical areas must flow into NAPPF
- Teaming is essential in all areas

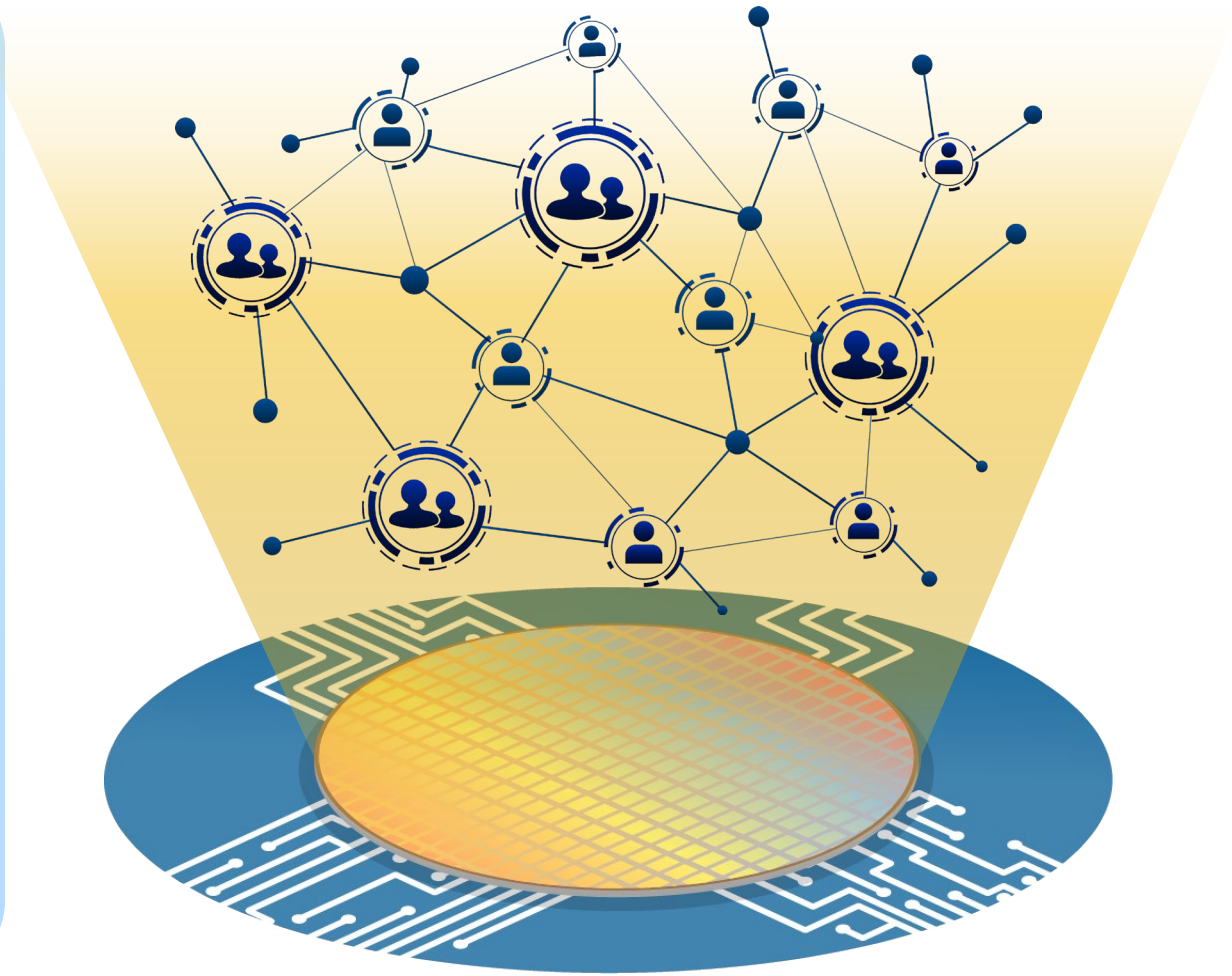
Collaboration is Critical for Success



Successful execution will require collaboration between proposers and each R&D Area. Proposers must clearly understand the ideas presented in each R&D Area. We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.

Benefits of Teaming

- Complementary skillsets
- Shared goals
- Trust and commitment
- Diversity of experiences, backgrounds, locations and even work status
- Open communication
- Small business / start-up engagement
- Inclusion of education and workforce development



Application Process

Step	Description
1 Concept Paper	**Mandatory Concept paper broadly describes approach to technical areas, impacts, plans, project team, capabilities, and budget estimates.** There is a 10 page limit on concept paper narrative. A merit assessment of eligible, complete, and responsive concept papers. Successful applicants will be invited to submit full applications. Submission instructions contact NOFO@nist.gov with opportunity number 2025-NIST-CHIPS-NAPMP-01 in subject
2 Evaluation	**Merit Reviews will be conducted for Concept Papers**. Reviews will consider criteria: Relevance to economic and national security; Overall scientific and technical merit; Project management; and transition and impact strategy.
3 Full Application	**Full Applications are a detailed proposal describing project description, impacts, team, technical plan, EWD, Research Security, CVDP, and IP management. This is not an exhaustive list.** Submission of full applications will be through Grants.gov.
4 Evaluation	**Merit Reviews will be conducted for Full Applications**. Reviews will consider criteria: Relevance to economic and national security; Overall scientific and technical merit; Project management; and transition and impact strategy.

Concept Paper Requirements

	Key Forms and Documents	Description
A	**Cover Sheet**	A one-page document that does not contribute to concept paper narrative page limit
B	**Executive Summary**	Executive Summary is a one-page summary/abstract suitable for dissemination to the public. It should be a self-contained document that broadly describes project team, objectives, impacts, and education/workforce goals.
C	**Quad Chart**	Quad chart format selected by applicant that contains problem statement, proposed solution, concept of project, technical objectives and key participants.
D	**Table of Contents**	For concept paper narrative, does not contribute to page limit
E	**Concept Paper Narrative**	The concept paper narrative is a word-processed document of no more than 10 pages and must contain the following: project impact statement, project-level technical plan, project-level non-technical plan, project team, and budget estimate. Applicants and recipients should have an active registration in SAM.gov
F	**Budget Summary**	Budget must be between $10,000,000 and $150,000,000. Construction activities are not an allowable cost under this program. However, costs related to internal modifications of existing buildings that would be necessary to carry out the proposed research tasks may be allowed, at NIST's sole discretion. In addition, recipients and subrecipients may not charge profits, fees, or other increments above cost to an award issued pursuant to this NOFO

Concept Paper Evaluation Criteria

1	**Relevance to Economic and National Security**	• This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals, as expressed in Section 1.1.1.
2	**Overall Scientific and Technical Merit**	• This criterion addresses the quality, innovativeness, and feasibility of the proposed Concept Paper Narrative and the potential for meeting the objectives of this NOFO, as expressed in Section 1.1.3.
3	**Project Management**	• This criterion addresses the degree to which applicants demonstrate that they have the appropriate personnel and access to required equipment and facilities
4	**Transition and Impact Strategy**	• This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to workforce development and the broader domestic research, development, and innovation ecosystem.

Full Application Requirements

	Key Forms and Documents	Description
A	**Forms**	SF-424, Research & Related Budget, CD-511, Research and Related Other Project Information, SF-LLL
B	**Project Narrative**	The Project Narrative is a word-processed document of no more than twenty-five (25) pages (single-spaced between lines), which is responsive to the program description and the evaluation criteria.
C	**Resume(s) or CV(s)**	Not to exceed 2 pages per individual. These do not contribute to the Project Narrative page limit. Resumes or CVs are required for all key personnel including the principal investigator(s).
D	**Budget Narrative and Justification**	Not to Exceed 5 pages. These do not count against the Project Narrative page limit. There is no set format for the Budget Narrative and Justification; however, the written justification should include the necessity and the basis for the cost, as described in NOFO. See section 4.6.1.2.
E	**Additional Documents**	Indirect Cost Rate Agreements, Subaward Budget Form, Letters of Commitment and/or Interest, Data Management Plan, Current and Pending Support Forms

Concept Paper Review Process

1	**Initial Review**	• Concept papers and full applications received by the respective deadlines will be reviewed to determine eligibility, completeness, and responsiveness to this NOFO and stated program objectives.
2	**Review of Concept Papers**	• Merit Review, Evaluation Panel, Adjectival Rating.
3	**Selection of Successful Concept Papers**	• Selection of Successful Concept Papers and Invitations to Submit Full Applications.

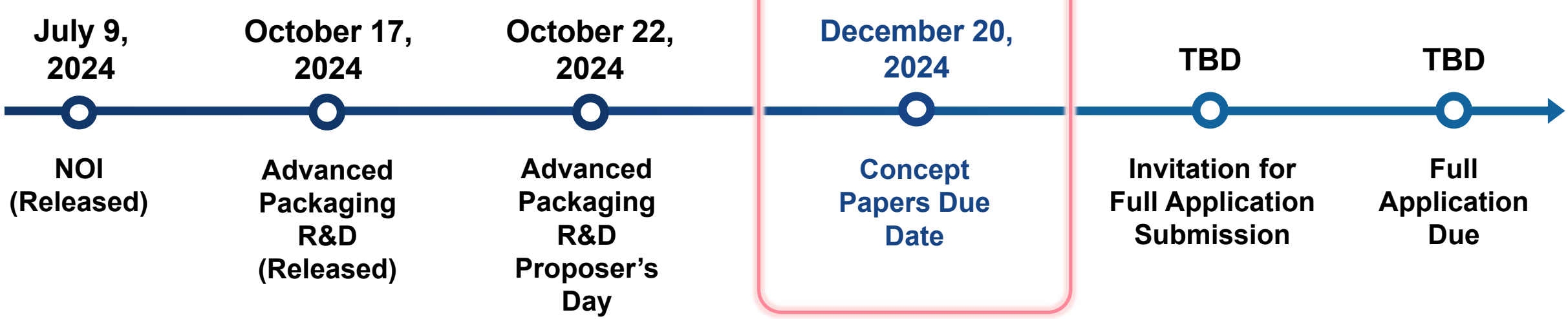
Full Application Evaluation Criteria

1	**Relevance to Economic and National Security**	• This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals (See Section 1.1.1).
2	**Overall Scientific and Technical Merit**	• This criterion addresses the quality, innovativeness, and feasibility of the proposed Concept Paper Narrative and the potential for meeting the objectives of this NOFO, as expressed in Section 1.1.3.
3	**Project Management**	• This criterion addresses the degree to which applicants demonstrate/ that they have the appropriate personnel and access to required equipment and facilities
4	**Transition and Impact Strategy**	• This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to workforce development and the broader domestic research, development, and innovation ecosystem.

Full Application Review Process

1	**Merit Review**	• At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate professional and technical expertise relating to the topics covered in this NOFO.
2	**Evaluation Panel**	• Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate technical expertise will conduct a panel review of the ranked applications.
3	**Pre-Selection Interviews and Site Visits**	• At CHIPS R&D's discretion, applicants may be requested to participate in Pre-Selection Interviews and/or Site Visits during the evaluation panel phase, either at CHIPS R&D, the applicant's site, or a mutually agreed upon location, or via conference call or webinar.
4	**Adjectival Rating**	• The evaluation panel will provide a final adjectival rating and written evaluation of each full application to the Selecting Official for further deliberation.
5	**Selection and Federal Awarding Agency Review of Risk Posed by Applicants**	• The Selecting Official will make final award recommendations. NIST will also conduct the research security review described in Section 2.7.6 and the results will be provided to the Selecting Official.

Key Dates



CHIPS for America QR Code:
CHIPS NAPMP NOFO 2
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CHIPS for America CHIPS R&D Office Policy Overview

Richard-Duane Chambers

Policy Overview Agenda & Objectives

Agenda

- Overview of CHIPS R&D Office Goals
- International Collaboration
- Unique Directives Informing Work
- Key Required Plans
  - Intellectual Property Rights Management Plan
  - Commercial Viability and Domestic Production
  - Education and Workforce Development
  - Research Security

By the end, attendees should better understand

- CHIPS R&D objectives and policy context
- CHIPS R&D domestic and international research requirements
- Key required plans for proposals

Overview of CHIPS R&D Office Goals

Vision

A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce, and leads the world in semiconductor research and innovation.

Mission

Accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic tools, resources, workers, and facilities.

2030 Goals

- **U.S. Technology Leadership:** The United States establishes the capacity to invent, develop, prototype, and deploy the foundational semiconductor technologies of the future.
- **Accelerated Ideas to Market:** The best ideas achieve commercial scale as quickly and cost effectively as possible.
- **Robust Semiconductor Workforce:** Inventors, designers, researchers, developers, engineers, technicians, and staff meet evolving domestic commercial-sector and government needs.

Policy and National Security Context

Unique or Emerging Directives

CHIPS and Science Act (2022)

- Prohibit Federal funding to participants in malign foreign talent recruitment programs
- Research security training

CHIPS Act (2021)

- Domestic production requirements
- Domestic control requirements to protect intellectual property from foreign adversaries
- Workforce initiatives as a required component of most CHIPS-funded activities

Executive Order 14080 (2022)

- Prioritize strengthening and expanding regional manufacturing and innovation ecosystems

National Security Policy Memorandum 33 (2021)

- Research security program requirements
- Disclosure of conflicts of interest / commitment

Application Requirements

- ❑ Foreign Partner Justification
- ❑ Intellectual Property Rights Management Plan
- ❑ Commercial Viability and Domestic Production (CVDP) Plan
- ❑ Education and Workforce Development (EWD) Plan
- ❑ Research Security Plan

Domestic & Int'l Research Requirements

"NIST adheres to the principle that U.S. research leadership benefits from mutually beneficial international collaborations, including welcoming international scientists"

- **Lead applicant must be a domestic entity;** foreign organizations, excluding foreign entities of concern (FEOCs), can participate.
- **Funded R&D activity should occur in the United States** but CHIPS R&D may approve the completion of certain tasks outside the United States.
- **Any disbursement of funds** outside the United States **must be approved by CHIPS R&D.**

Justification for Foreign Participant:

- Foreign partner's involvement is essential to program objectives
- Applicant and foreign partner have adequate IP and data protection agreements in place.
- The partnership doesn't jeopardize the project's pathway to domestic production.
- Foreign partner is not based in a foreign country of concern.
- Foreign partner agrees to comply with nondisclosure agreements, laws and regulations and to undergo a security review.

Frequently Asked Questions

Who is eligible to apply as the lead applicant?

Only domestic entities are eligible to apply as the lead applicant for the award.

A domestic entity is one that is incorporated within the United States (including a U.S. territory) with its principal place of business in the United States (including a U.S. territory). This includes non-profit organizations; accredited institutions of higher education; State, local, and Tribal governments; and for-profit organizations.

Frequently Asked Questions

What is a foreign entity of concern?

Foreign entities of concern , as defined in 15 U.S.C. § 4651(8) and implementing regulation at 15 C.F.R. 231.104, include entities owned by, controlled by, or subject to the jurisdiction or direction of the governments listed in 10 U.S.C 4872(d): China, Russia, North Korea, or Iran.

An entity is owned by, controlled by, or subject to the jurisdiction or direction of a government of a foreign country where:

(i) The entity is: a citizen, national, or resident of a foreign country listed in 10 U.S.C. 4872(d); and located in a foreign country listed in 10 U.S.C. 4872(d);

(ii) The entity is organized under the laws of or has its principal place of business in a foreign country listed in 10 U.S.C. 4872(d);

(iii) 25 percent or more of the entity's outstanding voting interest, board seats, or equity interest is held directly or indirectly by the government of a foreign country listed in 10 U.S.C. 4872(d); or

(iv) 25 percent or more of the entity's outstanding voting interest, board seats, or equity interest is held directly or indirectly by any combination of the persons who fall within subsections (i)–(iii).

Domestic Control of Intellectual Property

15 U.S.C. 4656(g): "The head of any executive agency receiving funding under this section shall develop policies to require domestic production, to the extent possible, for any intellectual property (IP) resulting from microelectronics research and development conducted as a result of such funding and domestic control requirements to protect any such intellectual property from foreign adversaries."

Key Requirements

- At least one domestic entity must own or co-own any IP from the funded R&D and must have full rights to enforce the applicable IP for a period of years determined prior to the final award.
- The domestic entity must notify NIST before selling, transferring, or assigning ownership of the IP to another entity.
- IP from the funded R&D cannot be sold, transferred, or assigned to a foreign adversary, to include FEOCs and foreign countries of concern. IP cannot be licensed (except in certain limited circumstances) to a foreign adversary.

IP Rights Management Considerations

- Identify any pre-existing IP needed for the project, IP that may be developed with CHIPS R&D funding, and the path for accessing pre-existing or developed IP for new partners or associated recipients.
- Describe any desired deviations from standard IP regulations and terms.
- Describe how the proposed management and ownership of IP support the CVDP plan and any existing or planned protocols to ensure domestic control of CHIPS R&D-funded IP.
- Describe any additional desired licensing provisions.

Frequently Asked Questions 4

The NOFO states that at least one domestic entity must own or co-own any IP resulting from R&D conducted under the NOFO and have full rights to enforce applicable IP rights for at least a period of years, to be determined prior to the final award. What is a "period of years"?

CHIPS R&D will determine the "period of years" for which domestic control requirements are in effect on a case-by-case basis.

Commercial Viability and Domestic Production

"Applicants should propose measurable CVDP targets that demonstrate the viability of the proposed business model and of domestic production. Where relevant, CVDP milestones should complement technical milestones."

1. **Market Analysis Topics**
2. **Customer Analysis Topics**
3. **Financial Plan Topics**
4. **Domestic Production and Scale-up Topics**

Key Components:

- **Market Analysis:** A clear description of the value proposition of the proposed technology or product and identification of competitors.
- **Customer Analysis:** An assessment of demand for the funded innovation by current and potential customers or categories of customers, at volumes necessary for commercial viability.
- **Financial Plan:** A realistic and sustainable business model that considers cost, revenue, and access to capital.
- **Consensus Building:** Plans to collaborate (e.g., with standards bodies) to promote technology adoption

Key Point: Plans are intended to be an "initial assessment" or an "overview", with updates occurring across the award period. Applicants should not feel compelled to have all the answers before the research is complete!

Frequently Asked Questions 5

What factors might CHIPS R&D consider when evaluating applications that propose non-domestic production?

CHIPS R&D aims to improve the U.S. capacity to invent, develop, prototype, manufacture, and deploy the foundational semiconductor technologies of the future. However, consistent with 15 U.S.C. 4656(g), CHIPS R&D does not require exclusive domestic production, as this goal may be served by conducting activities overseas.

Where domestic production may not be possible, applicants should identify, as practicable at the time of application, factors driving overseas production, such as:

- Lack of domestic production capabilities
- Relative cost of domestic vs. foreign production, at relevant production volumes
- Potential economic or national security benefits from having distributed production among U.S. and overseas sites
- Potential risks of U.S.-based production such as market acceptance or changes to the value proposition
- Other factors the applicant deems relevant to the invention's success

Education and Workforce Development

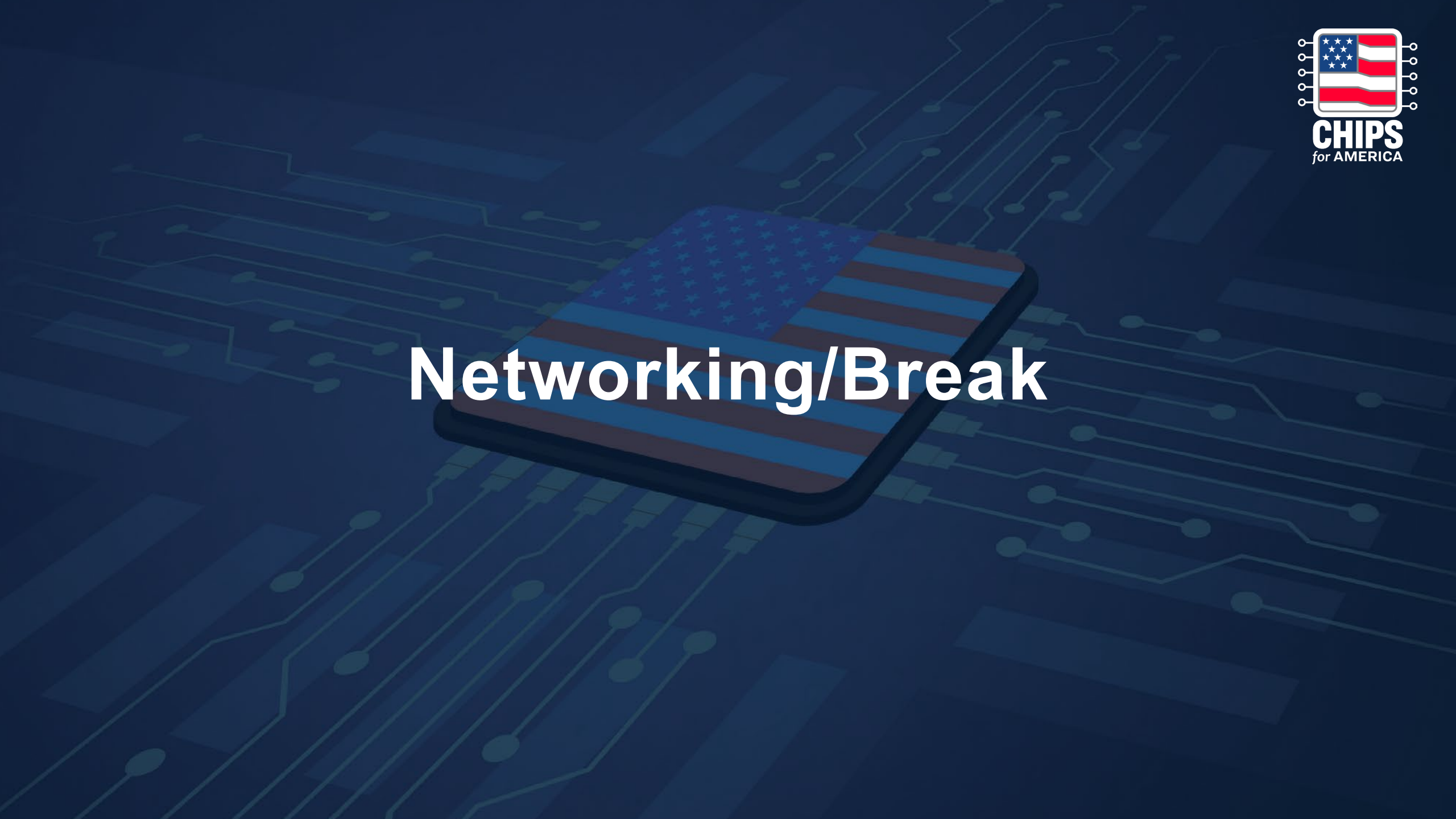
CHIPS R&D recommends that EWD plans include the following elements, where applicable:

1. **Workforce Needs**
2. **Metrics and Milestones**
3. **Industry-Relevant Training**
4. **Strategic Partnerships**
5. **Recruitment and Retention**

Key Components:

- **Workforce Needs Assessment:** An assessment of the relevant workforce needs for some portion or portions of the semiconductor industry
- **SMART Targets:** A description of the specific goals EWD activities are expected to achieve and quantifiable metrics (e.g. students trained, graduated, hired, and retained) to demonstrate success toward EWD targets
- **Training Opportunities:** A description of the proposed EWD activities and demonstration of alignment with specific job opportunities and skills needs, consistent with the workforce needs assessment, and leverage known best practices

Key Point: EWD Plans will be evaluated based on the extent to which they include rational and feasible targets, milestones, and metrics; provide alignment with U.S. industry needs; and encourage participation by underserved communities.



Networking/Break

Research Security

Greg Strouse

Education and Workforce Development (cont.)

CHIPS R&D recommends that EWD plans include the following elements, where applicable:

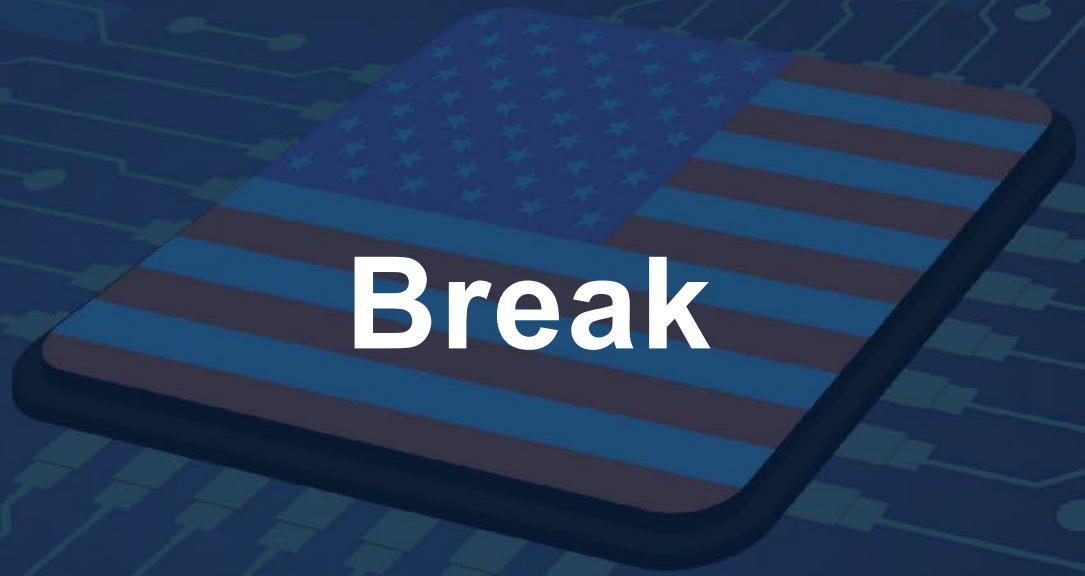
1. Workforce Needs
2. Metrics and Milestones
3. Industry-Relevant Training
4. Strategic Partnerships
5. Recruitment and Retention

Key Components:

- **Workforce Needs Assessment:** An assessment of the relevant workforce needs for some portion or portions of the semiconductor industry
- **SMART Targets:** A description of the specific goals EWD activities are expected to achieve and quantifiable metrics (e.g. students trained, graduated, hired, and retained) to demonstrate success toward EWD targets
- **Training Opportunities:** A description of the proposed EWD activities and demonstration of alignment with specific job opportunities and skills needs, consistent with the workforce needs assessment, and leverage known best practices

Key Point: EWD Plans will be evaluated based on the extent to which they include rational and feasible targets, milestones, and metrics; provide alignment with U.S. industry needs; and encourage participation by underserved communities.

Break



Research Security Agenda & Objectives

Agenda

- Safeguarding CHIPS Science through Research Security
- NIST IR 8484 – Research Security Framework
- Research Security Plan
- Research Security Reviews of NAPMP Applications
- Selected FAQs
- Questions and Contact information

By the end, attendees should better understand

- What is Safeguarding Science and Research Security
- What is the NIST Research Security Framework
- What is a research security plan
- How will an application be reviewed
- Answers to the FAQs
- Who to contact regarding research security

Safeguarding CHIPS Research Science

Safeguarding Science
facilitates open science and research security that values collaboration while protecting U.S. national security and economic security interests.

Research Security
is protecting the means, know-how, and products of research until they are ready to be shared.

Risks to U.S. Scientific Research Advantages

- **National Security** – Transfer of research products accelerates foreign military applications
- **Economic Security** – Loss of technical advantages results in the loss of U.S. global market competitiveness
- **Intellectual Property** – Some governments violate core research integrity principles and facilitate the transfer of original ideas from the United States

NIST IR 8484 – Safeguarding International Science Research Security Framework

Framework Implementation

- Strikes a balance between scientific research security and fostering international collaboration
- Implements a methodology to review research and make risk balanced determinations

Research Security Program Implementation

- Strategic communication and training
- Composite multi-disciplined open-source analysis
- Risk-balanced determination and mitigation
- User friendly tools, checklists, and templates

NIST Internal Report
NIST IR 8484

Safeguarding International Science

Research Security Framework

Gregory F. Strouse
Office of the Associate Director for Laboratory Programs
Laboratory Programs

Philip A. Bennett
Research and Technology Protection
Commerce Office of Security

Timothy R. Wood
Research Protections Office
Laboratory Programs

Mary Bedner
CHIPS Research and Development Program
CHIPS Program Office

Claire M. Saundry
International and Academics Affairs Office
Director's Office

This publication is available free of charge from:
https://doi.org/10.6028/NIST.IR.8484

August 2023

U.S. Department of Commerce
Gina M. Raimondo, Secretary

National Institute of Standards and Technology
Laurie E. Locascio, NIST Director and Under Secretary of Commerce for Standards and Technology

https://doi.org/10.6028/NIST.IR.8484

Research Security Plan: Key Components

Provide a written plan describing internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity. Provide a point of contact on research security issues within the project leadership team.

- Establishing a Research Security Team and Policies
- Scope of Program – Assessing At-risk Technologies and IP
- Communication and Training Research Personnel and Staff
- Reviews, Risk Determination and Mitigation
- Reviewing Personnel Appointments
- Reviewing Foreign Travel Requests
- Reviewing Collaboration and Service Requests
- Implementing Technology Control (e.g., Data Mgmt and Export Controls)
- Cybersecurity

Standardized Review Process

Proposal

- Critical and Emerging Technology (CET)
- Mil/Civ applications
- Focus of an adversary
- Export control

Applicant Institutions

- Foreign entity of concern
- Foreign ownership, control and influence
- Export control
- Technology control plan
- Cyber-Physical security
- Research Security Plan

Covered Individuals

- Research integrity
- Foreign entity of concern
- Malign foreign affiliations
- Associations with foreign adversaries
- Conflicts of interest and commitment

Research Security Reviews of CHIPS Applications

CHIPS for AMERICA

- **Understanding the research and type**
  - Fundamental or Proprietary
- **Implementation**
  - Open-source analysis of all relevant information by a multi-disciplined team
  - Risk Analysis (**RAFT**)
    - **R**ecruitment, **A**ffiliations, **F**unding, and **T**echnology
- **Risk Determination - Low, Medium, or High**
  - High does not always mean No
  - May include clarifications and/or mitigations
- **Clarifications and Mitigations**
  - Clarifications are questions that need answers prior to a final risk determination
  - Mitigations are changes that reduce initial risk determination

Frequently Asked Questions 6

Do entities applying for CHIPS R&D research funds need to demonstrate that they have a research security program in place before applying for a research award and/or before receiving research funding?

- At present, CHIPS R&D does not require applicants to demonstrate the existence of a research security program in order to apply for or receive funding.
- However, applicants must provide a written plan (i.e., a research security plan) describing internal processes or procedures for addressing foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity, as applicable.

Frequently Asked Questions 7

Will CHIPS R&D provide funding or other resources to establish or improve a research security program or to the meet other CHIPS R&D research security requirements?

- To date, CHIPS R&D has not established any specific programs or set-asides to support the development of a research security program.
- However, limited funding may be available to implement a research security plan, subject to the objectives of the individual notice of funding opportunity (NOFO) and the approval of the relevant program director.
- For entities selected to receive funding, NIST may provide assistance to establish or improve research security activities consistent with NIST best practices (NIST IR 8484).

NIST Internal Report
NIST IR 8484

Safeguarding International Science

Research Security Framework

Gregory F. Strouse
Office of the Associate Director for Laboratory Programs
Laboratory Programs

Philip A. Bennett
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Commerce Office of Security

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Questions ?

CHIPS for AMERICA

Contact Information

researchsecurity@nist.gov

Ready, Set, Submit!

Concept Paper & Invited Full Application Preparation & Submission

NIST | NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Financial Assistance Agreements Management Office

Agenda

PLAN AHEAD TO STAY AHEAD

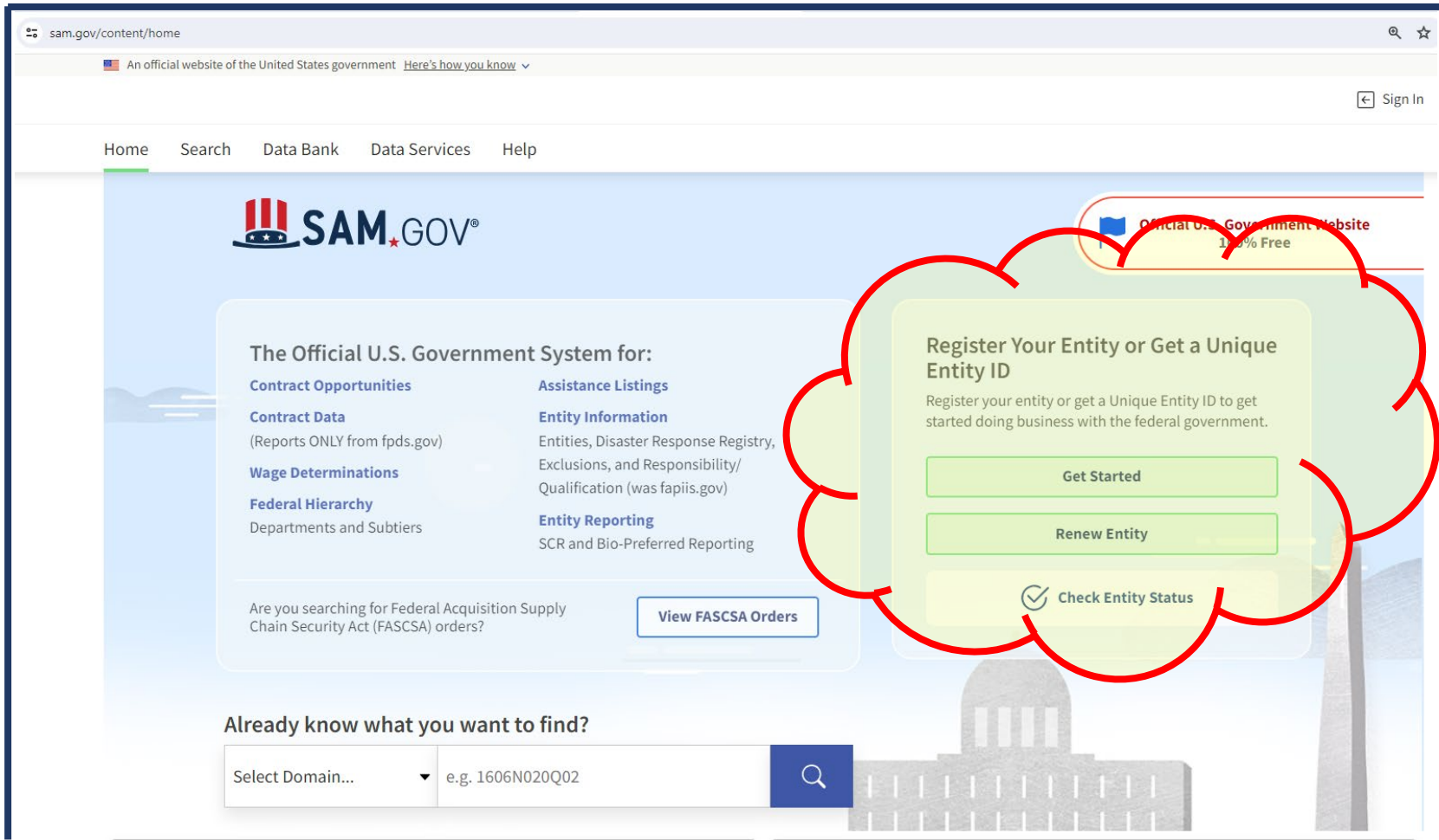
- SAM.gov Registration
- Grants.gov Registration
- Tips for Success

SAM.gov

Link: https://sam.gov/content/home

Help Desk: Monday - Friday from 8AM - 8PM EST U.S. calls: 866-606-8220

- 100% FREE to register
- Must have an active account
- Unique Entity ID (UEI)
- Start Early: the process takes about 10 days, but can take up to 6 weeks!
- Complete the Representations & Certifications, especially the Financial Assistance Response page
- Register in SAM.gov before Grants.gov



Grants.gov

After obtaining a UEI for your organization from SAM.gov, you must register in Grants.gov. There is no fee for registering with Grants.gov. Your organization's EBiz POC must:

1. Create a Grants.gov account with the same email address as used in SAM.gov for the EBiz POC, and
2. Add a profile with Grants.gov using the UEI obtained from SAM.gov.

The EBiz POC can then delegate administrative roles to other users. Read the Help article, Manage Roles for Applicant for instructions.

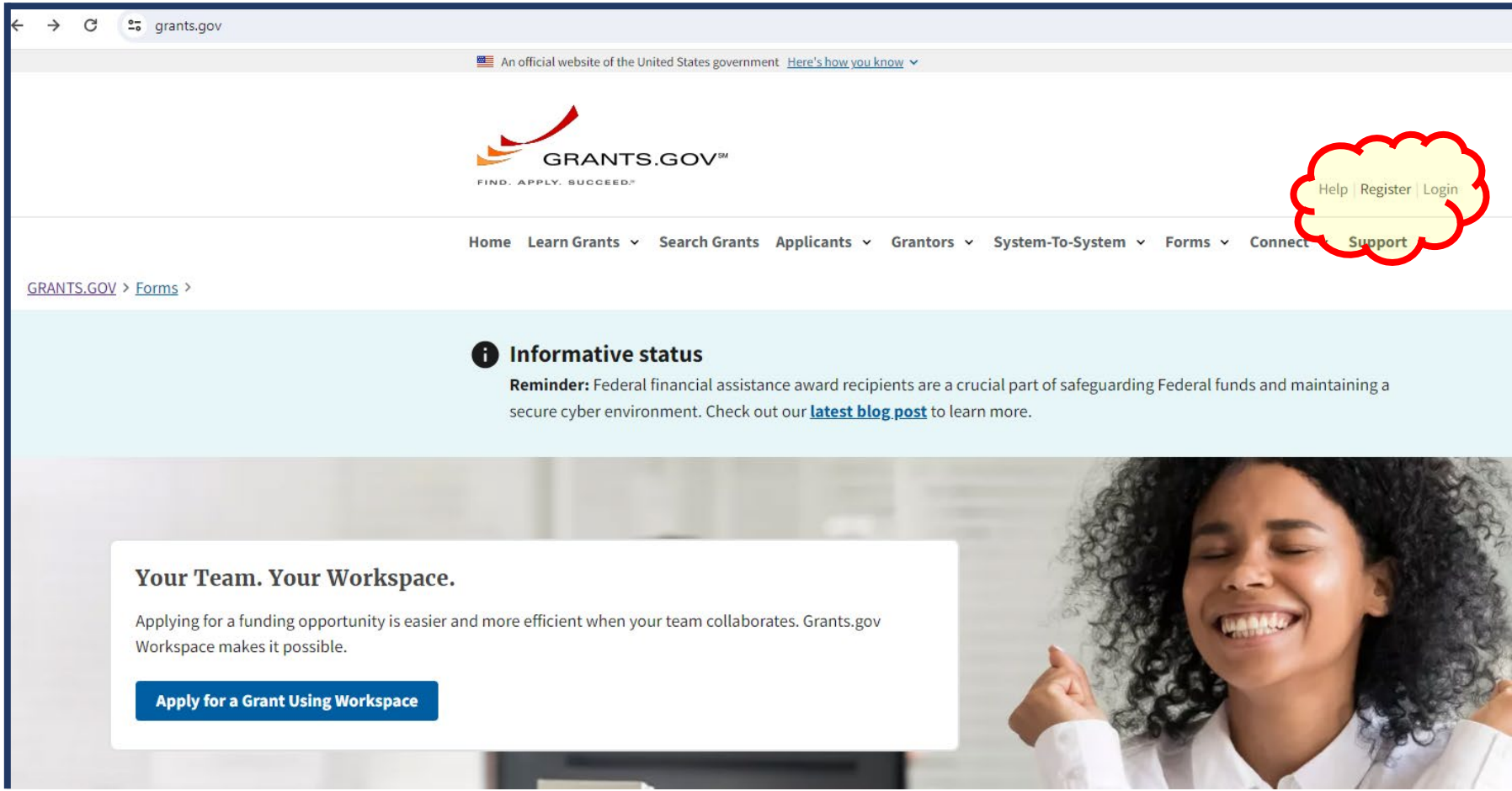
Visit the Grants Learning Center to find information about every phase of the grant management process, from applying and reporting to the award closeout.

Grants.gov (cont.)

Link: https://www.grants.gov/applicants/applicant-registration

Help Desk: 1-800-518-4726 (24/7 excluding holidays) or support@grants.gov

- 100% FREE to register
- Grants.gov will be used to submit concept papers
- Separate instructions will be provided to applicants who are invited to submit full applications (after concept paper review)
- User Guide
- Applicant FAQs



On-Time Submission

- **All registrations, including SAM.gov, must be completed before the deadline**
  - **Concept Paper & Full Application must be free of Grants.gov errors; corrective submissions must be made BEFORE the submission deadline and will overwrite previous submissions**

    - Errors stop application processing and must be corrected

    - Warnings do not stop application processing and are corrected at your discretion based on your circumstances

  - **Submit early to allow time to correct any unexpected errors or submission issues**
    - Depending on the size of the file, transmittal may take SEVERAL MINUTES to HOURS.
    - Don’t wait until the deadline date to submit. The system may be slow due to last minute submissions.

Tips for Success

- Understand submission process in NOFO
- Do NOT apply with a full application in Grants.gov until invited
- SAM.gov registration must be active to apply in Grants.gov (Concept Paper & Full Application)
- Use correct UEI and EIN
- Designate the proper roles in the systems (e.g. - Authorized Rep in Grants.gov)
- Utilize “workspace” feature in Grants.gov to draft applications
- Limit the application file size / character limits / page limits per the NOFO
- Make sure you are using compatible software (e.g. - Adobe Reader)
- Do not pay to create accounts
- Late applications will not be accepted
- Register to SAM.gov and Grants.gov early!

Shanell V. Williams

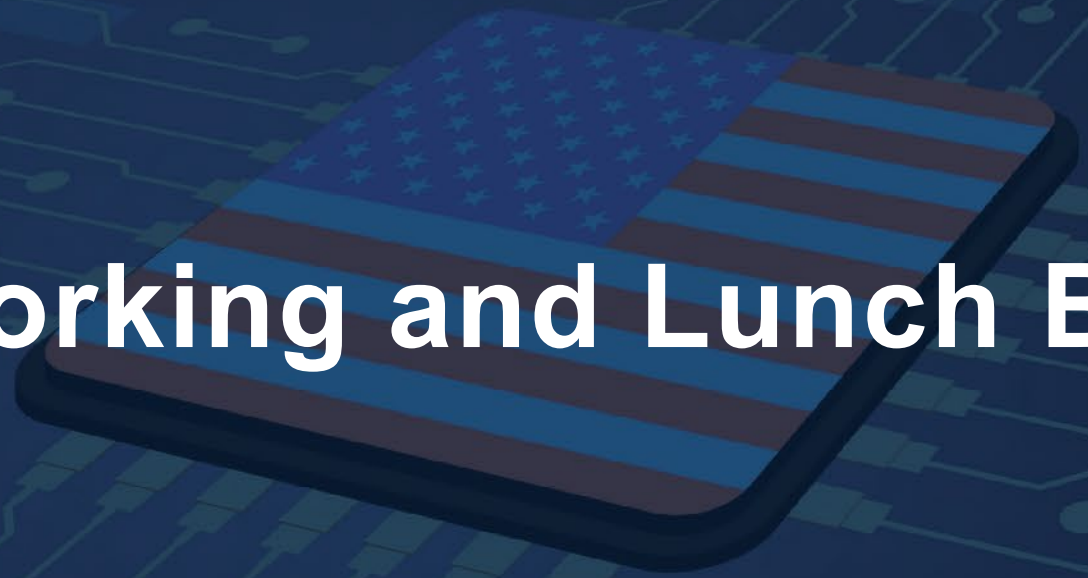
Other Transaction
Agreements Officer

E-mail:
shanell.Williams@nist.gov
with “2025-NIST-CHIPS-NAPMP-01 Questions” in subject line

Question & Answer Panel

Dev Palmer, Richard-Duane Chambers, Greg Strouse, Shanell Williams

Networking and Lunch Break



Lunch options

- On your own
  - “Olives” restaurant in the hotel lobby
  - “Olives” restaurant grab & go options in the hotel lobby
  - Venture out to one of the local restaurants:
    - https://www.google.com/maps/d/edit?mid=1udE_t1I0vEh3adeRn9HtqTQkbSnd8KM& usp=sharing
    - QR code links to map of local eateries, may want to order ahead.

QR Code:
Map of local eateries
https://www.google.com/maps/d/edit?mid=1udE_t1I0vEh3adeRn9HtqTQkbSnd8KM& usp=sharing

Afternoon Instructions

- Meet back in the Plaza Ballroom
- Brief overview of each R&D Area by the program managers followed by facilitated feedback sessions
- The Regency Room is available for discussions and networking during R&D Area overviews

Equipment, Tools, Processes, and Process Integration

Bob Soave

Equipment, Tools, Processes and Process Integration R&D Area

Drivers

- Develop, demonstrate and deliver advanced, flexible, extensible processes and equipment for chiplet-based advanced packaging architectures through R&D focused on critical steps within the packaging process flow
- Install resulting tools, process technologies and integrated process flows in the NAPPF as primary vehicles for advanced packaging development and prototyping

Critical Objectives

1. Low-damage, high-precision chiplet singulation methods
2. Advanced bonding processes for reliable fine-pitch connections
3. Processing and assembly methods for dense chiplet arrays and 3DHI stacks
4. Collective chiplet processing methods
5. Integrate advanced power delivery, thermal management and connectors
6. Manufacturable advanced packaging flows

Key Outputs

- Unit processes and integrated process sequences that meet scale-down and scale-out roadmap targets
- Equipment to run the processes at commercial scale
- Integrated packaging process flows based on the process technology and equipment developed in this R&D Area
- Test vehicles to characterize equipment, process and packaging flow efficacy

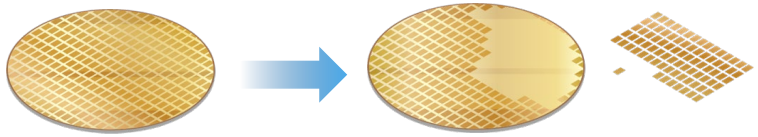
Out of Scope

- Processes and assembly methods used in conventional packaging, such as solder-based assembly and saw blade dicing

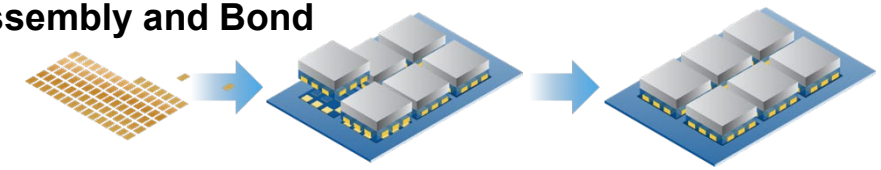
ETPI R&D Focus

Process Cluster Development

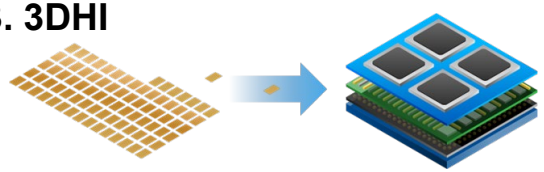
1. Chiplet Singulation



2. Assembly and Bond

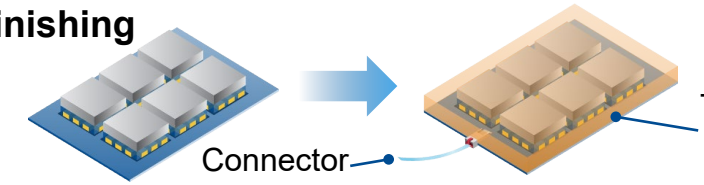


3. 3DHI

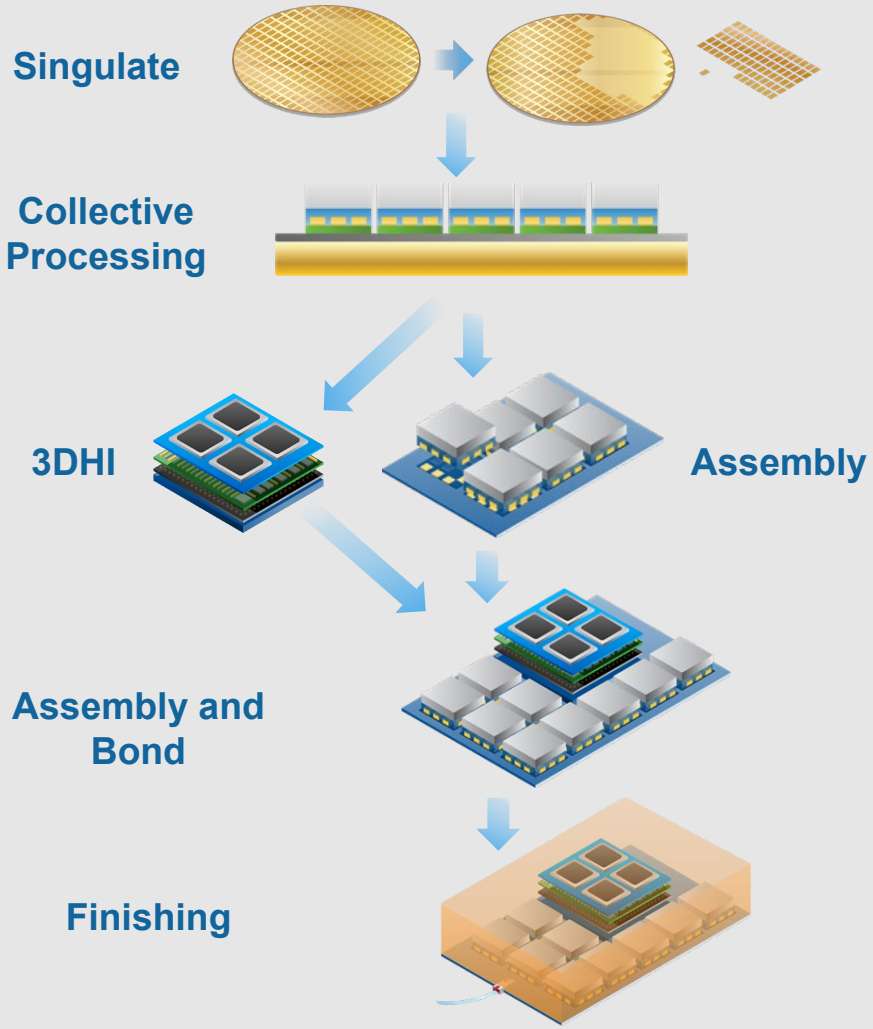


4. Collective Chiplet Processing

5. Finishing



Notional example: Integrated packaging flow from sequencing process clusters



Frequently Asked Questions 8

We have a new and innovative technology with potential benefits for fine-pitch assembly. Should we propose a focused program on the technology, propose a full tool and process program, or seek to join a team?

A good proposal delivers the entire solution, not just component technologies. The NOFO is open to a variety of proposer structures, but even large organizations may struggle to have all the resources and technologies to deliver a full solution, and thus teaming activity is often a successful strategy.

How can we participate if we do not have access to the facilities and range of processes required to fully develop, characterize and demonstrate our solution?

Applications are encouraged from multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of development capabilities required to achieve program objectives. Please see the CHIPS R&D Teaming List to explore opportunities.

Frequently Asked Questions 9

We have extensive experience extending traditional, tried-and-true packaging processes and equipment toward the expected targets for advanced packaging. Should we submit a proposal?

The NOFO targets significant advances over state of the art. Proposals must clearly show how solutions will achieve the scale-down dimensions and scale-out assembly targets required for chiplet-based adv. packaging architectures.

Can a proposal for an integrated packaging flow (IPF) be a "stand-alone" submission, or should an IPF be part of a process cluster development plan?

IPF development will require an extensive understanding of the process technologies, integration sequences and equipment capabilities developed in the clusters. While the NOFO is open to a variety of proposal structures, IPF development plans that are linked to major cluster development programs are encouraged.

Power Delivery and Thermal Management

David LaVan

Power Delivery and Thermal Management R&D Area

Drivers

- Address power delivery, power efficiency, and thermal management challenges for advanced packaging
- Ensure that thermal dissipation and power delivery will no longer be gating factors that limit advanced packaging

Critical Objectives

- Power Delivery and Management
- Thermal Management
- Higher Fidelity Power and Thermal Models
- Integrated Power and Thermal Management

Key Outputs

- Test devices and utility chiplets
- Standards, metrologies and data derived from test devices
- Test and evaluation at prototype- and pilot-scale manufacturing
- Proven equipment, tools, processes, materials, models and devices with improved performance available for the CHIPS ecosystem

Out of Scope

- Application-specific thermal and power solutions
- Conventional air-cooling approaches
- Discrete packaged devices and passives
- Development of batteries

Four Critical Objectives

Objective	High Performance System	Low-Power System
1. **Power Delivery and Management**	Power delivery at high density and high efficiency for 3DHI devices	Design optimization, energy efficiency, and integrated energy harvesting technologies
2. Thermal Management	Thermal solutions compatible with advanced substrates, 3DHI, and other advanced packaging design aspects	Compact and lightweight thermal solutions
3. Power and Thermal Models	Validated, higher fidelity thermal and power models that accurately predict power and thermal distributions across chiplet stacks and accelerate design and evaluation	
4. Integrated Power and Thermal Management	Integrated designs and models that couple power delivery and thermal management for use with fine-pitch, bonded stacks of chiplets	

Proposals for the Thermal and Power Delivery R&D Area must address one or more of these four objectives

Frequently Asked Questions 10

Should a company that develops thermal analysis software tools join a team that is targeting the PD&TM area or the EDA area?

There are several interdependencies between R&D Areas. Proposers are encouraged to carefully read the NOFO for details on goals and timeline for where their work best fits. The government cannot fund the same capability under multiple awards.

Should we apply if our technology would come close to meeting the listed targets but maybe not hit the targets within five years. Is there any point in proposing it?

With proper explanation, proposals that do not meet listed targets, or those that include additional targets, will be considered. Applicants must indicate whether they will meet, exceed, or not meet the target or whether the target is not applicable for their approach.

Are you interested in thermal technologies designed to maintain constant temperature instead of just cooling? For example, for photonics applications.

A driver for this work is to ensure that thermal dissipation and power delivery will no longer be gating factors that limit advanced packaging. Any innovation that furthers this goal, that is not specifically stated as out of scope, will be considered.

Frequently Asked Questions 11

Where are the system boundaries for both power and thermal design?

Proposers are encouraged to keep in mind the end goal of developing solutions and transferring the leading solutions to the NAPPF or other facilities for prototyping and piloting, with the best solutions made accessible to the CHIPs ecosystem. Anything required to do that should be inside the system boundary. For example, a laboratory scale chiller used to evaluate a thermal solution would be within scope. A data center scaled chiller probably would not be.

How should we divide costs if we intend to propose collaborations with other R&D Area (or propose solutions to multiple R&D Areas using some shared resources)?

Proposers are encouraged to carefully read Section 1.8 Project Coordination of the NOFO for guidance about coordination activities to plan into a submission.

Connector Technology, Including Photonics and Radio Frequency (RF)

Chris Myatt

Connector Technology, Including Photonics and RF R&D Areas

R&D Area Drivers

- Recent years have seen an explosion of progress in high performance computing. Data transmission in these systems requires innovation for high data-rate, low latency, small footprint, error-free, and energy efficient connections.

Objectives

- Development of short-range, wired connections to enable high speed connectivity between neighboring packages.
- Development for intermediate range wired, photonic, or wireless connectors between local wafer-scale systems (but not necessarily nearest neighbor).
- Development of long-range connectors capable of connecting wafer-scale systems at a range up to and exceeding the length of a server site, or approximately 1 km

Key Outputs

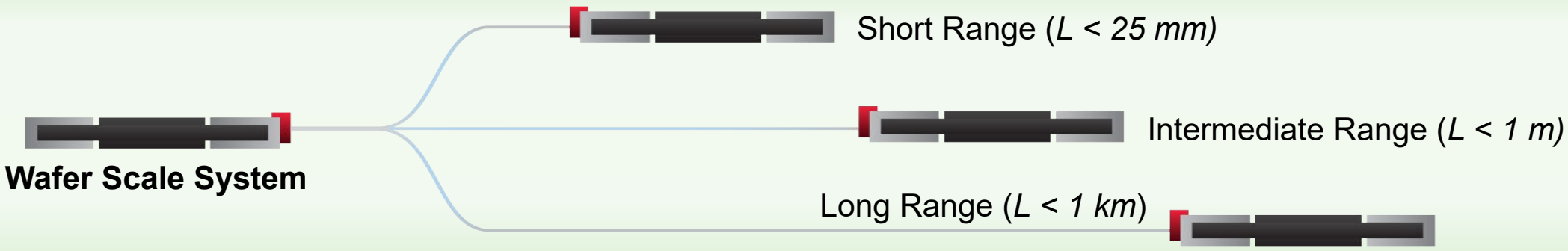
- Novel connectors, tools, materials, processes and devices with improved performance
- Standards and metrologies derived from test devices; test and evaluation at proto- and pilot-scale manufacturing
- Provide new connector solutions, including devices, equipment, tools, processes, and process integration, to research projects in other areas of packaging research

Out of Scope

- Traditional ball grid array (BGA) or land grid array (LGA) connectors,
- Conventional wire bonding
- Traditional free space optical components

Three Length Scale Objectives

Objective	Length Scale	Key Characteristics
Short Range (e.g. Wired)	L < 25 mm	Data rates of > 10 Gb/s/channel & density of 10 Tb/s/mm Power efficiency < 0.1 pJ/bit including all energy for full functionality
Intermediate Range (e.g. RF, Wired, or Photonic)	L < 1 m	Aggregate data rate > 100 Tb/s bidirectional from package Power efficiency < 0.1 pJ/bit including all energy for full functionality
Long Range (e.g. Photonic)	L < 1 km	Aggregate data rate > 100 Tb/s bidirectional from package Power efficiency < 0.1 pJ/bit including all energy for full functionality



Optimize for: $\text{s-FoM} = \dfrac{(\text{BW/shoreline}) * \text{link length}}{\text{Efficiency} * \text{connector area} * \text{latency}}$

Jangam, Iyer, 10.1109/TCPMT.2020.3022760

Frequently Asked Questions 12

Our solution involves chiplets, wiring (electrical or optical), and the tooling to assemble these components. Should we apply to multiple R&D Areas?

The Connectors R&D Area assumes that solutions are based on chiplets, and that all tooling and automation needed for a connector assembly will be developed under this R&D Area. It will be necessary to collaborate with other NAPMP awardees, such as for ETPI, Chiplets, and Substrates R&D Areas.

We have a new technology, such as a new material, that can enable novel connectors. Should we propose a narrow program on the material, propose a full program, or seek to join a team?

A good proposal delivers the entire solution, not just component technologies. The NOFO is open to a variety of proposer structures, but even large organizations may struggle to have all the resources and technologies to deliver a full solution, and thus teaming activity is often a successful strategy.

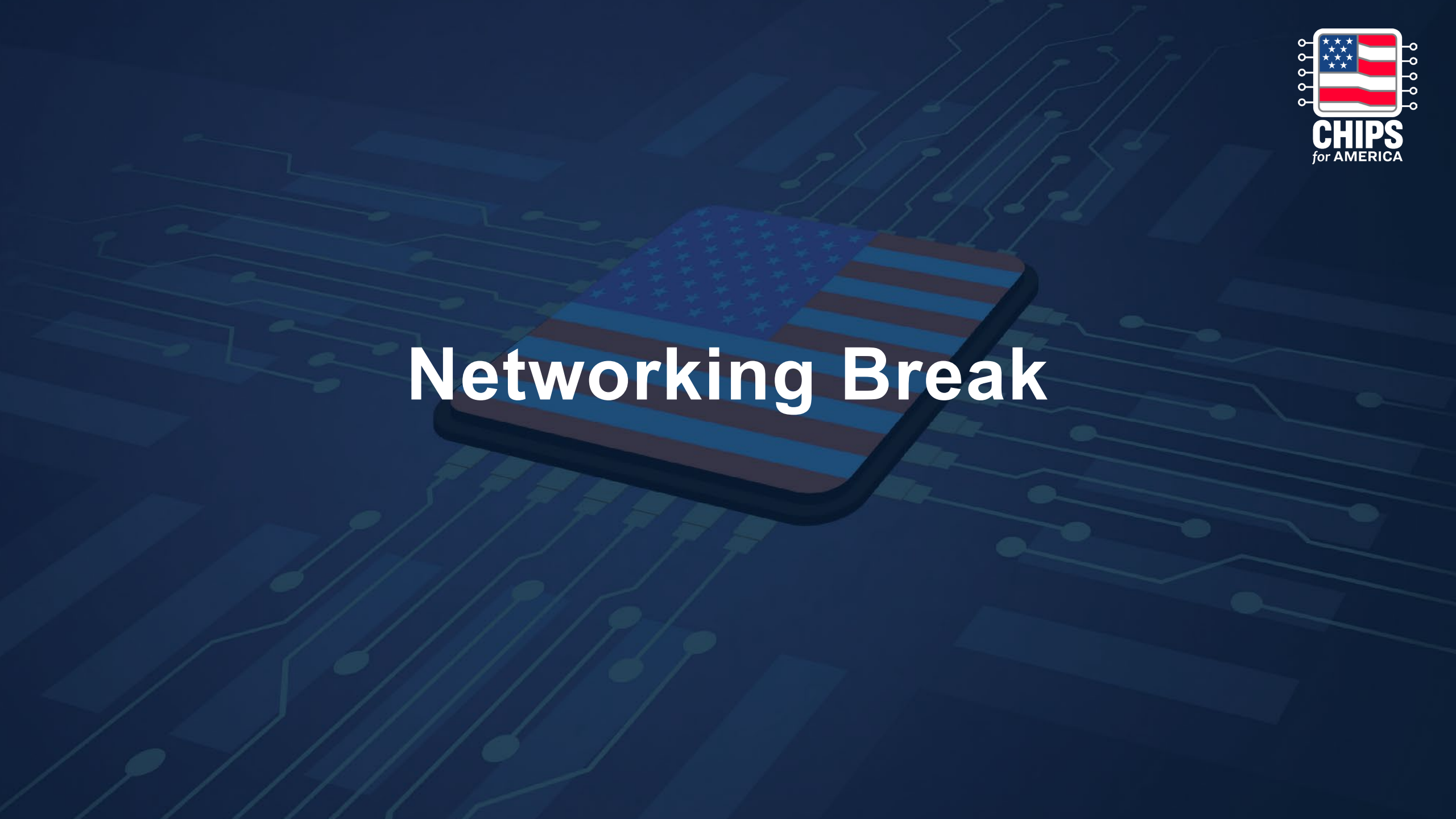
Frequently Asked Questions 13

What are the metrics for assembly rates for devices incorporating these connectors?

While we do not include specific metrics for assembly, proposals should address manufacturability and where necessary include roadmap development for integration into a full manufacturing flow.

A connector is system dependent, based on distance, power envelope, data rates, etc. Do we propose a connector that fits a specific need of our system?

Solutions to each Objective will need to be adaptable. The context may be informed by your system needs, but a successful solution should meet the requirements of the NOFO and be compatible with other R&D Area solutions, as adapted to specific circumstances.



Networking Break

Chiplets Ecosystem

Bapi Vinnakota

CHIPS for AMERICA

Chiplets R&D Area

R&D Area Drivers

- Leverage Advanced Packaging attributes:
  - "Wire abundance": Hundreds to thousands of wires between chiplets as an inflection point that influences system design
  - Ultra-large packages: Build systems from hundreds to thousands of chiplets in one package
  - Heterogenous integration: incorporation of separately manufactured components

Critical Objectives

- Scale-down: Die-to-die interfaces based on hundreds/thousands of wires between chiplets at bond pitches of 10μm and lower
- Scale-out: Wafer-scale systems built with hundreds to thousands of chiplets
- Ecosystem: Unique functional and physical modularity for heterogeneous integration
- Technology Demonstrators: Implement and demonstrate innovations in chiplets and packaging. In one of either High-Performance or Low-Power domains.

Key Outputs

- Technology demonstrators with packages/chiplets at 10μm bond pitch to show value of advanced packaging for applications
  - Optional: Chiplets/system designs that uniquely exploit wire abundance
- "Wire-like" low-power low-latency die-to-die interface implemented.
- Specification for functional and physical modular socket-based ecosystem.
- Analytical study on scale-out capabilities

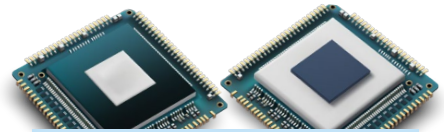
Out of Scope

- Chiplet designs that are extensions of conventional approaches
- Unmodified reuse of existing chiplets
- Standalone chiplet designs for any function not coupled to a chiplet ecosystem
- Target the development of new chiplets to integrate with existing chiplets
- Chiplet designs based on commodity packaging
- Wire bonding for D2D interconnect,

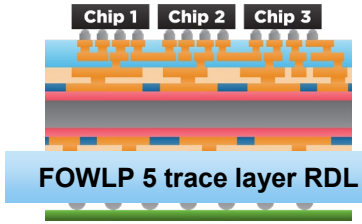
A Chiplets/Systems Design Inflection Point Enabled by Advanced Packaging

Today: packages more like **boards**

Tomorrow: packages more like **chips**

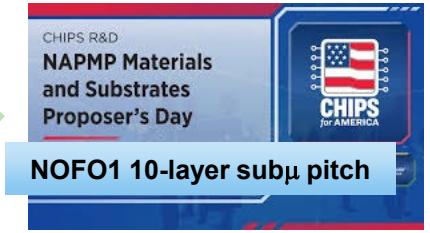


fine line 5 trace layer PCB

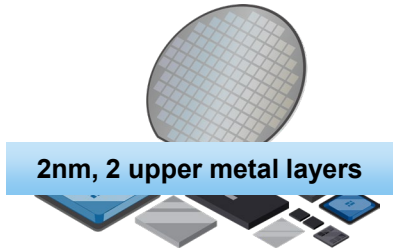


FOWLP 5 trace layer RDL

10x wire density & growing



NOFO1 10-layer subμ pitch



2nm, 2 upper metal layers

Estimated wire density in wires/mm

axis marks not to scale

≈ 20 | ≈ 50 | ≈ 6,000 | ≈ 20,000[2]

Wire Scarcity → **Wire Abundance**

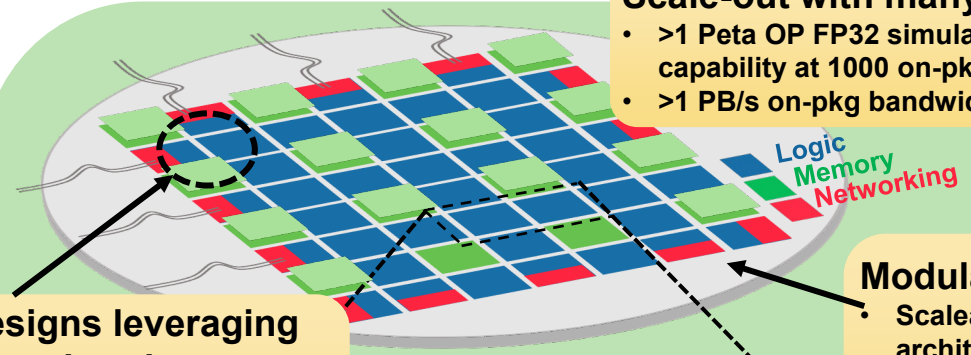
Chiplets/Systems Today	With	Chiplets/Systems Tomorrow[3]
High-speed high-power interface	Wire abundance	**Scale-down** wire-like 2D/3D interface at 10μm and lower bond pitches
Monolithic wafer-scale	10-100x larger packages	**Scale-out** wafer-scale systems that exploit wire abundance
Board-like integration	Function & physical modularity	**Ecosystem** for IP-like heterogeneous chiplet integration

[1] P. Chiang,et al, "InFO_oSTechnology for Advanced Chiplet Integration," 2021 IEEE 71st ECTC, San Diego, CA, USA, 2021, pp. 130-135.
[2] Illustrative, approximate wire density numbers estimated from current state of the art.
[3] NAPMP Vision Paper: The Vision for the CHIPS for America National Advanced PackagingManufacturing Program (nist.gov)

Example Targets: High Performance Domain

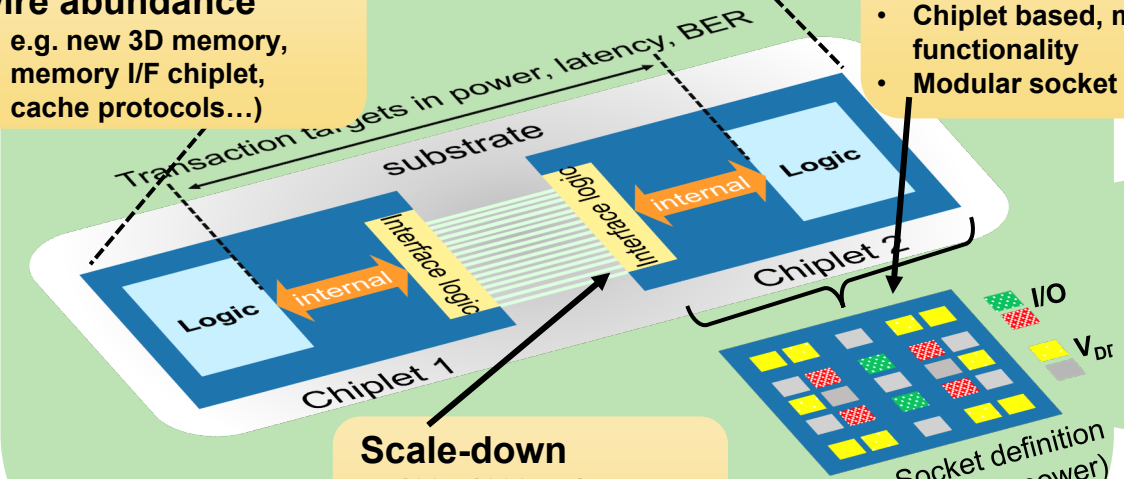
Innovations in Scale-Down, Scale-out and Ecosystem

Scale-out with many chiplets
- >1 Peta OP FP32 simulated capability at 1000 on-pkg chiplets
- >1 PB/s on-pkg bandwidth



Designs leveraging wire abundance
- e.g. new 3D memory, memory I/F chiplet, cache protocols…)

Modular Ecosystem
- Scaleable chiplet architecture
- Chiplet based, modular functionality
- Modular socket definition

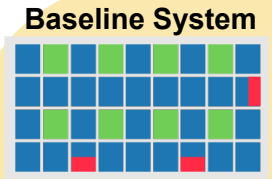


Scale-down
- 100s-1000s wires
- ≤10 µm bond pad pitch
- Wire-like interface

implementations

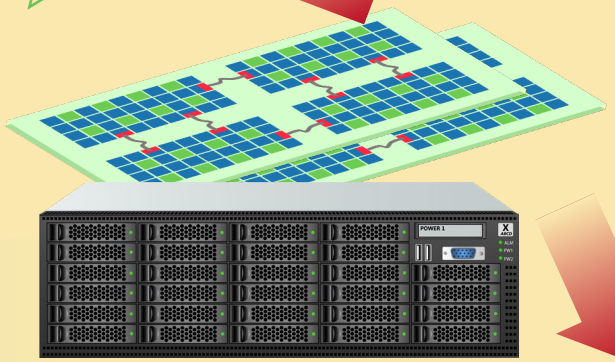
context

Technology Demonstrator



Domain specific accelerators

Unit Package
- 32 chiplets in a 3200 mm² Unit Pkg
- 2 chiplet differentiated variants
- ≤10 µm bond pad pitch



System Demonstrator
- 8 Unit packages aggregated into one system per variant

Application Demonstration
- 2 software application demonstrations per variant

PyTorch
Meta Llama
Open Neuromorphic
OpenMD

Frequently Asked Questions 14

How do we participate if we do not have access to an advanced packaging process/capability, for example with 10um bond pitch, particularly for the early development D2D test vehicle?

This capability is needed for successful execution. In the concept paper, proposers will be expected to identify potential solutions that can provide access for project execution. There are facilities in the US that provide this capability. Please see the Teaming List . Consider teaming with ETPI groups.

Is teaming the only competitive option for a start-up/small-business to participate in a contract on the scale of $100M?

While not required, teaming is encouraged.

Frequently Asked Questions 15

Are the results of this R&D Area expected to results in standards. What is the relationship of the R&D Area program to existing chiplet standards such as UCIe, AIB, and BoW?

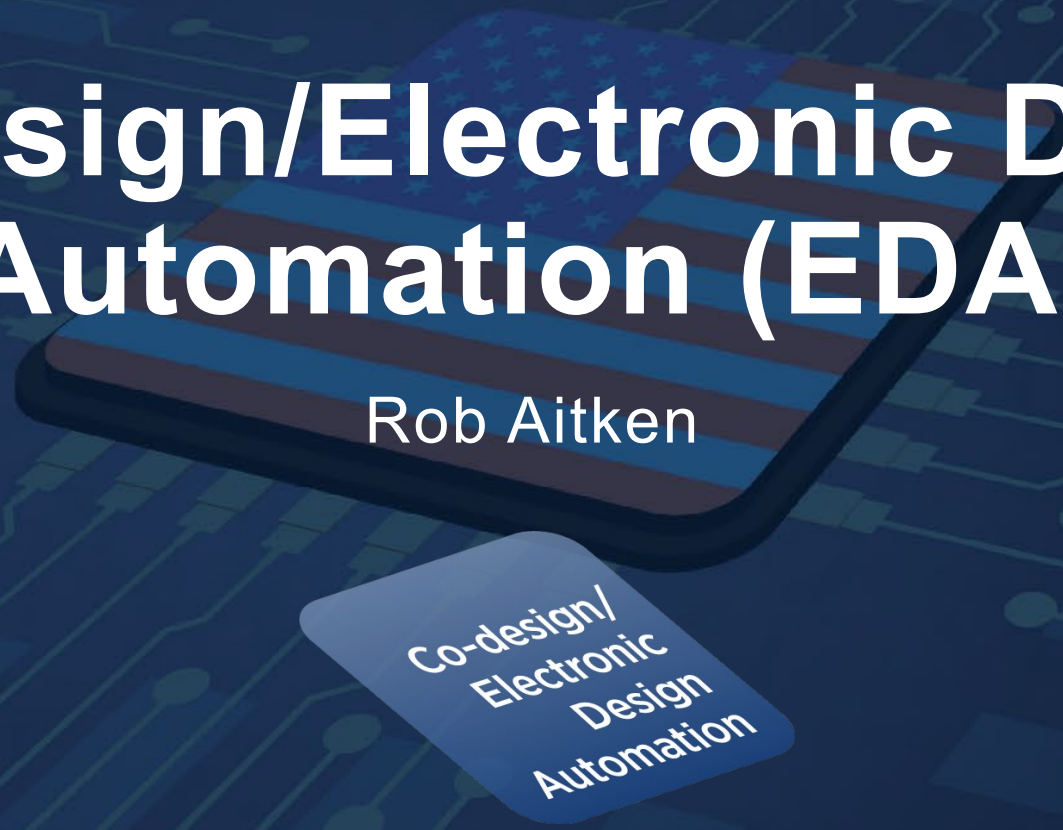
Yes, this R&D Area encourages standards that leverage wire abundance. The intent of this R&D Area is to focus on leveraging wire abundance to drive an approach that optimizes efficiency.

Is it a hard requirement to deliver a relevant Technology Demonstrator?

Yes, this requirement is intended to drive manufacturing readiness for designed solutions. Proposers must deliver either a high-performance or low-power demonstrator. There may be additional funding available to scale successful Technology Demonstrators towards wafer scale implementations.

Co-design/Electronic Design Automation (EDA)

Rob Aitken



EDA R&D Area

R&D Area Drivers

- Scale-out Advanced Packaging designs containing hundreds of Chiplets on a single substrate are complex physical objects and systems that exceed the capabilities of existing EDA solutions. New EDA abstractions and capabilities are needed for wafer-scale Chiplet-based AP systems.

Critical Objectives

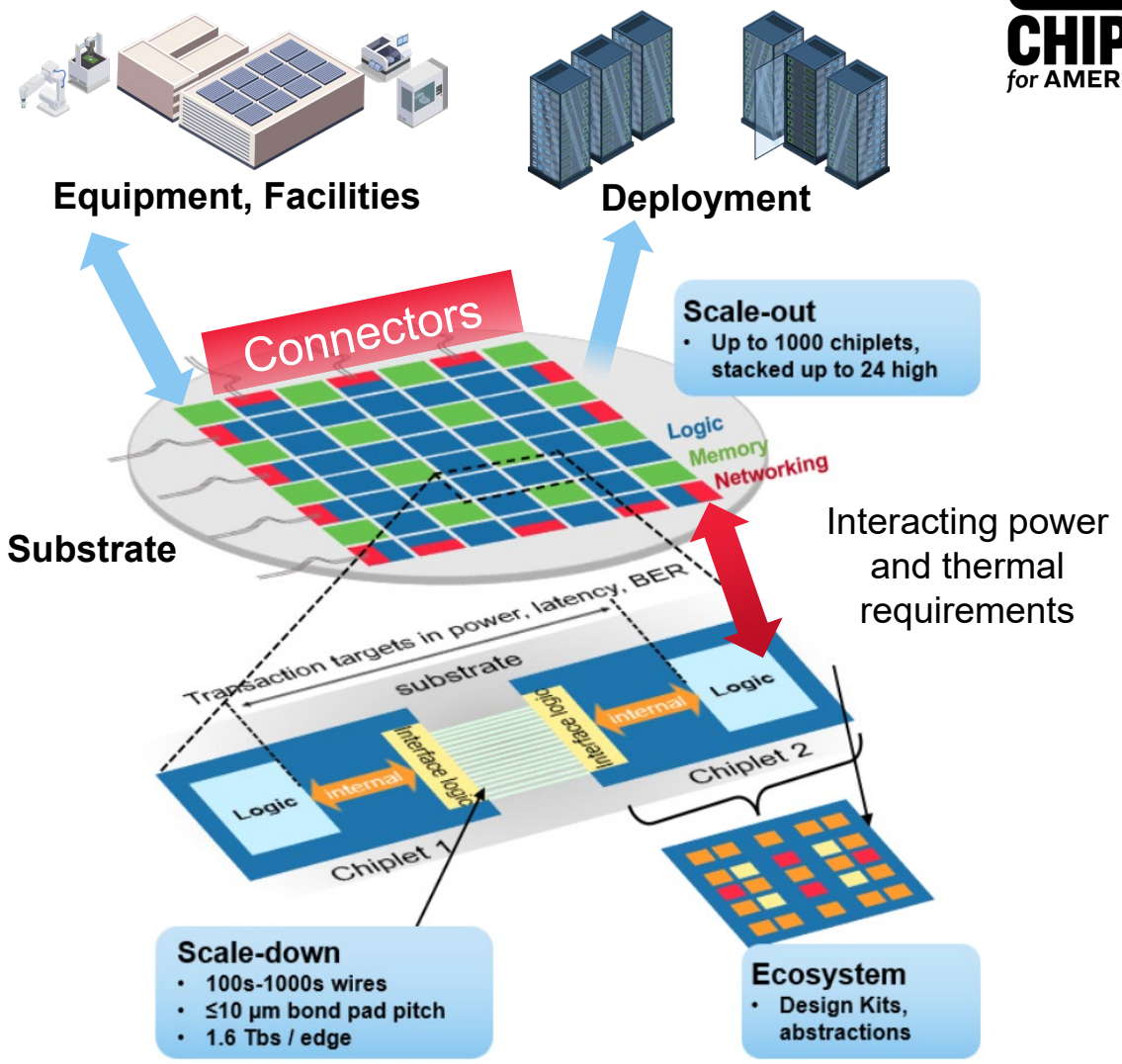
- Design Implementation and Verification (Design)
- Embedded Security (Security)
- Test, Repair, Resilience, Reliability, and Fault Tolerance (Resilience)
- Independent Integration, Verification and Validation (IV&V)

Key Outputs

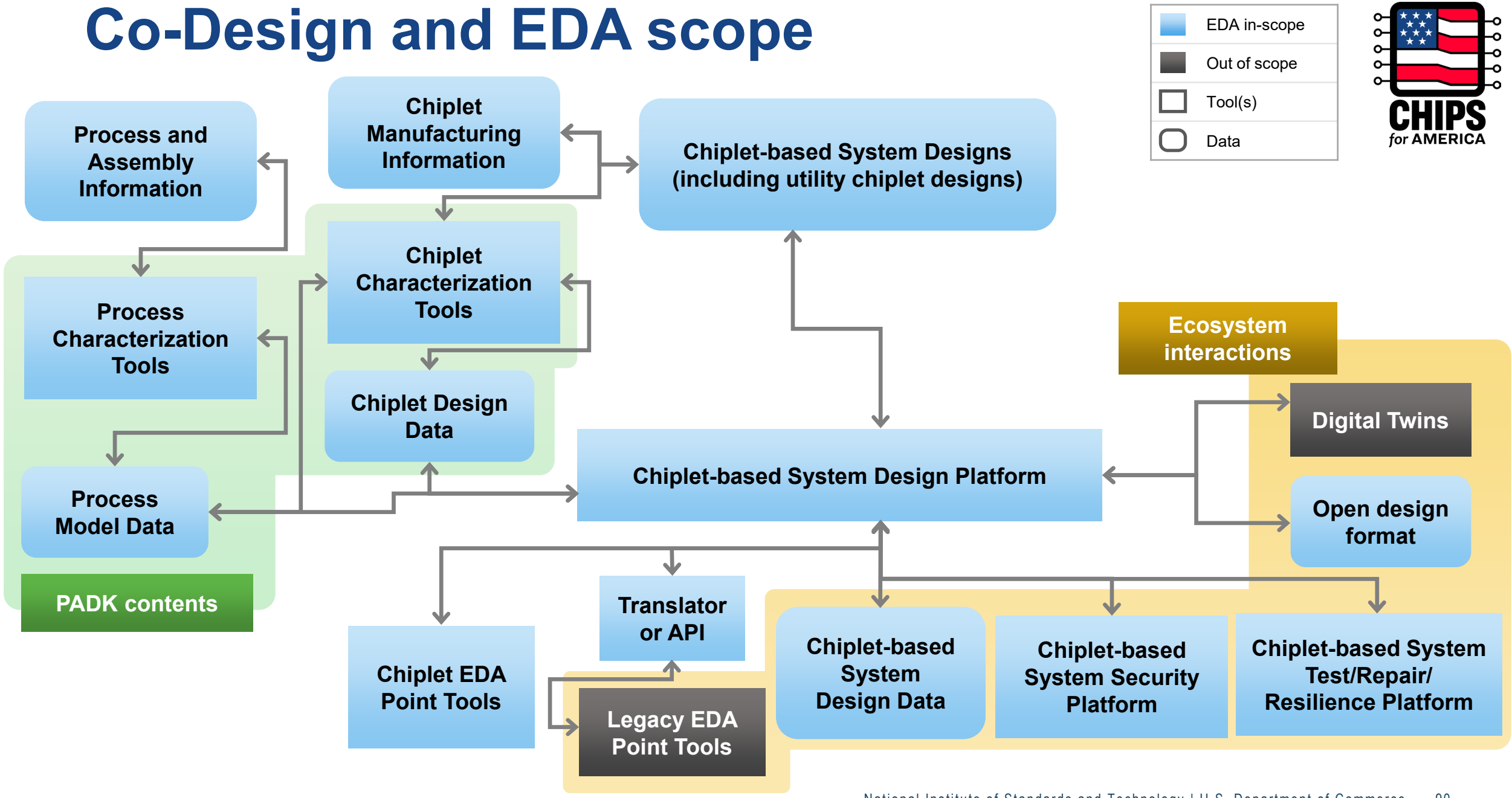
- A Chiplet-level layer of abstraction
- Documented Design, Security, and Resilience Platform architectures and tools;
- Demonstrations of functionality for each tool and;
- Objective specific outputs as described in the NOFO

EDA RDA Drivers

- A scale-out, scale-down package is a highly complex physical object
  - Encapsulates electro-thermal-mechanical interactions across a wide range of distance and time scales
- A scale-out, scale-down package is a highly complex system of chiplets
  - Requires new layers of abstraction, new approaches to design, verification, security, and resilience
- Critical R&D Objectives
  - **Design** Implementation and Verification
  - Embedded **Security**
  - Test, Repair, **Resilience**, Reliability, Fault Tolerance
  - Independent Integration, Verification and Validation (**IV&V**)



Co-Design and EDA scope



EDA R&D Area Objective Out of Scope

Out of Scope Design

- Design capabilities for purely monolithic systems, silicon tapeout or core circuit IP block development
- Development of any chiplet-level application, operating system (OS), or driver software
- System architecture, neuromorphic solutions, and solutions primarily focused on chiplet-level EDA

Out of Scope IV&V

- Proposals that feature hardware or manufacturing demonstrations
- Proposals that are based around non-cloud computing platforms
- Proposals that seek to alter or replicate rather than integrate and evaluate deliverables from other Objectives

Out of Scope Resilience

- Proposals primarily focused on new test equipment or intra-chiplet DFT techniques
- Communication standards conformance demonstrations, including bit error rate (BER) demonstrations
- Fault tolerant system architectures
- New information coding techniques
- Demonstrated compliance with ISO 26262 or other domain-specific functional safety standards is not required

Out of Scope Security

- Software security (e.g. software-based pointer checks)
- System security service functionality (e.g., encryption services)
- Secure communications protocols
- Encryption techniques including fully homomorphic
- Explainable AI
- Anything subject to national security classification
- Developing or managing external asset management capability
- Intra-chiplet hardware security techniques (e.g., physically unclonable functions, logic locking)

Frequently Asked Questions 16

Are open-source tools allowed, encouraged, discouraged or not allowed at all?

Open-source tools are allowed, and are neither encouraged nor discouraged

How does the PADK as you've defined it relate to other design kits out there?

The PADK will be defined and delivered by Objective 4, and needs to be aware of, and even contribute to, other standards and proposed standards in the ecosystem, but will be developed to meet NAPMP needs.

Frequently Asked Questions 17

Can you elaborate on what you mean by "Proposals for this R&D Area must address at least one of Objectives 1-3"?

Proposals can cover any combination of Objectives 1-3, but they must address all the R&D aspects of each objective covered. Proposals offering the most complete solution for each Objective will be preferentially selected.

How are the performers for the objectives meant to work with each other?

Collaboration with other performers within the R&D Area and with other R&D Areas is critically important to the success of the program, and applicants should plan for collaboration with other teams.

NAPMP Next Steps

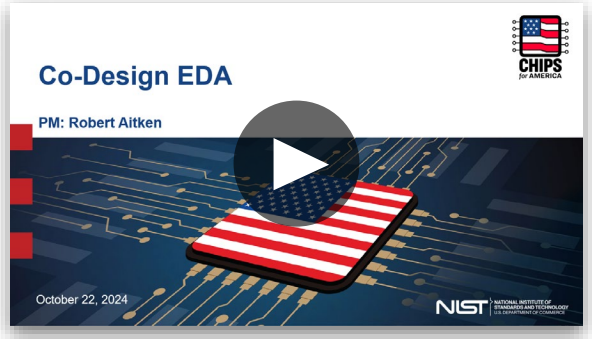
Dev Palmer

Next Steps

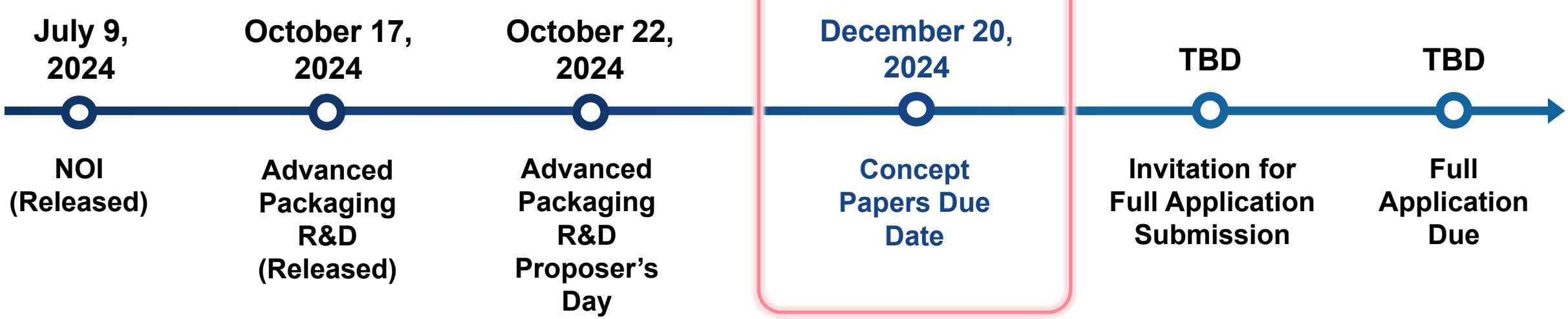
- Visit CHIPS.gov for resources, including:
  - Funding Updates List
  - Funding Opportunities
  - Vision for Success papers
  - Applicant Guides and Templates
  - FAQs and fact sheet
- Join our mailing list
- Contact us at askchips@chips.gov

In Depth Overview of R&D Areas

- Available 10/22/2024
- R&D Area Concept
- R&D Area Drivers
- Key Outputs and Deliverables
- In Scope/Out of Scope
- Program Structure
- Phased Approach
- Collaboration with R&D Areas
- Webinar Links *(coming soon)*
  - Please, visit the **CHIPS for America Webinars** webpage for recording links: https://www.nist.gov/chips/chips-america-webinars



Key Dates



CHIPS for America QR Code:
CHIPS NAPMP NOFO 2
(full text)

Thank you