CHIPS AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes (CARISSMA) Notice of Funding Opportunity

Webinar will begin at 3:00 PM ET.

Will the webinar be recorded?

- Yes, the webinar will be recorded, and both the recording and the slides will be available on the CHIPS R&D Funding Opportunities page here: https://www.nist.gov/chips/chips-rd-fundingopportunities.

Where can I find information on the NOFO being discussed today?

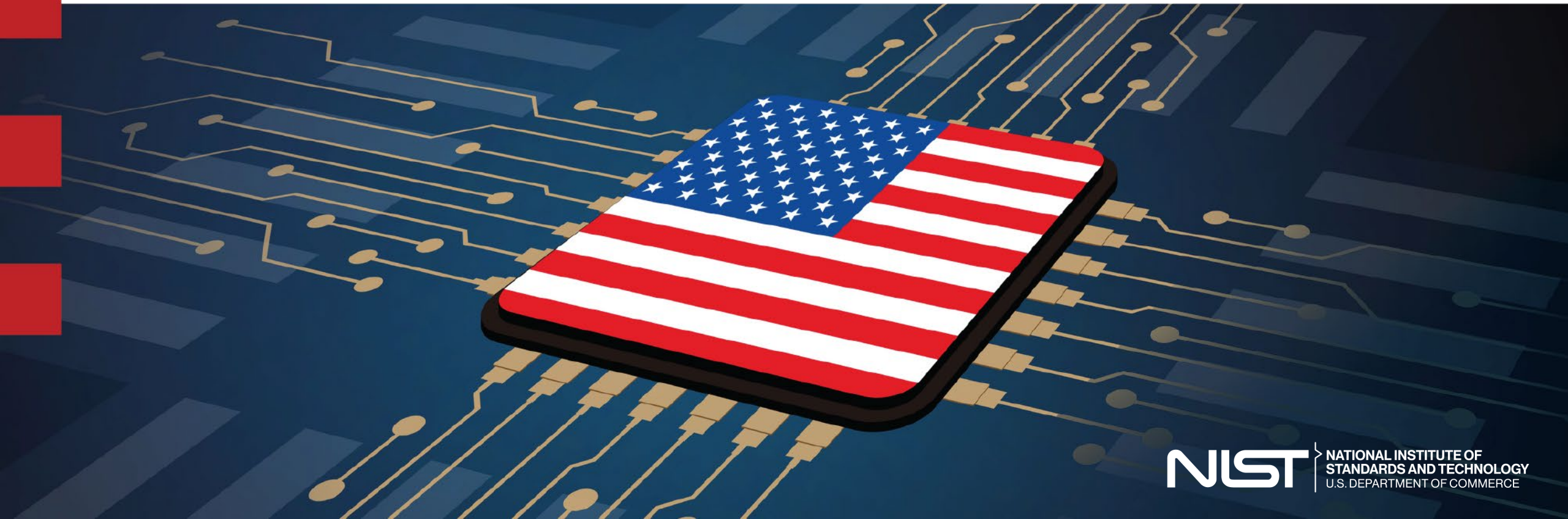
- Interested individuals can find the NOFO on grants.gov: grants.gov/search-results-detail/356912.

What if I have additional questions?

- If you have questions, please contact us at askchips@chips.gov.

CHIPS AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes (CARISSMA)

November 8, 2024



NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Disclaimer

The Notice of Funding Opportunity (NOFO) 2025-NIST-CHIPS-AIAE-01 document is the official competition document.
The following presentation is only a summary of the NOFO document. Please review the NOFO thoroughly prior to starting the application process. Any apparent or actual conflict between the NOFO and this presentation must be resolved in favor of the NOFO.

Today's Speakers

Sarah Georgin

Special Project Manager
CHIPS R&D Office

James Warren

Materials Genome Program Director
NIST

Agenda and Objectives

Agenda

- Introduction to the CHIPS Research & Development (R&D) Office
- CHIPS AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes (CARISSMA) Notice of Funding Opportunity (NOFO) Overview
- Application Process
- CARISSMA NOFO Application Topics
- FAQs
- Next Steps and Additional Resources

By the end, attendees should better understand:

- Vision for Success for the CARISSMA
- Topics this NOFO will address
- How to submit an application in response to this NOFO

Introduction to the CHIPS Research and Development (R&D) Office

CHIPS for America

$39 billion for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

$11 billion for R&D

Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

Together with CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

CHIPS for America Vision

Economic Security

This act enables us to build more resilient supply chains for important components.

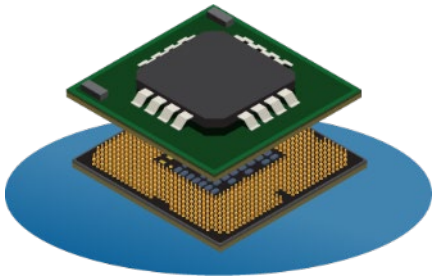
National Security

This act enables us to bring the most sophisticated technologies back to the U.S.

Future Innovation

Chips are key to the technologies and industries of the future, so we need to be at the forefront. This act will ensure long-term U.S. leadership in the sector.

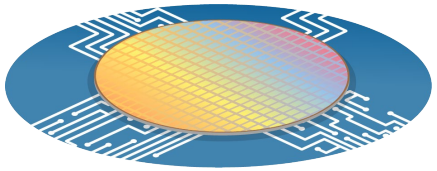
CHIPS R&D Programs



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is a purpose-built nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

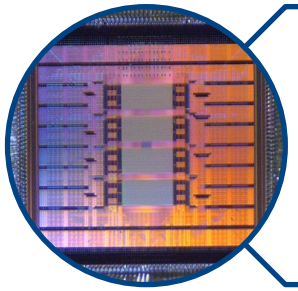
Manufacturing USA

CHIPS Manufacturing USA Program

CHIPS Metrology Program

Workforce Initiatives

2030 Goals

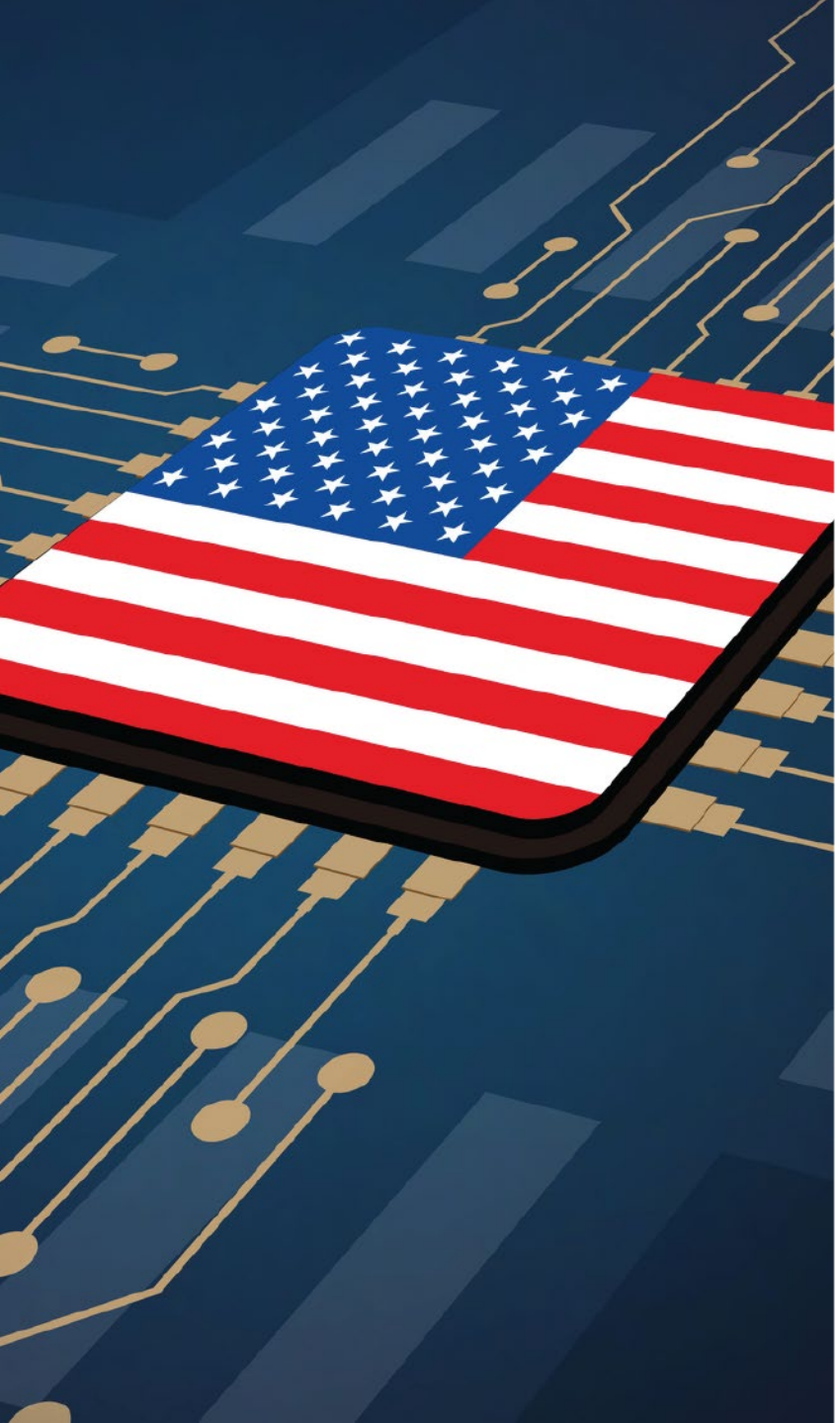


U.S. technology leadership

Accelerate ideas to market

A robust semiconductor workforce

CARISSMA NOFO Overview



CARISSMA NOFO Objectives

1) Accelerate research into and delivery of targeted, industry-relevant, sustainable semiconductor materials and processes through the application of AI/AE;
2) Propagate models for incorporating sustainability metrics into semiconductor industry materials design and discovery, in addition to continued advancement in power, performance, area, cost, or other relevant technology metrics;
3) Expand the capabilities of emerging research institutions and other emerging R&D participants through cohesive, innovative teams of universities, industry, government labs, and other stakeholders; and
4) Build an exceptional workforce of university graduates and faculty with AI/AE R&D expertise.

If successful, CHIPS R&D investments under this NOFO should demonstrate that new sustainable semiconductor materials and processes, meeting industry needs, can be designed and adopted for industry testing within five years. Further, the investment should accelerate a step-change in the number of universities, researchers, and graduates participating in the U.S. semiconductor R&D ecosystem.

Eligibility

Eligible Applicants

- Domestic accredited institutions of higher education and domestic non-profit or for-profit organizations that manage consortia of accredited institutions of higher education.
- Domestic entity is one incorporated within the United States (including U.S. territories) with its principal place of business in the United States (including U.S. territories).

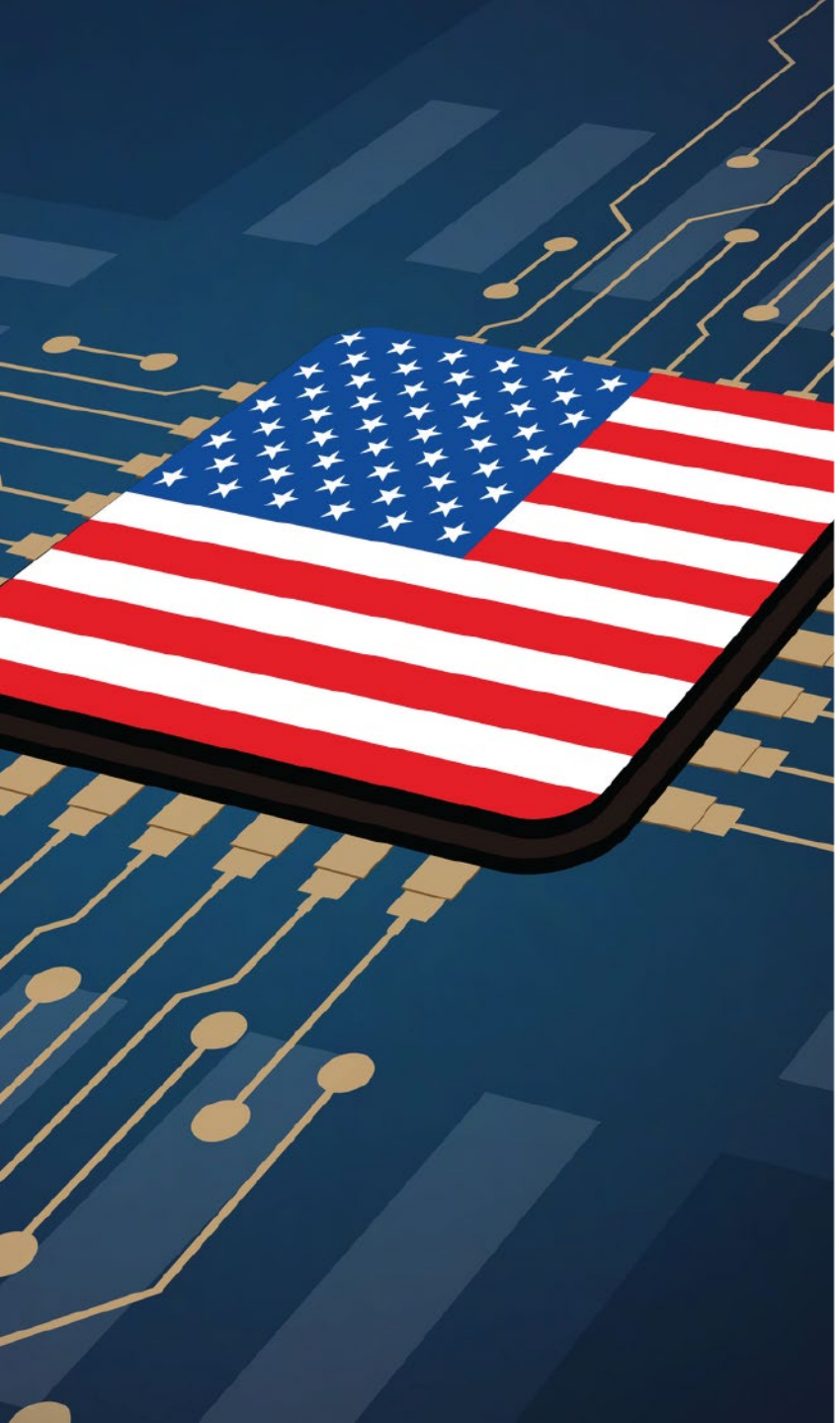
Eligible Subrecipients

- Institutions of higher education; for-profit organizations or non-profit organizations;
- State, local, territorial, and Tribal governments; Federally Funded Research and Development Centers; Federal entities;
- Foreign partners

Additional Requirements

- Eligible Applicants may only submit one concept paper under this NOFO
- Entities may be included as subrecipients on multiple concept papers and applications

Applicants should familiarize themselves thoroughly with the eligibility requirements within the NOFO



University-led Project Teams

RESPONSIVE APPLICATIONS MUST PROPOSE A COLLABORATION AMONG:

- One or more semiconductor industry companies,
- Research universities and/or national laboratories with demonstrated experience in AI/AE or in related fields, and
- At least one ERI (or a domestic non-profit or for-profit organization that manages a consortium of ERIs).

CHIPS R&D FURTHER ENCOURAGES COLLABORATIONS THAT INCLUDE:

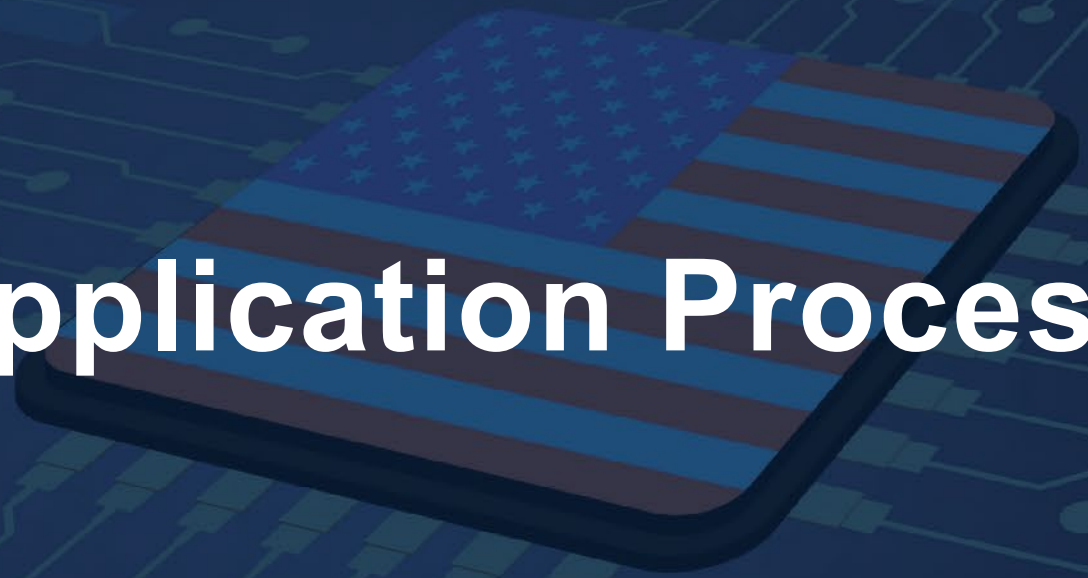
- Civil society or labor organizations focused on environmental sustainability or human health and safety, where appropriate.
- Multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and development capabilities needed to achieve the objectives of this NOFO

CARISSMA NOFO Award Information and Timeline

- Up to approximately **$100 million** in total funding
- Individual awards ranging from approximately **$20 million to $40 million**
- Expecting team of **universities and other research entities** with significant experience in AI-powered autonomous experimentation (AI/AE); semiconductor industry partners; emerging research institutions; and civil society organizations focused on environmental sustainability or human health and safety.

Key Dates

Application Process



Registration Requirements

System for Award Management (SAM.gov)

- Organizations must register with both SAM.gov and Grants.gov to apply.
- Receive Unique Entity ID (UEI), a 12-character alphanumeric ID assigned to an entity.
- SAM.gov registration process can take up to ten days.

Grants.gov

- All applications will be submitted through Grants.gov.
- Applicants should visit Grants.gov for information on any scheduled closures for routine maintenance.
- Large files take several minutes to upload into Grants.gov.

All concept papers due ***no later than*** 11:59 p.m. Eastern Time on **January 13, 2025**

Concept Paper Requirements

Section	Additional Details	Page in NOFO
SF-424 (R&R), Application for Federal Assistance	The SF-424 (R&R) must be signed by an authorized representative of the applicant's organization.	Pg. 51
Technical Content: Cover Sheet and Proposal	The Concept Paper Narrative must not exceed 10 pages with exclusions to page limit noted	Pg. 51
Concept Paper Quad Chart	One-page summary/abstract, suitable for dissemination to the public	Pg. 52
Budget Estimate	A rough order of magnitude estimate of the total project budget, including the lead applicant and any subrecipients. A full budget narrative is required for full applications, if invited.	Pg. 55
Letters of Commitment	Applicants should include letters of commitment from each planned team member (including any subrecipients and unfunded collaborators)	Pg. 55
Letters of Interest	(Optional, but encouraged) Letters of interest should indicate willingness from any third party to support this proposed effort	Pg. 55

Do not submit any classified materials. All "Proprietary" or "Sensitive Business Information" must be clearly marked

Nothing listed supersedes the NOFO. There are additional requirements for full applications detailed in the NOFO

Concept Paper and Full Application Evaluation Criteria

The CHIPS R&D merit review process will assess concept papers against the following five criteria (1 and 2 will receive the greatest and approximately equal weight, 3-5 will receive approximately equal weight) :

(1) Relevance to economic and national security

(2) Overall scientific and technical merit

(3) Project Management (Concept Paper)/Project Management, Resources, and Budget (Full Applications)

(4) Transition and impact strategy

(5) Education and workforce development

The evaluation will be qualitative, not numerical.

Nothing listed supersedes NOFO.

For more information, please reference page 75-77 in the NOFO.

Concept Paper and Full Application Selection Factors

The selection factors in this competition are

(1) **Merit Review:** Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival rankings

(2) **Relevance to Program and Mission:** Alignment with the objectives of this NOFO as well as the mission, goals, and priorities of the CHIPS R&D

(3) **Full application only** **Funding:** The amount available to be awarded under this NOFO is subject to the availability of funds and applications received. CHIPS R&D reserves the right to make no awards under this NOFO

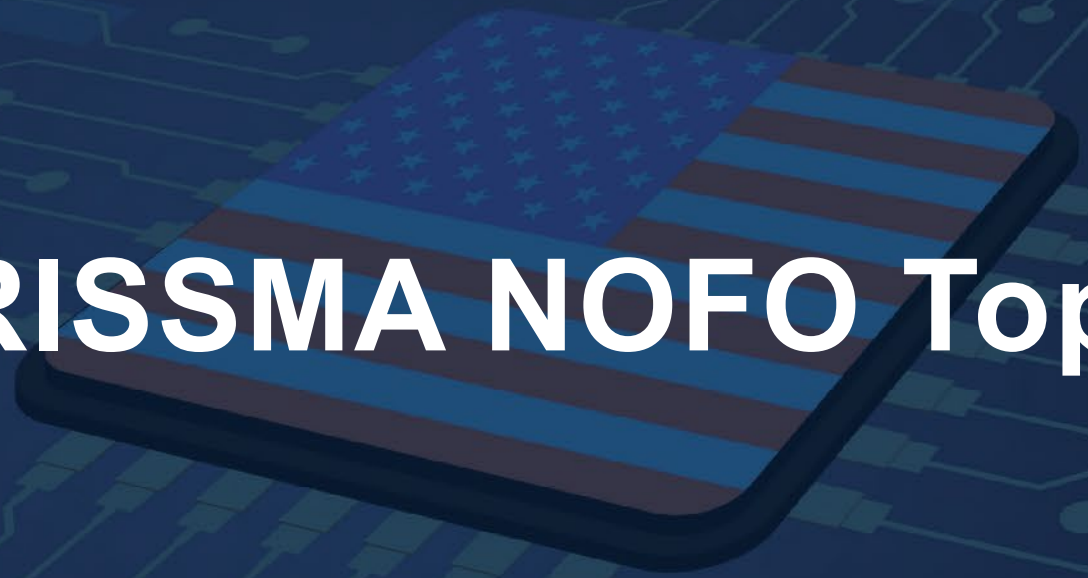
(4) **Non-Duplication:** The degree to which the proposed project duplicates other projects funded by NIST or other Federal sources

(5) **Diversity of Projects and Participants**. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity (including small and medium enterprises, universities, non-profit research organizations, etc.) in the overall CHIPS R&D portfolio

(6) **Broader Impacts and Workforce Development**. The potential for the proposed project to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, environmental responsibility, and regional economic development goals, including plans for broader impact

Nothing listed supersedes NOFO.
For more information, please reference page 75-77 in the NOFO.

CARISSMA NOFO Topics



Program Structure

The Funding Opportunity is structured around:

- **Three Operational Areas**: Responsive applicants must propose activities, milestones, and deliverables to address all three operational areas
- **Materials Classes and Applications**: Responsive applicants must propose focusing on specific material classes and applications relevant to semiconductor manufacturing
- **Co-optimization Targets:** Responsive applications must propose to pursue targeted, industry-relevant materials and processes that co-optimize power- and performance-related materials, process, or device characteristics and sustainability targets
- **Programmatic Targets:** Responsive applications must propose to pursue improvements in the domestic capabilities for AI/AE research and in the research-trained semiconductor workforce. Responsive applications must further propose to pursue the domestic transfer of CHIPS-funded technologies.

Nothing listed supersedes NOFO.

Operational Areas

Responsive applications to this NOFO must propose activities, milestones, and deliverables to address the following three Operational Areas (OAs):

(1) **OA1: Convening, Roadmapping, and Technology Transfer**: Establishing lasting collaborations between stakeholders, refining Co-optimization and Programmatic Targets, and transferring research outputs for further use.

(2) **OA2: AI/AE Infrastructure and Research**: Establishing AI/AE capabilities, to include infrastructure at ERIs and other research universities or access to such infrastructure, and conducting basic and applied research into early TRL materials and processes that address semiconductor industry needs.

(3) **OA3: Education and Workforce Development**: Developing and expanding the total number of domestic researchers skilled in AI/AE methods relevant to the semiconductor industry materials and processes.

Proposals must address ALL three operational areas

Nothing listed supersedes NOFO.
For more information, please reference page 17 in the NOFO.

Materials Classes and Applications

- Applicants must propose focusing on specific material classes and applications relevant to semiconductor manufacturing.
- Proposals must demonstrate the expected impact on metrics related to both the sustainability of semiconductor manufacturing and to materials, process, or device performance characteristics, which may include device performance, power, area, and cost (PPAC).
- Proposals may seek to either improve existing materials an processes or enable realization of next-generation materials, processes, or devices.

Table 2. Non-Exhaustive List of Notional Materials Classes and Applications

• Abatement catalysts • Adhesives • Atomic Layer Deposition (ALD) • Antireflective Coatings • Chemical Mechanical Planarization (CMP) slurries • Dielectrics and insulators • Dopants • Epitaxy and deposition gases • Etch gases • Filters and membranes • Heat transfer fluids (HTFs) • Interconnects • Lubricants	• Memory materials • Metals and conductors • PFAS • Polymers and resins • Photonic materials • Photoresists • Photoacid generators (PAGs) • Redistribution Layer films (RDLs) • Solvents • Substrates • Surfactants • Thermal Interface Materials (TIMs) • Underfills • Wet etchants • 2D materials

Nothing listed supersedes NOFO.

Co-optimization Targets

- Co-optimization Targets are grouped into four Themes:
  - **Theme 1:** Materials, Process, or Device Power- and Performance- related Characteristics
  - **Theme 2:** Emissions and Hazardous Waste
  - **Theme 3:** Energy Consumption
  - **Theme 4:** Water Consumption
- Applicants must propose to pursue targeted, industry-relevant materials and processes that co-optimize power- and performance-related materials, process, or device characteristics (Theme 1) and sustainability targets (Theme 2–4)
- Applications that pursue manufacturing sustainability (Themes 2–4) without co-optimizing for Theme 1 will be considered out of scope. Proposals must address at least one or more of Themes 2, 3, or 4, to target improvements in the sustainability of current or future semiconductor manufacturing techniques. Proposals that improve device performance without addressing manufacturing sustainability will be considered out of scope.

For more information, please reference page 18-20 in the NOFO.

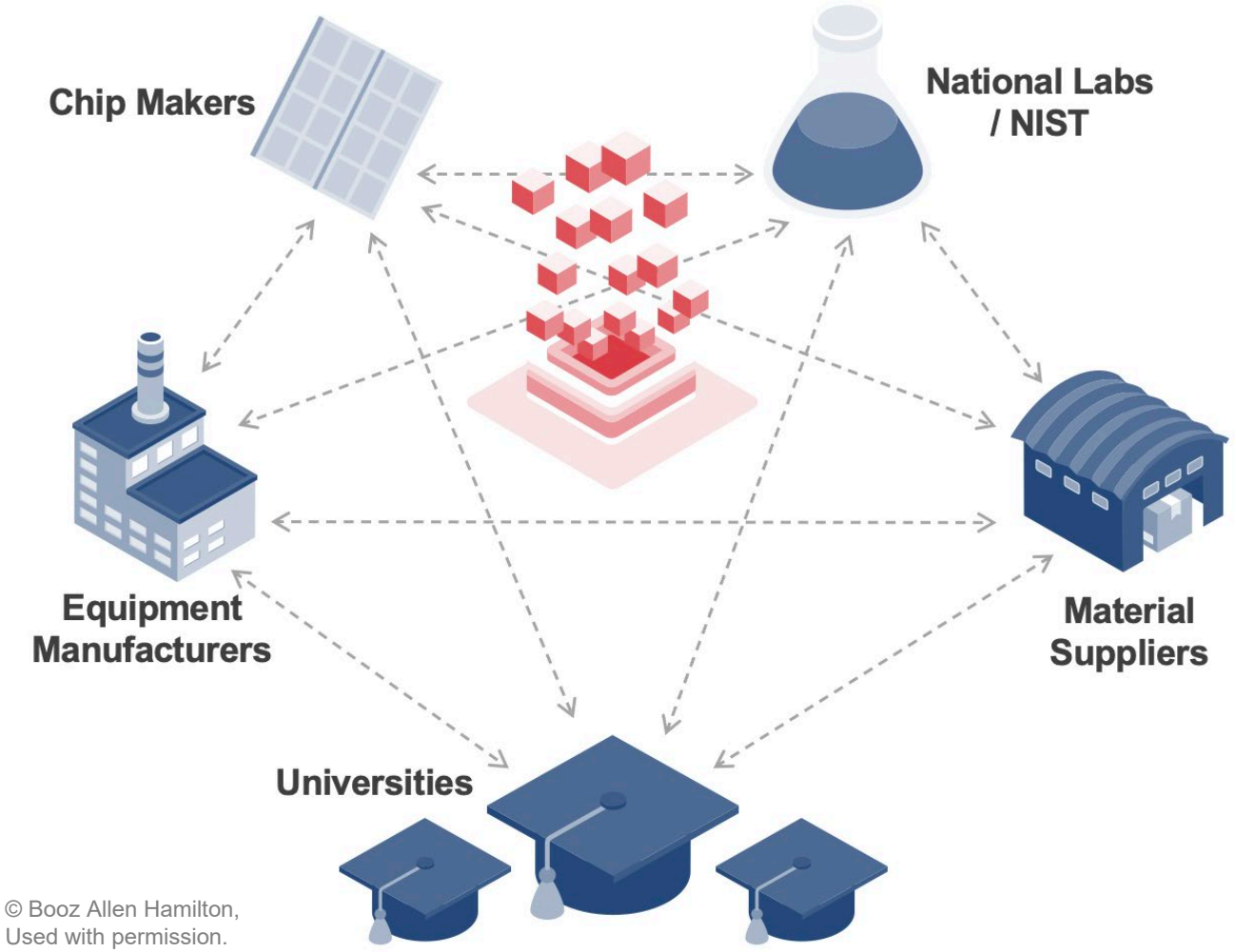
Programmatic Targets

Applicants must propose **SMART** targets to pursue the following themes:

- **Theme 5: Research Capacity:** Applications must demonstrate how CHIPS-funded activities will increase the overall research capacity of the domestic semiconductor innovation ecosystem, particularly as it relates to AI/AE
- **Theme 6: Education and Workforce Development (EWD):** Applications must provide a plan to achieve improvements in the availability of state-of-the-art (SOTA) research-trained personnel
- **Theme 7: Domestic Technology Transfer:** Applications must demonstrate, with rigor increasing across the award period of performance, the ability for CHIPS-funded research outputs to successfully transfer to the domestic commercial marketplace

Nothing listed supersedes NOFO.

Partnership and Collaboration Models



Federated AI/AE

- Structures can range from a more centralized “hub” to a fully federated model
- Federation of the digital and physical infrastructure of AI/AE systems is both possible and potentially desirable
- AI/AE researchers can virtualize pieces of the workflow and digital objects (e.g., computer code, digital twins, data, and control software enabling remote operation)
- A “multi-agent” approach, which combines information from diverse research campaigns, can support AI/AE research strategies
- System provides the ability to remotely access equipment hosted by collaborators from other institutions.

Notional Example of Project Phases

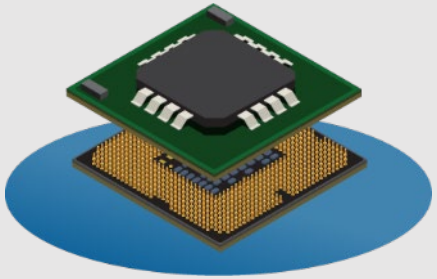
- Finalize teaming structure, including for industry and civil society partner organizations
- Establish Research Advisory Board
- Refine Co-optimization and Programmatic Targets based on technoeconomic and lifecycle analyses
- Refine the Phase-specific Research Plan and CV, including a roadmap from R&D to industry adoption
- Determine AI/AE system components and workflow design
- Install, integrate, and test equipment and software
- Assemble project team with faculty, staff, students, and post-docs onboarded
- Refine EWD Plan and begin to develop and teach AI/AE curricula at participating universities
- Join CHIPS Manufacturing USA Institute and the NSTC, as appropriate

- Continue to conduct basic and applied research based on Phase 1 results
- Demonstrate effective industry-university feedback loops with progress toward targets
- Demonstrate an effective collaboration environment, workflow, throughput, and quality of R&D output of AI/AE systems
- Refine digital twins, custom software, application programming interfaces (APIs), and co-optimization algorithms
- Deploy preliminary materials digital twins
- Deliver first-round materials to industry for assessment with respect to Co-optimization Targets and AI/AE system performance
- Update EWD plan and continue to train students and post-docs using relevant AI/AE curricula

- Conduct tests, led by industry, to establish the performance of multiple co-optimized sustainable semiconductor materials and processes
- Catalog and accelerate technology transfer and adoption by industry partners and secure industry commitments to deploy the technology
- Affirm the commercial viability, environmental impact, and supply chain impacts of potential research outputs
- Disseminate equipment and materials digital twins to industry, the CHIPS Manufacturing USA Institute, and the NSTC, as appropriate
- Execute plans to ensure sustained leadership, capabilities, and capacity for AI/AE at universities, including ERIs, and in the private sector
- Deliver final reports and best practice at CHIPS R&D

CHIPS R&D Programs

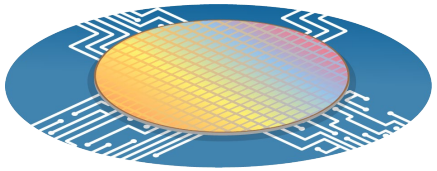
Research outputs should prove relevant and translatable to industry, the NSTC, the CHIPS Manufacturing USA program, and other CHIPS programs. Activities must include participating in the CHIPS Manufacturing USA Program.



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast

Natcast is a purpose-built nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

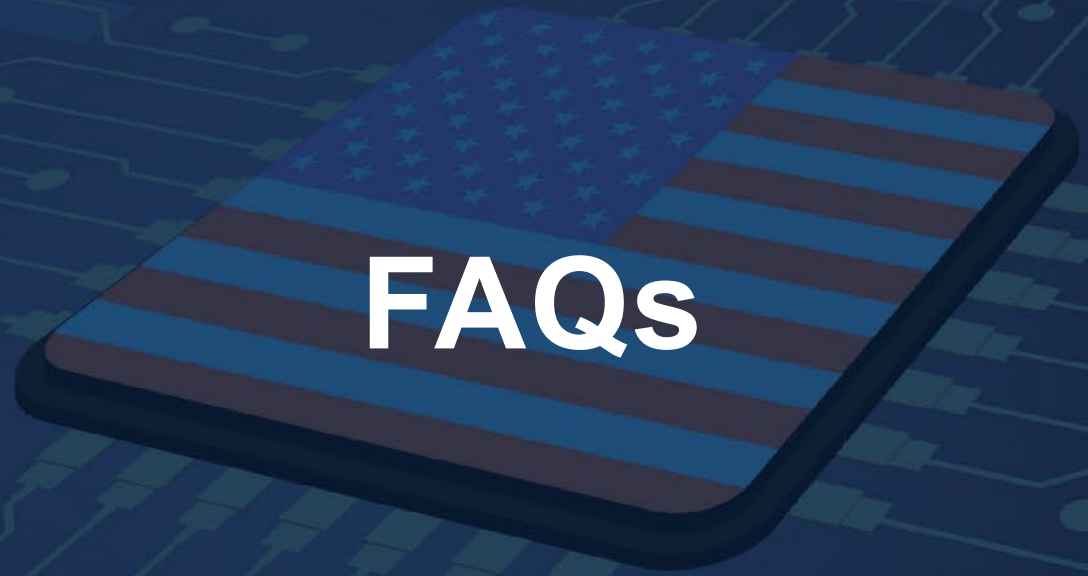
Manufacturing USA®

CHIPS Manufacturing USA Program

CHIPS Metrology Program

Workforce Initiatives

FAQs



Frequently Asked Questions

Can applicants submit more than one concept paper?

Eligible applicants may submit only one concept paper and, if invited, one full application.

Can an organization be listed as a subrecipient on multiple applications?

Yes. Eligible subrecipients may be included in more than one application.

How much funding will be awarded?

CHIPS R&D anticipates a total Federal commitment of up to approximately $100 million, with multiple awards in amounts ranging from approximately $20 million to $40 million per award.

Frequently Asked Questions (cont.)

What is an emerging research institution?

An emerging research institute (ERI) is an institution of higher education with an established undergraduate or graduate program that conducts less than $50 million per year in Federal research expenditures.

Do I need to have a partnership with an Emerging Research Institution to be considered for this funding opportunity?

Project teams must include faculty from one or more ERIs serving as a Principal Investigator or co-Principal Investigator.

Next Steps and Additional Resources

Join us for Proposers' Day, Friday November 15!

- **What:** CHIPS R&D will host a one-day meeting for potential applicants to the CARISSMA NOFO. This will be a hybrid event, composed of a morning plenary session, afternoon networking sessions, and a poster session enabling entities to share information, foster collaboration, and advance shared goals. In-person attendance is highly encouraged.
- **When:** Friday, November 15, 2024
- **Where:** Herbert. C. Hoover Building, Department of Commerce
- Deadline to register is **Monday November 11th at 5 PM EST**
- **Register here:** https://www.nist.gov/news-events/events/2024/11/chips-rd-carissma-program-proposers-day

Next Steps

- Verify your eligibility and complete all registration requirements.
- Download the NOFO and look through the full document, Contact NIST to address any questions.
- Review the Technical Targets, Co-optimization Targets, and Programmatic Targets. Review all Operational Areas
- Determine Project Team
- Draft your concept paper, ensuring all required sections are completed and identified needs are addressed.
- Apply via Grants.gov **by 11:59 p.m. Eastern Time on January 13, 2025.** Give yourself ample time to complete the application.

Resources

- **2025-AIAE-CHIPS-01 NOFO** link: grants.gov/search-results-detail/356912
- **NIST CARISSMA** page: https://www.nist.gov/chips/notice-funding-opportunity-carissma
- **NIST CARISSMA Frequently Asked Questions** (FAQs): https://www.nist.gov/chips/frequently-asked-questions-carissma-nofo
- **CHIPS R&D CARISSMA Program Proposers' Day**: https://www.nist.gov/news-events/events/2024/11/chips-rd-carissma-program-proposers-day
- **CHIPS R&D Funding Opportunities** page: https://www.nist.gov/chips/chips-rd-funding-opportunities
- **Strategic Opportunities in U.S. Semiconductor Manufacturing**: https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

Thank You!