CHIPS R&D Chiplets Interfaces Technical Standards Workshop

DRAFT AGENDA

DAY 1: December 12, 2023/ 8:30 AM - 5:35 PM		
TIME	**TOPIC**	**PRESENTER**
7:30 –8:30 am	Check-in	
8:30 –8:35 am	Introduction to the workshop / review agenda / logistics	Jan Obrzut (*CHIPS R&D*)
8:35 –8:45 am	Welcome remarks	Subramanian Iyer (*CHIPS R&D*)
8:45 – 9:00 am	**Keynote** – Importance of Technical Standards in the Semiconductor Ecosystem	Kathleen Kingscott (*IBM Research*)
9:00 – 10:30 am	**Panel 1: Tutorial on chiplets interface standards**	Lalitha Immaneni (*Intel*) *Moderator*
	1) Die-to-die parallel interfaces for the emerging chiplet market 2) Open domain-specific architecture (ODSA) open physical and logical die-to-die interfaces for chiplets 3) Standards for device test 4) The realities of physical limits and prospects for 2 / 2.5 -D and 3-D interconnects	1) Elad Alon (*Blue Cheeta Analog*) (Virtual) 2) Bapi Vinnakota (*Open Compute Project*) 3) Sreejit Chakravarty (*Ampere*) 4) Dev Gupta (*APSTL*) (Virtual)
10:30 –10:45 am	Break	
10:45 –11:45 am	**Breakout Session 1**: Discuss and prioritize ideas related to panel 1	Led by *SIDEM* and *Corner Alliance* facilitators
11:45 –12:00 pm	**Report Out** from Breakout Session 1	Workshop participants and facilitators
12:00 –1:15 pm	Lunch	
1:15 –2:15pm	**Panel 2: What is the state of the art in chiplets interfaces?**	Gretchen Greene (*NIST*) *Moderator*
	1) DARPA CHIPS standards 2) Packaging and chiplet standards gaps 3) Advanced packaging, assembly, test and failure analysis 4) Experience and ideas for enhancing the chiplet ecosystem, die-to-die interfaces, packaging supply chain limitations, business model challenges, and optical packaging requirements. 5) Chiplets interfaces challenges in packaging	1) Andreas Olofsson (*Zero ASIC*) 2) Lalitha Immaneni (*Intel*) 3) Yan Li (*Samsung*) 4) Chen Sun (*Ayar Labs*) (Virtual) 5) Jeff Rearick (*AMD*) (*Virtual*)
2:15 –3:15pm	**Breakout Session 2**: Discuss and prioritize ideas related to panel 2	Led by *SIDEM* and *Corner Alliance* facilitators
3:15 –3:30pm	**Report Out** from Breakout Session 2	Workshop participants and facilitators
3:30 –4:00pm	Break	

4:00 –4:45 pm	**Panel 3: What is the current state of research in chiplets?**	Veruska Malave (NIST) *Moderator*
	1) Photonics packaging 2) TBD 3) Security-aware computer aided design, test, verification, validation, and reliability 4) The tradeoffs between performance and resources in natural and engineered systems	1) Peter O'Brien (*Tyndall Institute*) (Virtual) 2) Ganesh Subbarayan (*Purdue University*) 3) Ramesh Karri (*NYU*) 4) Pamela Abshire (*U. Md*)
4:45 –5:15 pm	**Breakout Session 3**: Prioritize ideas from panels 1, panel 2, and panel 3	Led by *SIDEM* and *Corner Alliance* facilitators
5:15 – 5:35pm	**Report Out** from Breakout Session 3	Workshop participants and facilitators
5:35pm	Adjourn	

DAY 2: December 13, 2023/ 8:30 AM – 12:00 PM		
8:30 –9:30 am	**PANEL 4: Summary Discussion/Takeaways from Day 1**	Andreas Olofsson (*Zero Asic*) *Moderator*
	Questions: • What are the technical standards gaps? • What information is needed to address the gaps? • How do we prioritize which standards to work on? • Who can help with the standards development effort? • Which SSO's should be working on these issues?	Panelists: 1) Bapi Vinnakota (*Open Compute Project*) 2) Lalitha Immaneni (*Intel*) 3) Chen Sun (*Aylar Labs*) (Virtual) 4) Melissa Grupen-Shemansky (*SEMI*) 5) Debendra Das Sharma (*UCIe Consortium Standards*) (*Virtual*)
9:30 – 10:30 am	**Breakout Session 4**: Discuss and prioritize ideas related to panel 4	Led by *SIDEM* and *Corner Alliance* facilitators
10:30 –11:00 am	Break	
11:00 –12:00pm	**Report Out** from Breakout Session 4 and consolidation of priorities	Workshop participants and facilitators
12:00 –12:30 pm	Discuss next steps	Jan Obrzut & Yaw Obeng (*CHIPS R&D Office*)
12:30 pm	End of workshop - adjourn	