Research Challenges for CMOS Scaling: Industry Directions

NIST EEEL:
Frontiers of Characterization and Metrology for Nanoelectronics
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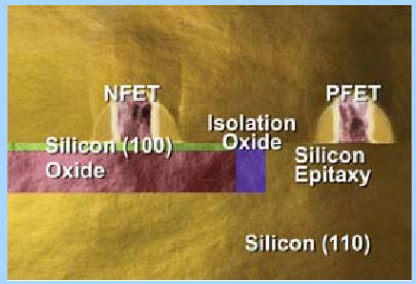
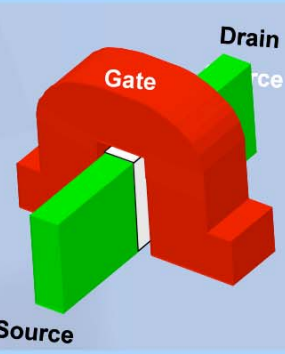
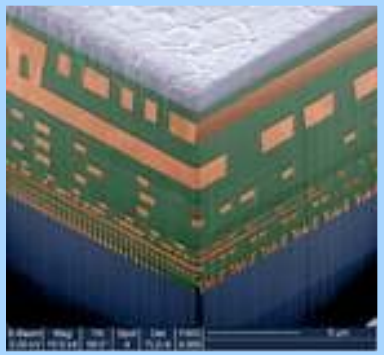
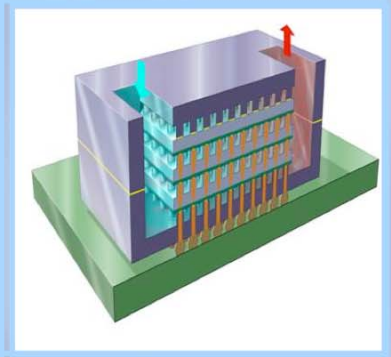
T.C. Chen, IBM Fellow
V.P., Science & Technology
IBM Research



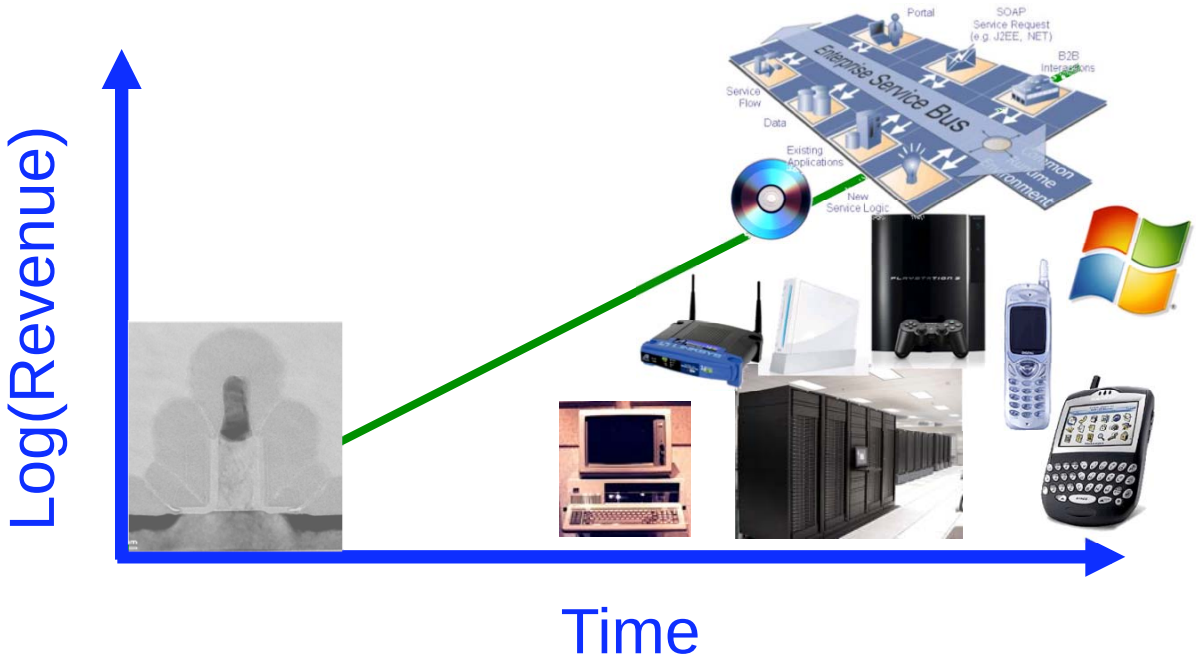






Environment: *IT Industry*

The Transistor Historically Fueled IT Growth

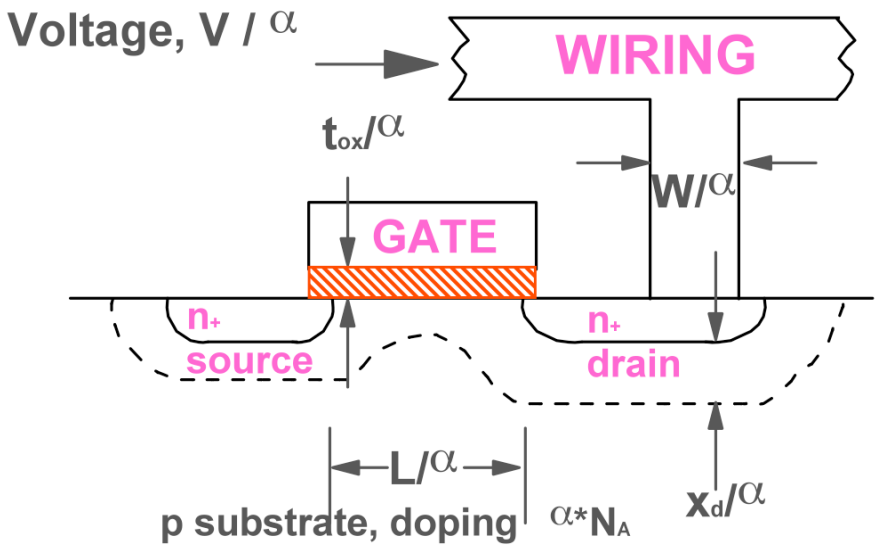


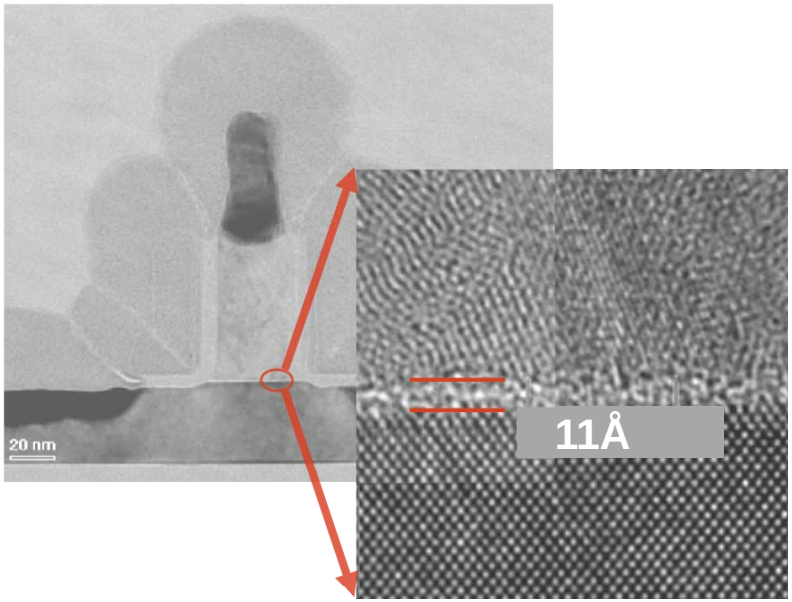
IT Industry:
Infrastructure
& Solutions

- **How far can silicon technology be extended ?**

CMOS Scaling Rules

Dimensions Approaching Atomistic & Quantum-Mechanical Boundaries





SCALING:

Voltage:	V/α
Oxide:	t_{ox}/α
Wire width:	W/α
Gate width:	L/α
Diffusion:	x_d/α
Substrate:	$\alpha * N_A$

R. H. Dennard *et al.*,
IEEE J. Solid State Circuits, (1974).

RESULTS:

Higher Density:	$\sim\alpha^2$
Higher Speed:	$\sim\alpha$
Power/ckt:	$\sim 1/\alpha^2$
Power Density:	~~~Constant~~

Atoms are NOT Scalable!

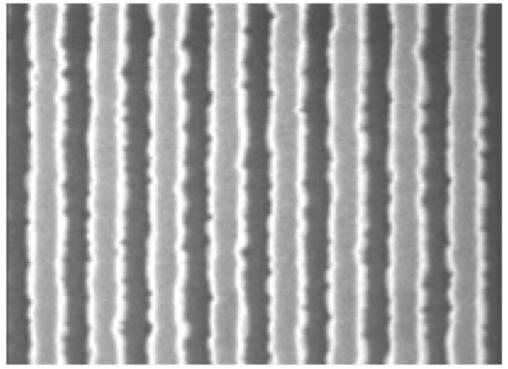
Challenges in Extending Si-CMOS Technology

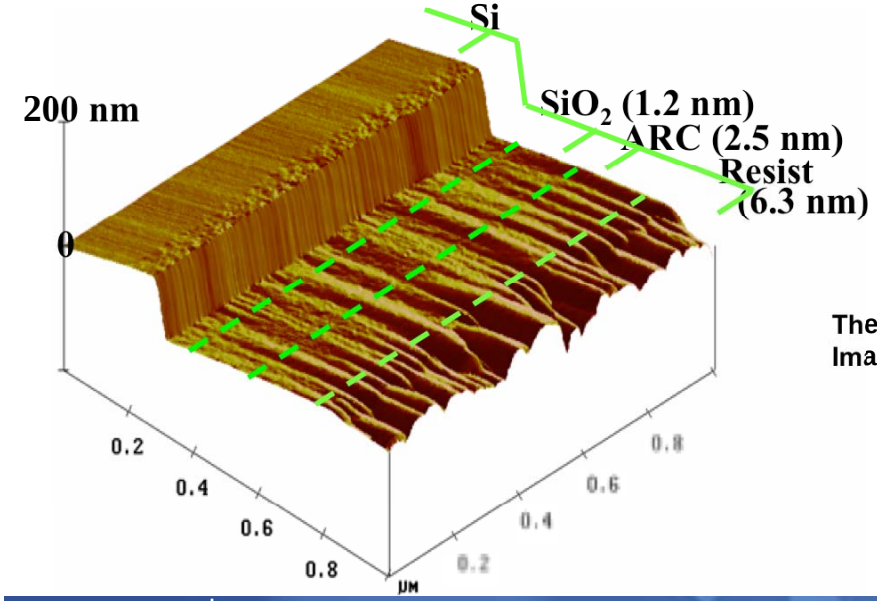
Dimensions Approaching Atomistic & Quantum-Mechanical Boundaries

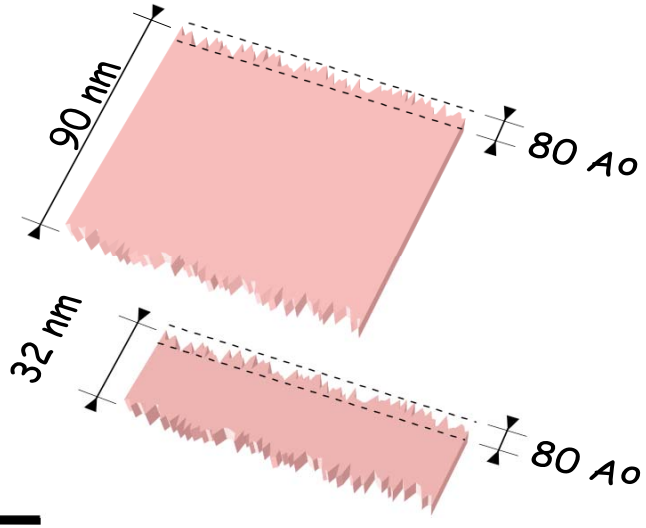
- **Growing Device & Chip Power Dissipation**
- **Increasing Process & Device Variability**
- **Degraded Device Performance With Scaling**
- **Formidable Lithography Capability & Process Complexity**
- **Degraded Interconncet RC Performance Scaling**

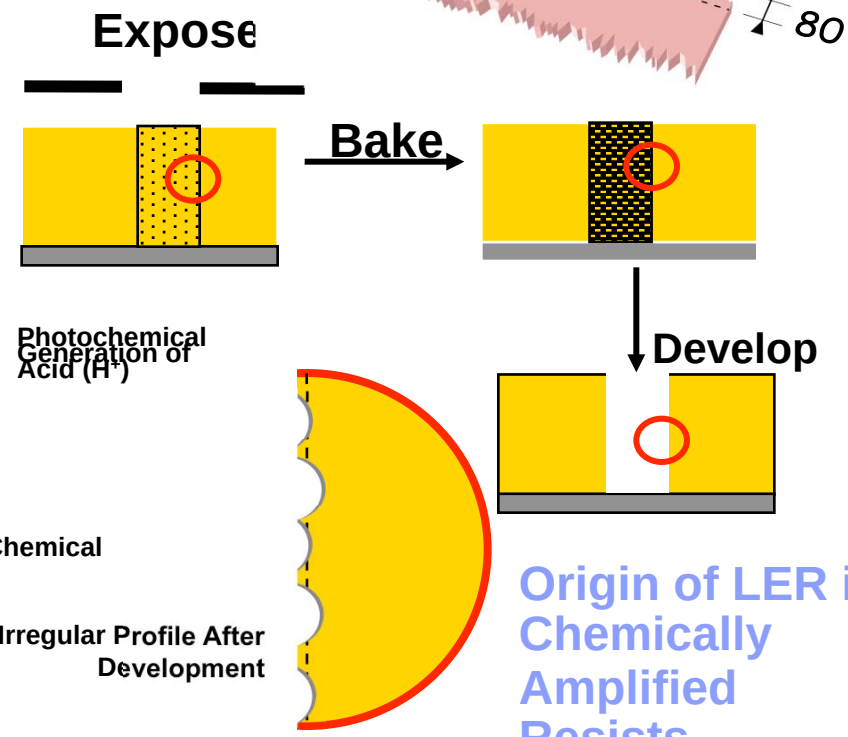
Localized Variability

Example: *Line Edge Roughness (LER)*





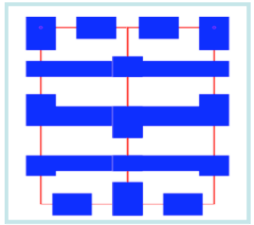
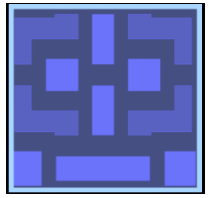
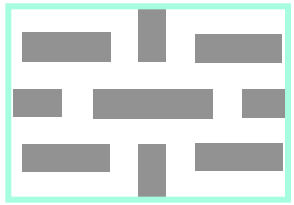
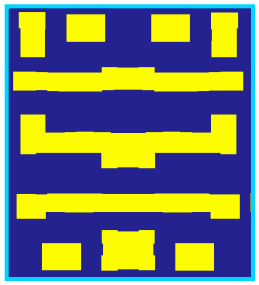
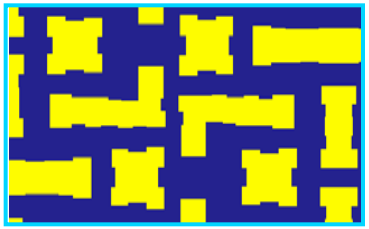
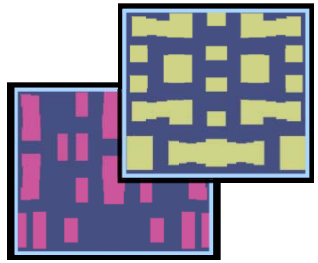
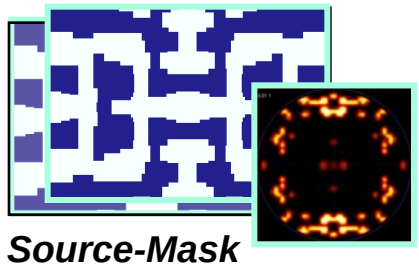
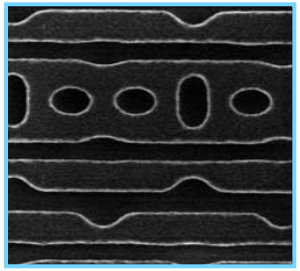
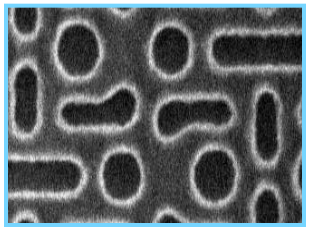
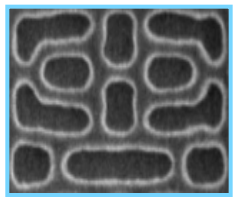
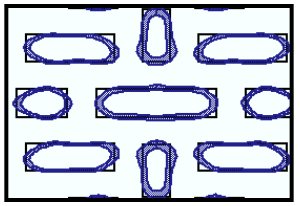




Origin of LER in Chemically Amplified Resists

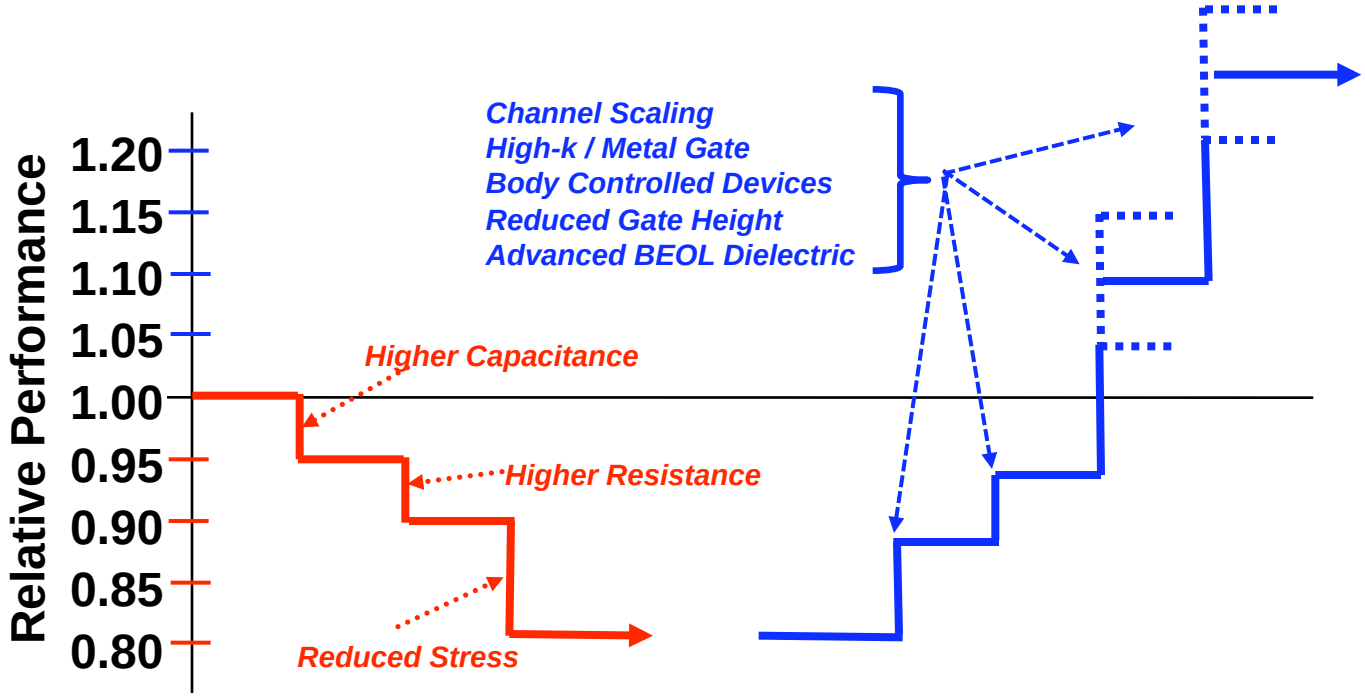
RET: Enabling Lower k1 Factors

Designs Get More Regular, Resolution Enhancement Techniques Get More Complex

Design =	*Mask*	*Mask + Correction + Assist*	*2 Masks + Correction + Assists*	*Optimized Mask(s) + Optimized Source*
	90 nm	**65 & 45 nm**	**32 & 28 nm**	**22 nm & Beyond**
Design (M1 SRAM)				
Mask				 *Source-Mask Optimization*
Wafer / Contour				

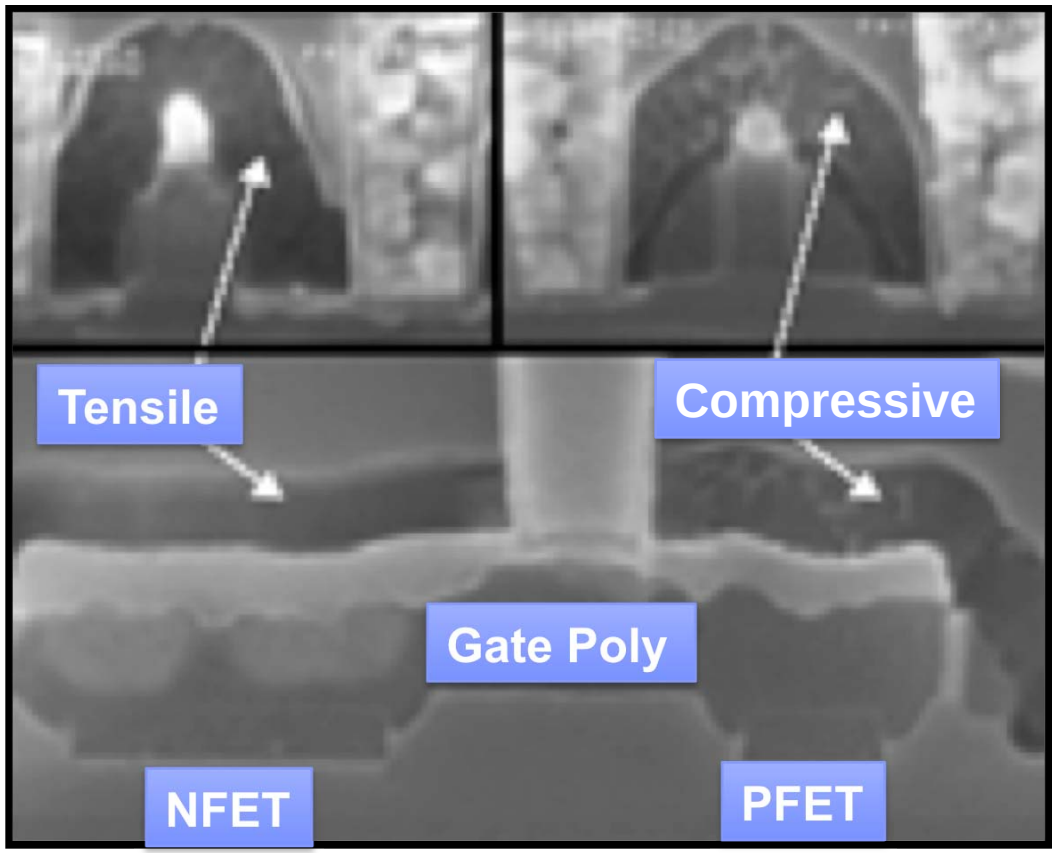
Performance Degradation at Tight Pitch

Significant Innovation In Performance-Enhancing Elements Required



Stress Engineering Innovation

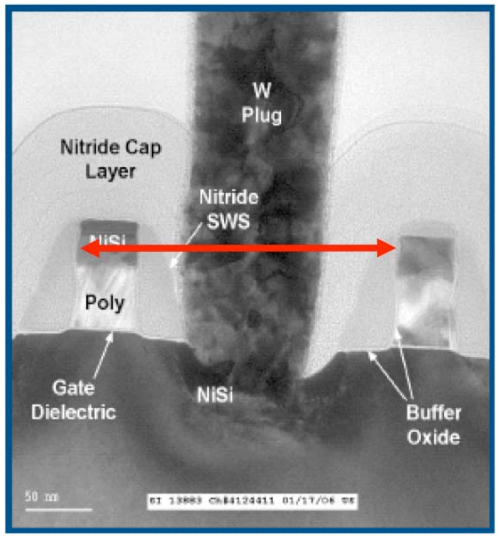
Example: *Dual Stress Liner for 90nm*

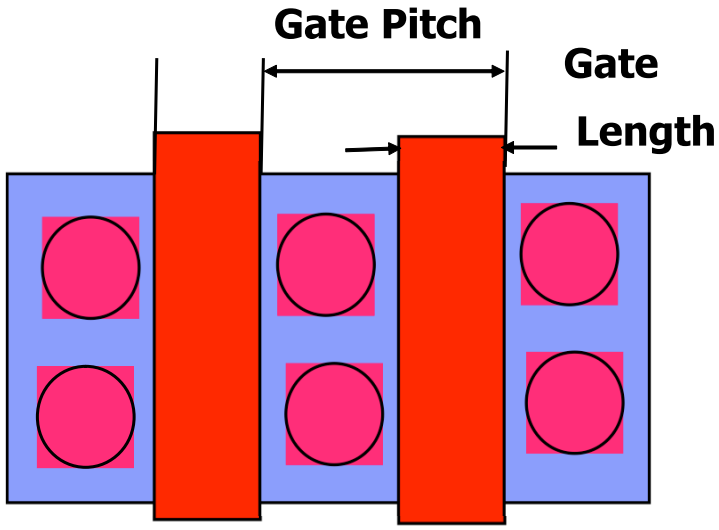


H.S. Yang et al. IEDM 2004

Gate Length Requirement

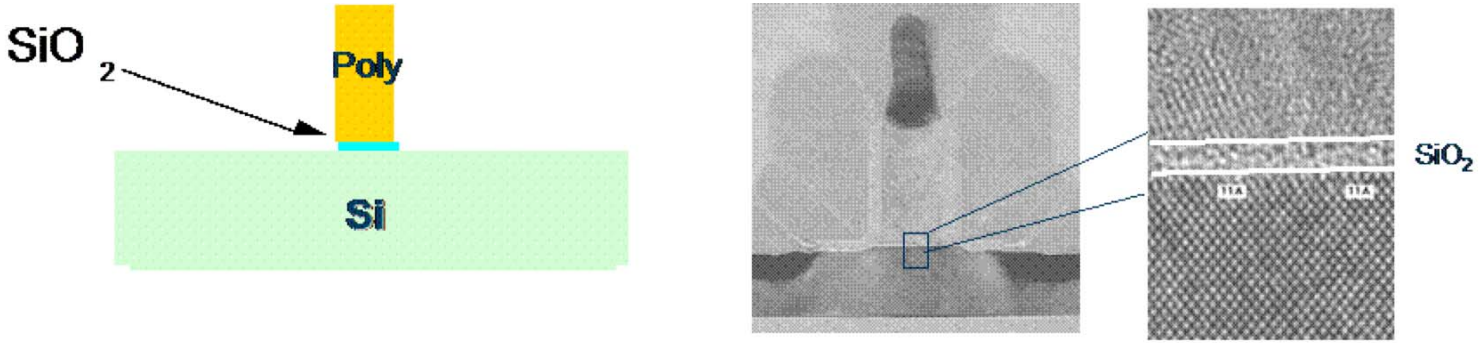
Node	Device Pitch (nm)	Nominal L (nm) (required to fit pitch)
45	170-180	40-45
32	120-130	30-37
22	80-100	20-30
15	60-70	15-23
11	45-50	12-18





High-k Gate First Flow: *Simple and Scalable*

Material Breakthrough Enables Conventional High-temperature Processing



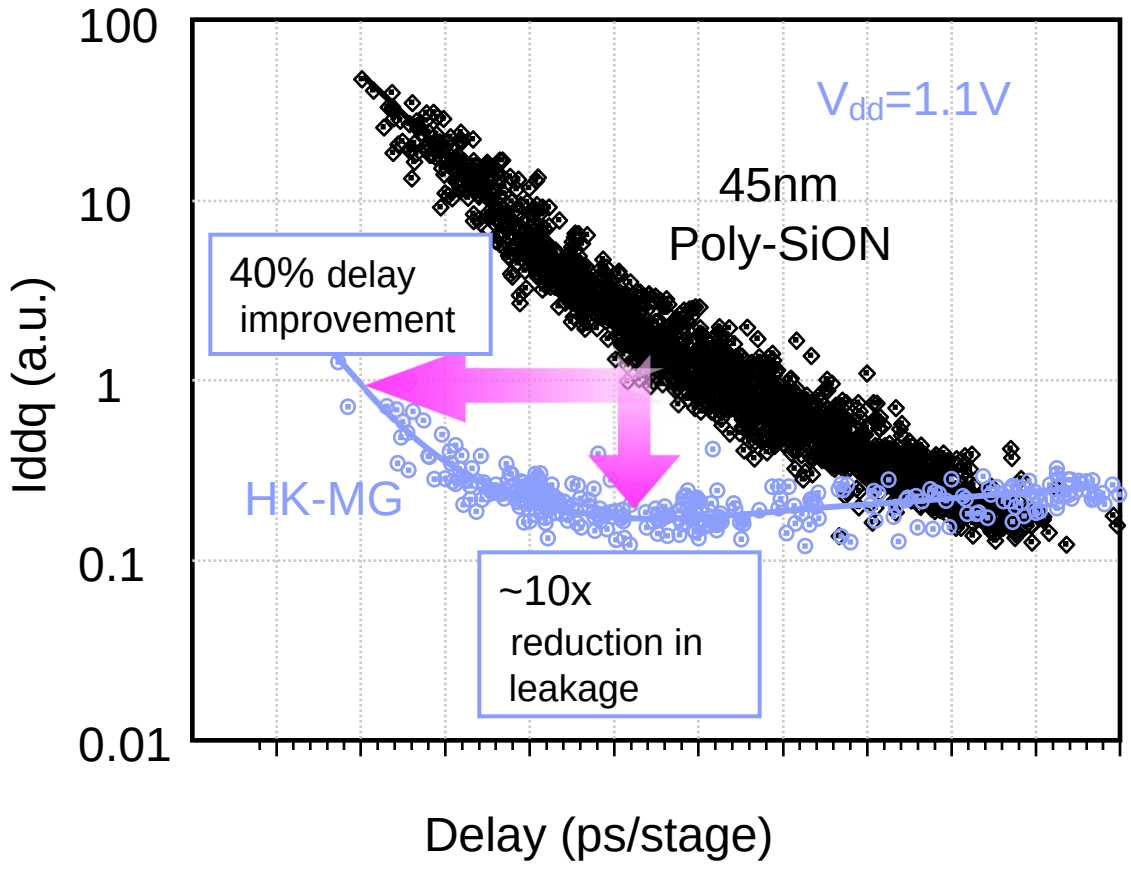
Conventional (Non High-K)

Gate First Process with HKMG

Scalable process for future technology

AC Performance Improvement with HK-MG

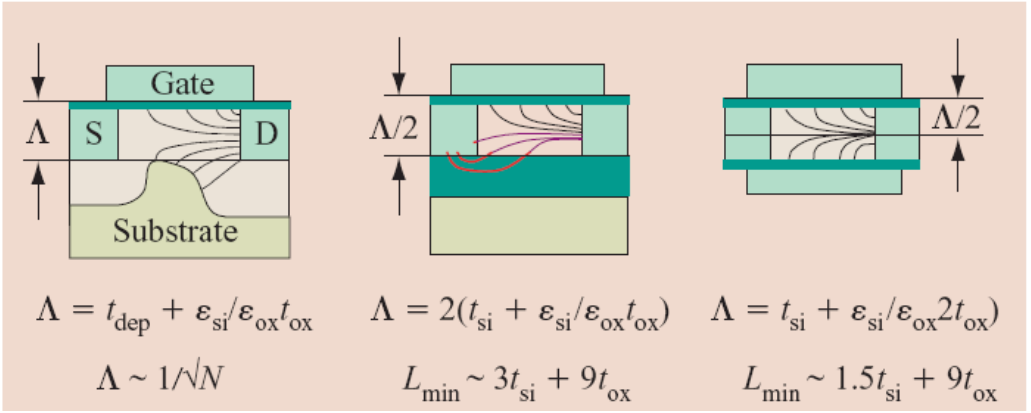
40% Delay Improvement At Fixed Leakage Or 10x Leakage Reduction At Fixed Delay



X. Chen et al., VLSI 2008

FinFET Advantages

- **Better short channel control**
- **Short channel effect is controlled by the thickness of the thin body instead of channel doping**
  - Reduced random dopant fluctuation
  - Improved mobility due to lower vertical field and less coulombic scattering
  - Improved DIBL and SS due to better control of SCE
- **Much lower parasitic junction capacitance**
- **Performance boost for pFET with <110> conducting surfaces**

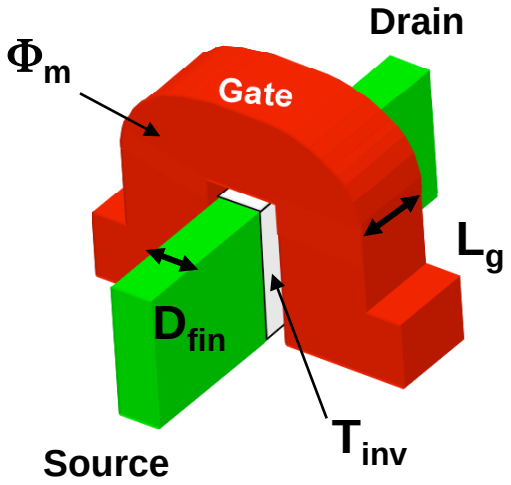


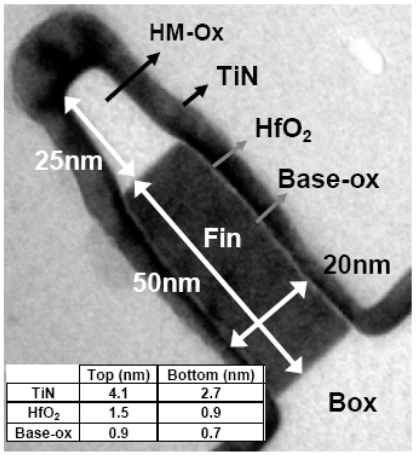
Planar bulk **Planar FDSOI** **FD DGFET**

W. Haensch, et al IBM J of R&D July 2006

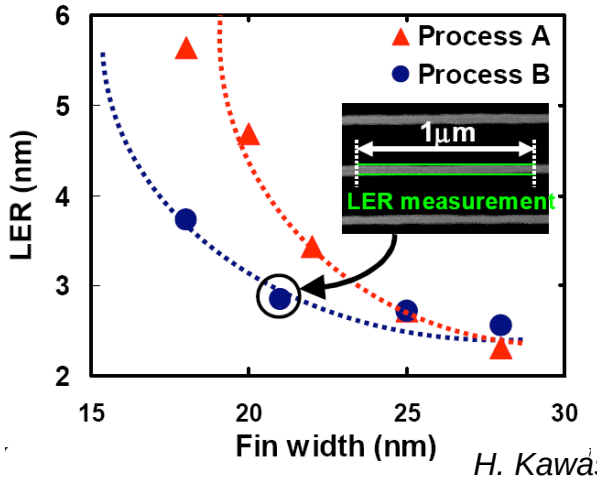
FinFET Challenges – Variability Control

- **Variability in FinFETs**
  - Fin thickness (Dfin) variation
  - Gate length (Lg) variation
  - Metal gate-workfunction (Fm) variation
  - Tinv variation
  - Vertical extension doping homogeneousness along the sidewall
  - Resistance variation





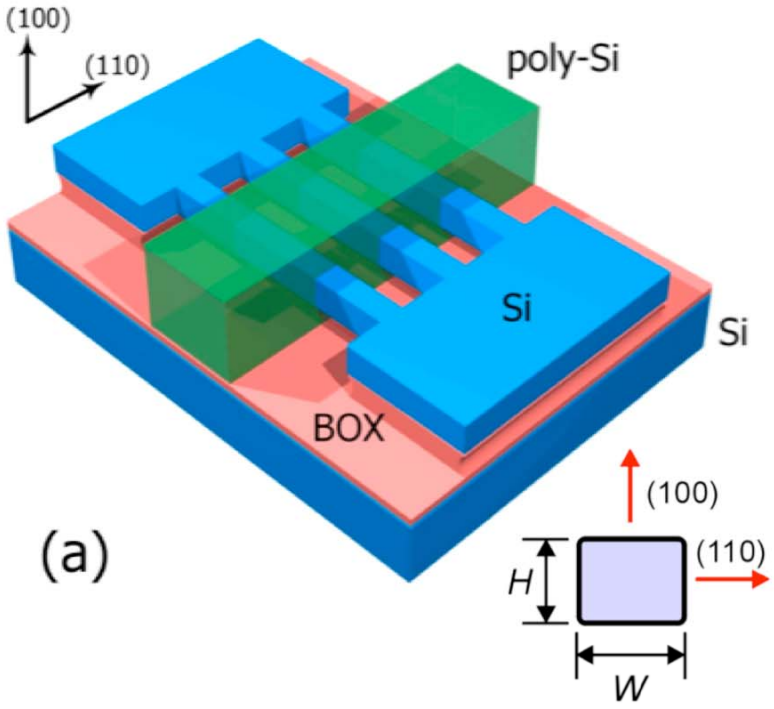
	Top (nm)	Bottom (nm)
TiN	4.1	2.7
HfO_2	1.5	0.9
Base-ox	0.9	0.7

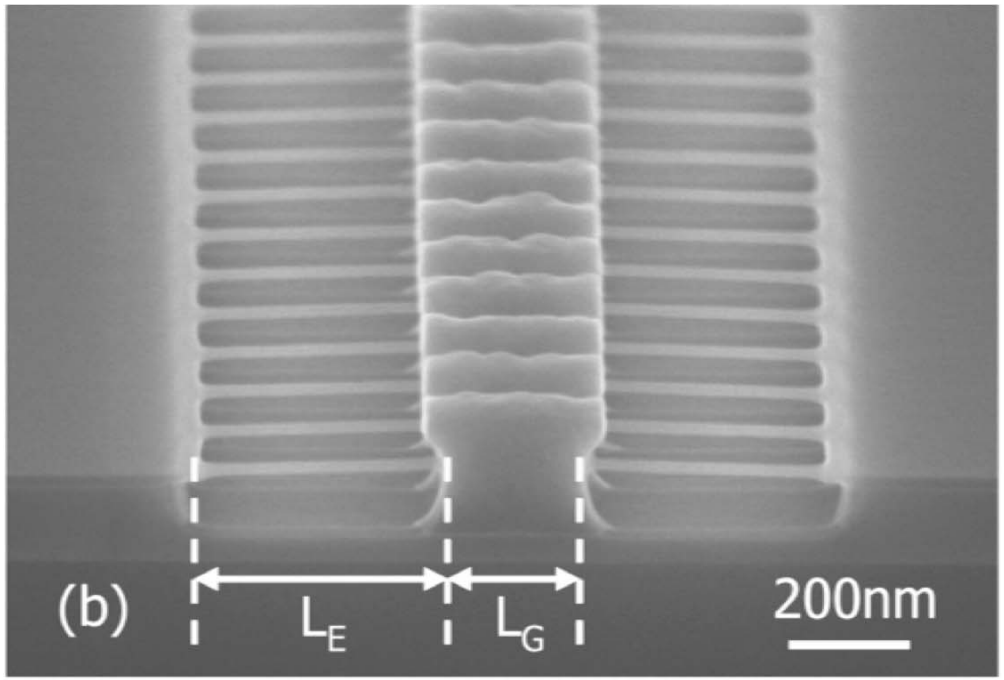


H. Kawasaki, et al IEDM 2008

Silicon Nanowires

The Ultimate Si Field Effect Transistor

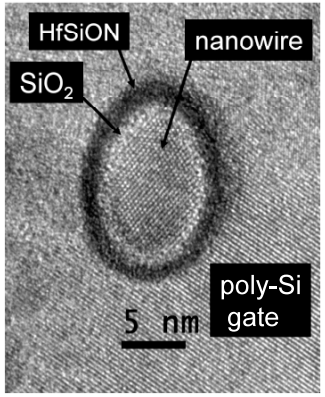


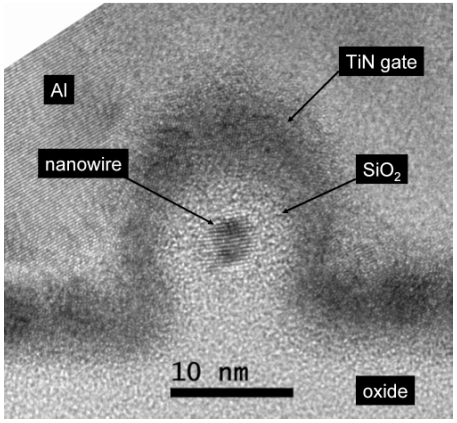


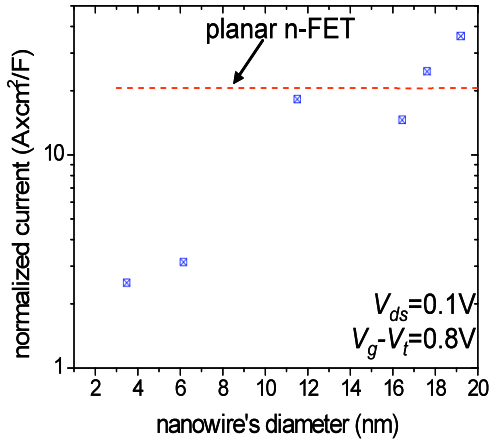
O. Gunawan et al., DRC 2008

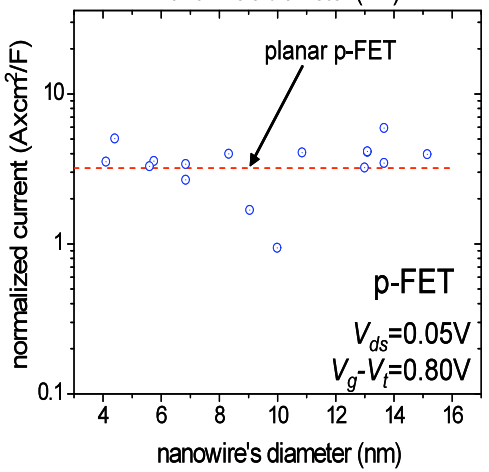
Current scaling with Si Nano-wire dimensions

The Ultimate Si Field Effect Transistor





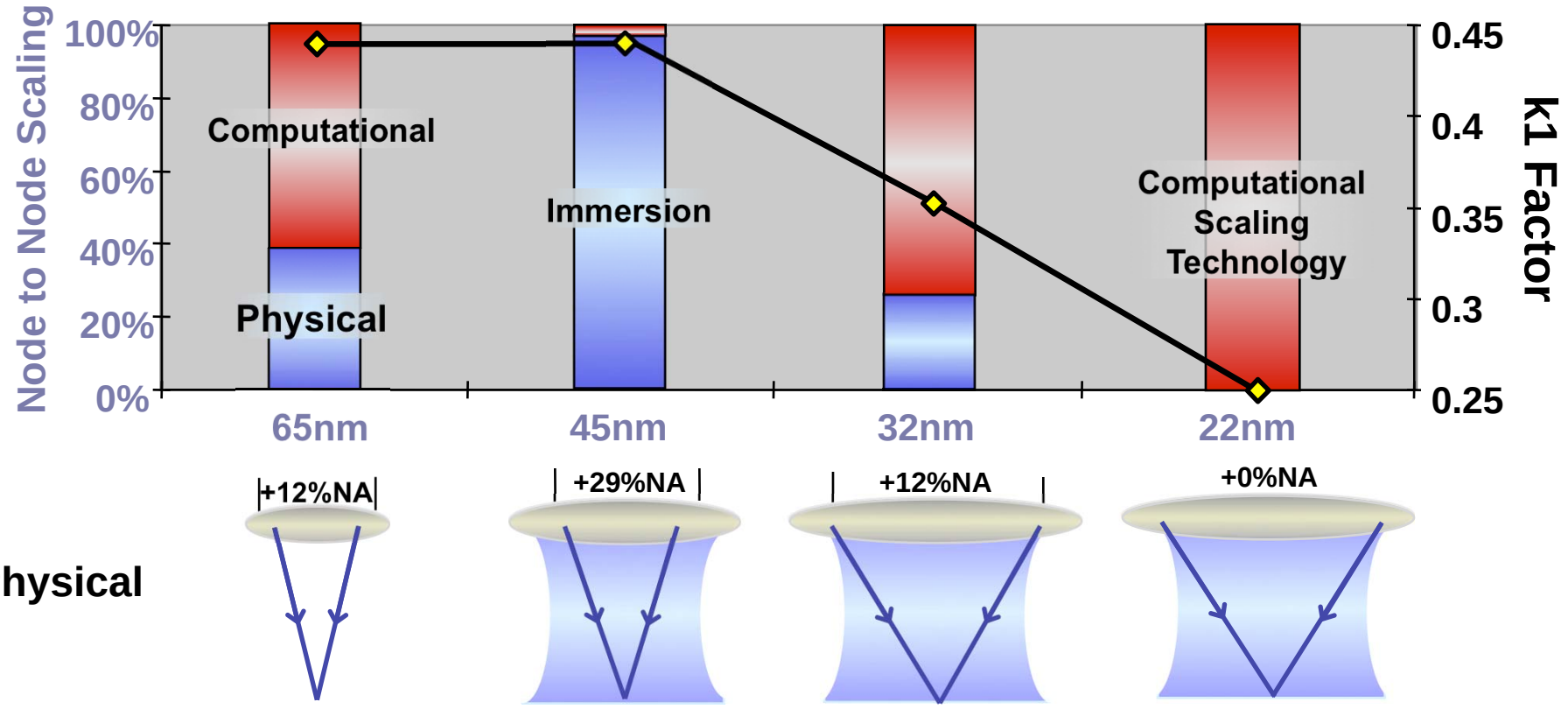




G. Cohen, DRC 2008

Computational and Physical Efforts Keep Litho Scaling Alive

Computational Scaling Technology Required beyond 32nm

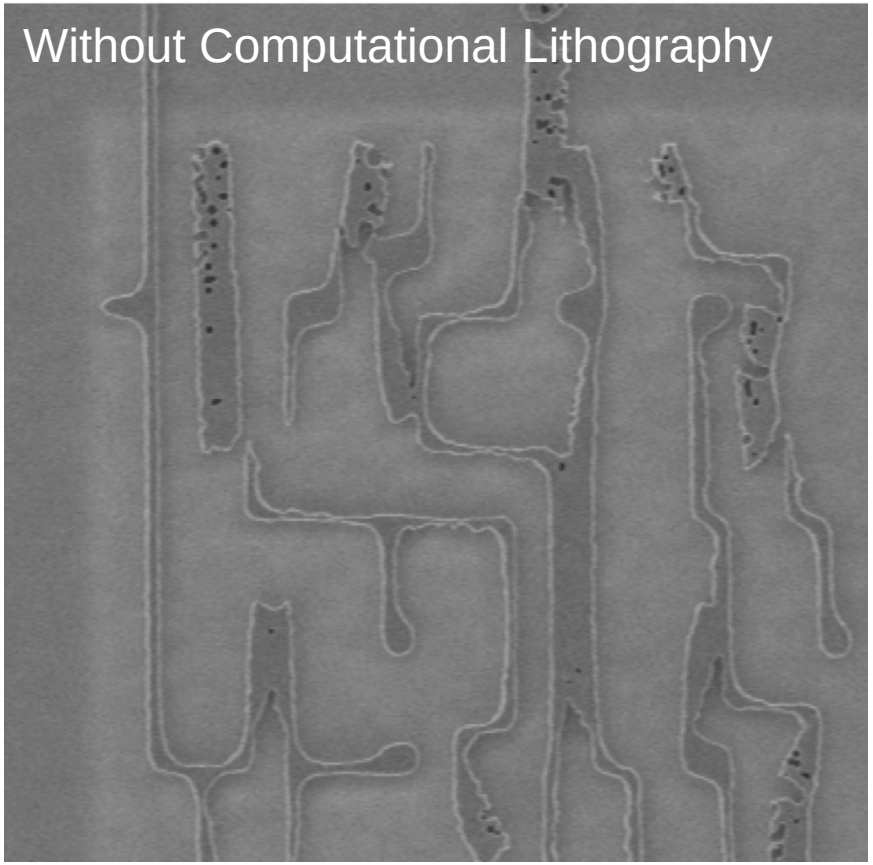


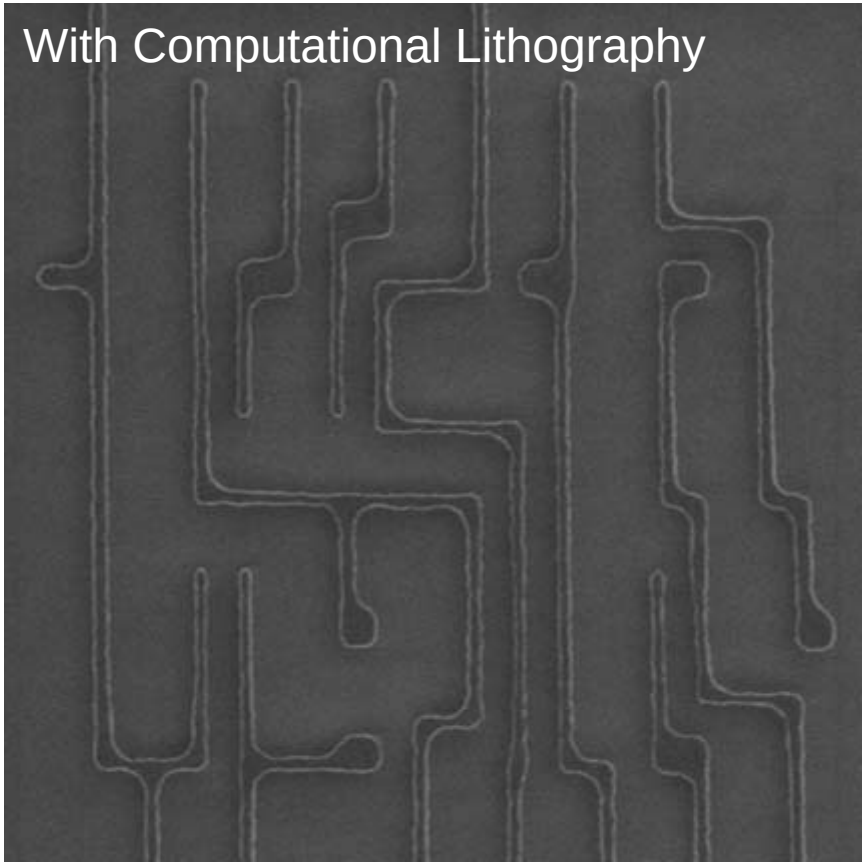
Physical

Computational model-based OPC, frequency doubling RET, SMO, DfM

Why We Do Computational Lithography

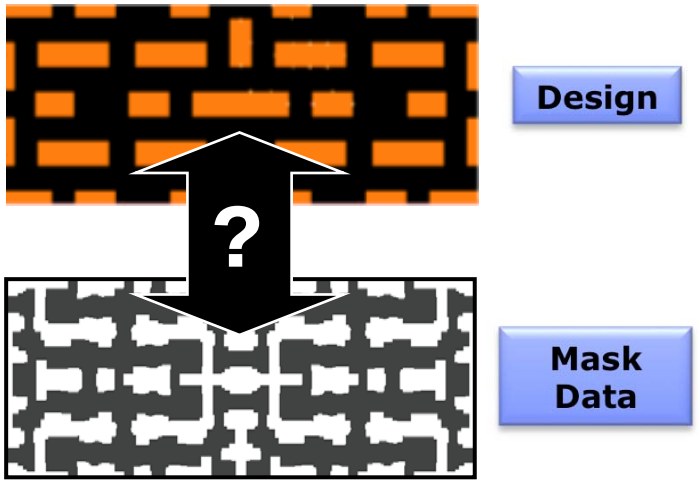
Enabling On-Wafer Pattern Realization

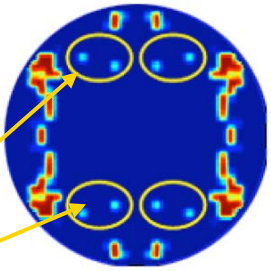




Mask Inspection Challenges for Adv RETs (SMO)

- **Defining a defect is difficult when one-to-one correspondence between mask shape and wafer print is broken**
- **Mask inspection systems (e.g. AIMS) must emulate the complete photolithography process in order to predict the defect impact on wafer**
- **Inspection systems need to support highly complex illuminators & match the exact configuration of the scanner**





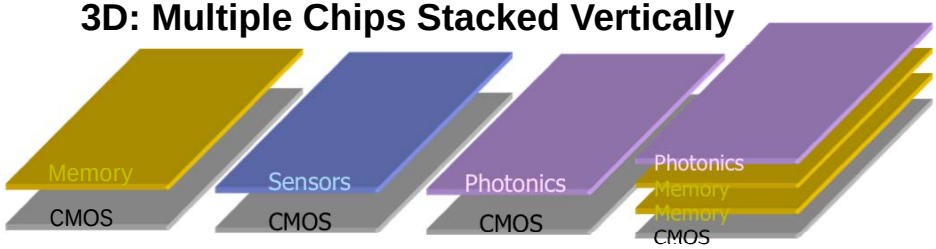
Effect of Missing Isolated Pixels		
	Common PW	CPW DOF
Perfect Source	0.32	70nm
Removed Pixels	0.21	63nm

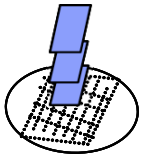
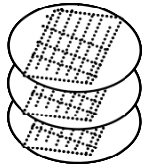
Three Dimensional Integration (3DI)

3D Integration Incorporates Multiple Chips Into a Single Package

- **3D Technology integration is a family of technologies enabling vertical stacking of semiconductor chips and other components**
- **It is the next revolution in Semiconductor technology roadmap and is fundamental to staying on the path of performance improvement**
- **Compared to conventional 2D 3D integration can provide:**
  - Massive bandwidth
  - Much higher capacity
  - Variety of chips (& functions) in a single stack
    - → More functionality in a smaller size
  - Power reduction and better performance

3D: Multiple Chips Stacked Vertically

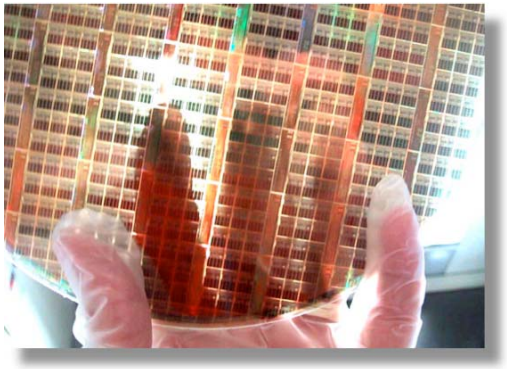


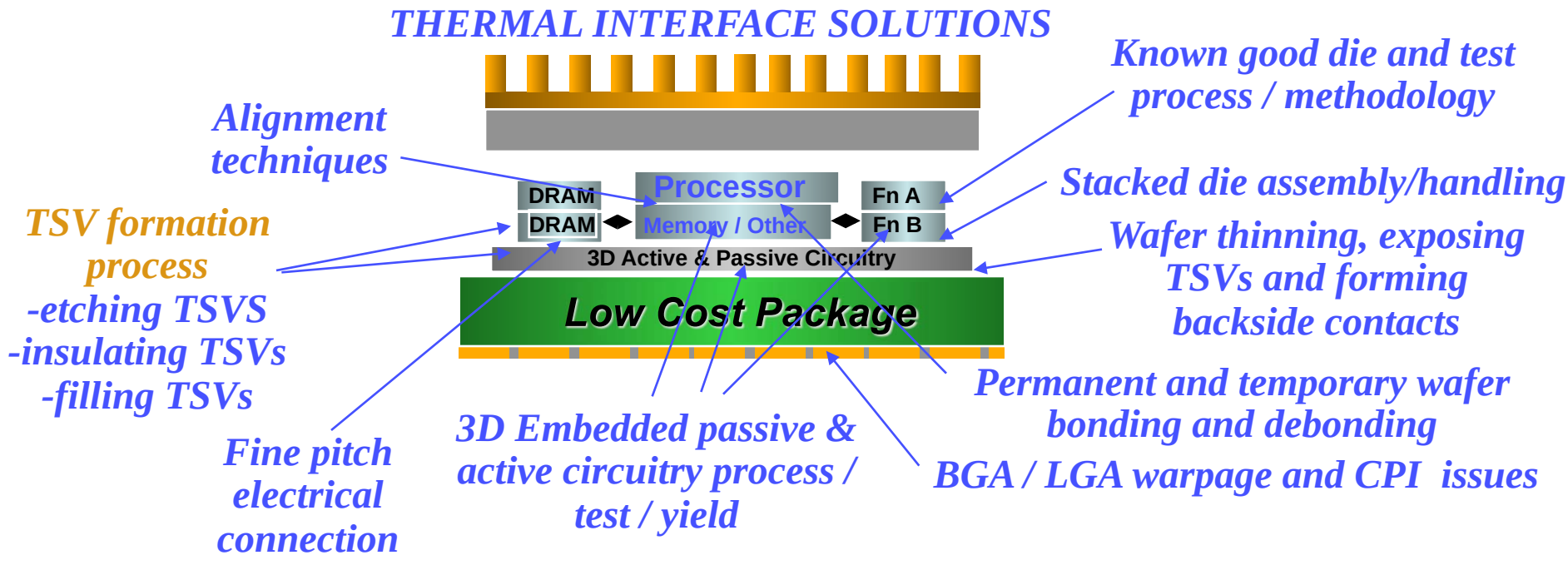
	Chip to Chip	Chip to Wafer	Wafer to wafer
			
Pro	Flexible, use of KGD	Flexible, use of KGD	Low cost
Con	Handling and bonding	Handling and bonding	Overall yield, chip size
Wafer thickness	< 4 µm to > 150 µm	< 4 µm to > 150 µm	< 4 µm to > 150 µm
Bonding technology	Solder Metal to Metal Adhesive	Solder Metal to Metal Adhesive	Solder or Metal Oxide bonding Adhesive

The integration of 3D technology will enable performance, form factor, power savings, and cost requirements of the next generation of electronic devices

The 3D/TSV Solution – Fundamental Technologies

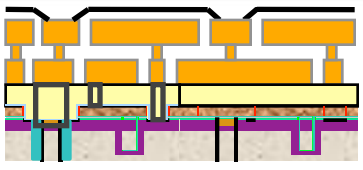
- Enabling the product roadmap requires a suite of technologies
- Each technology in the suite presents significant challenge
- In addition to technology, Systems Re-architecture and EDA tool development are required





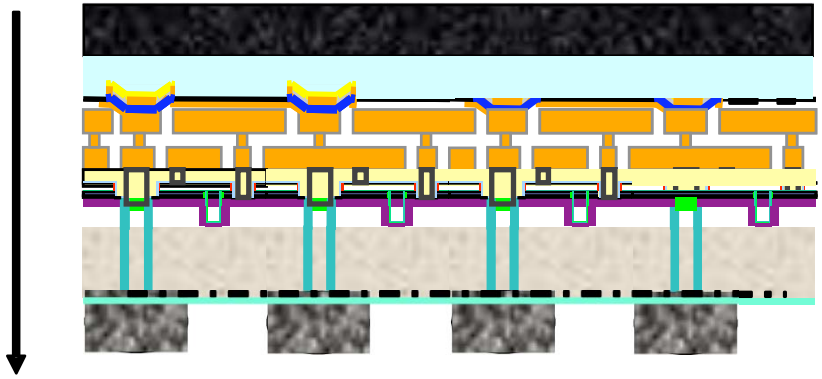
3D Metrology

Wafer Fabrication = TSV, circuits, wiring, etc, …



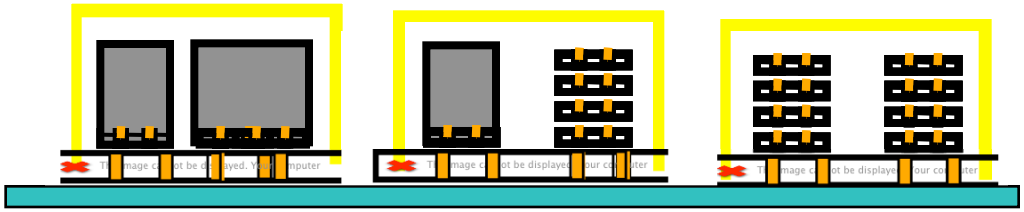
- TSV Diameter, depth, pitch, aspect ratio, density, uniformity
- TSV Interconnection to CMOS FEOL / BEOL level
- TSV Dielectric uniformity, conductor fill, defect free
- Wafer planarity

Wafer Finishing = wafer handle, wafer thinning, back side finishing, bumping



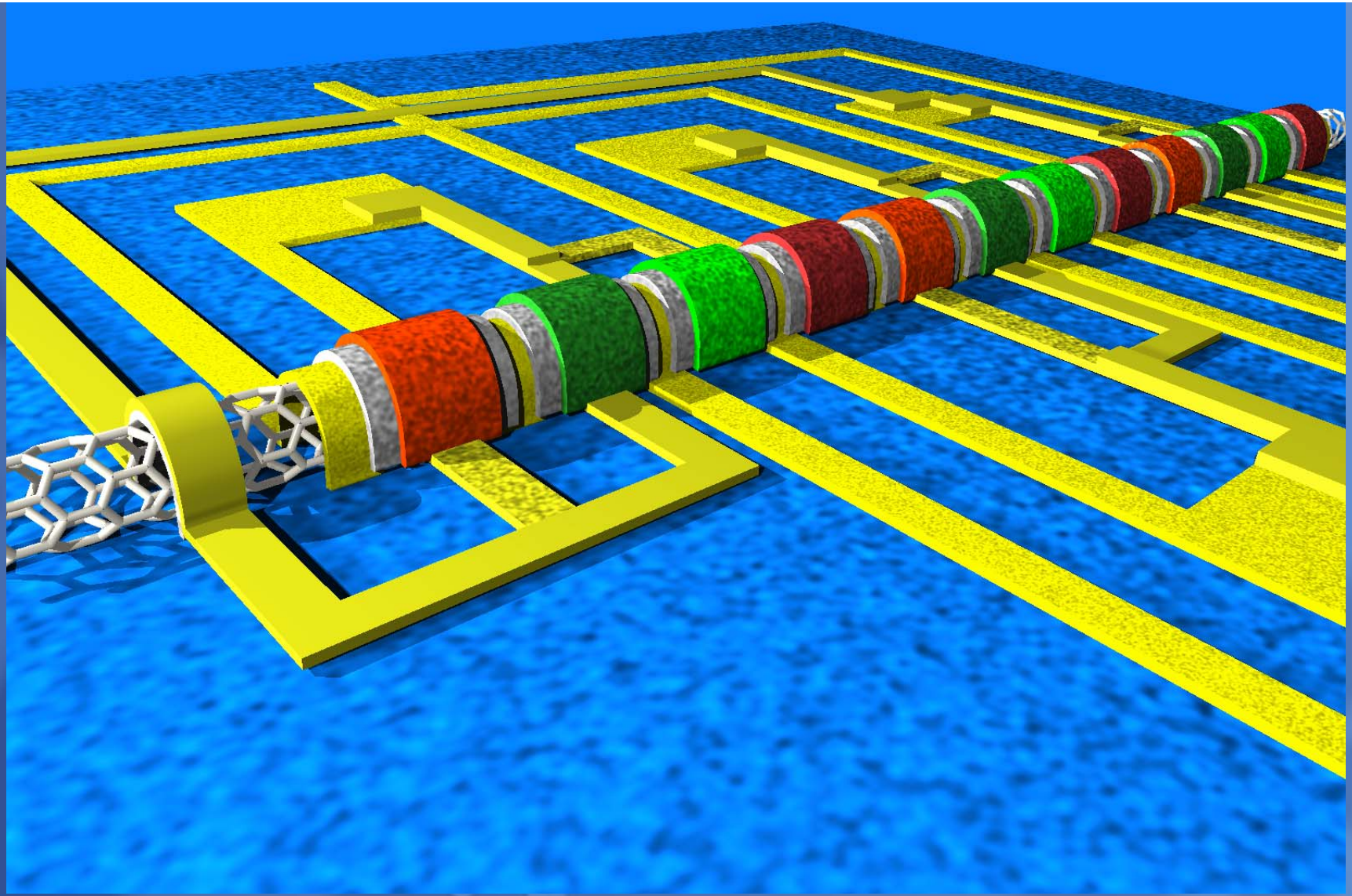
- Mechanical Wafer handle adhesion
- Wafer thinning uniformity, absolute thickness
- Backside wafer finishing
- Wafer bow with handle wafer, free standing
- Bump size, uniformity

Assembly / Integration = Si carrier, die, die stacks, module, TIM, lid, test, SMT board

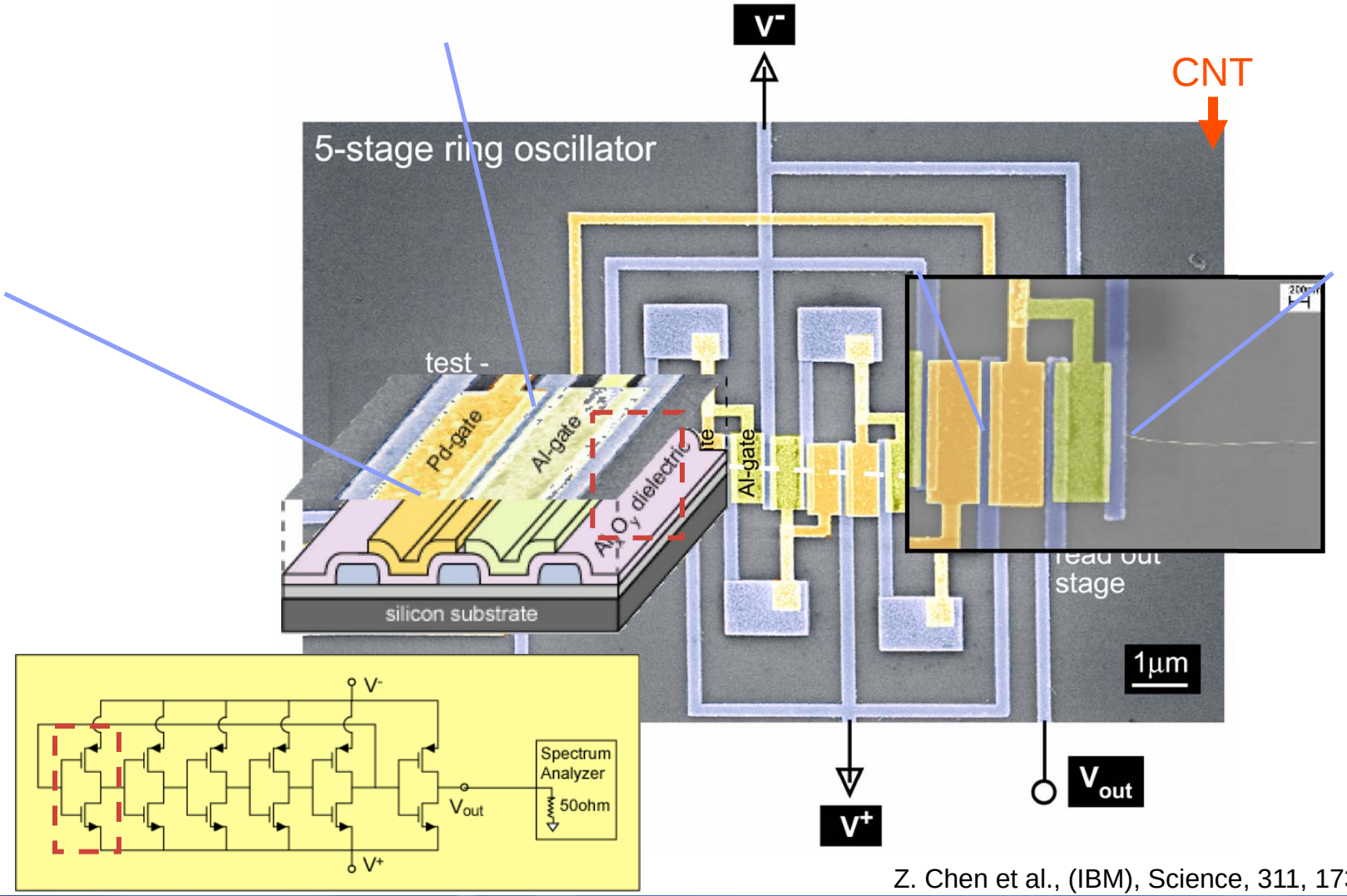


- Wafer test positional accuracy, KGD test
- Stack alignment, electrical contact resistance
- Thermal stack resistance, Electrical stack resistance

CMOS ring oscillator built on a single carbon nanotube



CMOS Ring Oscillator on Individual Carbon Nanotube



Z. Chen et al., (IBM), Science, 311, 1735 (2006).

Conclusions

- **Continued CMOS scaling will require continued Innovation and optimization in materials and device structures**
- **Successful implementation of High-k, Strain Engineering, and Body-controlled Devices will enable device performance enhancement**
- **3D Integration is fundamental to staying on the path of system-level performance improvement for microelectronics industry**
- **Beyond Si at least another Decade of technology innovation is foreseeable**