TECHNOLOGY IN THE INTERNET ERA

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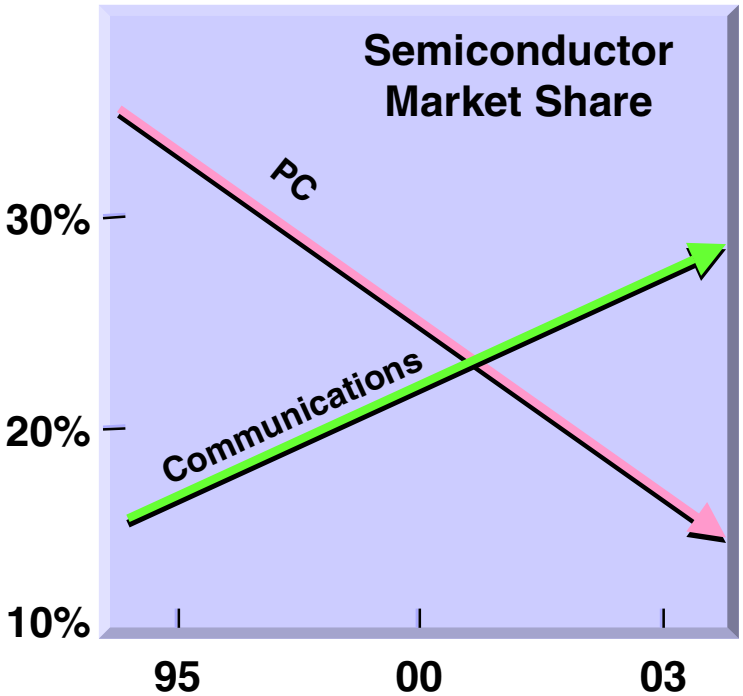
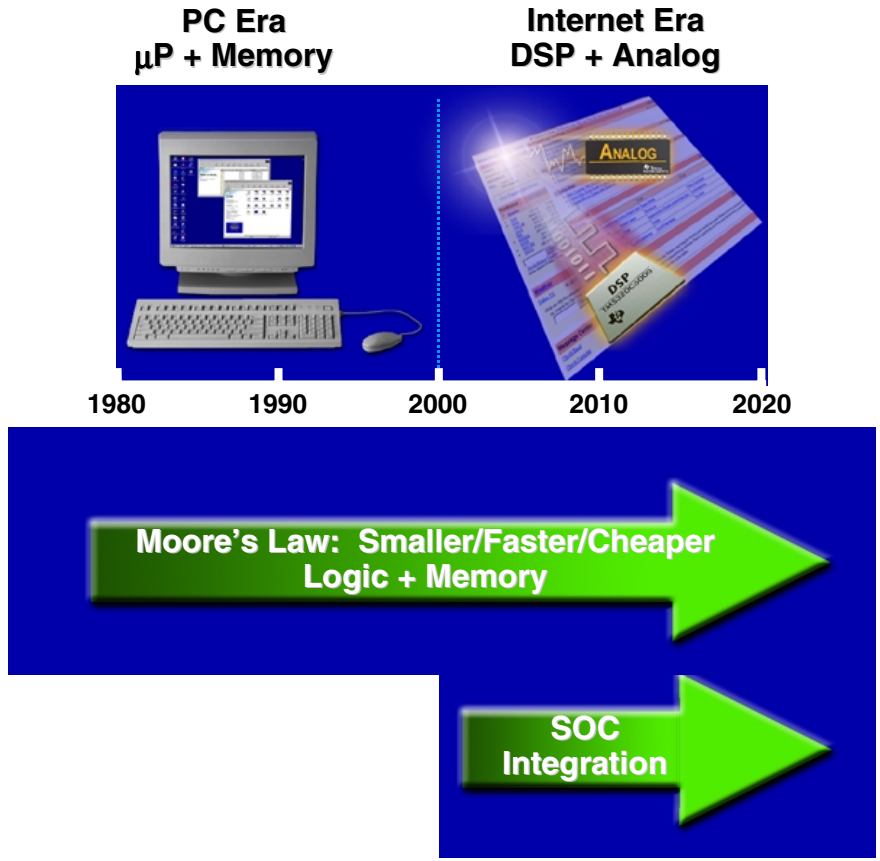
TECHNOLOGY IN THE INTERNET ERA

AGENDA

- Internet Era
- Moore's Law: Grand Challenges
- SOC Integration
- Implications/Predictions

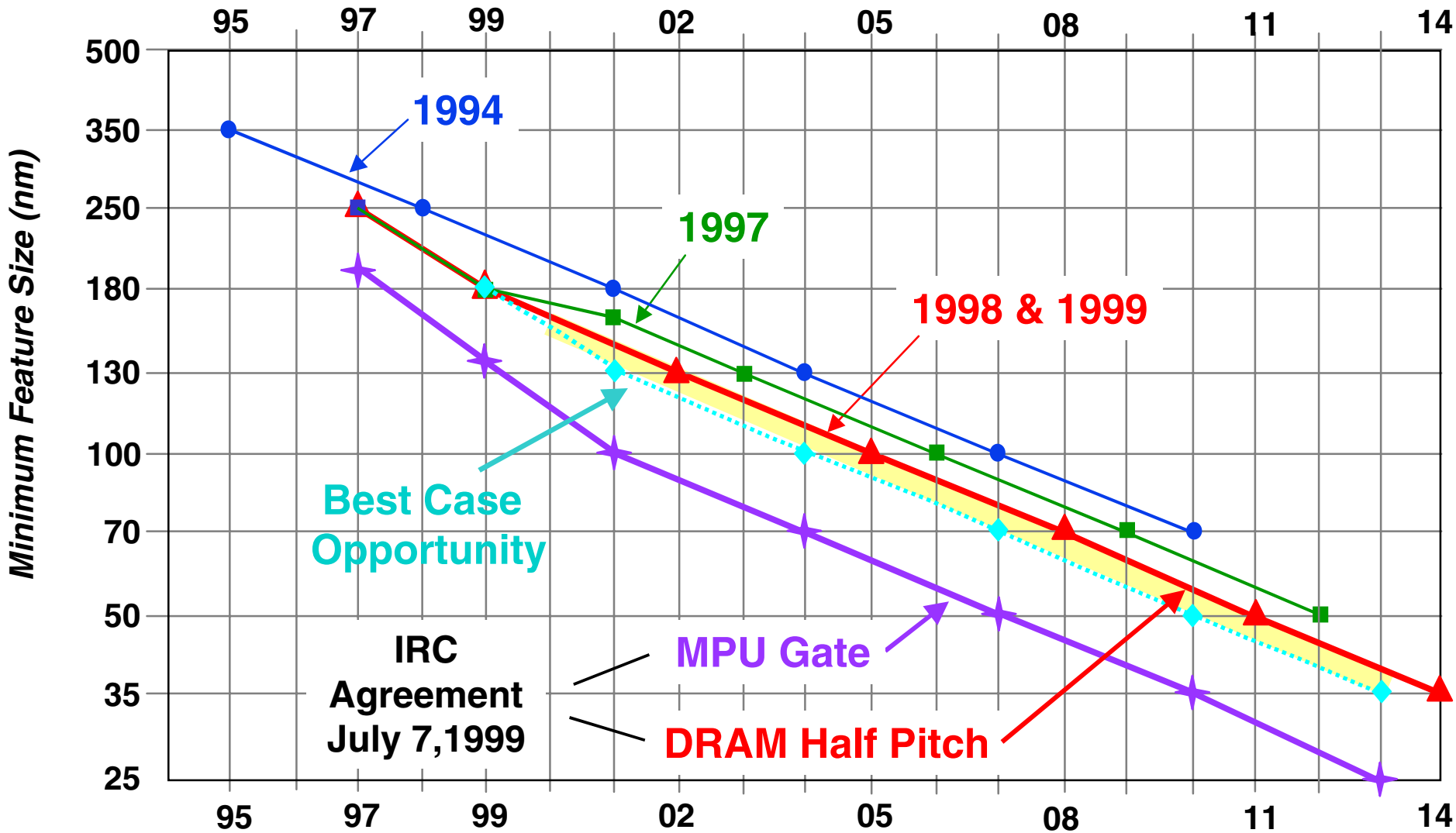
SOC INTEGRATION IN INTERNET ERA
Dawn of Internet Era





Transistor Scaling will continue to be an important Technology Driver in the Internet Era. But it will no longer be the sole driver: SOC Integration will be increasingly important.

CMOS Scaling Roadmap (ITRS'99)



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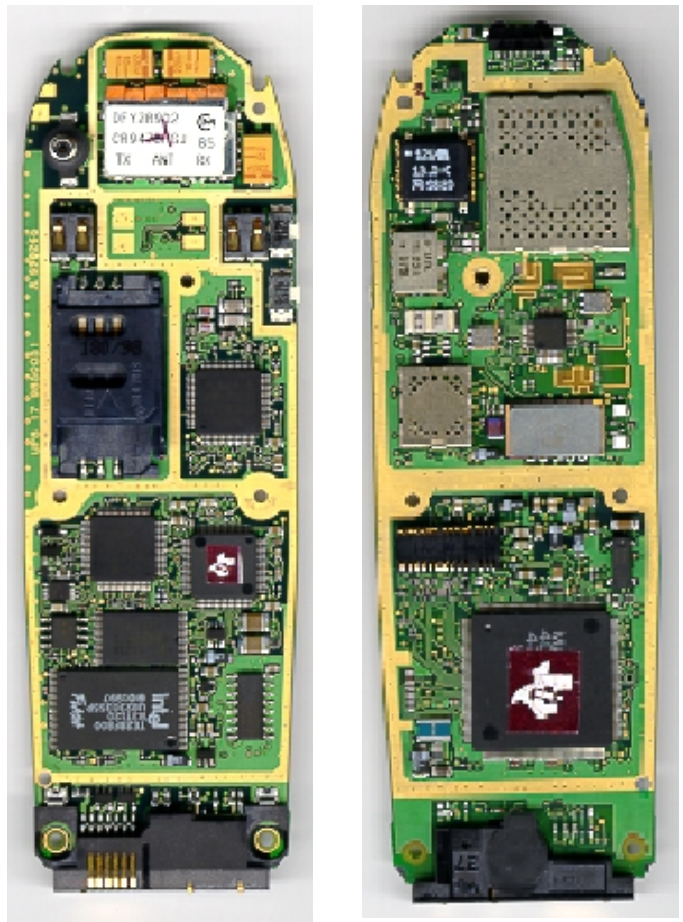
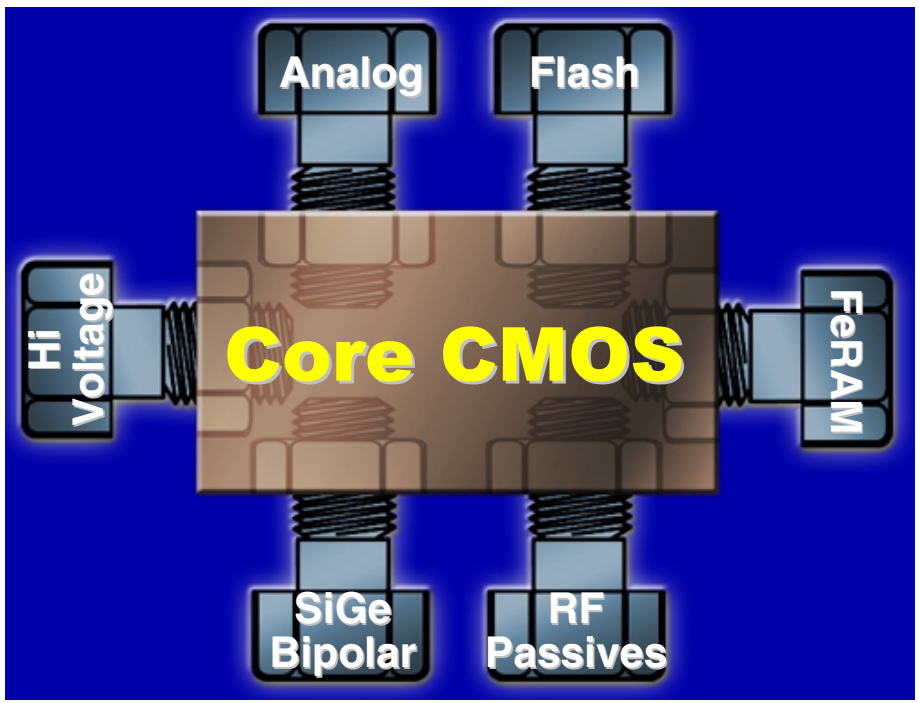
Today's Cell Phone

ICs	12
Discretes	16
Passives	214
Other	8
Total	250



- Transistor scaling is not the most significant enabler for cost reduction
- SOC integration requires technologies for
  - DSP
  - SRAM
  - FLASH
  - Radio RF/IF
  - Analog functions
  - Power management

TECHNOLOGY IN THE INTERNET ERA
Technology Strategy



1) Core CMOS driven by Moore's Law

2) Bolt-on modules driven by needs for SOC Integration

TECHNOLOGY IN THE INTERNET ERA

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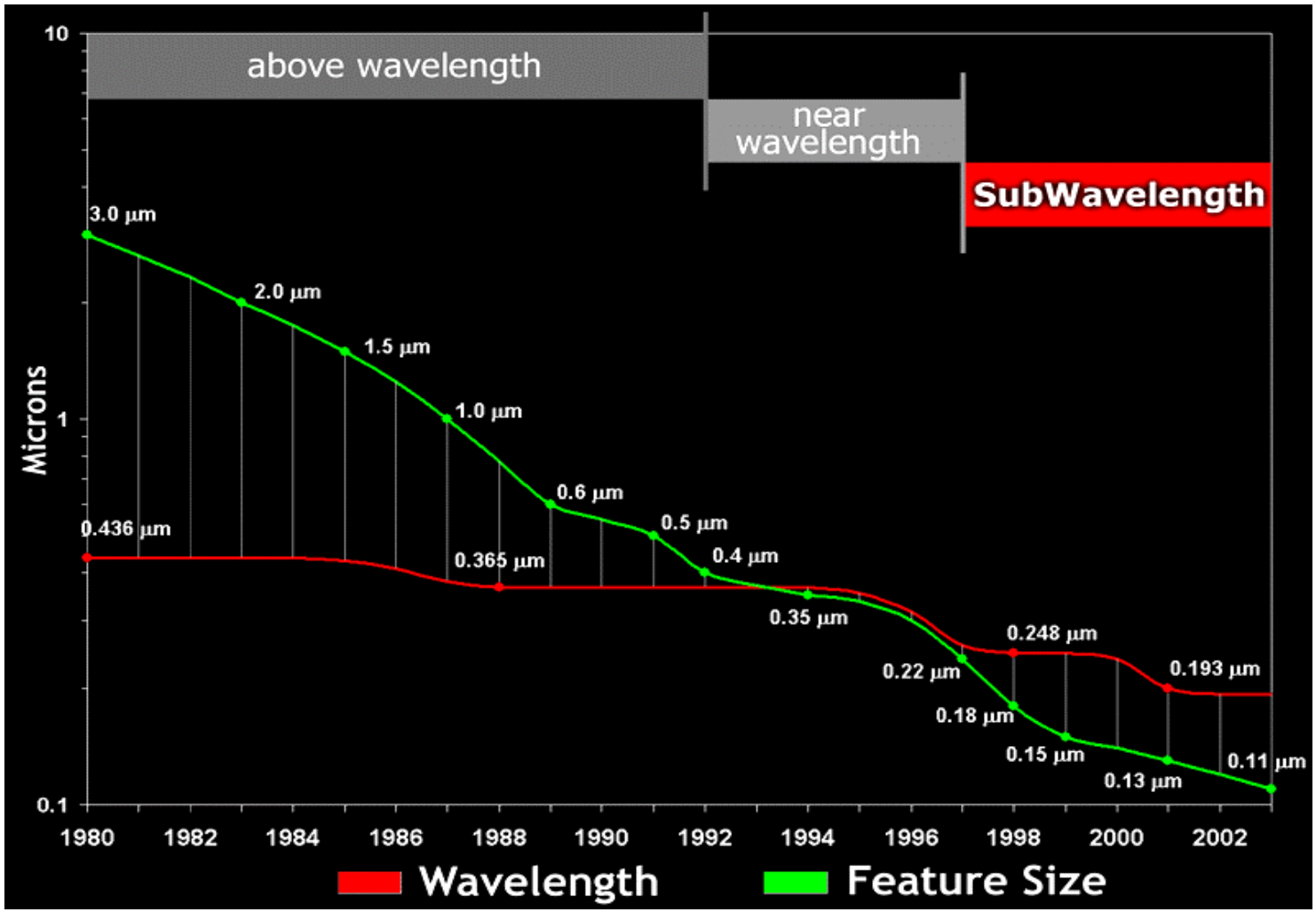
- ⟹ Moore's Law: Grand Challenges
  - Lithography
  - Gate Insulator
  - Static Leakage Reduction
- SOC Integration
- Implications/Predictions

TECHNOLOGY IN THE INTERNET ERA
Lithography



TECHNOLOGY IN THE INTERNET ERA
Lithography

$$R = k_1 \frac{\lambda}{NA}$$

Today $L_{poly} = 100$ nm

$\lambda = 248$ nm

OPC

Optical diffraction and proximity etch effects cause distortion

$$X_{Si}(f) = E(f)\, X_{mask}(f)$$

In OPC, we predistort mask

$$X_{mask}(f) = E_{est}^{-1}(f)\, X_{desired}(f)$$

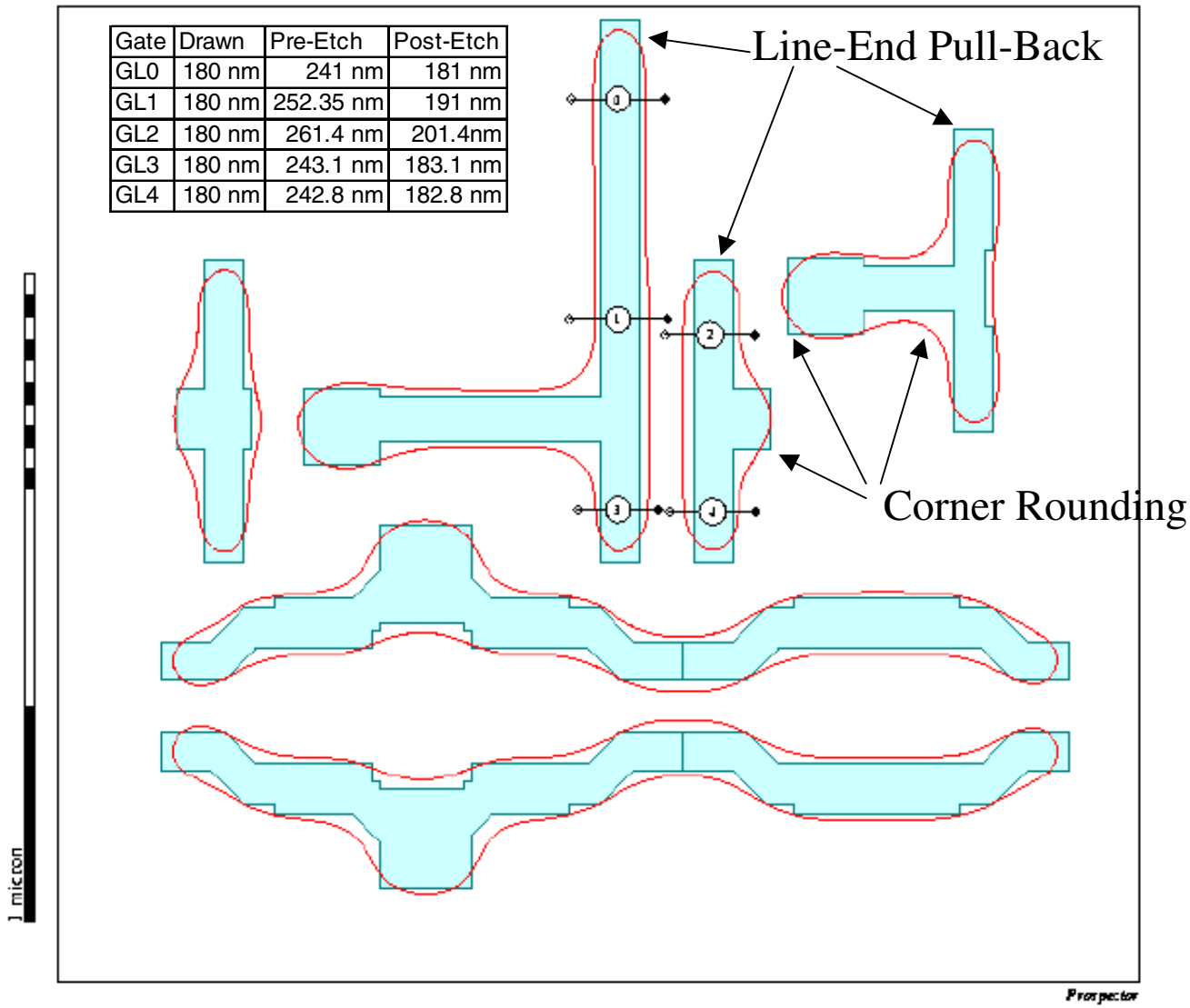
With the result that

$$X_{Si}(f) = E(f)\, E_{est}^{-1}(f)\, X_{desired}(f)$$
$$\approx X_{desired}(f)$$

TECHNOLOGY IN THE INTERNET ERA

Lithography Beyond the Wavelength of Light

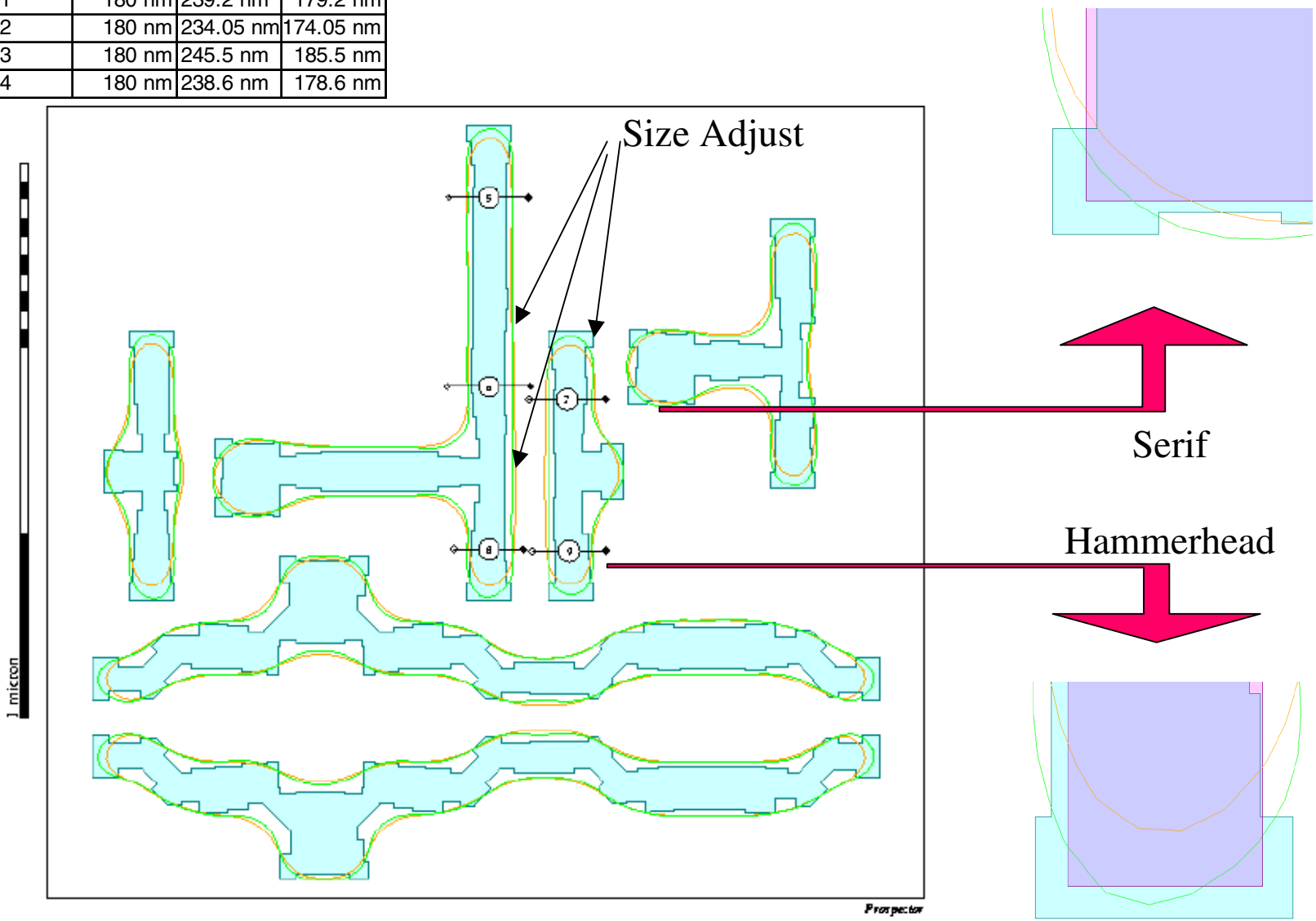
Gate	Drawn	Pre-Etch	Post-Etch
GL0	180 nm	241 nm	181 nm
GL1	180 nm	252.35 nm	191 nm
GL2	180 nm	261.4 nm	201.4nm
GL3	180 nm	243.1 nm	183.1 nm
GL4	180 nm	242.8 nm	182.8 nm



TECHNOLOGY IN THE INTERNET ERA

Lithography Beyond the Wavelength of Light

Gate	Drawn	Pre-Etch	Post-Etch
GL0	180 nm	241 nm	181 nm
GL1	180 nm	239.2 nm	179.2 nm
GL2	180 nm	234.05 nm	174.05 nm
GL3	180 nm	245.5 nm	185.5 nm
GL4	180 nm	238.6 nm	178.6 nm



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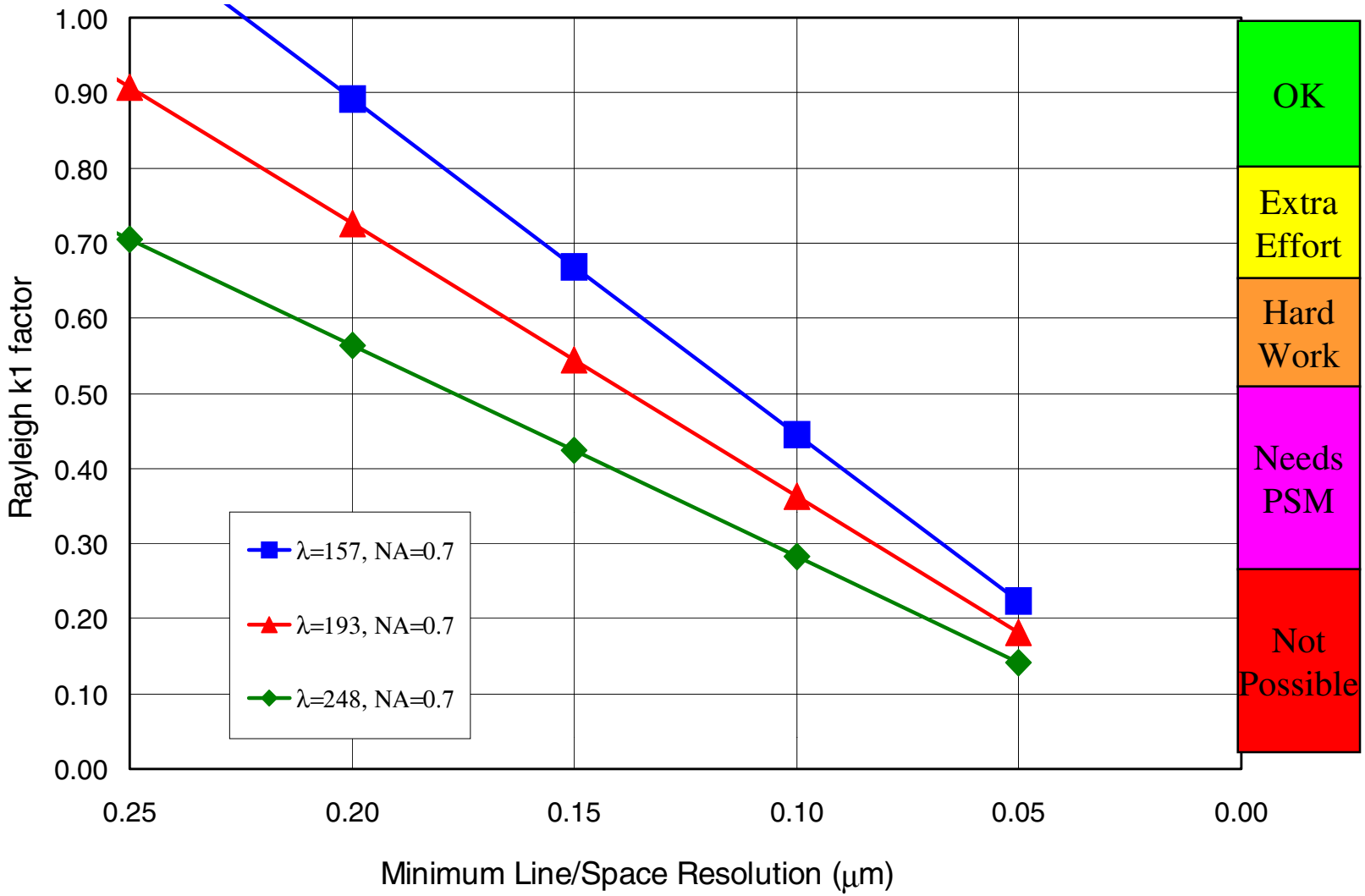
Optical Lithography Challenge



TECHNOLOGY IN THE INTERNET ERA
Lithography

Year	Line/Space	Exposure 2	K_1
1997	250 nm	248 nm	**0.70**
1999	180 nm	248 nm	**0.52**
2001	130 nm	248 nm	**0.37**
2003	100 nm	193 nm	**0.36**
2005	70 nm	157 nm	**0.30**
2007	50 nm	157 nm	**0.22**
2009	35 nm	157 nm	**0.10**

$$R = k_1 \frac{\lambda}{NA}$$

Table assumes NA = 0.7

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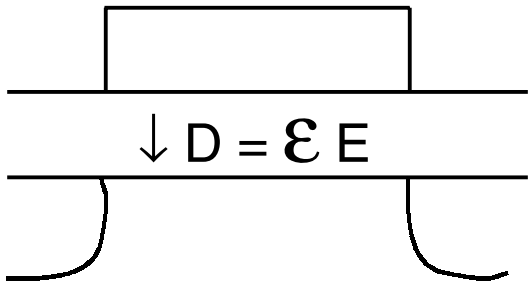
Gate Insulator



Speed ~ I_{drive} / CV
Power ~ CV^2f

- Max charge in channel

  $q = D_{max} - D_{th} = \varepsilon (E_{max} - E_{th})$

- For the past several generations, max charge has been limited by

  $\varepsilon_{SiO_2} = 3.9\ \varepsilon_o$

  $E_{max} = 8$ MV/cm

- Speed power improvements have been achieved by reducing V and maintaining I_{drive} constant
- $E_{max} \approx V/t_{ox}$
- As voltage comes down t_{ox} must come down

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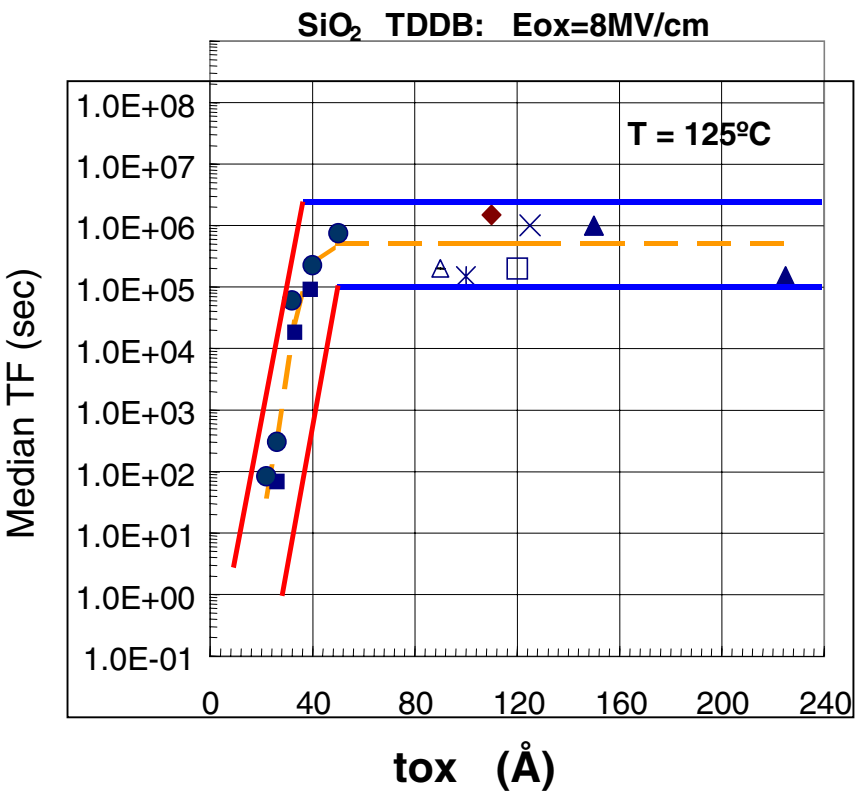
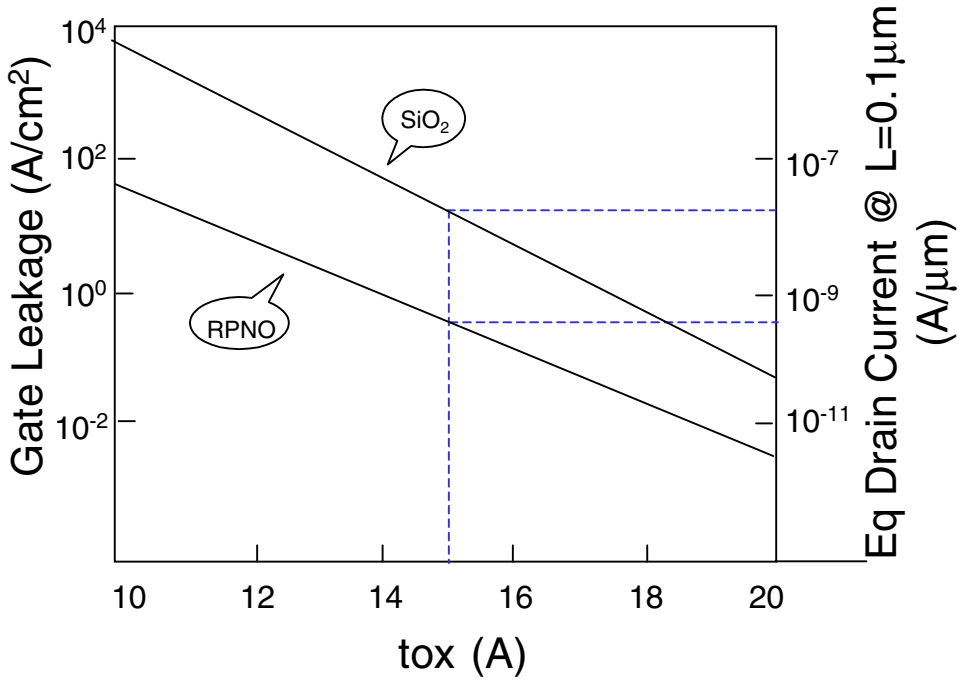
Gate Insulator

Two issues limit how thin we can make SiO_2 gate oxide

Reliability



Gate Tunneling



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Gate Insulator

High k gate insulators have many advantages

$$D \approx k \varepsilon_o V/t_{ins}$$

- t_{ins} can be made thicker while maintaining constant D $\Rightarrow$ I_{drive}. Thereby
  - Reducing gate tunneling
  - Improving reliability
- $D - D_{th} = q$ can be increased if k is sufficiently large, thereby increasing I_{drive}

TECHNOLOGY IN THE INTERNET ERA

Gate Insulator

- High-k alternatives
  - Nitrided SiO_2 (k = 4.0)
  - RPNO (k = 4.6)
  - Si_3N_4 (k = 7.5)
  - Zr, Hf Silicate (k = 15)
  - Ta_2O_5
  - TiO_2
  - ZrO_2
  - Y_2O_3
  - $SrTiO_3$
- To qualify as an SiO_2 replacement a high-k insulator must
  - Have reliability comparable to SiO_2
  - Have interface properties as good as SiO_2: comparable mobility

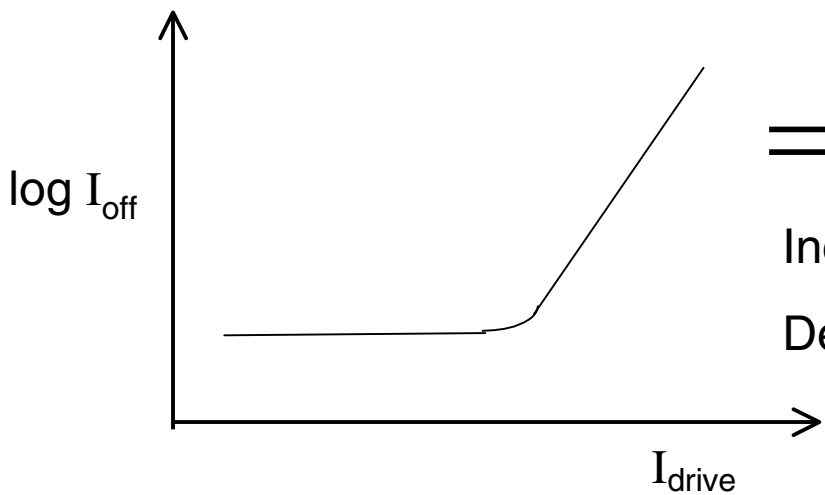
TECHNOLOGY IN THE INTERNET ERA

Static Leakage Current

$$I_{drive} \approx \frac{C_{ox}\, v_{sat}\, (V_{DD} - V_T)}{1 + 2\, v_{sat}\, R_{SD}\, C_{ox}}$$

$$I_{off} \approx A \exp\left[\frac{-qV_T}{mkT}\right]$$

$$I_{drive} \approx \frac{C_{ox}\, v_{sat}}{1 + 2\, v_{sat}\, R_{SD}\, C_{ox}} \frac{mkT}{q} \left(\log_e I_{off} + \text{const}\right)$$



$\Rightarrow$

Increasing C_{ox} & v_{sat}

Decreasing R_{SD} & m

TECHNOLOGY IN THE INTERNET ERA
Static Leakage Current

Transistor Leakage Current	Chip Static Power
10 pA/μm	5 μW
100 pA/μm	50 μW
1 nA/μm	500 μW
10 nA/μm	5 mW
100 nA/μm	50 mW

Assume W ≈ 0.5 μm

V_{DD} = 1V

1M gates

TECHNOLOGY IN THE INTERNET ERA
Static Leakage Current

- Gate tunneling current is becoming comparable to sub-threshold off leakage.
- High performance demands higher leakage
  - Low V_t => increased sub-threshold leakage
  - Thinner oxide => increased gate tunneling current
- Radically new design techniques will be required that will reduce chip level leakage.
- Technology for hand-held products will continue to diverge from technology for desk-top products.

TECHNOLOGY IN THE INTERNET ERA

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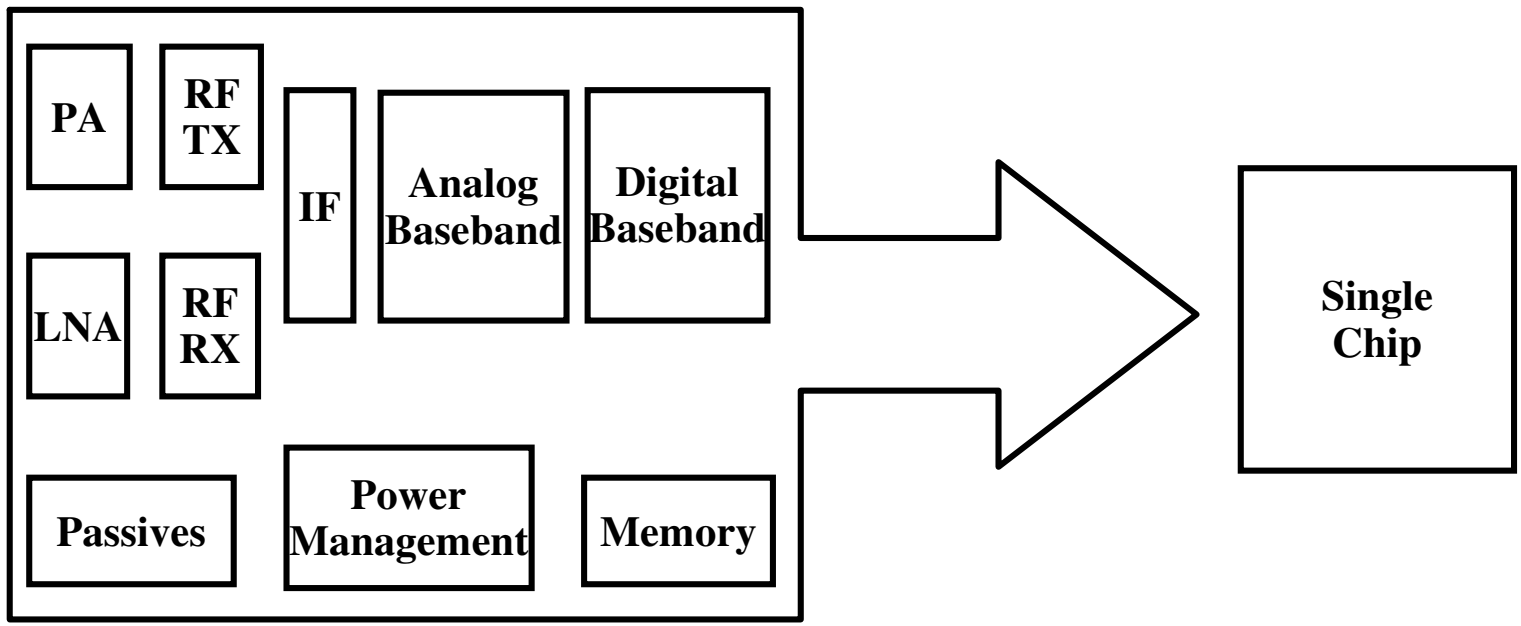
    - Static Leakage Reduction
- ⟹ SOC Integration
- Implications/Predictions

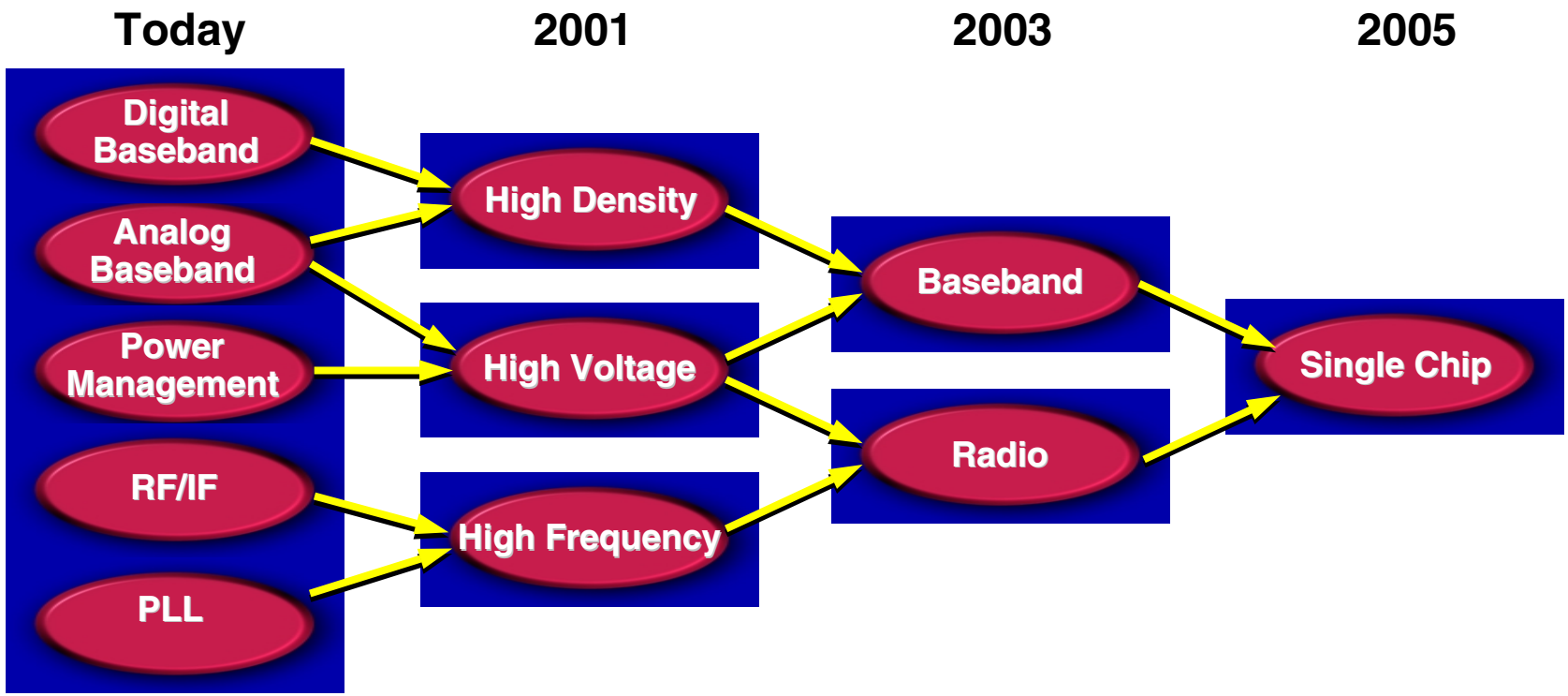
TECHNOLOGY IN THE INTERNET ERA

SOC Integration: Cell Phone



TECHNOLOGY IN THE INTERNET ERA

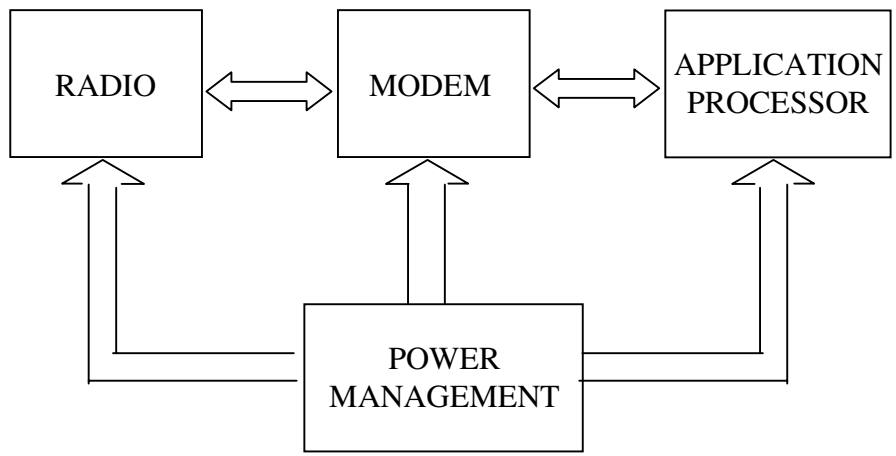
SOC Integration: Cell Phone



TECHNOLOGY IN THE INTERNET ERA

SOC Integration: Internet Products

- Technology Strategy also needs to support SOC Integration strategies for
  - Mass Storage
  - ADSL Modems
  - Short Distance Wireless
  - Cable Modems
  - VoIP/VoDSL
  - Digital Still Camera



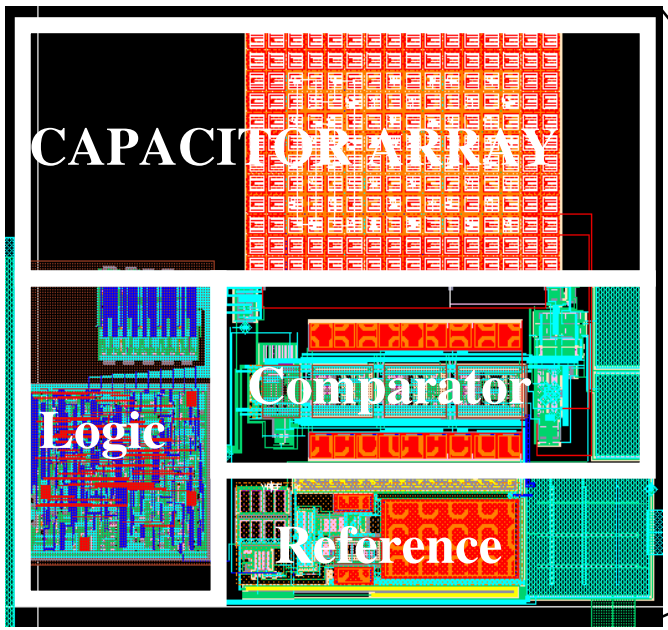
TECHNOLOGY IN THE INTERNET ERA

Technologies Required for SOC Integration

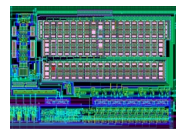
- High performance, high density digital CMOS logic having low active power, and in portable applications, low standby power
- Embedded RAM: SRAM or DRAM
- FLASH EEPROM or non-volatile memory replacement such as FeRAM
- Analog CMOS for Analog Baseband functions
- RF BiCMOS or CMOS for radio or tuner functions
- Extended Drain CMOS capable of withstanding 5-10V voltage surges
- Technologies to enable passive integration: capacitors, inductors, varactors

TECHNOLOGY IN THE INTERNET ERA

Shrinking Analog Functions

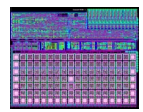


10-bit SAR ADC



0.5 µm
0.52 mm²

54%



0.35 µm
0.28 mm²

0.18µm
0.08 mm²

29%

On average, the area of analog functions shrinks linearly with feature size, eg: 50% reduction in feature size results in 50% shrink in chip area.

TECHNOLOGY IN THE INTERNET ERA

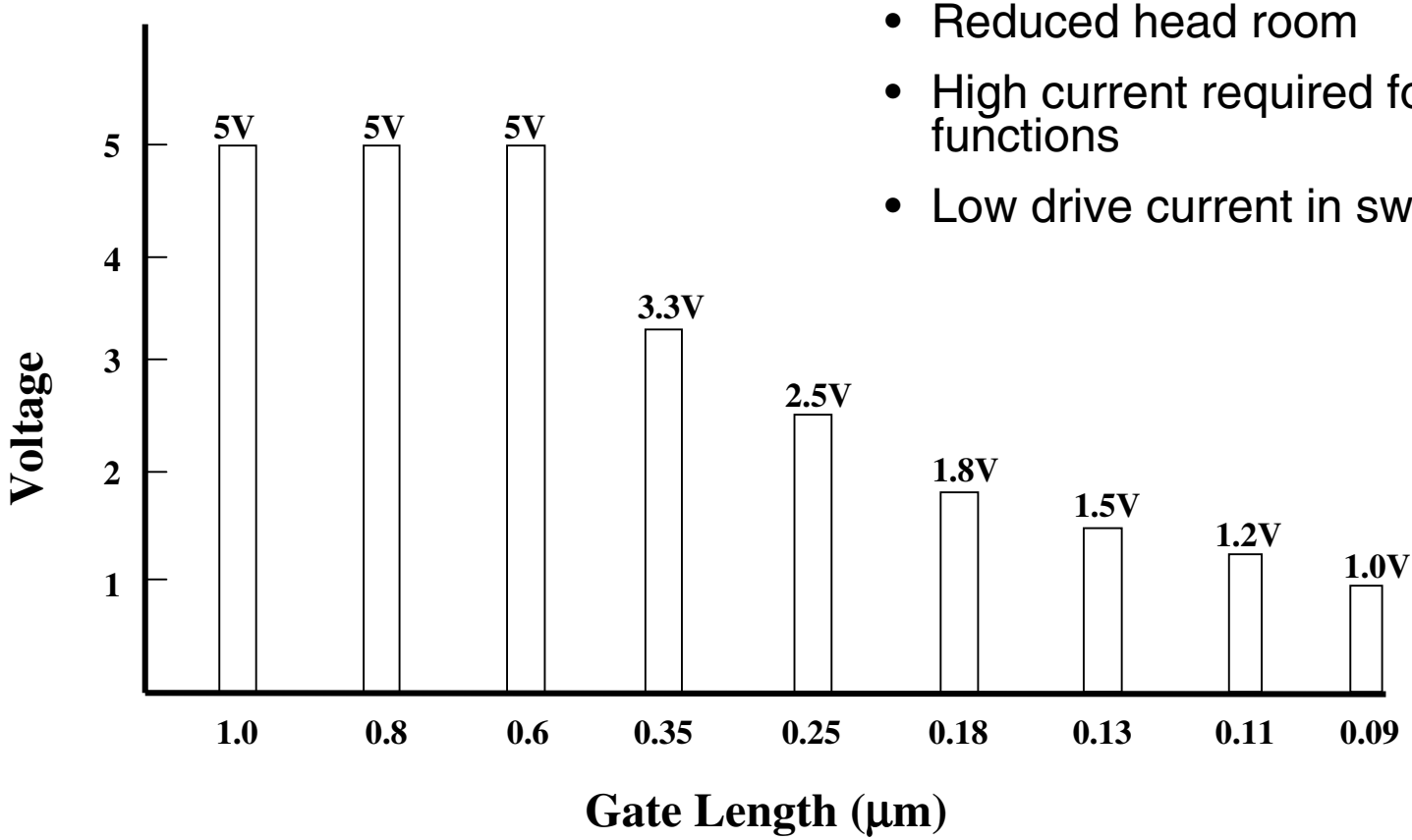
Analog SOC Integration

- SOC integration does not always mean integration of "digital functions" together with analog functions
- Analog functions benefit from shrinking feature size
- New architectures for "analog functions" use extensive digital logic
  - Digital compensation for fractional-N PLLs
  - On channel modulation for phase modulated systems (GSM)
  - Digital error correction in ADCs
  - Digital linearization of amplifiers and tuners

TECHNOLOGY IN THE INTERNET ERA

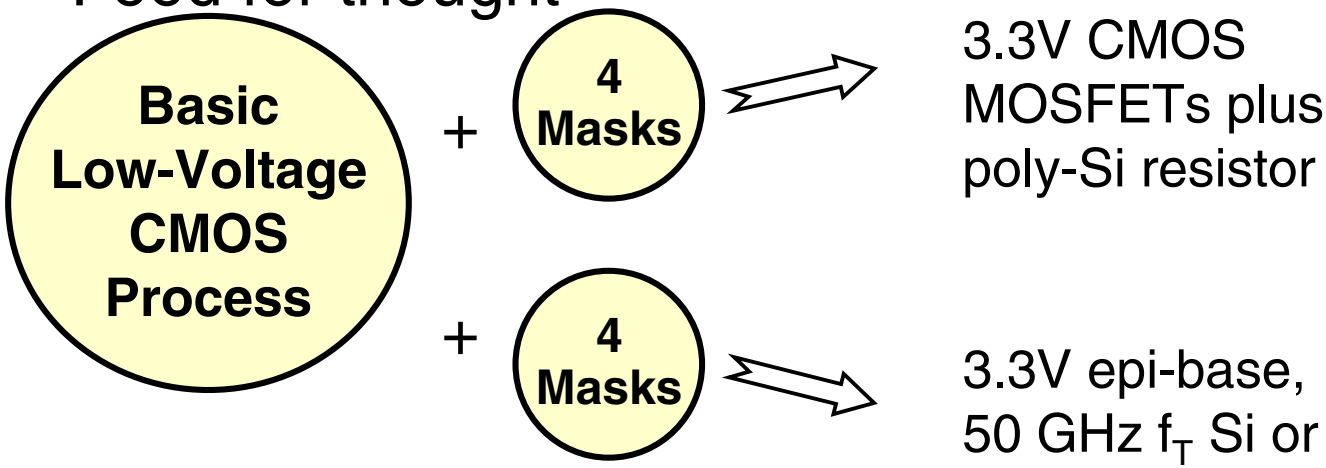
Analog SOC Integration: #1 Problem

- Reduced dynamic range: KT/C noise
- Reduced head room
- High current required for fixed power functions
- Low drive current in switches



TECHNOLOGY IN THE INTERNET ERA
Analog SOC Integration

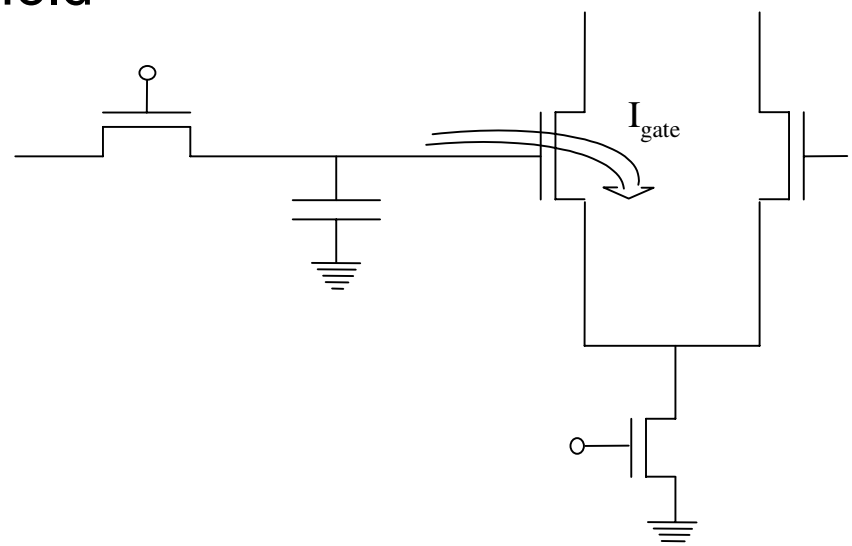
- In some cases, a higher voltage MOSFET is required: 3.3V → 2.5V
- This in general costs three masking steps
- Food for thought



TECHNOLOGY IN THE INTERNET ERA

Gate Tunneling

- At 25 A^{o} physical t_{ox}, gate tunnel current @ 1.5V is 10 pA/μm^2
- Consider a Sample-and-Hold Amplifier (SHA)
  - 1 V max signal
  - 1 pF capacitor
  - Input gate area 200μm^2
- Gate leakage = 2nA
- ΔV = 2mV / msec



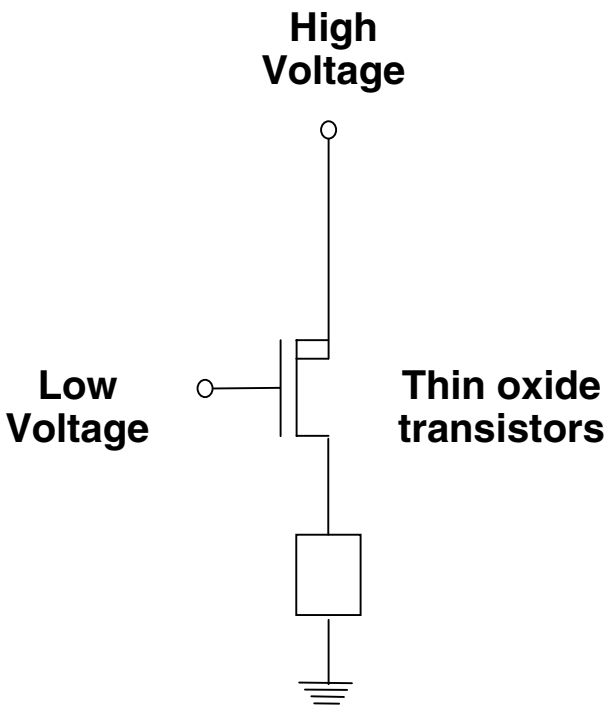
TECHNOLOGY IN THE INTERNET ERA

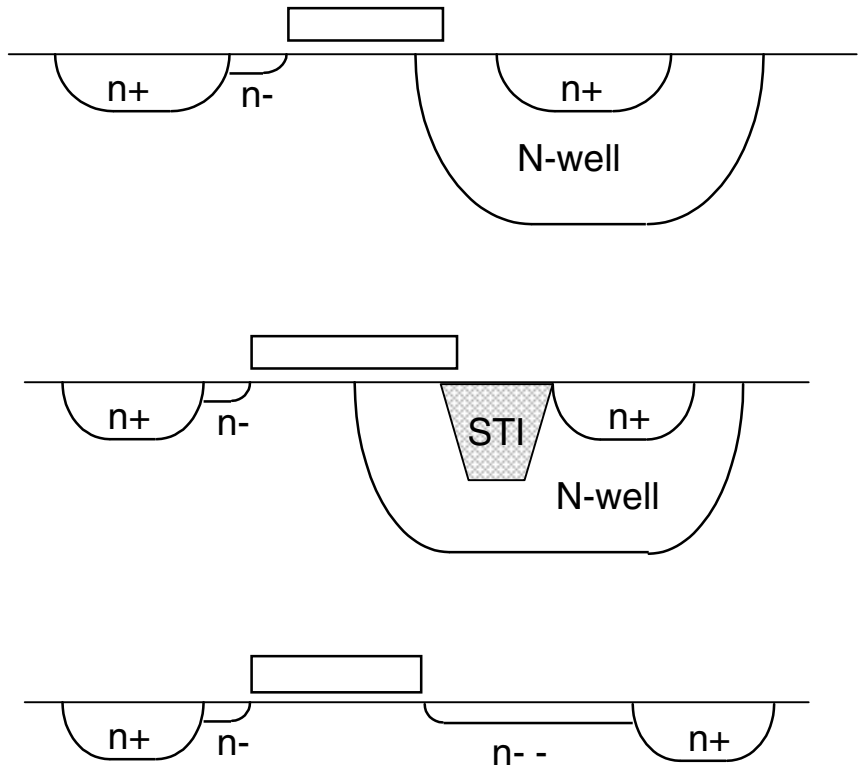
Other Issues

- Flicker noise (1/f Noise) getting progressively worse.
- Channel hot carrier induced substrate current problematic for some analog applications.
- Low V_T required for some analog and rf circuits.
- Feedthrough from digital logic to sensitive analog circuits requiring improved isolation.

TECHNOLOGY IN THE INTERNET ERA

Extended Drain CMOS





Applications

- **Output Drivers**
- **Power Management**

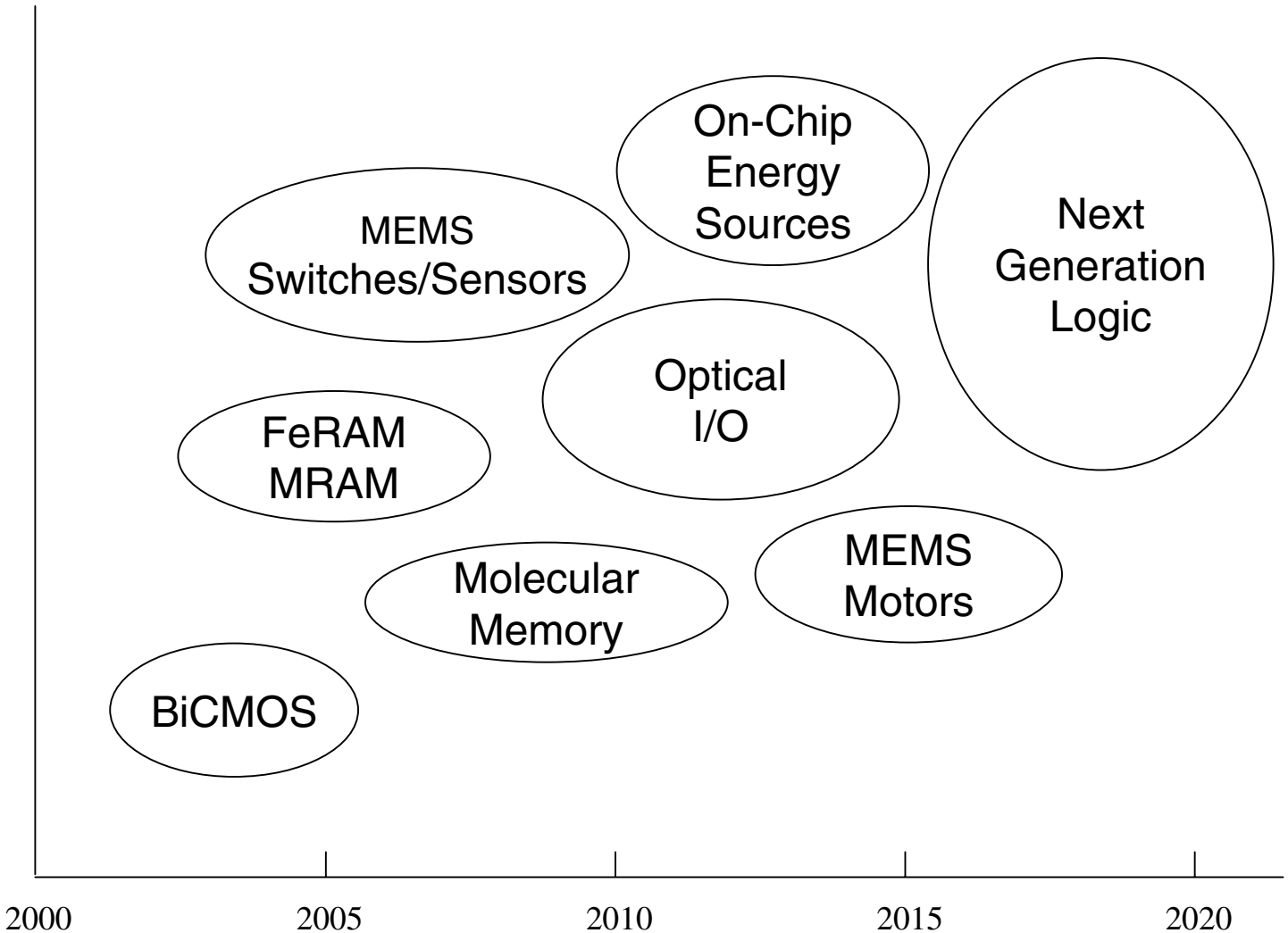
TECHNOLOGY IN THE INTERNET ERA

Passive Components

- Poly-Si resistors
- Metal-to-metal capacitor
- MOSCAP
- Bandgap reference: pnp
- Inductors

TECHNOLOGY IN THE INTERNET ERA

Other SOC Technologies



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    - Lithography
    - Gate Insulator
    - Static Leakage Reduction
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- ⟹ Implications/Predictions

TECHNOLOGY IN THE INTERNET ERA

Implications/Predictions

- The technology challenge becomes greater with each generation
- Si Technology R&D cost is escalating faster than revenue growth. Two reasons
  - The Grand Challenges of Moore's Law shrinking
  - The Challenges of SOC Integration

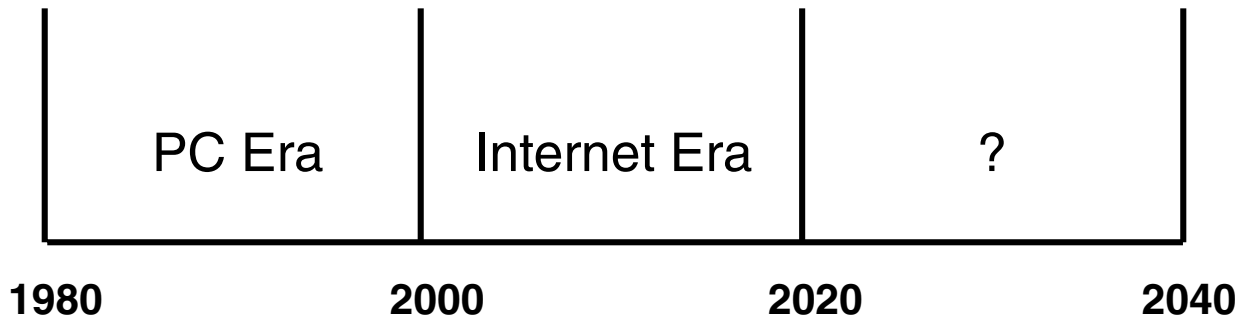
TECHNOLOGY IN THE INTERNET ERA

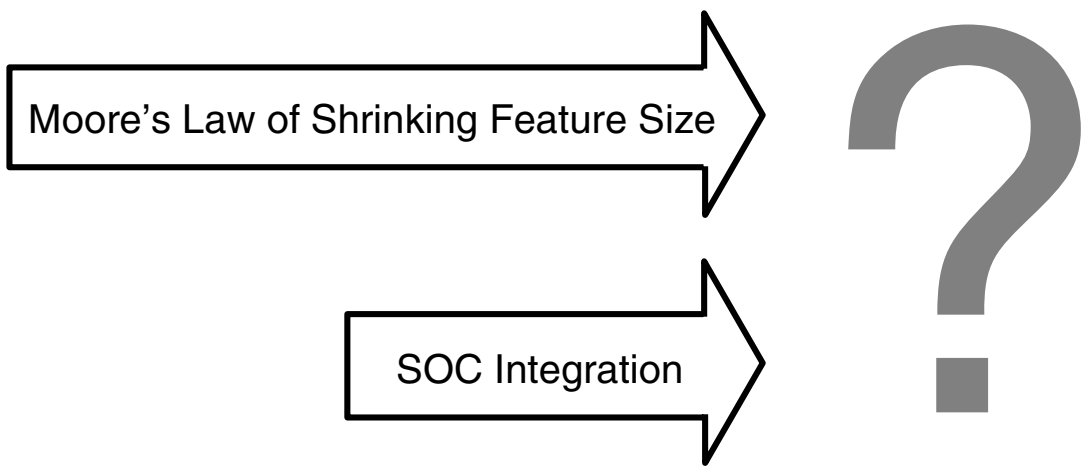
Implications/Predictions

- The high cost of Si Technology R&D will result in
  - Increased use of foundries by small companies
  - Consolidation of deep submicron manufacturing in a few large companies
  - Increased technology development cooperation among manufacturing companies

TECHNOLOGY IN THE INTERNET ERA

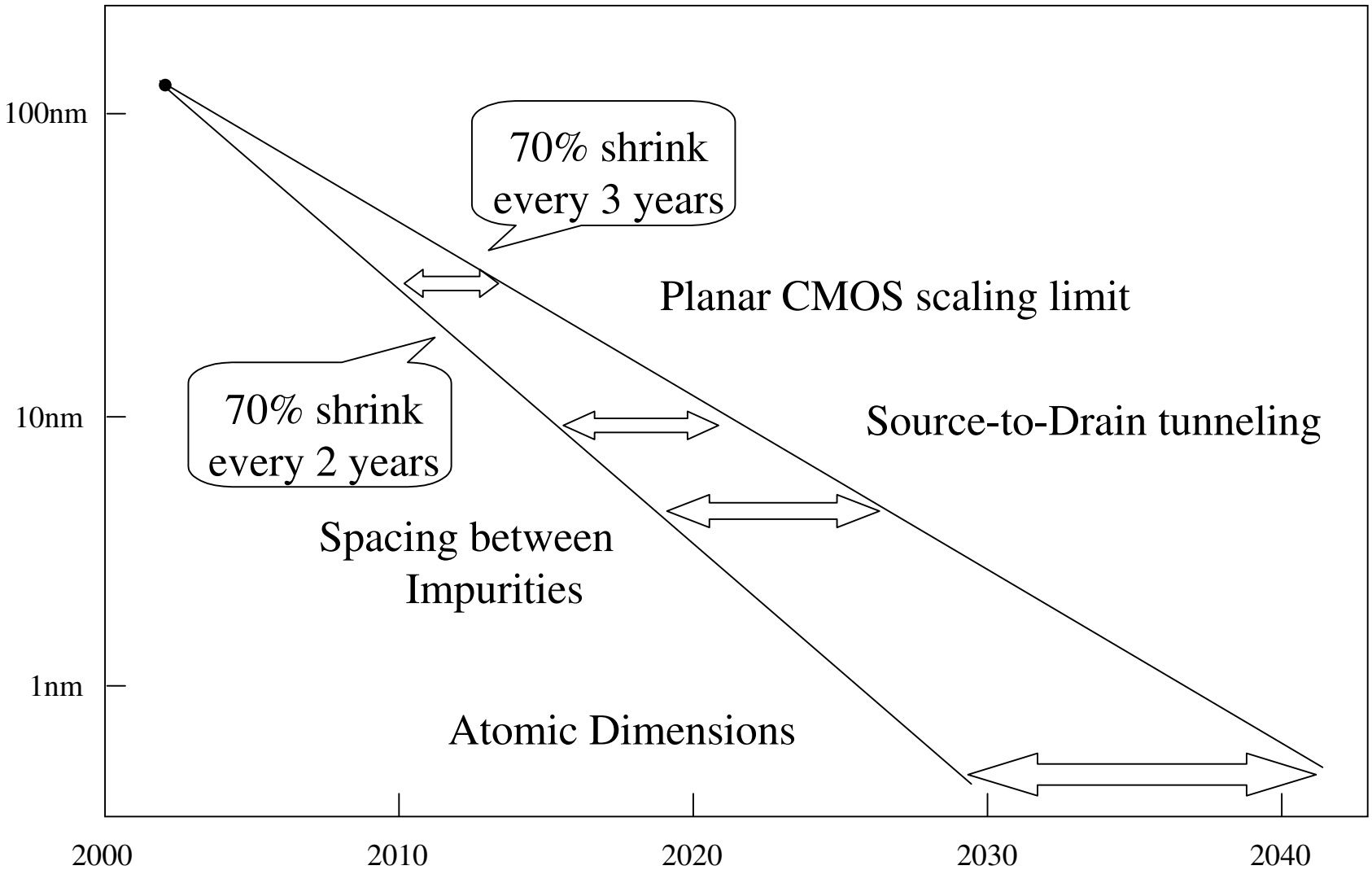
Implications/Predictions





TECHNOLOGY IN THE INTERNET ERA

Implications/Predictions



TECHNOLOGY IN THE INTERNET ERA

Implications/Predictions