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CHALLENGES OF ELECTRICAL MEASUREMENTS OF ADVANCED GATE DIELECTRICS IN METAL-OXIDE-SEMICONDUCTOR DEVICES

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- C-V Measurement Challenges
- EOT Extraction Challenges
- Interface State Density Measurements
- Extrinsic Defect Density
- Reliability Evaluation Challenges
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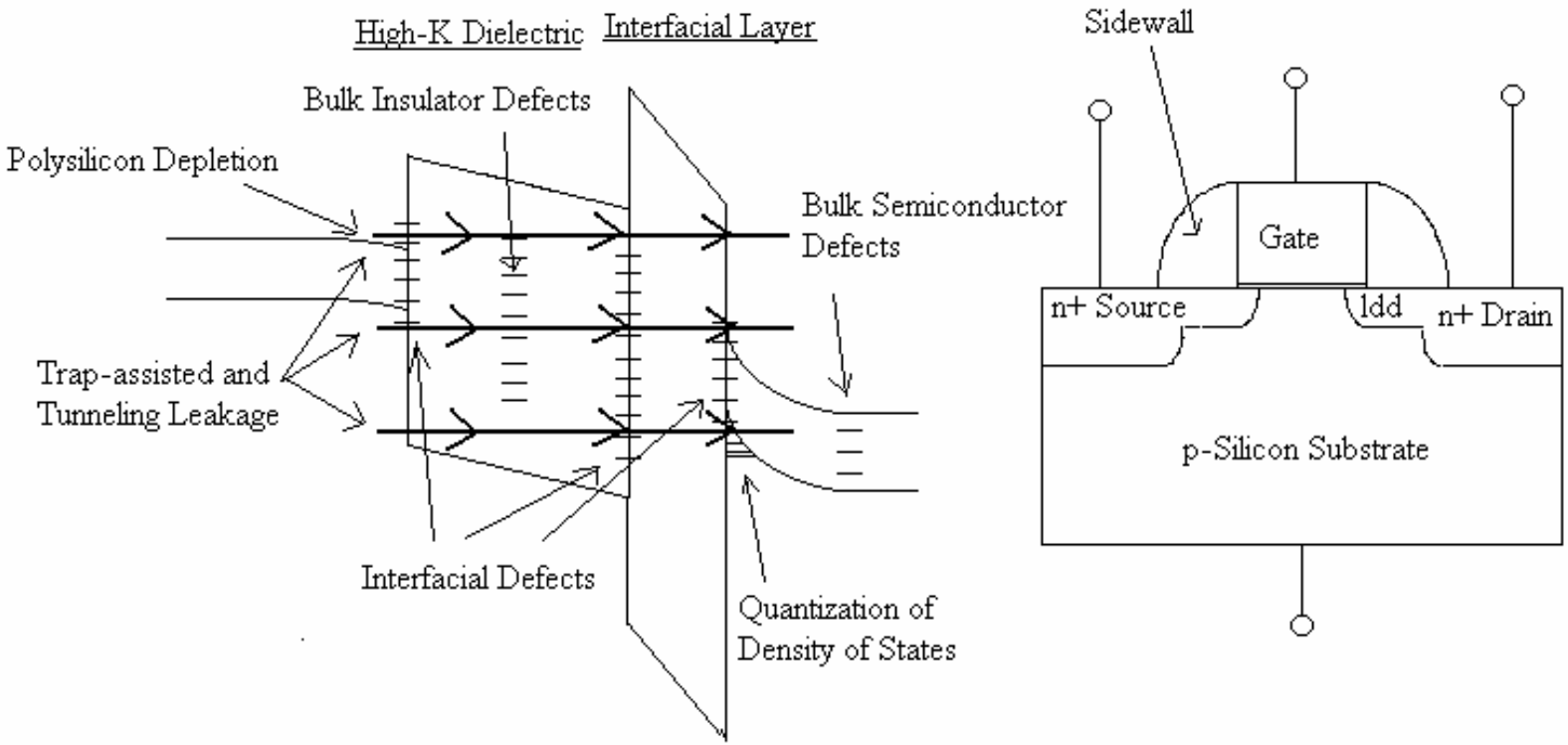
Introduction



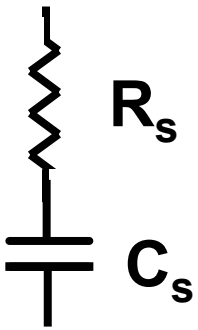
- **Lots of effects and unknowns, only four terminals! (two on capacitors!)**
- **We will need many well-chosen measurements to extract our required parameters.**

C-V Measurement Challenges

A Primer of Capacitive Impedance Measurements

- Capacitance measurements with an LCR meter provide two output parameters, an energy-storage component (L or C) and an energy loss component (R or G).
- These are expressed in terms of either a series or parallel equivalent circuit.

Series Circuit



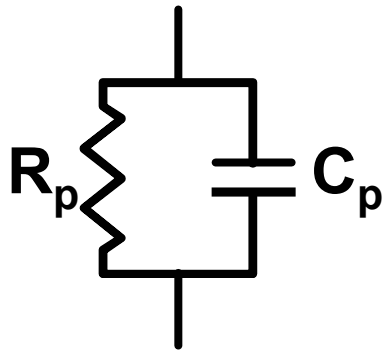
- They are truly equivalent:

$$C_s = C_p * (1 + D^2)$$

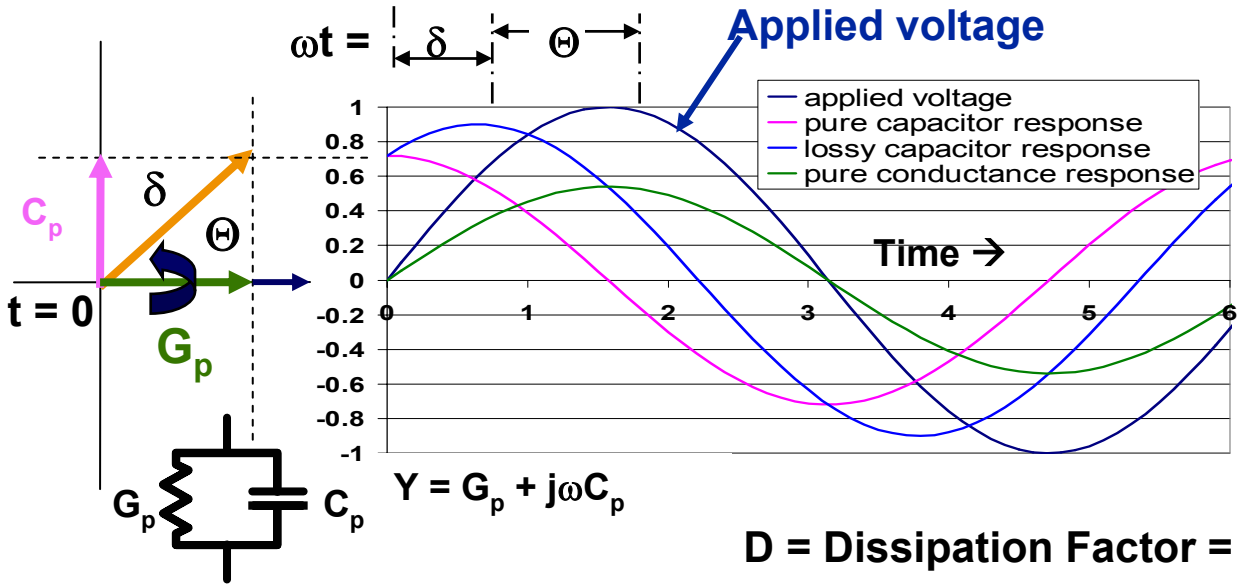
$$D = \omega R_s C_s = 1/\omega R_p C_p = 1/Q$$

- D is called the *Dissipation Factor*
- Q is called the *Quality Factor*
- They express the magnitude and phase of the sample's response to the applied signal.

Parallel Circuit



C-V Measurement Challenges



D = Dissipation Factor = tan δ

- Ideal resistors have a response exactly in phase with the applied voltage (like the green curve).
- Ideal capacitors have a response completely out of phase with the applied voltage (like the pink curve).
- Lossy capacitors, like ultra-thin oxides or some high-k dielectrics, are somewhere in between (like the blue curve).

C-V Measurement Challenges

Measurement Conditions and Errors

- Applied ac voltages should be close to the thermal voltage (25 mV at room temperature) to maintain the small-signal approximation.
- Open and short-circuit (and perhaps calibrated load) zeroing must comprehend test fixture and cabling. Probe station resonance effects may become important at higher frequencies.
- Light and ambient shielding will be important for some measurements.
- Even with great care taken, errors are an inherent part of all measurements.

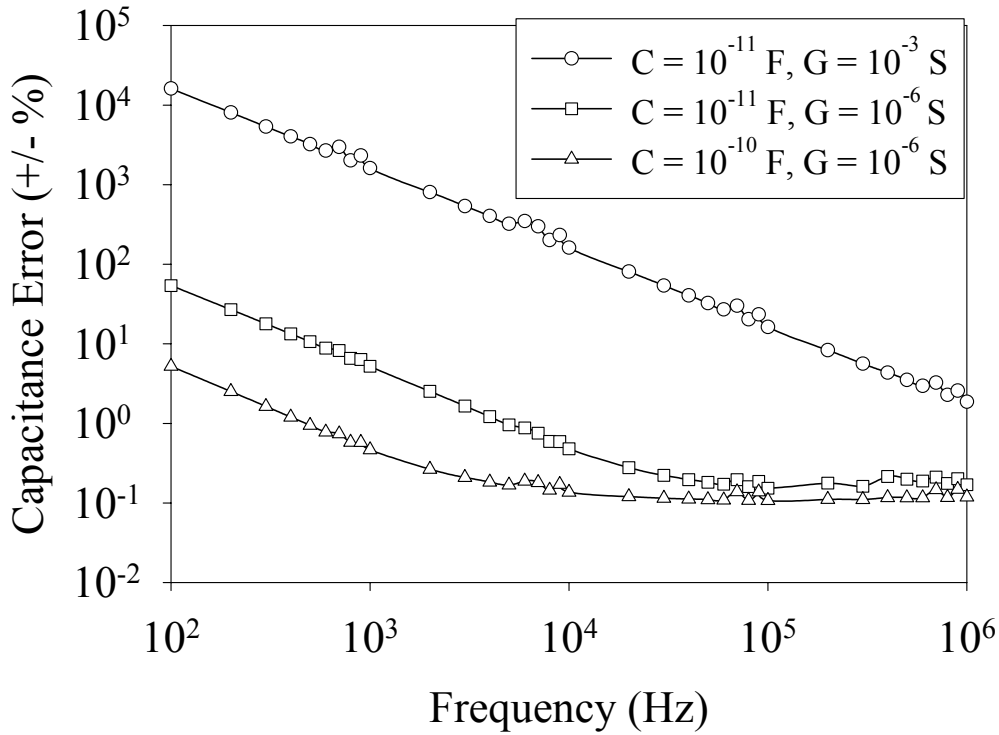
C-V Measurement Challenges

Measurement Conditions and Errors

- A calculation of relative measurement accuracy of the widely used Agilent 4284A LCR meter has been done. It depends upon the measurement frequency and the nominal capacitance and conductance of the sample under test.

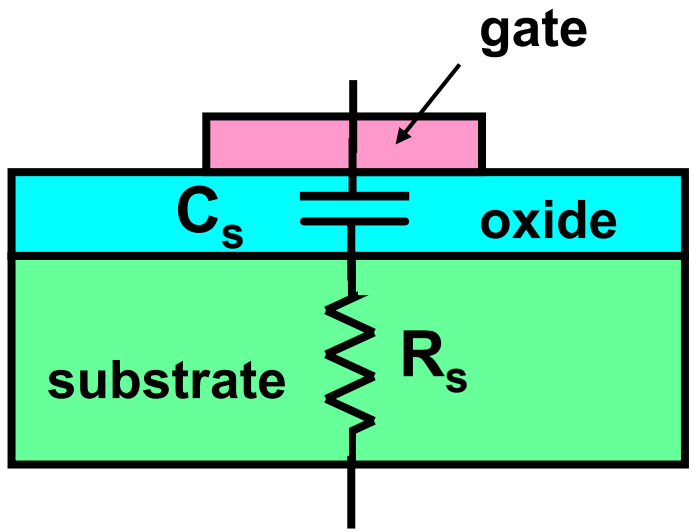
- The relative capacitance measurement accuracy of an LCR meter decreases with:
  - → decreasing frequency
  - → increasing conductance
  - → decreasing capacitance

- For some conditions, errors can truly dominate the measurement!



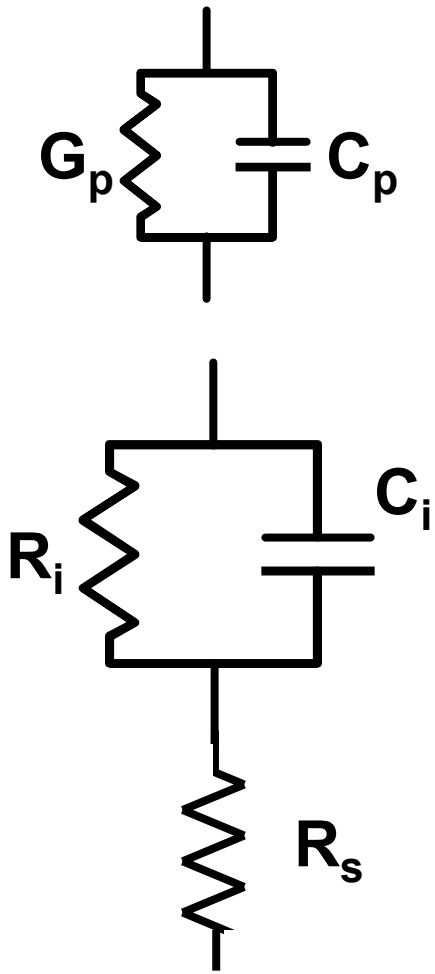
Relationship of LCR Meter Output to Sample Parameters

- In general, we can't count on LCR meter output parameters to relate directly to our sample parameters.
- Only in the simplified case shown here of a high-quality-factor, low leakage insulator on a resistive substrate can we hope to identify C_s with C_{oxide}, R_s with $R_{substrate}$ in a series-mode measurement.



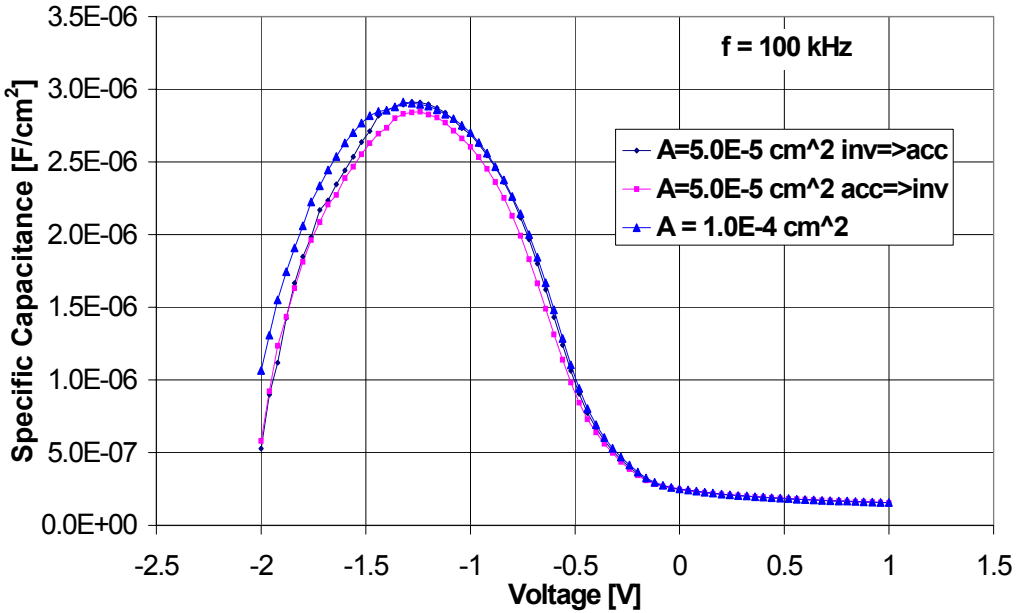
Evolution of Sample Equivalent Circuits

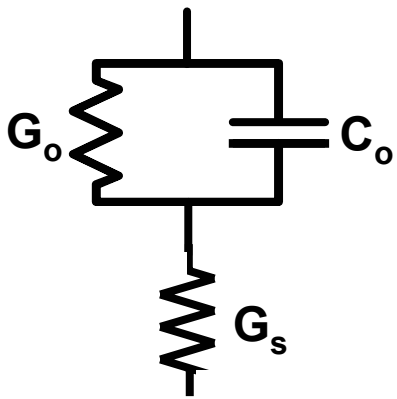
- For some samples, capacitive and resistive impedances of the insulator may be comparable, but still greater than the series resistance of the substrate or connections. Here, the parallel equivalent circuit output mode will provide a valid description of the sample.
- Eventually, however, all three may become of comparable size, and none can be ignored. We then need a 3-element equivalent circuit.



Shortcomings of a Two-Element Equivalent Circuit

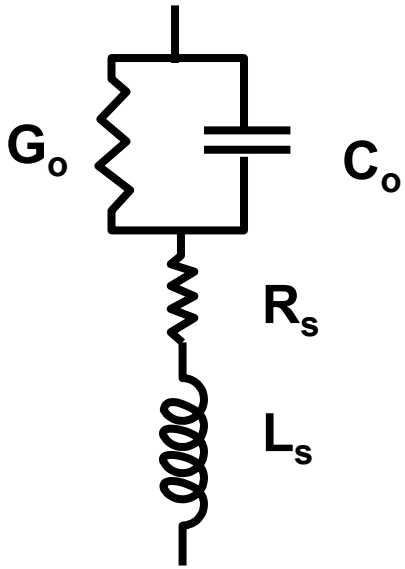
- Capacitance roll-over is a common consequence of using the two-element C_p meter output to represent a conductive dielectric on a resistive substrate.
- Use of the three-element model will *sometimes* yield a valid model of the structure.

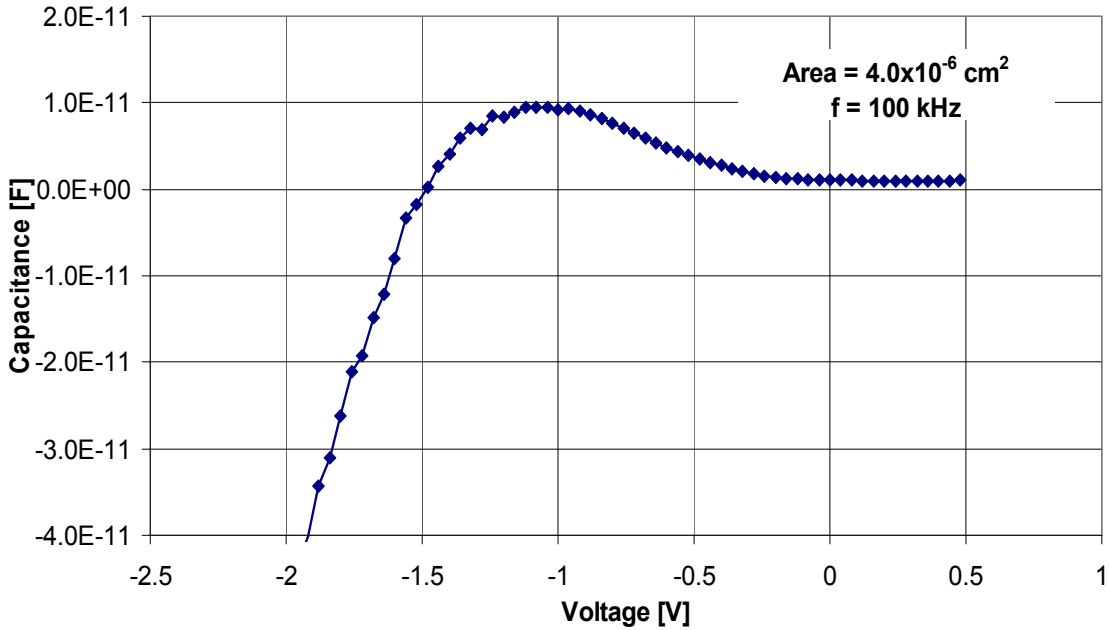




$$C_p \approx \frac{G_s^2}{(G_s + G_o)^2} * C_o$$

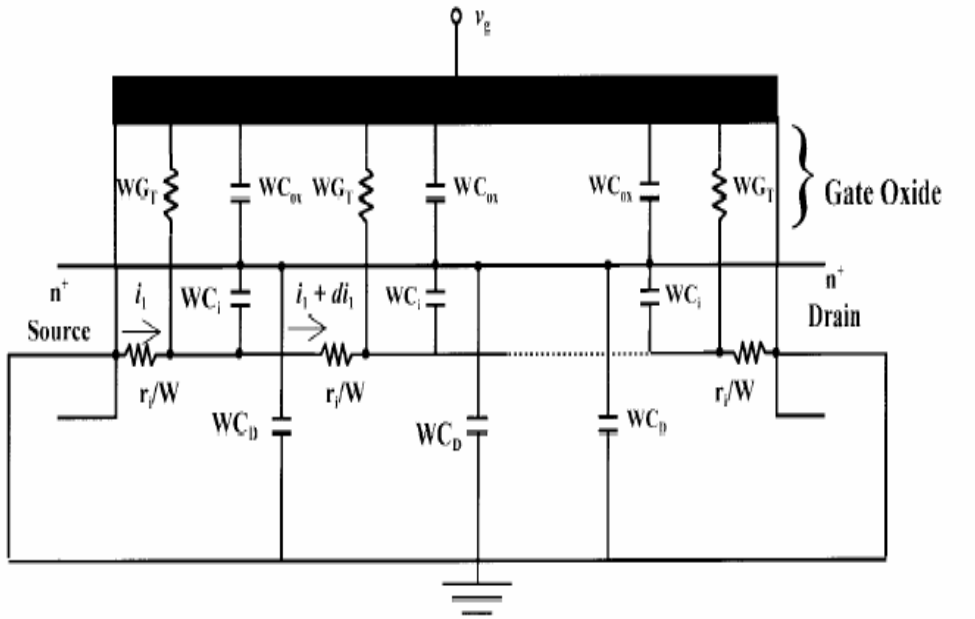
Shortcomings of a Three-Element Equivalent Circuit





- A series inductance in addition to the three-element circuit is necessary to model negative capacitance or capacitance rising above C_o.
- The source of the inductance is not clear; it could be a measurement effect or physical phenomenon.

A Distributed Transistor Channel Equivalent Circuit



- **This near-ultimate transmission line equivalent circuit was developed by Ahmed, et al.[1] It was used to show that channel lengths less than about 10 μm are needed to assure proper response of devices with 2 nm gate oxides.**

Modeling the C-V Measurements with an Equivalent Circuit

- Since a single capacitance measurement yields only two parameters, the real and imaginary parts of the impedance, we will need multiple measurements to solve for the 3, 4, or more elements in our equivalent circuits. Several approaches have been suggested:
  - An iterative technique to isolate and evaluate series components [2]
  - Use of two measurement frequencies to give four parameters
    - For the three-element equivalent circuit [3]
    - for the four-element circuit [4]
  - Evaluation of transmission line parameters for the distributed equivalent circuit [1]

Determination of EOT and CET

- Once an accurate capacitance value representing the dielectric is obtained from the modeling above, values of EOT and CET may be determined.
- Definitions:
  - EOT (Equivalent Oxide Thickness): The thickness of an SiO_2 film having the same specific capacitance as the dielectric film in question, without any effects from quantum confinement or polysilicon depletion in its electrodes.
  - CET (Capacitance Equivalent Thickness): This thickness determined by computing ε_{SiO2}*Area/C_{meas} where C_{meas} is the measured capacitance in inversion or accumulation at some defined voltage.

Significance of EOT, CET

EOT:

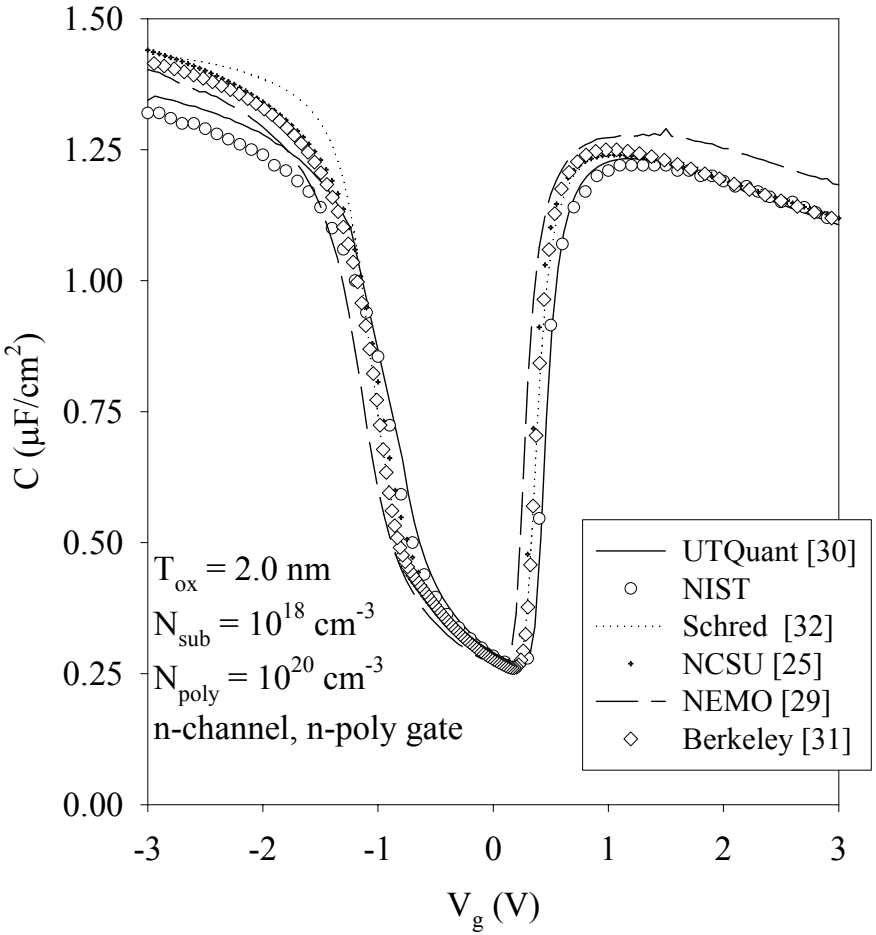
Because of its independence of device structural effects, this is basically a materials parameter. It is normally evaluated with the device biased in accumulation, where errors involved in its calculation are expected to be minimized.

CET:

The simplicity of its calculation suggests that all device-related shortcomings are included in this parameter. It does, however, govern device operating parameters such as drive current. Thus it is usually evaluated in inversion, the operating mode of the device, yielding the parameter CET(inv).

EOT Determination: A Choice of Simulators

- Simulators show a difference of up to 20% in the calculated accumulation capacitance.
- This will lead to significant differences in EOT from the same C-V data.
- Possible reasons include the use of approximations for quantum effects vs. Schrödinger equation, wave function boundary conditions, and type of carrier statistics.
- It is wise to choose one simulator, and always specify it when quoting values.

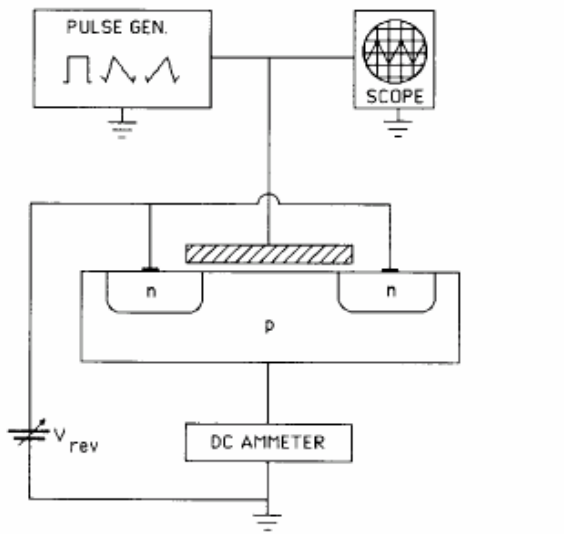


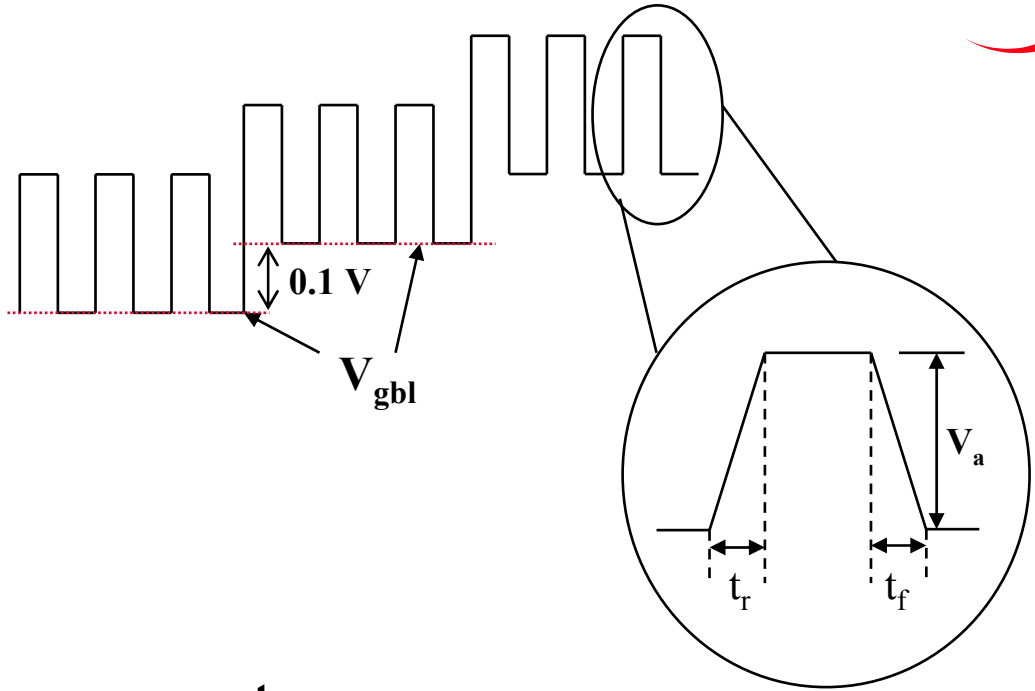
Interface State Density, D_{it}

Measurement of interface state density has been one of the greatest challenges in advanced dielectric characterization. This has been because most standard techniques have significant shortcomings for these structures. The standard techniques are

1. **Terman technique:** based on high-frequency C-V stretch-out. Low sensitivity for thin films, high frequency assumption often not met.
2. **High-low frequency C-V:** Quasi-static (low frequency) C-V not usually measurable because of high dielectric leakage.
3. **AC conductance-frequency:** Very sensitive but complicated technique; also leakage-sensitive.
4. **Charge pumping:** Requires transistor structures, also leakage sensitive, but corrections are possible.

Charge Pumping Measurement





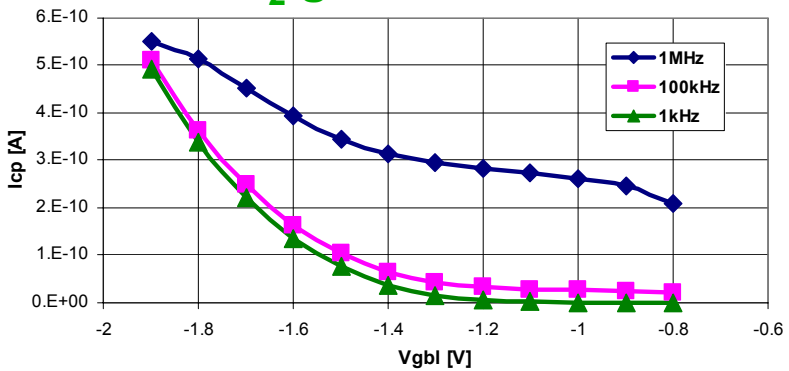
- **Base-level charge pumping measurement:**
  - **fixed amplitude V_a, base voltage stepped in 0.1V increments**
  - **rise and fall times t_r and t_f = 100 ns**
  - **traps fill from S/D during t_r, empty into substrate during t_f**
- **Charge pumping current is given by** $$I_{cp} = fqA_G \overline{D_{it}} \Delta E$$

f= **freq,** A_G= **channel area,** $\overline{D_{it}}$= **average** D_{it} **over** ΔE ($E_{f,inv}$ –$E_{f,acc}$)

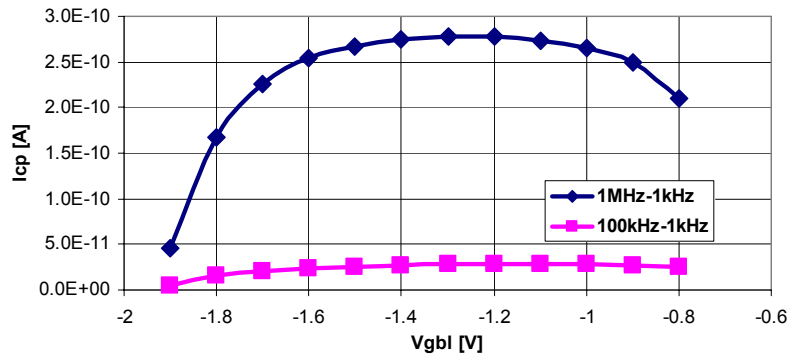
Leakage Correction: Key to D_{it} Measurement

2 nm SiO_2 gate

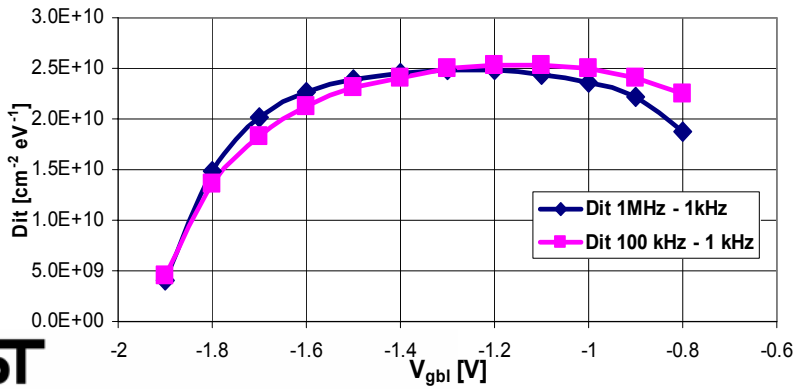
I_{cp}



Corrected I_{cp}



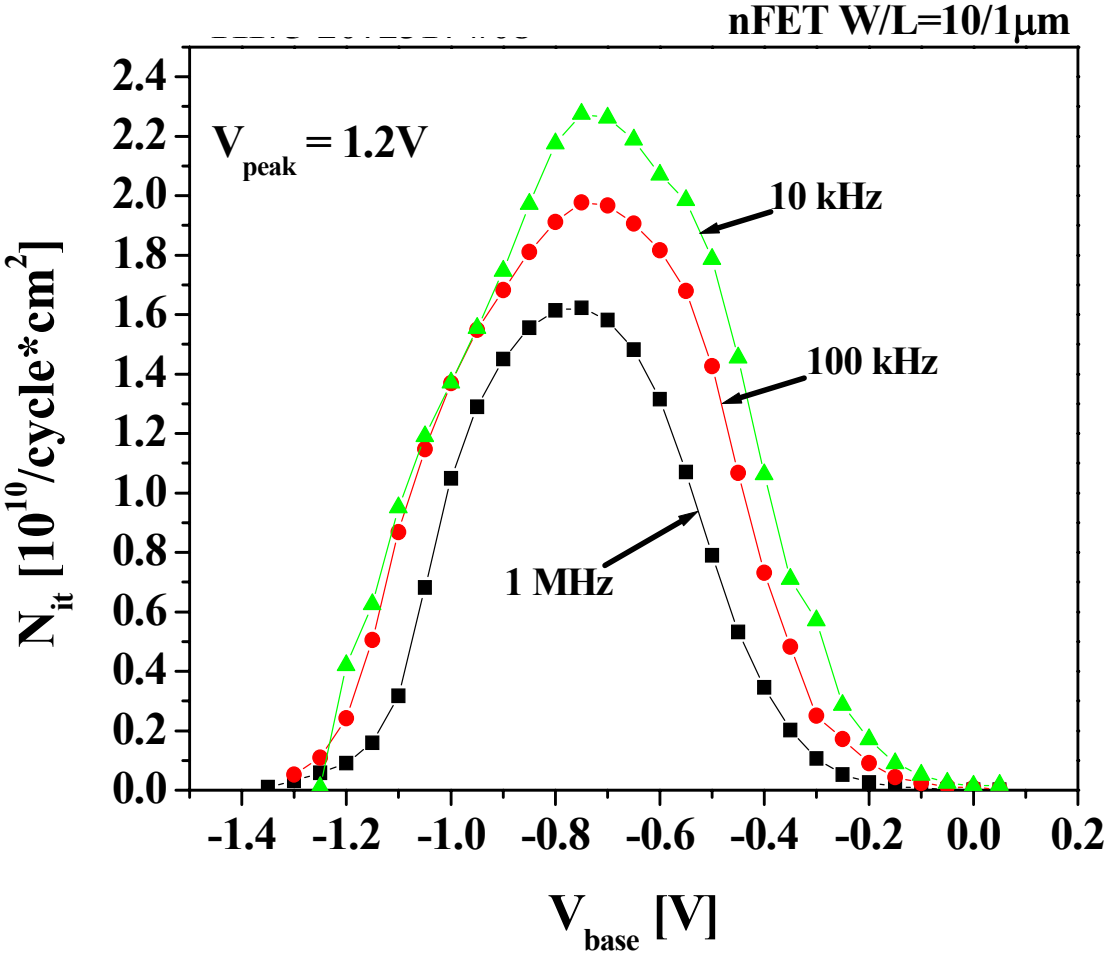
D_{it}



- **Measure I_{cp} at 1 kHz**
  - "Looks" like DC relative to 1 MHz, 500 kHz, or 100 kHz data
- **Subtract 1 kHz I_{cp} data from high frequency I_{cp} data**
  - Effectively removes DC leakage current
- **Use small transistors to reduce leakage current relative to the charge pumping current**
  - Example: W/L = 10/1 μm

Note frequency independence of D_{it} in the 100 kHz-1MHz range.

Charge Pumping in High-k Devices
Fixed Amplitude-Variable Base Measurement



- Frequency dependence of interface state density is a characteristic of many high-k gate stacks.
- It may be interpreted in terms of depth-related time constant variation [5], associated with bulk of interfacial traps.

Extrinsic Defect Density in High-k Films

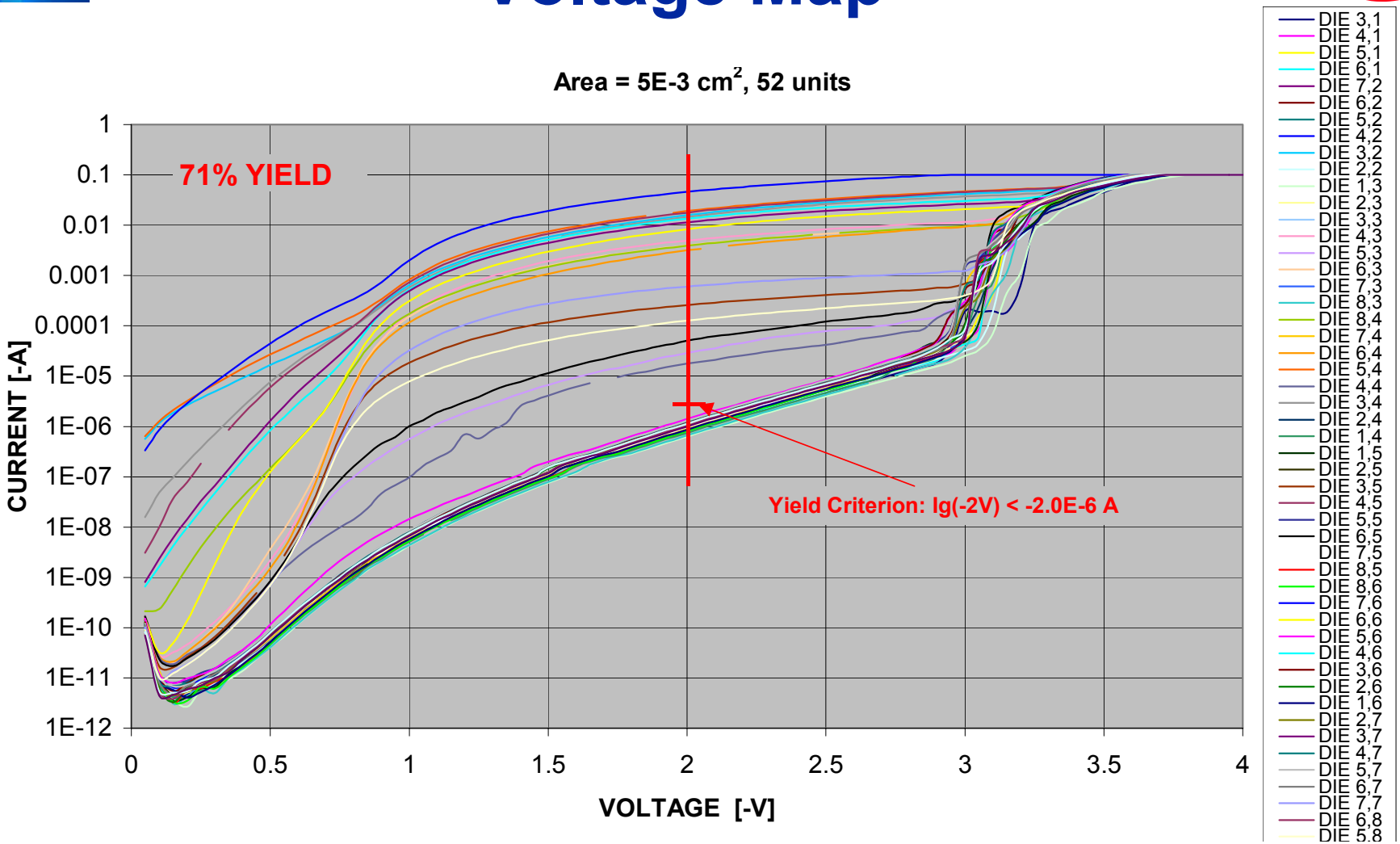
- Extrinsic defect distributions have been driven to relatively low levels in conventional SiO_2 gate dielectrics.

- High-k films, because of their structure and deposition conditions, may not have the same low defect densities we have become accustomed to in conventional devices.

- In thicker SiO_2 films, extrinsic defects are sensed by low oxide breakdown voltage, or early failure on constant-current/voltage stress tests. Such failures are often not easily sensed in high-k films, particularly in large-area devices needed for low defect density resolution.

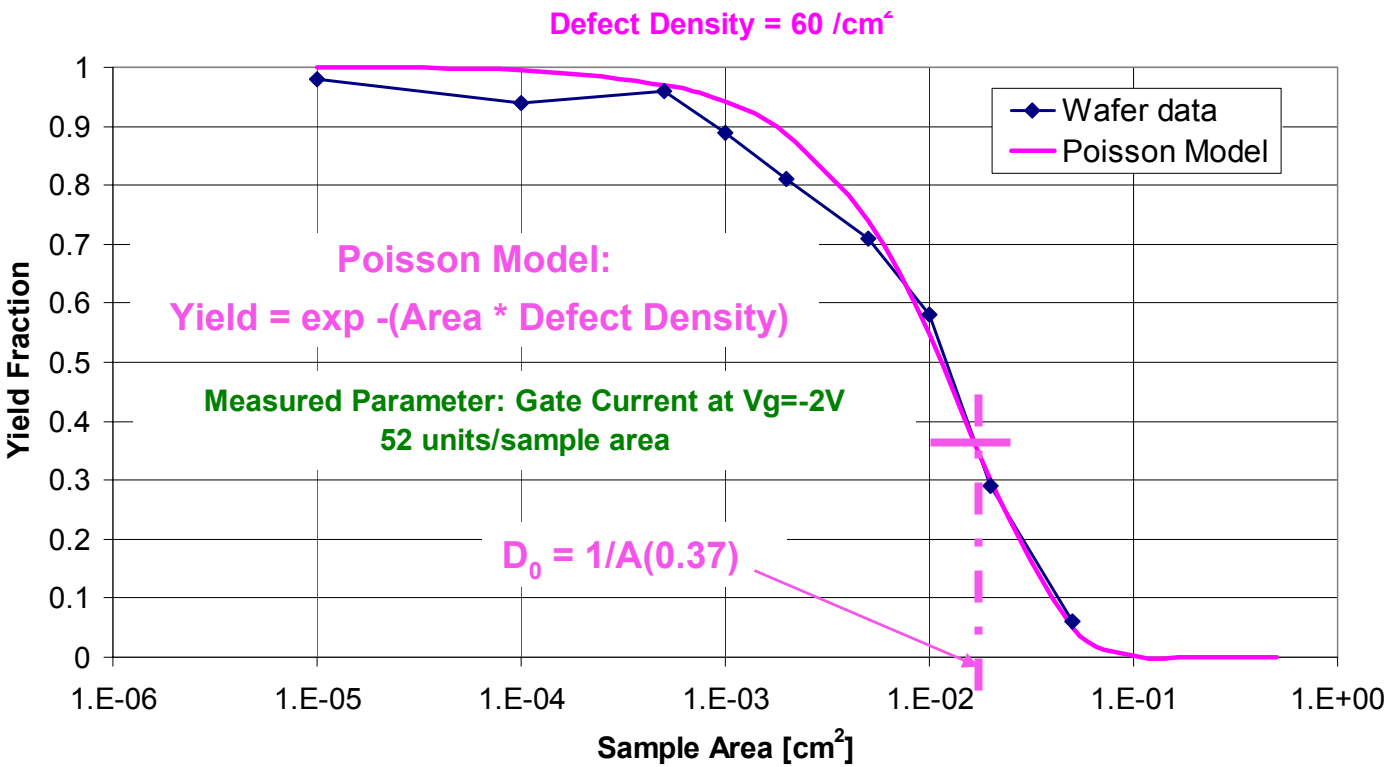
- It has been observed that defects in high-k films often result in a higher level of conductivity over their entire I-V characteristic.

Typical Full-Wafer Current-Voltage Map



- Yield criterion easily identified for a given wafer

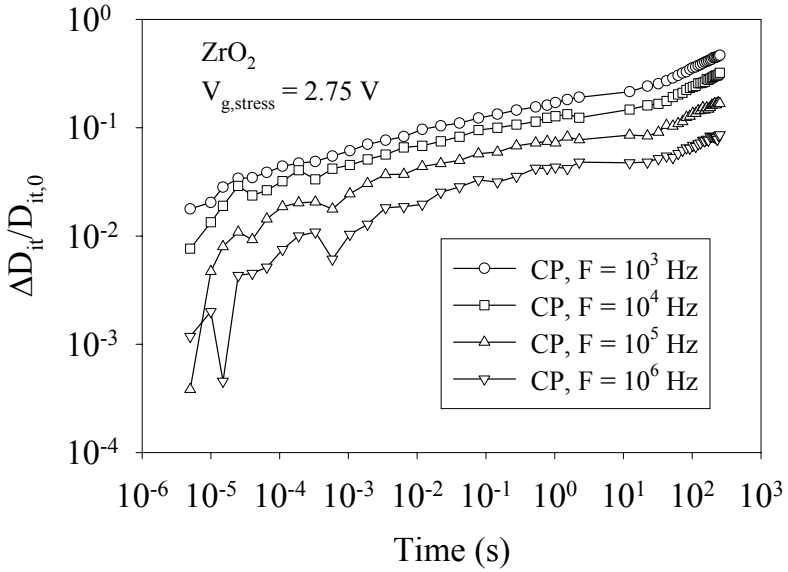
Extrinsic Defect Density Determination

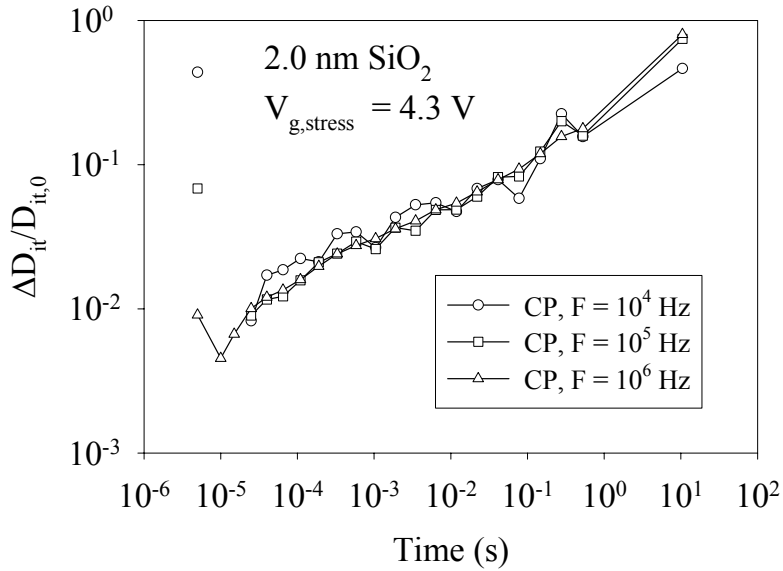


- **Assuming a good fit, defect density equals the inverse of the sample area for which the yield is 37%.**

- **Preliminary measurements show defect densities ranging from about 1 /cm² up to as high as 2.7x10⁴ /cm² or higher. No clear process dependence has yet been established.**

Reliability: Defect Distribution in High-k Dielectrics





- **Interface state density generation under constant voltage stress is compared for ZrO_2 and SiO_2 FET's, using charge pumping.**
- **Higher generation rates are observed in the bulk of the ZrO_2 film than at its surface; SiO_2 shows no frequency (or depth) dependence.**
- **Device parameter drift (e.g. D_{it}) may be a greater reliability problem in high-k films than dielectric breakdown.**

Summary

- The low, complex impedance of advanced gate dielectrics forces us to be thorough in our understanding, measurement, and analysis of MIS C-V characteristics.
- Multi-element equivalent circuits are required to describe these structures adequately, and parameter extraction requires sophisticated modeling.
- Many of our conventional measurement techniques are not applicable to these structures, or detailed correction procedures must be invoked.
- The different material properties of high-k dielectrics compared to SiO_2 suggest that we may find new primary reliability issues, requiring development of new characterization techniques.

Acknowledgement

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