Recent Developments in Electrical Metrology for MOS Fabrication

Gate Engineering
Channel Engineering
Source-Drain Extension Engineering

George A. Brown
SEMATECH
Mark C. Benjamin
Solid State Measurements,Inc.

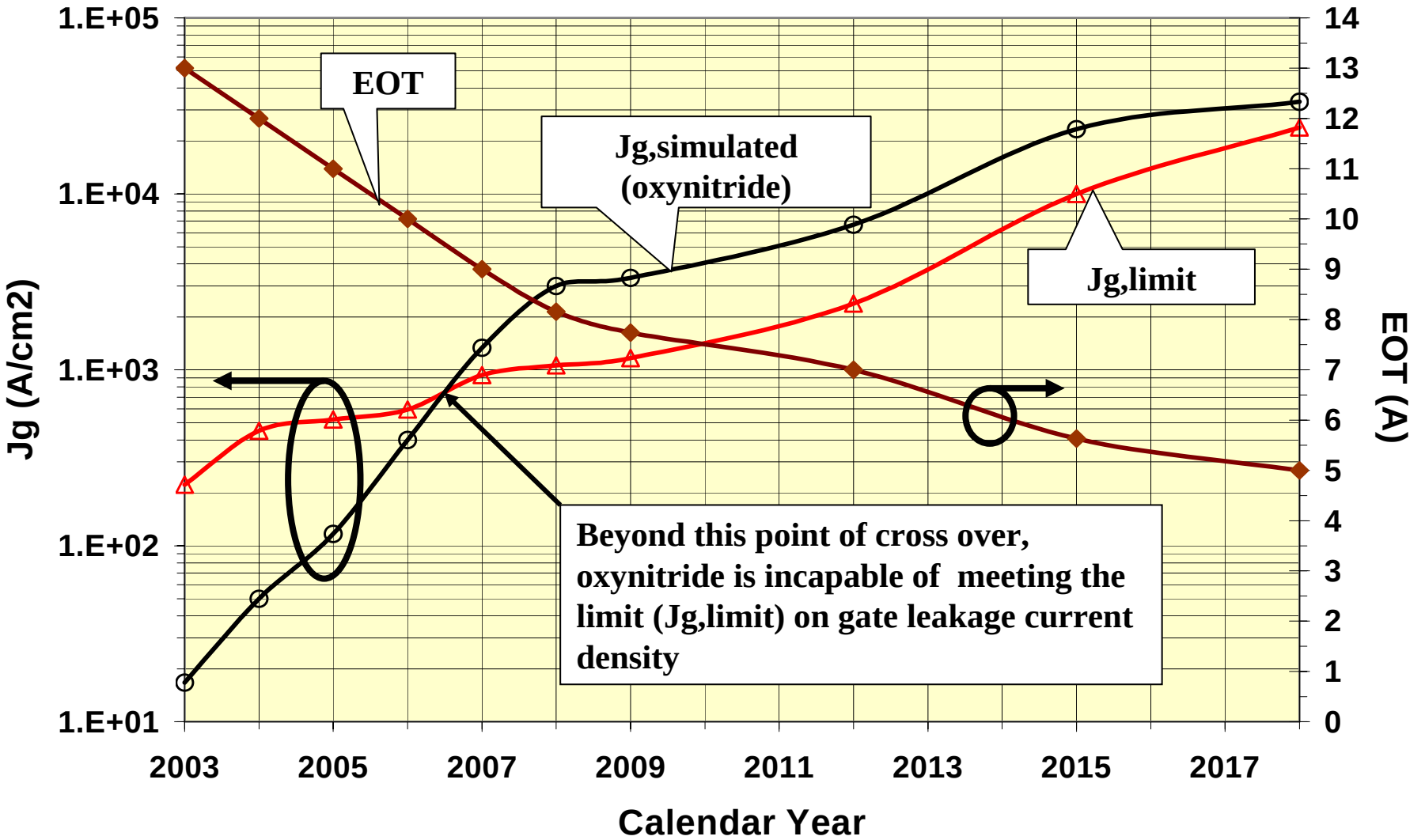
Gate Engineering

George A. Brown
SEMATECH

Introduction – Gate Dielectrics

- Brief Roadmap Review
- Traditional Gate Dielectric Electrical Metrology
  - Measurements, analysis, and limitations
- Improved Methods and Recent Developments
  - Critical C-V measurement parameters
    - High frequency
    - Low series resistance test structures
    - Adequate area resolution
  - UHFCAP structure
  - Multi-frequency C-V, D-ω characteristics
  - Interface State (D_{it}) Measurement: charge pumping
  - In-line C-V Measurements
- Summary

ITRS Roadmap for High Performance Gate Dielectrics (2004 update)



- Scaling beyond 1 nm, 10^3 A/cm^2 is almost upon us!

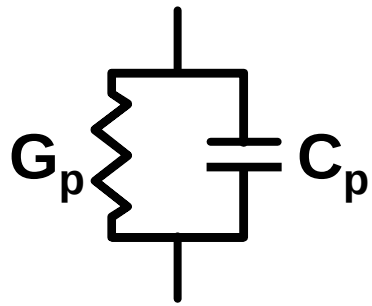
Evolution of gate dielectric electrical metrology

Parameter	Traditional Measurement Technique	Traditional Analysis Technique	Shortcomings for Advanced Devices	Improved Measurement Technique	Improved Analysis Technique
Oxide thickness, CET	100 kHz/1 MHz MOS C-V	Classical Poisson's Law Models	C-V distortion from high gate leakage	Low-Rs test structures, UHF C-V	Multi-element equivalent circuits
Oxide thickness, EOT	100 kHz/1 MHz MOS C-V	Classical Poisson's Law Models	Failure to account for quantum confinement, poly depletion		Schrodinger solvers for EOT
Interface State Density, Dit	Quasi-static C-V	Classical Poisson's Law Models	Gate leakage dominates quasi-static data	Charge pumping Brew's Dit	Pulse level, rise time to separate bulk trapping from Dit
Oxide Charge Tgrapping	MOS C-V Hysteresis	ΔVfb	inaccurate, poorly defined for high-k	Pulsed transient Id-Vg	Pulse rise time analysis

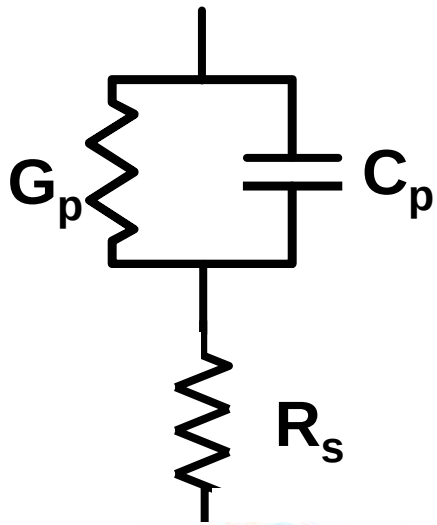
New methodologies must be developed to deal with the characteristics of radically scaled gate dielectric stacks.

Measurement of 0.5 nm EOT Gate Stacks with High Leakage

- High leakage gate stacks are modeled as parallel RC equivalent circuits.
- To resolve the capacitance, use of higher frequencies will reduce the capacitive impedance, making that element dominate the parallel resistance/conductance.
- But this only works if there is negligible parasitic series resistance in the test structure. Use of higher frequencies if series resistance is present only makes the capacitive impedance of interest negligible in comparison with R_s.



$$Q = \omega C_p / G_p$$



SEMATECH

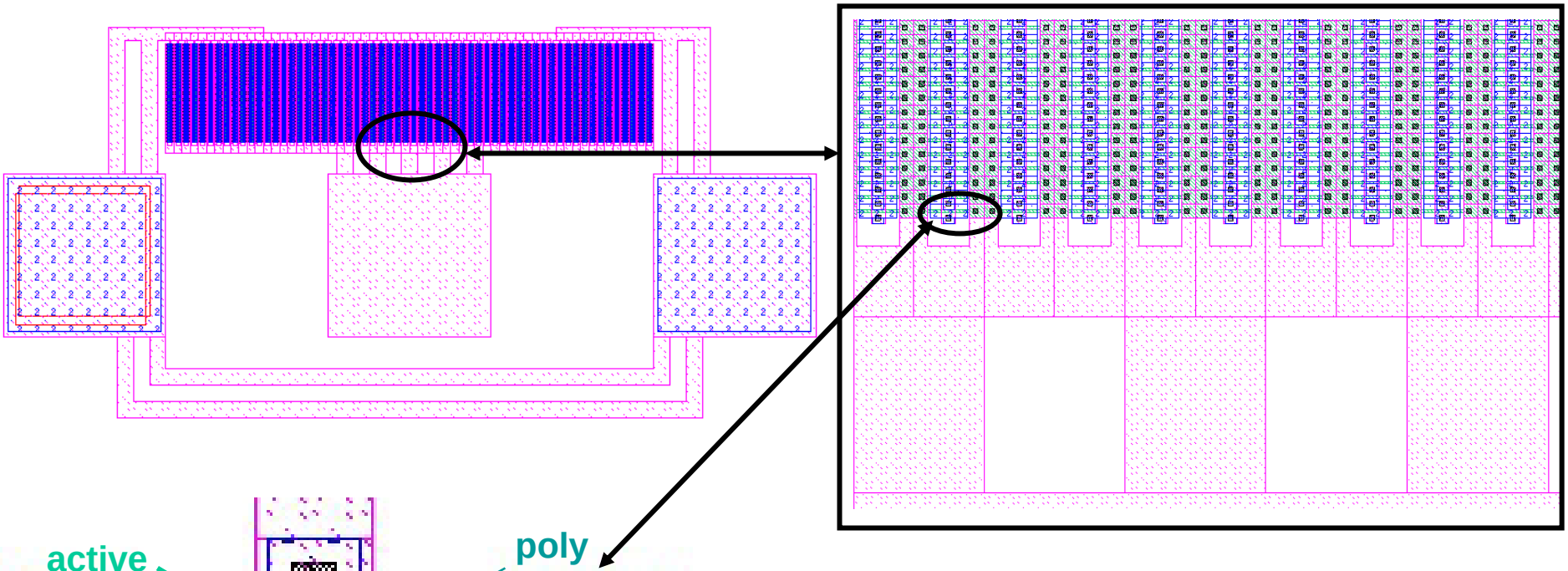
Requirements for EOT Measurement of High Leakage Gate Stacks

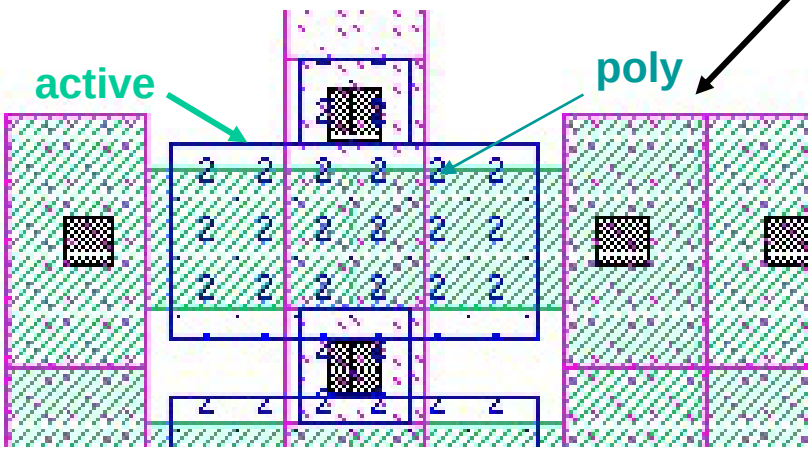
1. Capacitor test structure design with minimum series resistance.
   - Topside electrical contact to the capacitor substrate is required to eliminate the wafer chuck from the measurement circuit.

2. Use of measurement frequencies high enough to reduce the effect of the parallel conductance of the gate stack. *Dissipation factor must be reduced sufficiently to permit accurate measurements.*

3. Geometric resolution of the test structure effective area must be adequate to assure accurate and precise definition of EOT.

1-Port Philips UHF MOSCAP Design

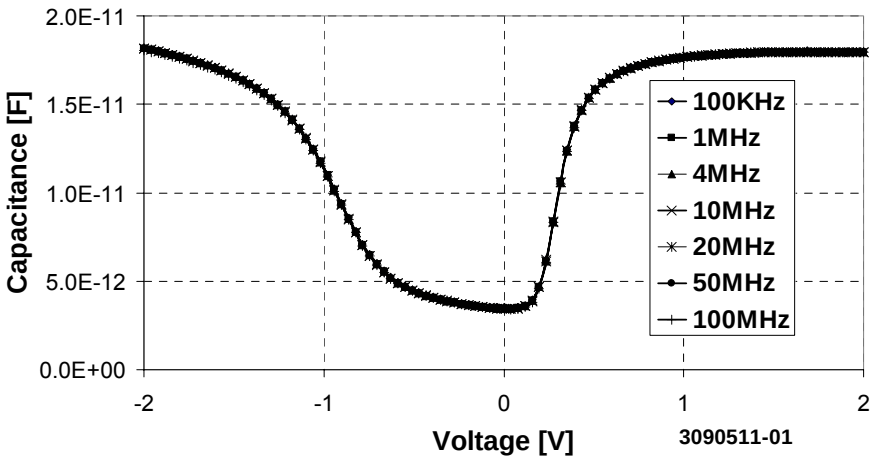




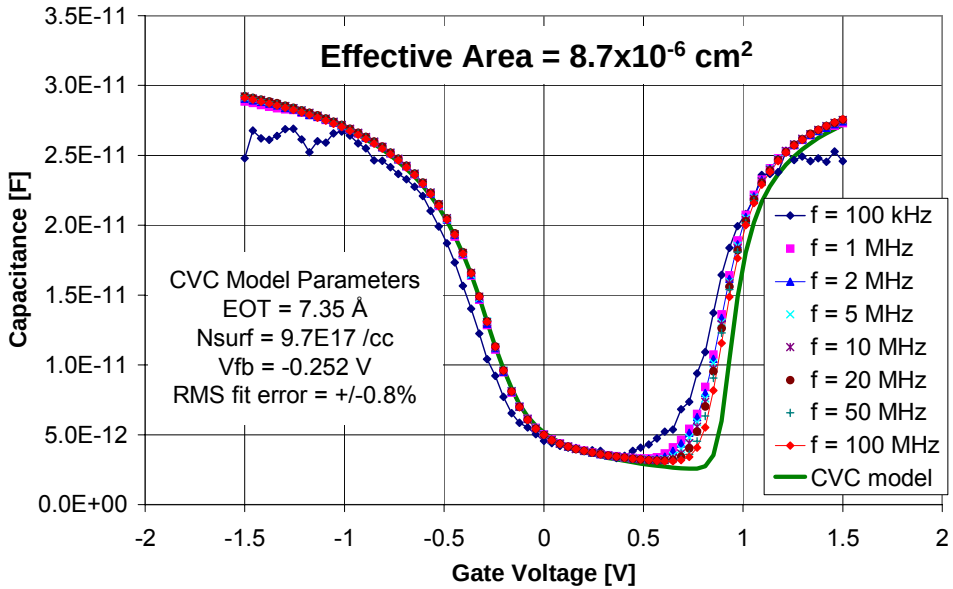
- Designed for low series resistance
- Uses 3-point (G-S-G) UHF probe head
- 720 - 1.0x2.6 μm capacitor elements
- Right and left ground pads connect p-well to S/D.

Multi-Frequency MIS C-V Measurements on the Philips UHF MOSCAP

2 nm SiO_2 – TiN gate electrode



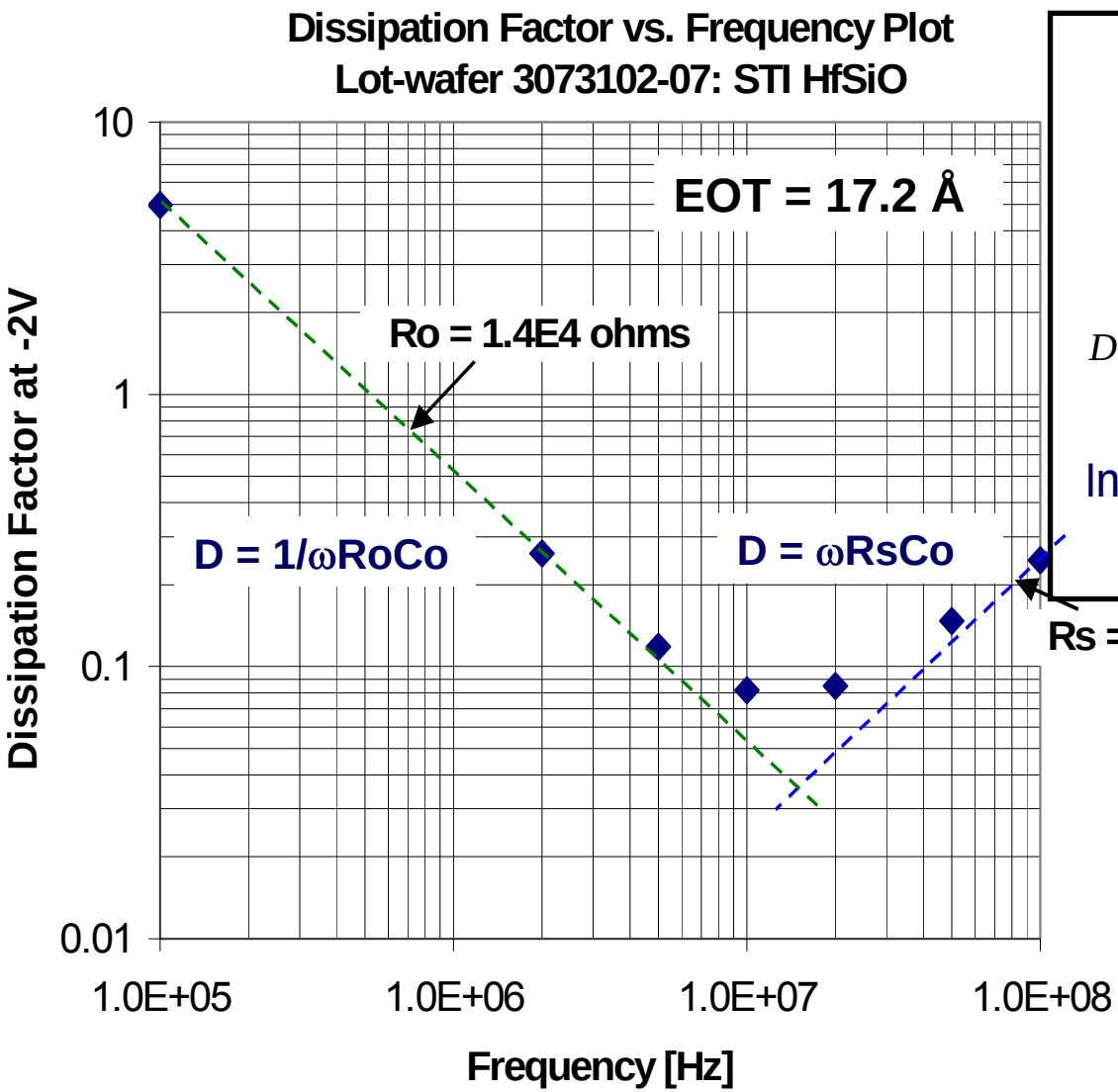
0.7 nm EOT HfO_2 – poly gate



Measurement: Agilent 4294A Precision Impedance Analyzer – IV Probe mode

- Frequency-invariant C-V data can be obtained in wafer form on 2 nm SiO_2 films with properly designed test structures.
- Some frequency dispersion is seen on more highly scaled high-k devices.

Three-element Equivalent Circuit Parameter Analysis from Dissipation Factor-Frequency Characteristics



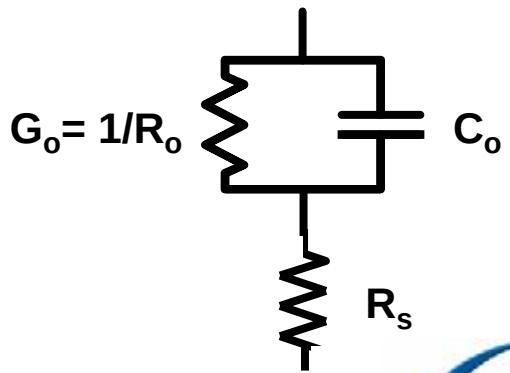
Extraction of Ro, Rs from D-ω Plots

For low frequencies, D ~ 1/f:

$$D = \frac{G_o(1+R_sG_o)}{\omega C_o} = \frac{1}{\omega R_o C_o}(1+\frac{R_s}{R_o}) \approx \frac{1}{\omega R_o C_o}$$

In the high frequency limit, D ~ f:

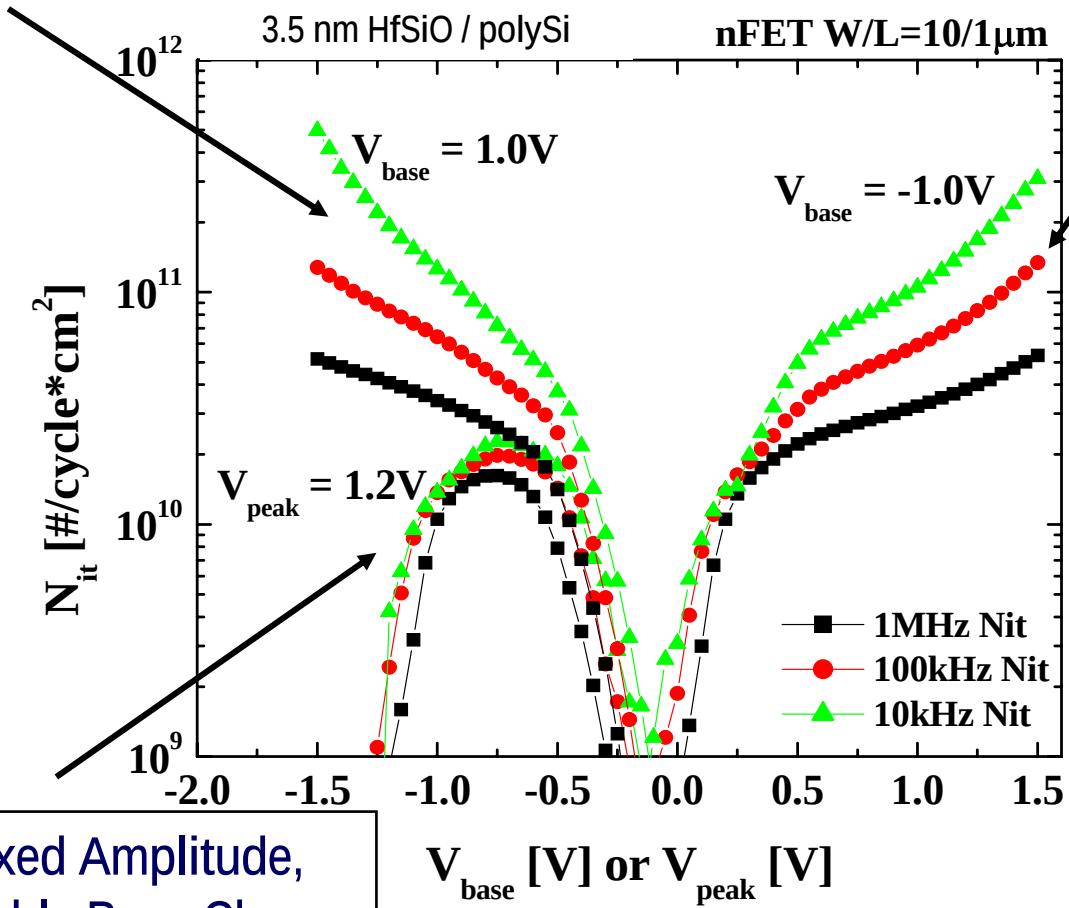
$$D = \omega R_s C_o$$



Dit: Comparison of Charge Pumping Techniques

Fixed Base, Variable Amplitude Charge Pumping (into accumulation)

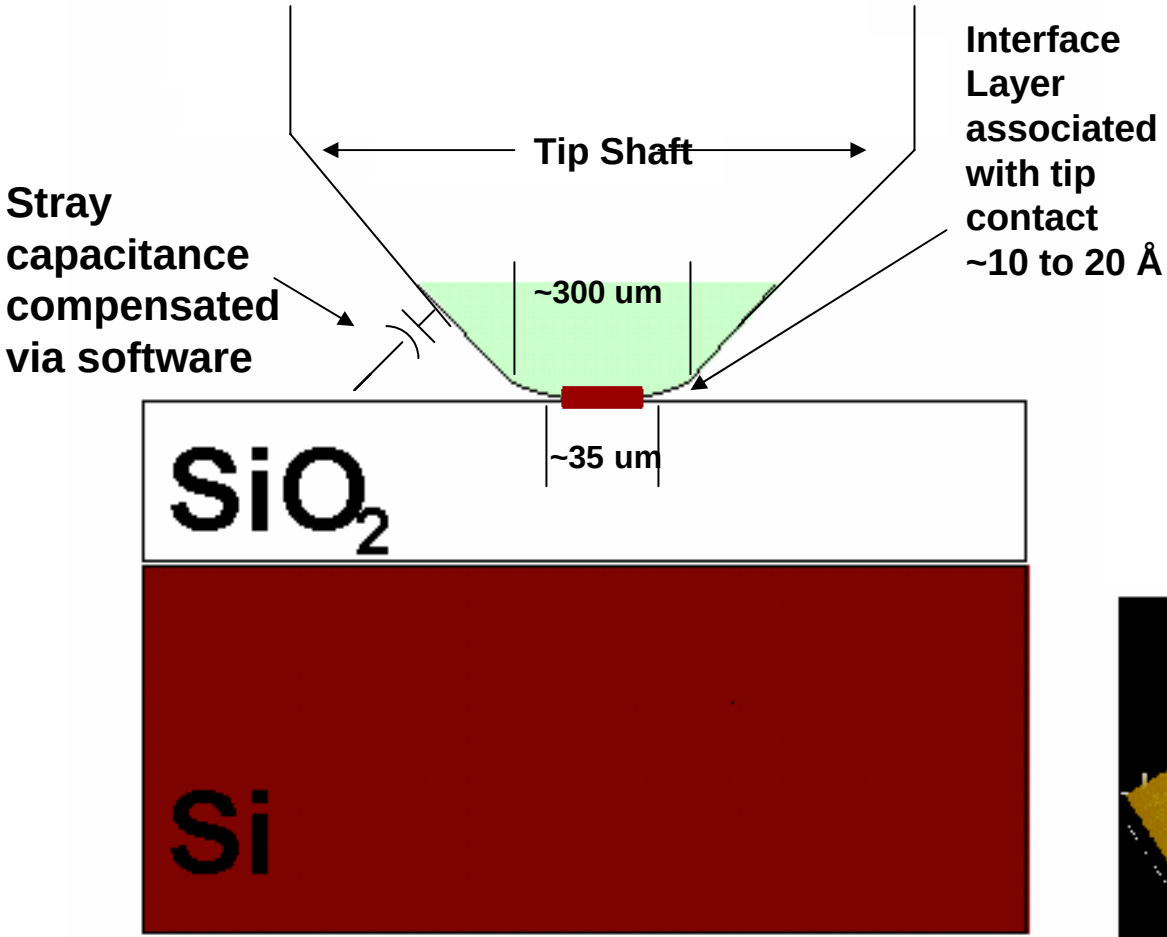
Fixed Base, Variable Amplitude Charge Pumping (into inversion)

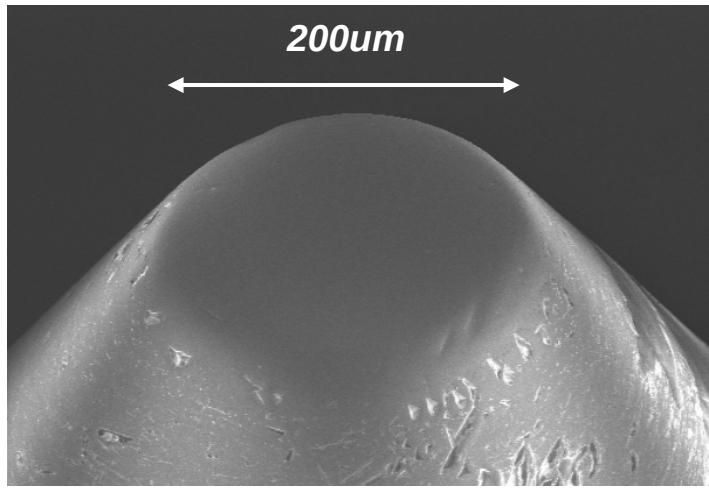


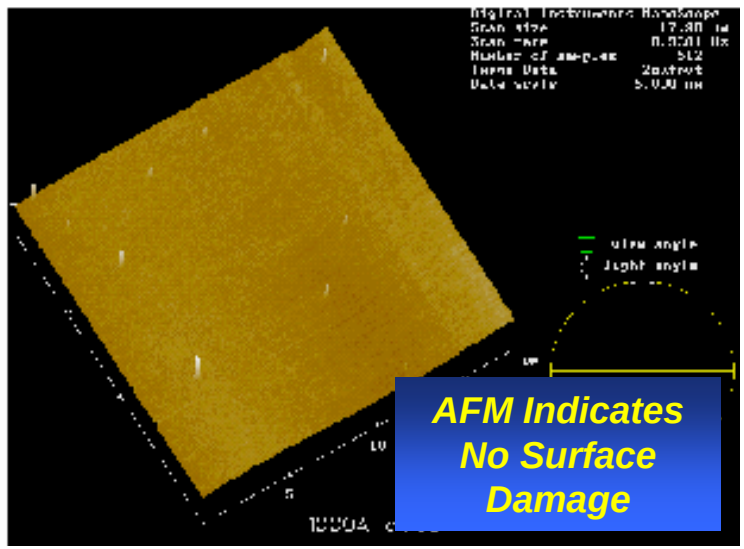
- These techniques provide alternative ways to characterize traps and trapping processes in high-k films.
- Information on energy and depth distribution of the traps may be obtained from these curves.

Fixed Amplitude, Variable Base Charge Pumping

EM-probe Description

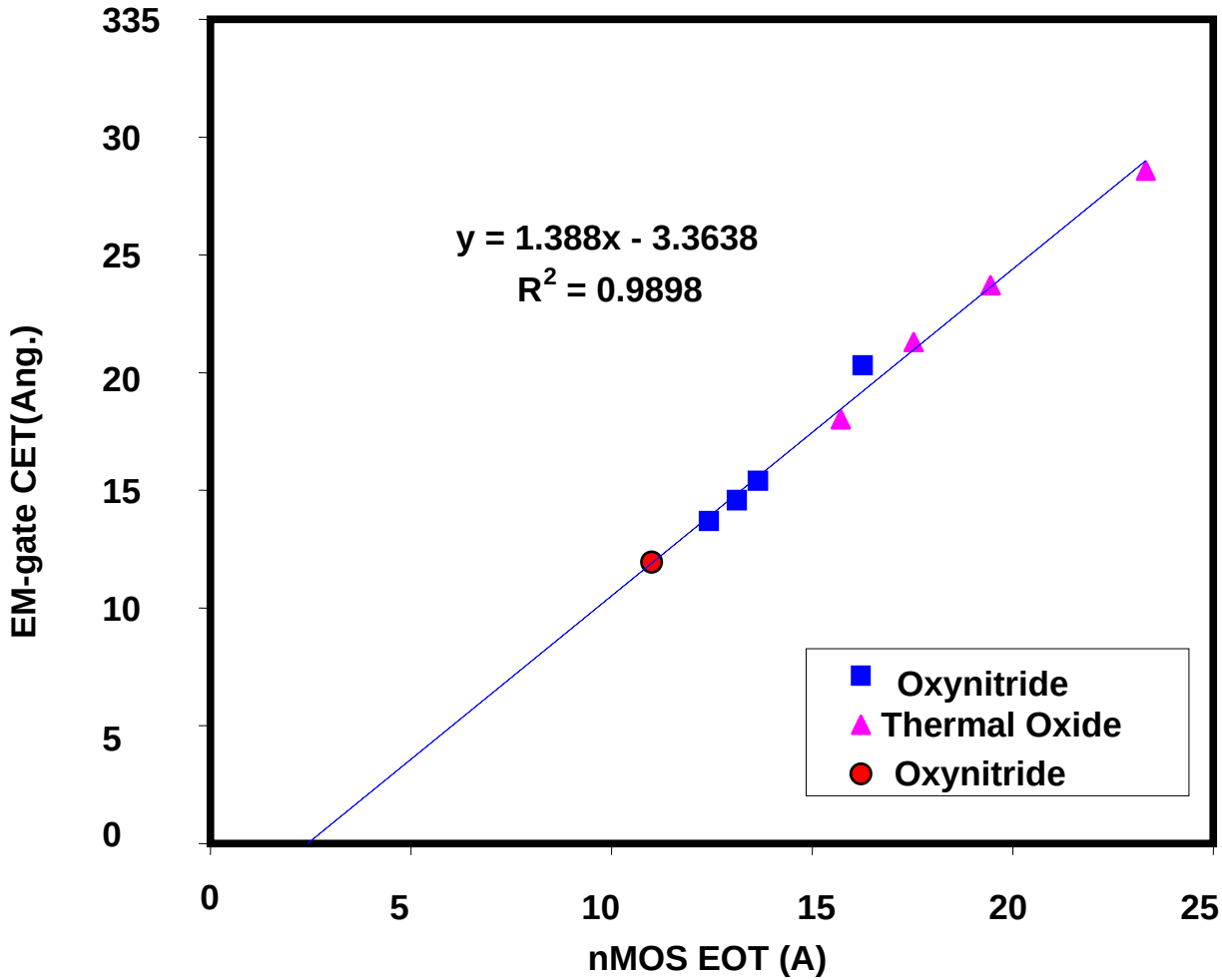






Small contact area provides superior performance for ultra-thin dielectrics

In-line Measurement of CET/EOT with EM-probe

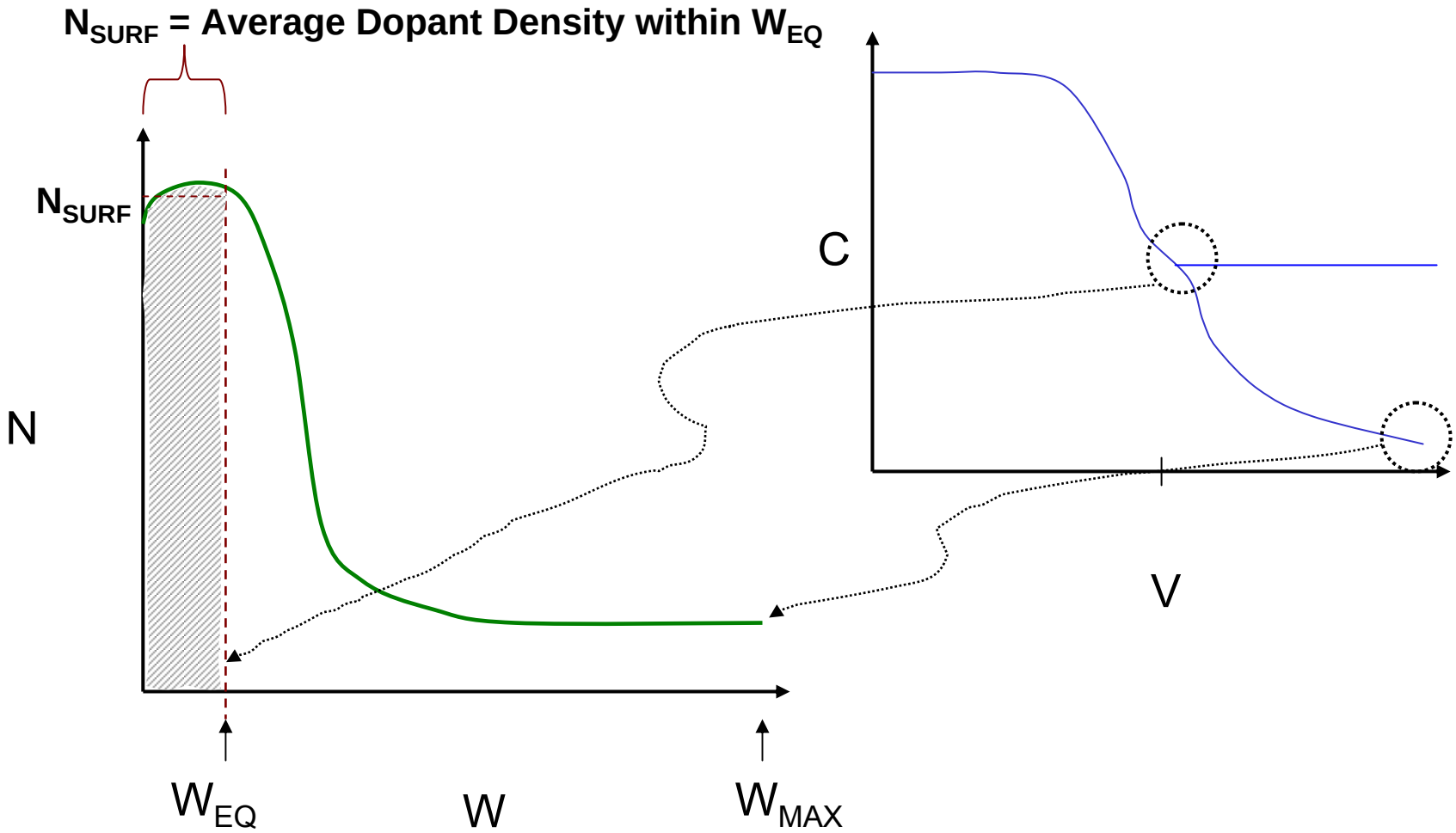


- Device-correlatable CET/EOT measurements can be made in-line for real-time process control down to ~1 nm.

Channel Engineering
SDE Engineering

Mark C. Benjamin
Solid State Measurements, Inc.

Relationship Between Dose and N_{SURF}

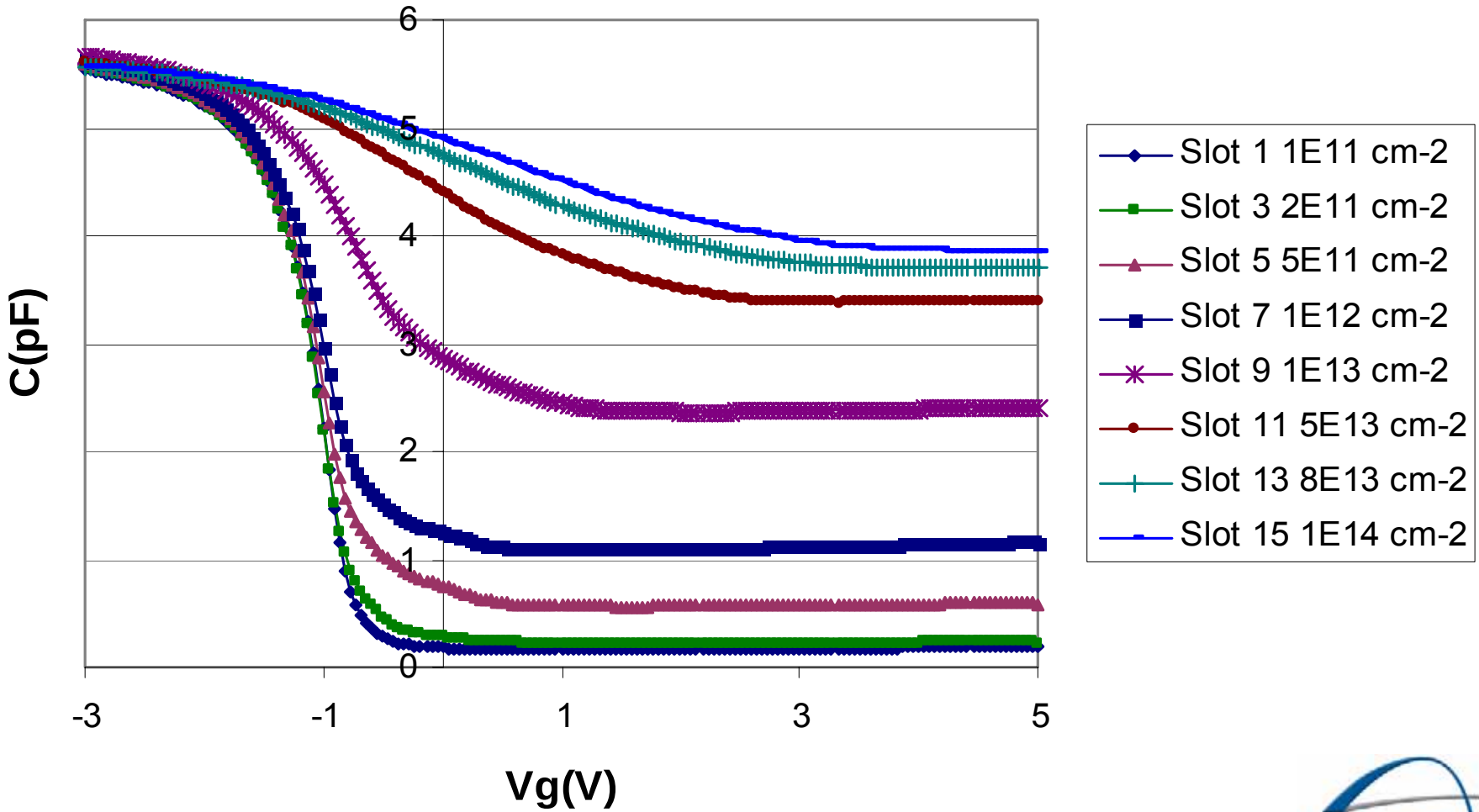


Equilibrium Dose = EQD = $\int N(w)dw$ from the surface to W_{EQ}

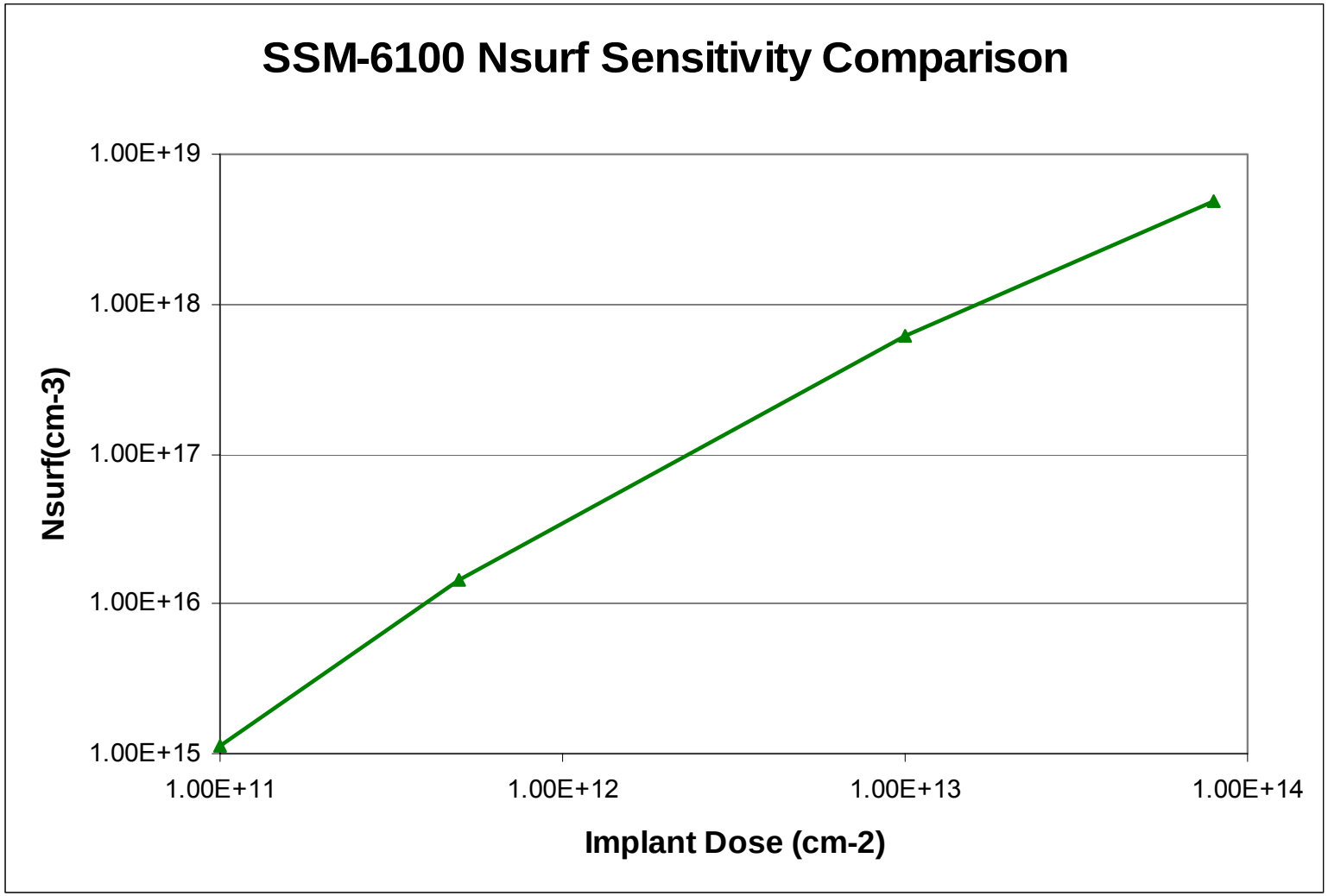
$= N_{SURF}W_{EQ} = SQRT(2\varepsilon k_S \psi_{SL,INV} N_{SURF}/q$

EM-gate Equilibrium CV Comparison

SSM-6100 EM-probe CV versus Implant Dose

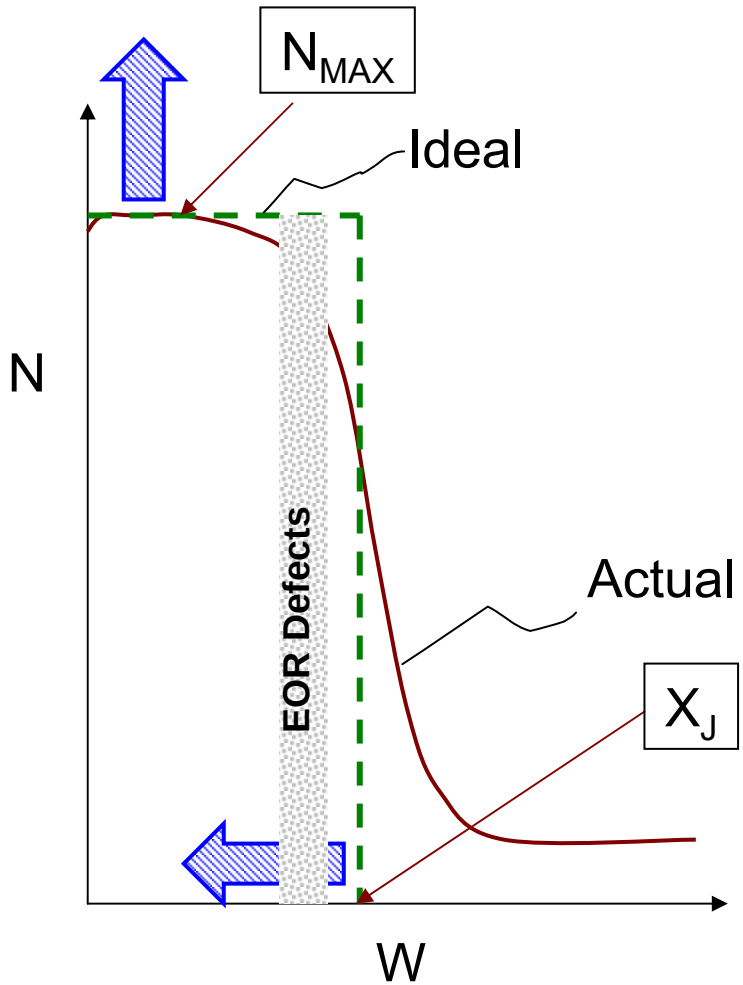


Sensitivity: Nsurf versus Implant Dose



Major Device and Materials Issues with USJ S/D Structures

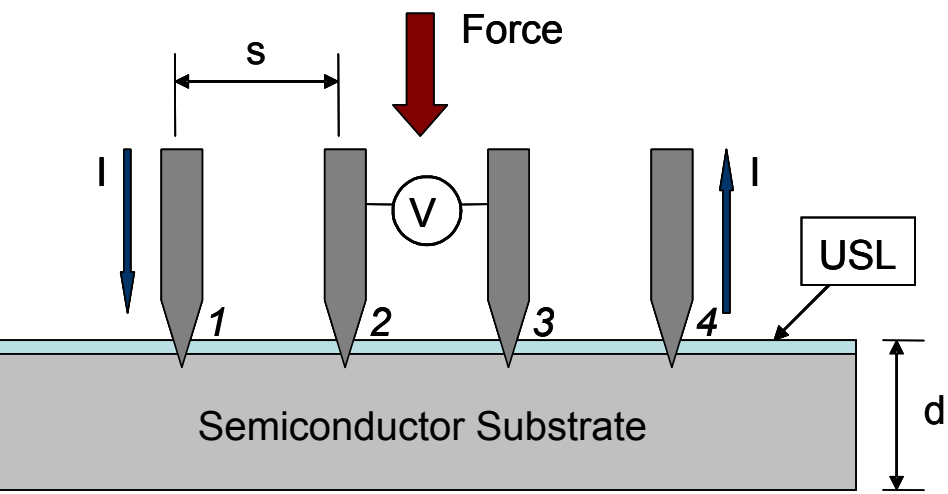
- Goal: *Increase Electrically Active N and Decrease W*
- Ideal ► BOX Profile!!



- Sheet Resistance (R_S)
- Surface Carrier Density (N_{SURF})
- Junction Depth (X_J)
- Carrier Density Profile Shape
- Junction Leakage
  - Sensitive to Implant EOR Damage

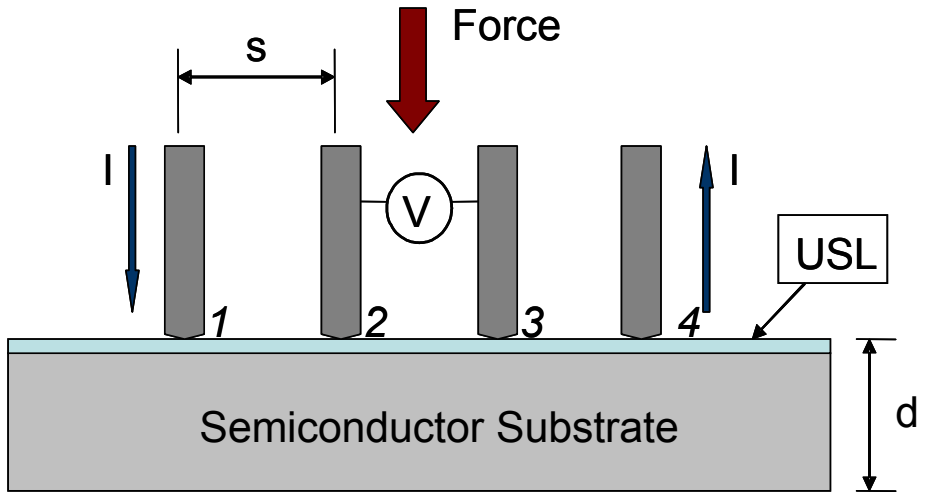
4pp: Conventional vs EM-Probe

Conventional Four Point Probe



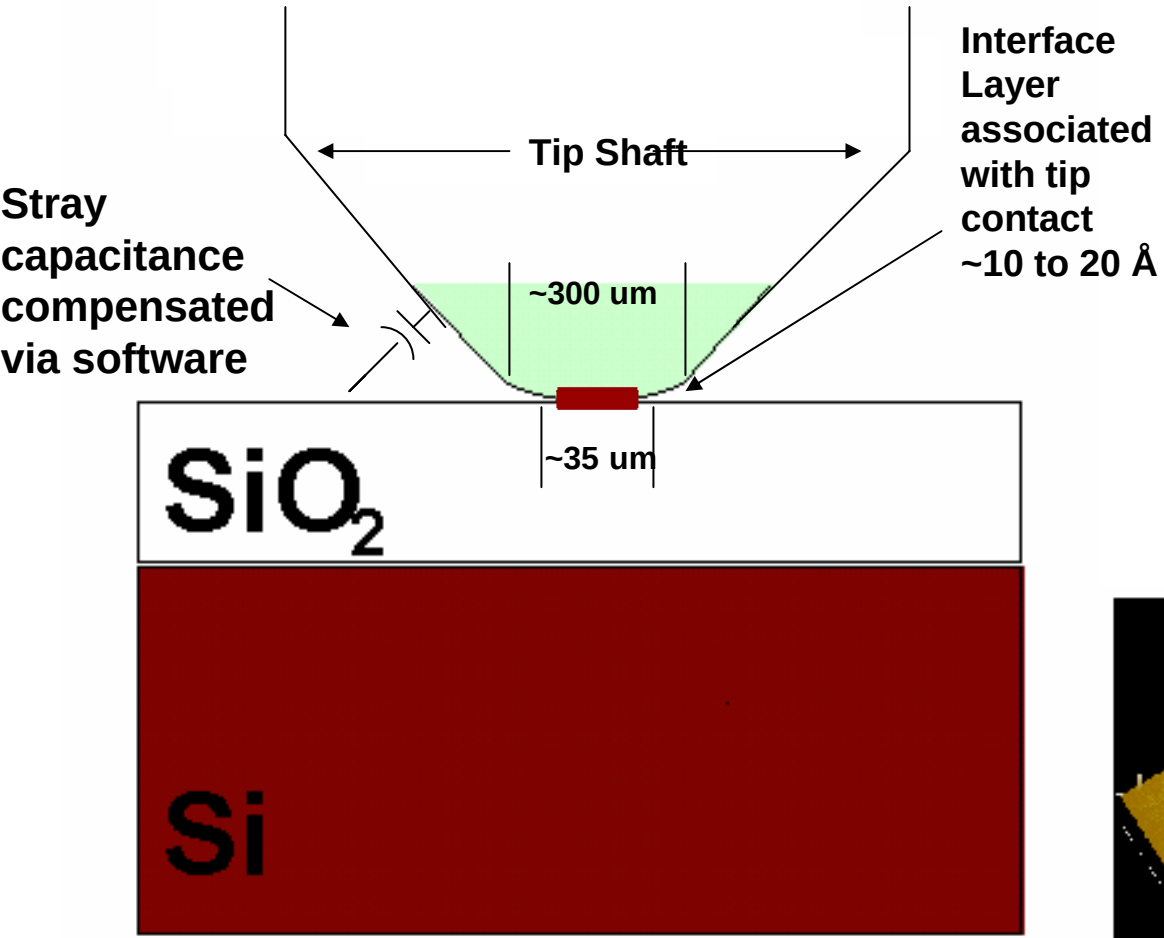
Sheet Resistance = R_S = CF(V/I)

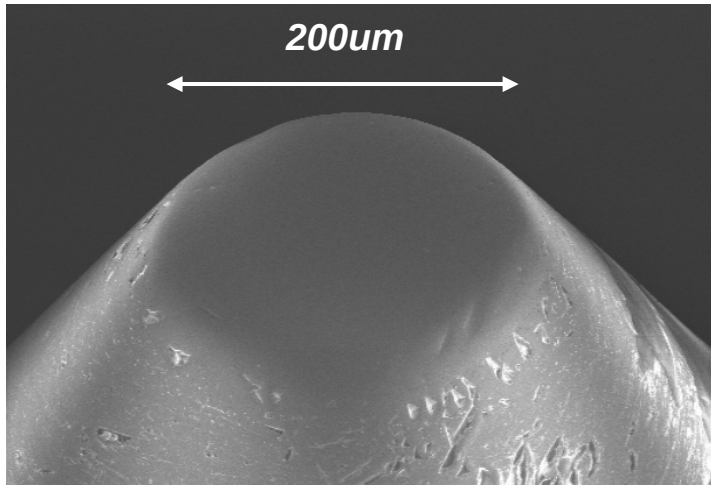
EM-probe Four Point Probe

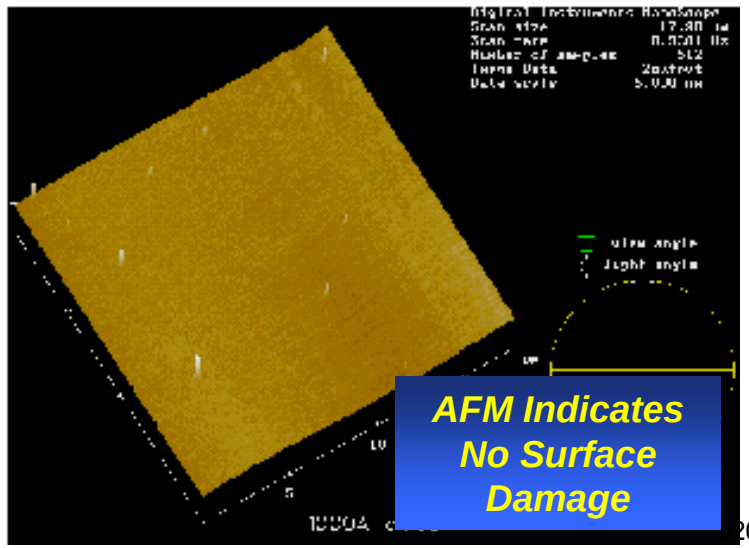


Sheet Resistance = R_S = CF(V/I)

EM-probe Description



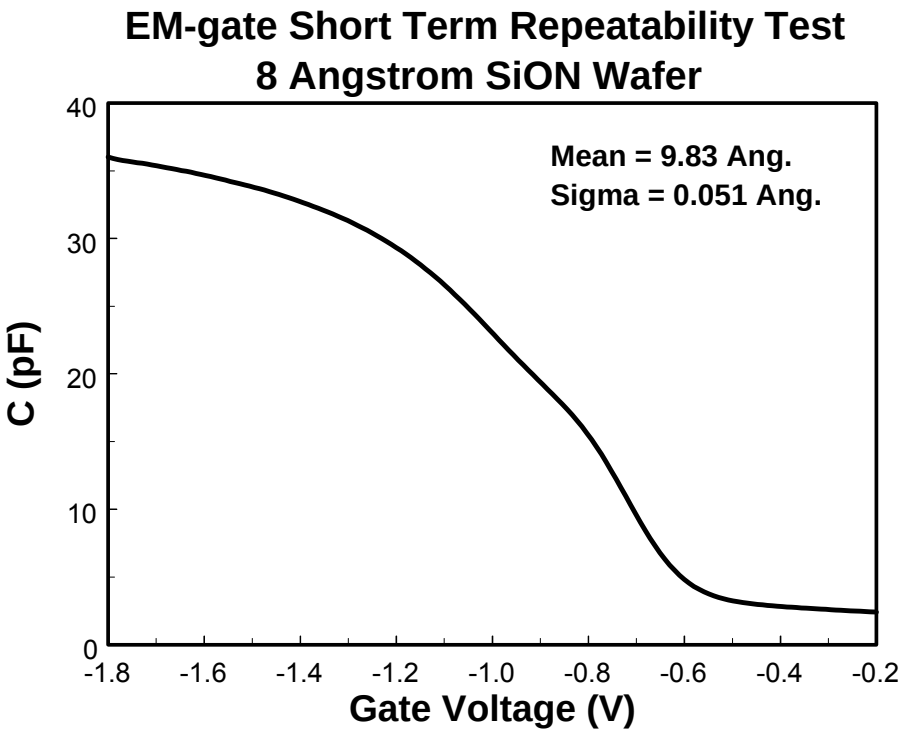


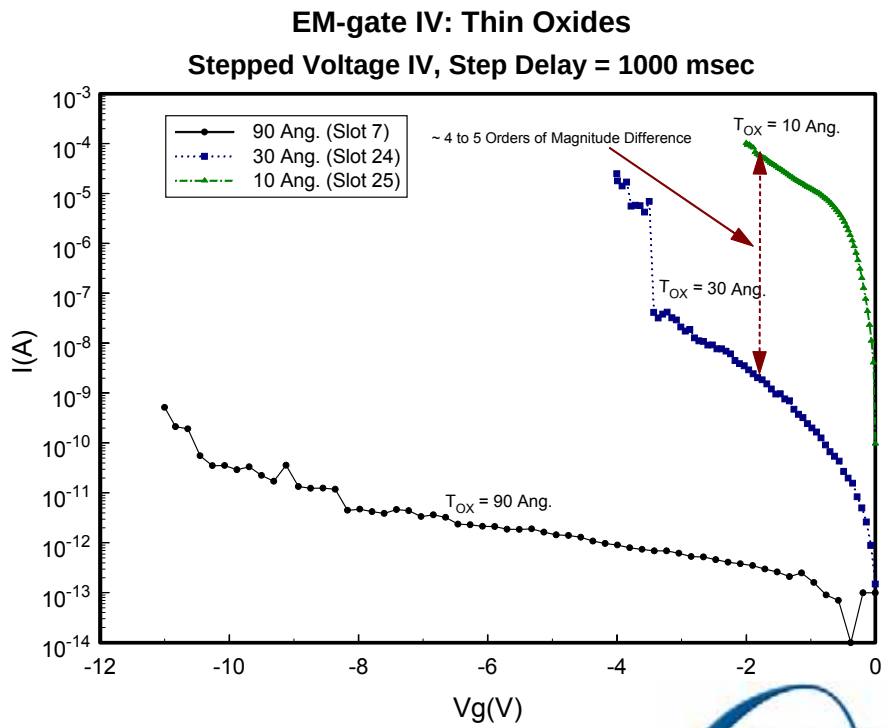


Small contact area provides superior performance for ultra-thin dielectrics

EM-Probe CV and IV: Non-penetrating

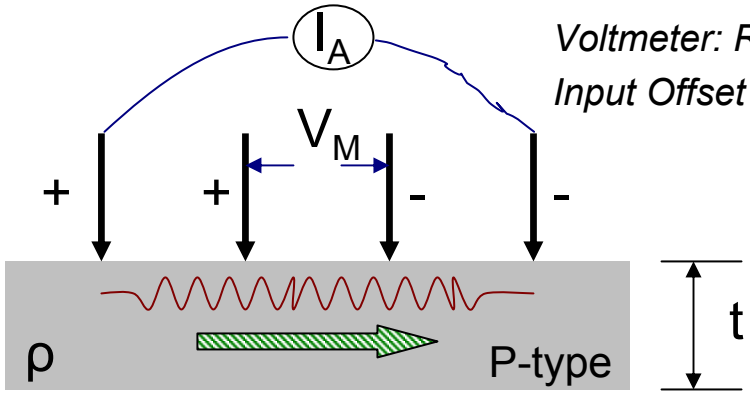
- EM-Probe CV and IV is used extensively to measure dielectrics with thicknesses less than 1 nm.





Basic Principle of Four Point Probe (4pp) Method for R_S

2



Voltmeter: Requires High Z_{IN}, low Input Offset Current

- Semi-Infinite Slab

Resistivity = ρ = $[q\mu p]^{-1}$ = RArea/l

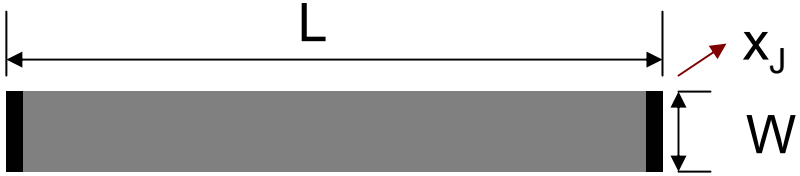
Resistance = V_M/I_A

Sheet Resistance = ρ/t = $CF(V_M/I_A)$; = $[q\mu \int N(x)dx]^{-1}$

Irvin's Curves

For Probes located far from Edge of Circular Sample, CF = 4.532

1

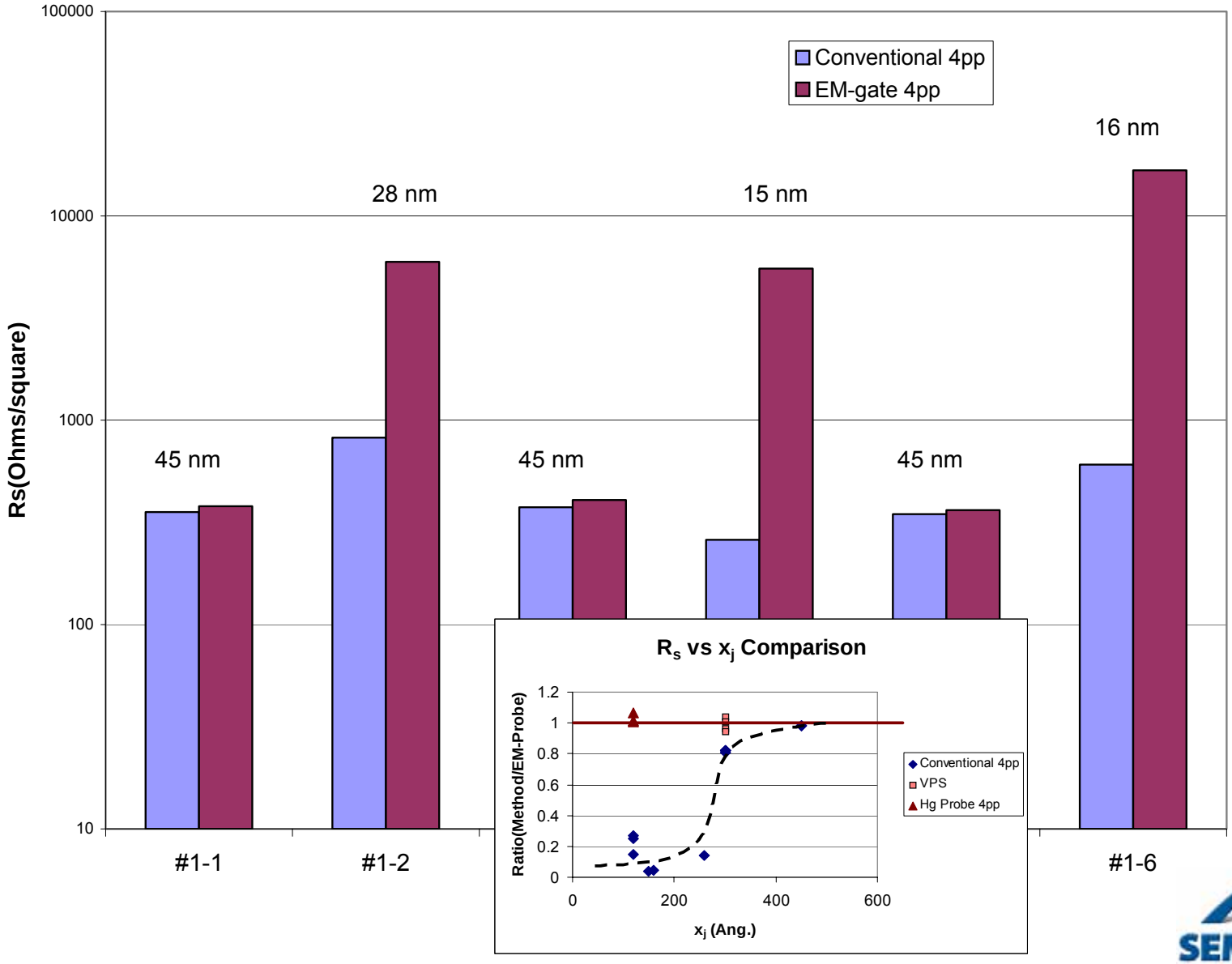


- Defined Structure

$R_S = (V/I)/(L/W)$, Units *Ω/Square*

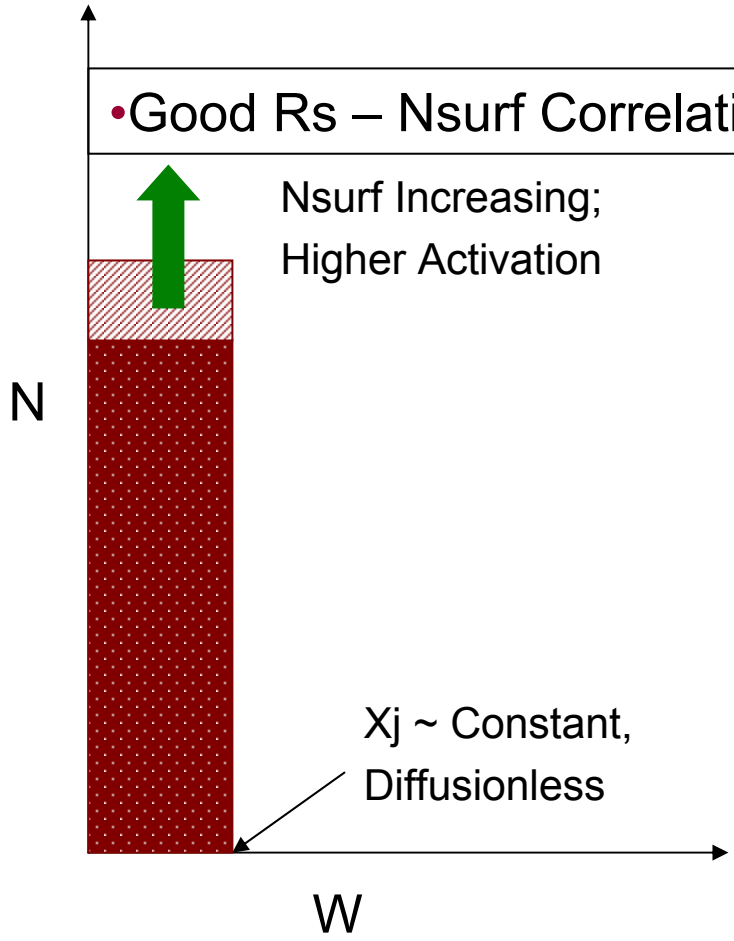
To eliminate Contact Resistance, Kelvin or Transmission Line(TLM) Structures are Used

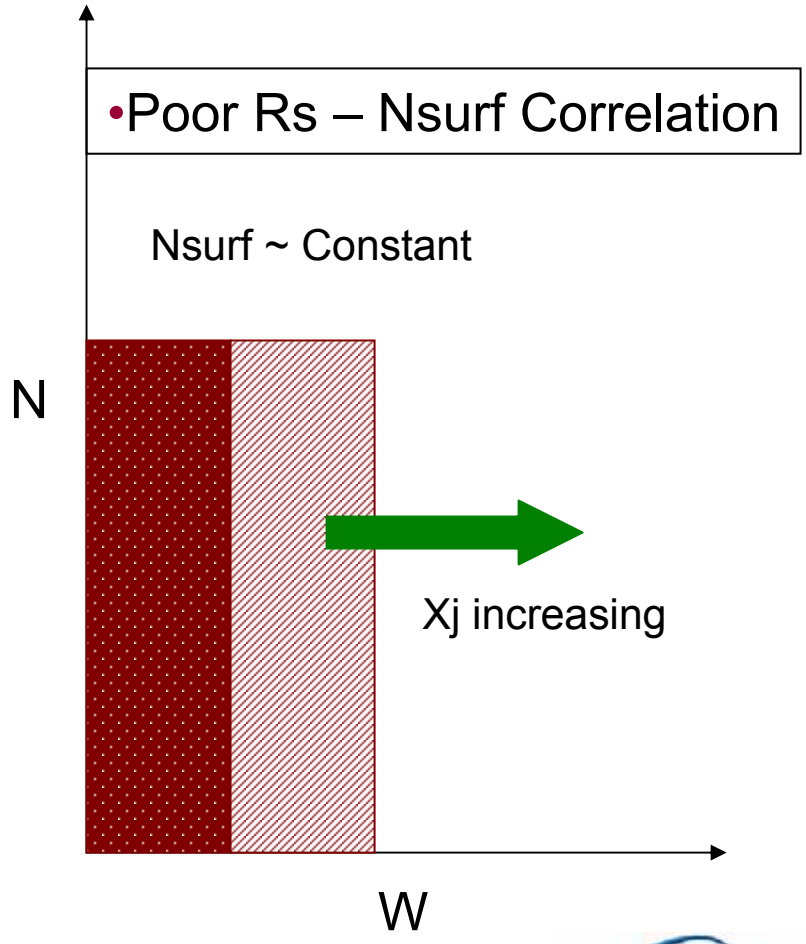
Conventional versus EM-Probe 4pp R_S Case 1: P+ USJ Structures



R_S – N_{SURF} Correlation: General Considerations

- Correlation Depends on Activation and x_J





Summary

- Gate Engineering requires new measurement and analysis techniques
- Channel engineering requires new measurement techniques for in-line metrology
  - Equilibrium Nsurf extends usefulness
- Source-Drain Extensions (USJ) require new measurement techniques
  - Junction leakage requires thought -> Nsurf ?