Metrology and Characterization Challenges for Complex 2.5D and 3D Packaging

Presented by: W. R. Bottoms

Frontiers of Characterization and Metrology for Nanoelectronics

Monterey, California March 21-23, 2017

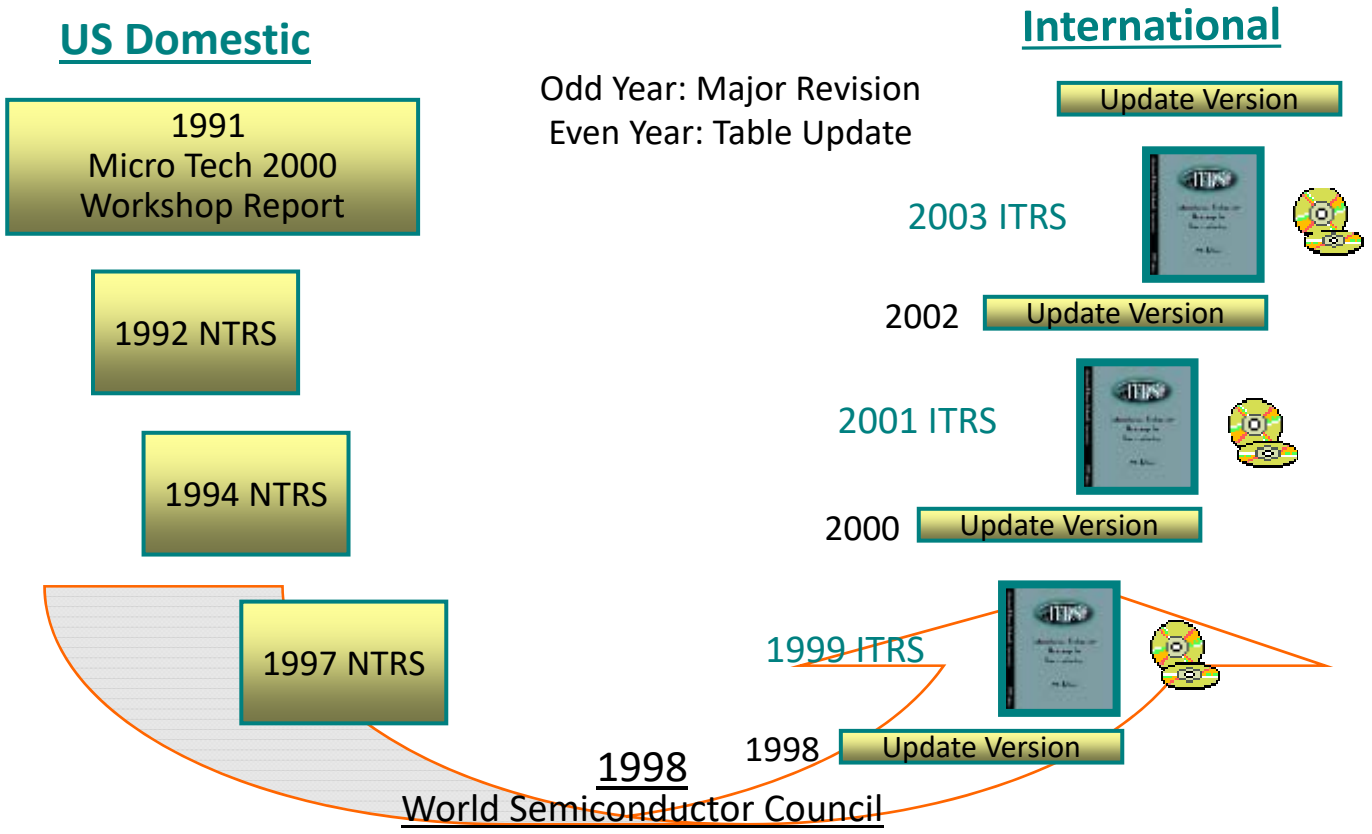
A Brief History of Electronics

Courtesy of John Hunt ASE

The Pace Of Progress Has Accelerated

A Brief History Of Roadmapping

ITRS – a Brief History



ITRS – a Brief History

US Domestic

International

Guided by Moore's Law we knew the challenges well in advance and metrology and characterization tools were available

The path to progress was known, difficult challenges were known and all things were right with the world

1998

World Semiconductor Council

26 years later...

….the world has evolved and is changing in ways never imagined.

Companies in the in the Increasingly Connected World

Source: The Economist, September 17th 2016. Special Report Companies, page 5.

2006 DEC 31st

- Exxon Mobil
- General Electric
- Gazprom
- Microsoft
- Citicorp
- Bank of America
- Royal Dutch Shell
- BP
- Petro China
- HSBC

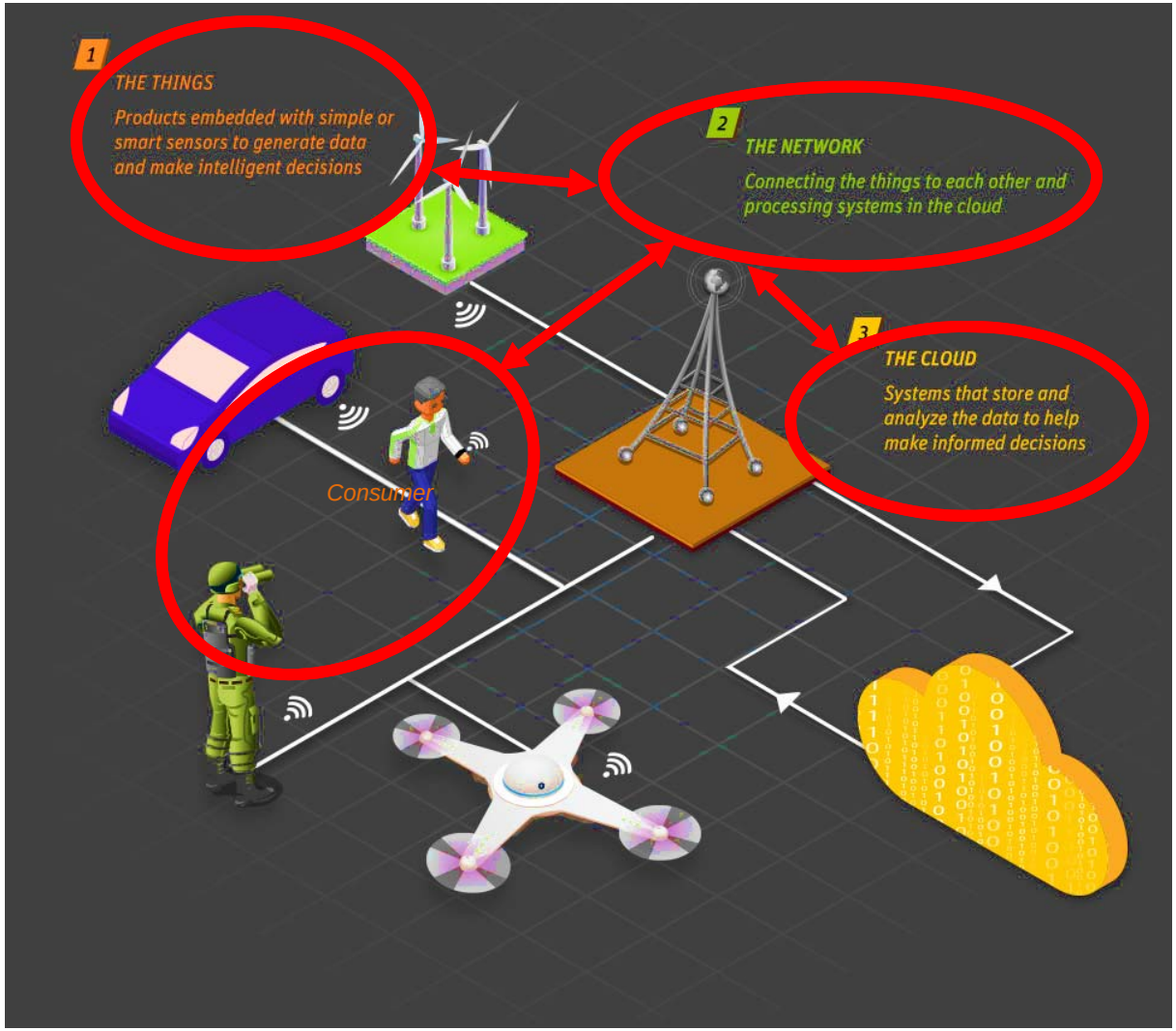
2016 Aug 24th

- Apple
- Alphabet (Google)
- Microsoft
- Berkshire Hathaway
- Exxon Mobile
- Amazon
- Facebook
- Johnson & Johnson
- General Electric
- China Mobile

Four Issues are Driving Change

- ✓ **The approaching end of Moore's Law scaling of CMOS**
- ✓ **Migration of Data, logic and applications to the Cloud**
- ✓ **The rise of the internet of things**
- ✓ **Consumerization of data and data access**

Everything Must Change



Everything Must Change

These 4 driving forces present requirements we cannot satisfy through scaling CMOS

Lower Power, Lower latency, Lower Cost with Higher Performance

We must bring all electronics closer together and interconnect with photonics

This can only be accomplished by Heterogeneous Integration in a 3D-Complex SiP

Performance Requirements To Support This View Of The Future Network

- ✓ **Higher bandwidth density**
- ✓ **Lower latency**
- ✓ **Increased data processing speed**
- ✓ **Expanded data storage**
- ✓ **Ensured reliability**
- ✓ **Improved security**

All at no increase in cost

Performance Requirements To Support This View Of The Future Network

- ✓ **Higher bandwidth density**

Each of these requirements pose difficult packaging challenges

- ✓ **Improved security**

All at no increase in cost

Potential Solutions To Support This View Of The Future

- ✓ Higher bandwidth density

WDM single mode Photonics to the package

- ✓ Lower latency

Flat photonic network- replace tree architecture

- ✓ Increased data processing speed

Increased parallelism- more cores & software to match

- ✓ Expanded data storage

3D memory, new memory devices, hierarchical memory architecture

- ✓ Ensured reliability in a world where transistors wear out

Intelligent redundancy

Continuous test while running

Dynamic self repair

Graceful degradation

- ✓ Improved security while maintaining process speed and latency

Hardware and software combined-distributed over the global network

Major Challenges

- ✓ **Cost**
- ✓ **Power**
- ✓ **Latency**
- ✓ **Bandwidth density**
- ✓ **Thermal management**

We must move things closer together

New Packaging Architectures Needed To Meet Future Market Demand

The End Of The ITRS

-- SIA announced in fall of 2015 that ITRS will be brought to closure with the 2015 Edition. The final ITRS edition was published July 8th 2016.

-- IEEE CPMT Society started planning for the Heterogeneous Integration Roadmap (HIR) Initiative to fill the void in 2015. Discussions ensued with EDS, Photonics, & SEMI to re-invent the Technology Roadmap for today's market & technology needs and look ahead 15 years into the future.

From ITRS to HIR

ITRS:

1991 - 2015

- ✓ Precompetitive
- ✓ 15 years outlook & 25 years for emerging materials & devices
- ✓ Sponsored by five global semiconductor associations. Appoint IRC & approve governance
- ✓ Volunteer driven
- ✓ Free access
- ✓ CMOS "Moore's Law" node driven
- ✓ 17 Technical Working Groups

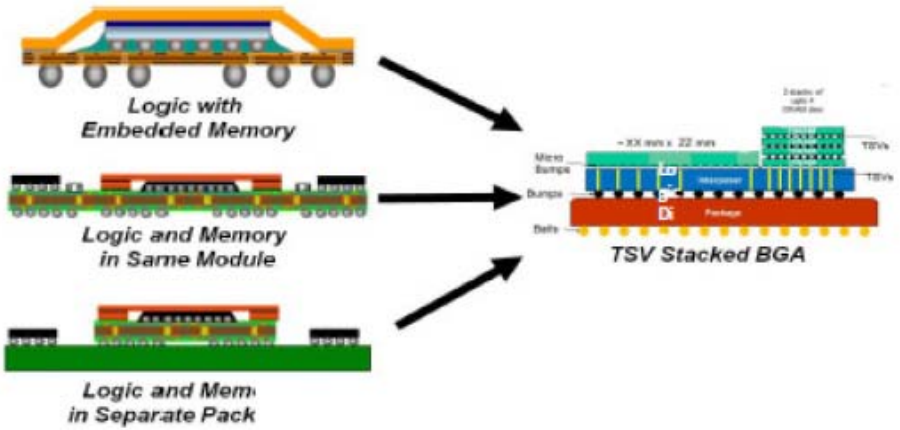
HIR:

2016 --

- ✓ Precompetitive
- ✓ 15 years outlook & 25 years for emerging materials & devices
- ✓ Sponsored by IEEE technical societies & organizations with similar outlook. Appoint IRC & approve governance
- ✓ Volunteer driven
- ✓ Free access
- ✓ Systems & application driven
- ✓ 19 Technical Working Groups

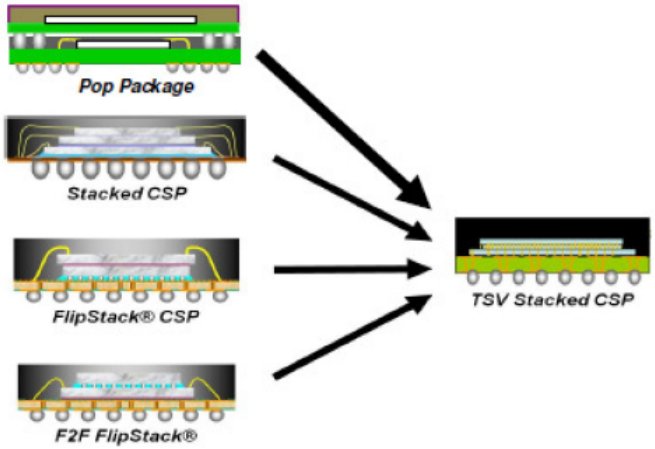
Advantages Of The 2.5D/3D Integration

2.5D Integration Improvement



- 100X improvement in die to die Bandwidth per watt
- Power reduced by 50%
- 5X latency reduction

3D-TSV Integration Further Improvement



- 8X improvement in Bandwidth
- Power reduced by 50%
- Reduced thickness

Source: Amkor

hMoore's Law Era Was Easy For Metrology And Characteriation

The Metrology and Characterization in the Moore's Law era was simple:

- ✓ Features bigger than the wavelength of light
- ✓ Easy access for mechanical test connections
- ✓ Relatively insensitivity to mechanical stress
- ✓ Use of well known and well characterized materials for dielectrics, semiconductors and conductors
- ✓ Equipment and processes were available

There was no fundamental change in this as the first 2.5D technology was introduced. Cost remains the major challenge

2.5D Brought Some New Challenges

As complexity of ICs increased the physical density of bandwidth on chip became a limitation and yield was dropping as the defect density decrease could not keep up with the die area increase. 2.5D was an answer to both problems. It allowed:

- ✓ Very high bandwidth interconnect between die using proven IC design and fab capability
- ✓ Partitioning an IC into multiple pieces to decrease die area and therefore increase yield
- ✓ Equipment and processes were available for manufacturing and characterizing this new interconnect layer.
- ✓ Cost was the biggest limitation.

The new problems were:

- ✓ The circuit we need to measure and characterize does not exist until the multiple die are connected through the interposer
- ✓ TSV structures are expensive and difficult to probe without damage
- ✓ High aspect ratio TSVs often have latent defects that limited reliability (partial voids, etc.)

Solutions to Challenges for 2.5D

Today there are several 2.5D products in production and with more on the way. The limitations have solutions that work but it is still a work on progress.

Cost

- ✓ A "should cost" nalysis of silicon interposers indicates cost less should drop by 50% as volume and competition increase
- ✓ High aspect ratio TSVs can be replaced by using thinned Si a few microns thick rather than hundreds of microns
- ✓ For many applications glass and organic interposers can provide the needed cost reduction and, in some applications, performance improvement
- ✓ Equipment and processes are available for manufacturing and characterizing this new interconnect layer.
- ✓ Interposer yields can be very high and redundancy can replace probing (a few are already doing this)

Solutions to Challenges for 2.5D

Today there are several 2.5D products in production and with more on the way. The limitations have solutions that work but it is still a work on progress.

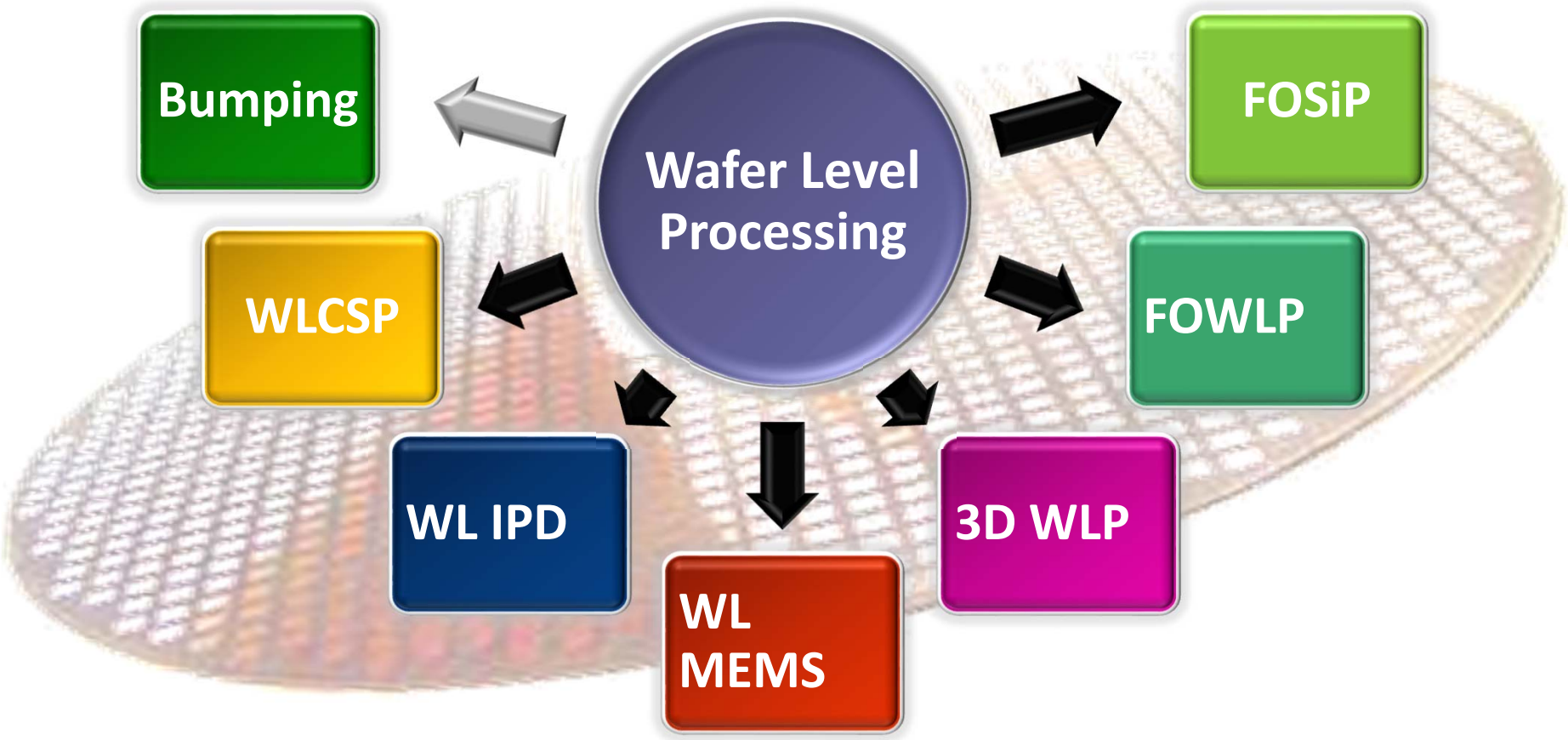
Cost

Wafer Level Packaging provides a lower production cost alternative for both 2.5D and 3D architecture

For many applications glass and organic interposers can provide the needed cost reduction and, in some applications, performance improvement

- ✓ Equipment and processes are available for manufacturing and characterizing this new interconnect layer.
- ✓ Interposer yields can be very high and redundancy can replace probing (a few are already doing this)

WLP Enabled New Package Opportunities

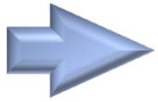


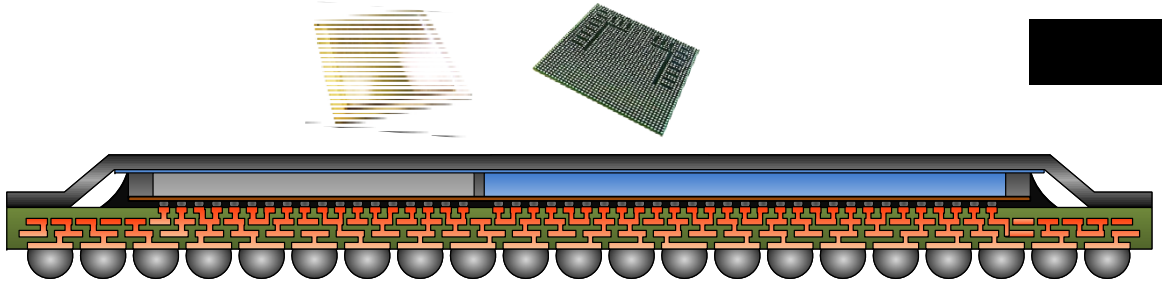
Source: ASE

High Density 2.1D Fanout – 2.5D Alternative

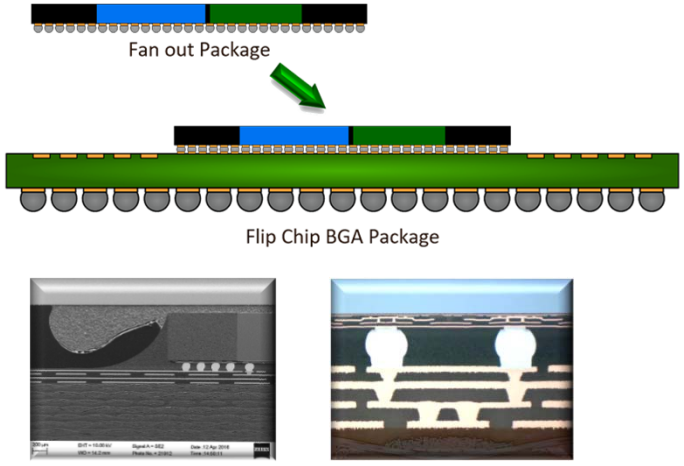
Organic 2.1D Interposer Applications

- APU + Memory
- GPU + Memory
- Network Applications
- SiP/ Modules





FOCoS – Fan Out Chip on Substrate (FO FCBGA)



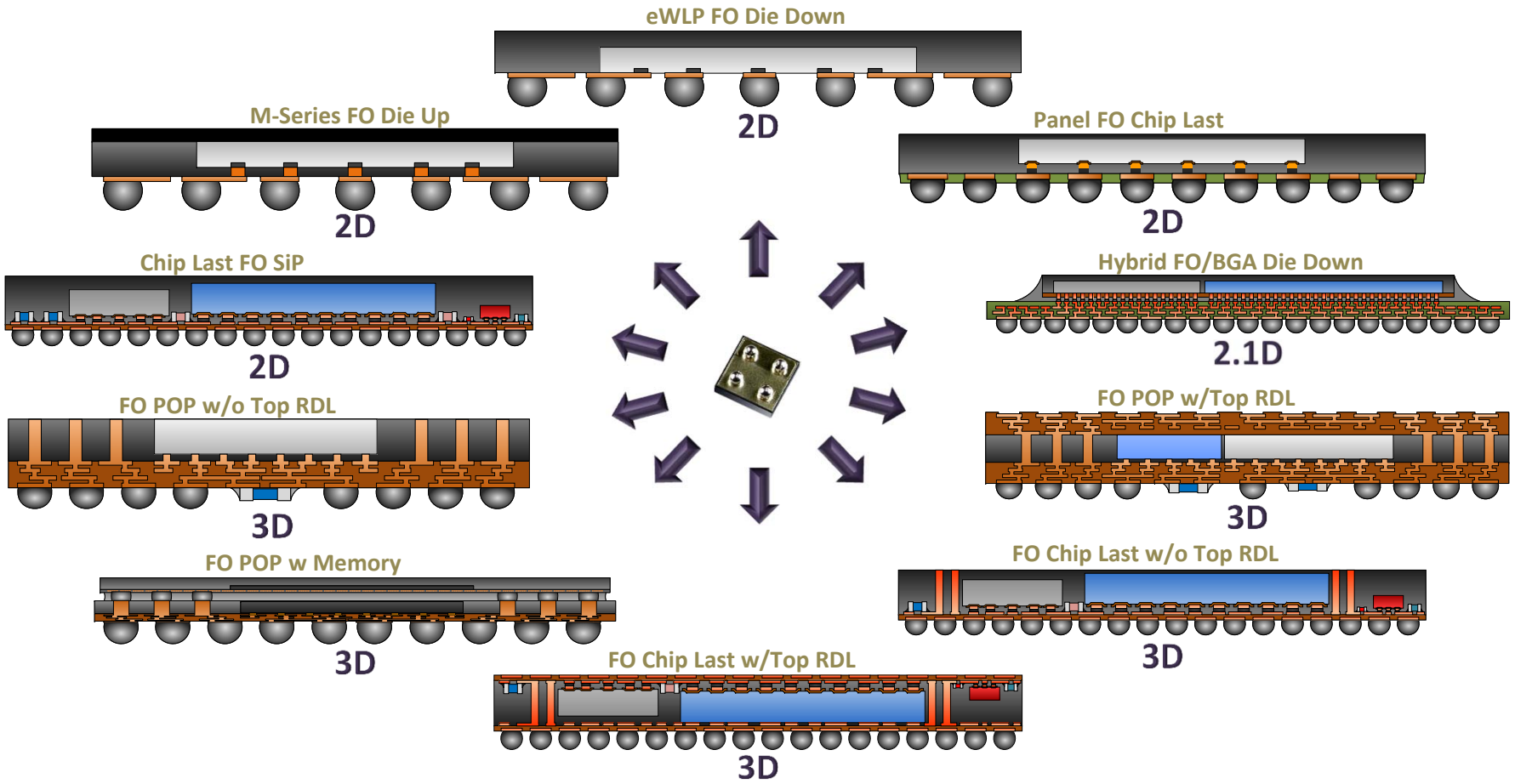
- Hybrid Solution
- Combines HD Fan Out with BGA
- High Density 2D & 3D Interconnection in RDL Layers, no need for interposer
- Multiple Designs In Production

- 2/2.5µm L/S
- 3 RDL Layers + UBM
- 16 & 28nm Die
- 45x45mm Package
- 24x26mm FO

Low Cost Volume Production for more than a Year

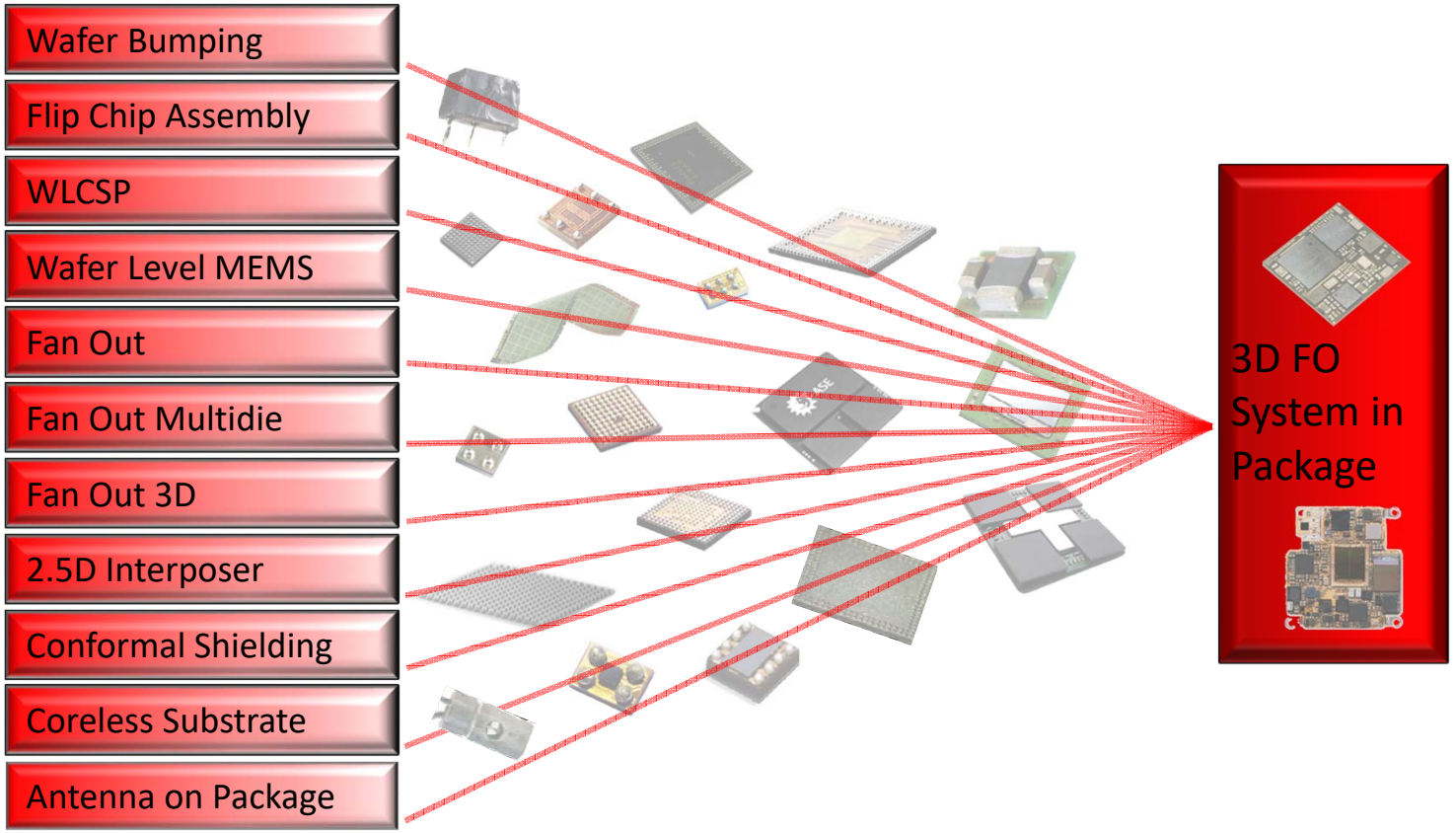
Source: ASE

WLP Fan In to Fan Out – 2D to 3D



Source: ASE

Convergence to 3D SiP



3D Packaging Poses New Difficult challenges

New complexity in measurement and characterization come with 3D driven by the market demand maintaining the pace of progress in size, cost, performance, power requirement and reliability while responding to the consumer demand for ever shorter product life cycles. The issues emerging include:

- ✓ Thermal management
- ✓ Measurement of embedded structures, layer alignment, etc.
- ✓ Test access for electrical characterization
- ✓ Transistors that wear out
- ✓ Power delivery for threshold and sub-threshold voltage operation
- ✓ High yield for handling and processing very thin layers

New materials, new processes and new equipment for production and characterization are required to address these issues.

.

Components Incorporated In 3D Sip

Over the next 15 years components incorporated into 3D packages include:

- ✓ Monolithic integrated photonic ICs (photonics, electronics and plasmonics)
- ✓ Other optical components that are not integrated in the SiPh-ICs.
- ✓ Si based logic and memory ICs
- ✓ MEMS devices
- ✓ Sensors
- ✓ GaN power controller circuits
- ✓ RF circuits
- ✓ Compound semiconductor lasers
- ✓ Optical interconnects to and from the outside world
- ✓ Electrical interconnects to and from the outside world
- ✓ Passive components
- ✓ Embedded passives and actives
- ✓ New devices and new materials that will be developed over next 15 years

Components Incorporated In 3D Sip

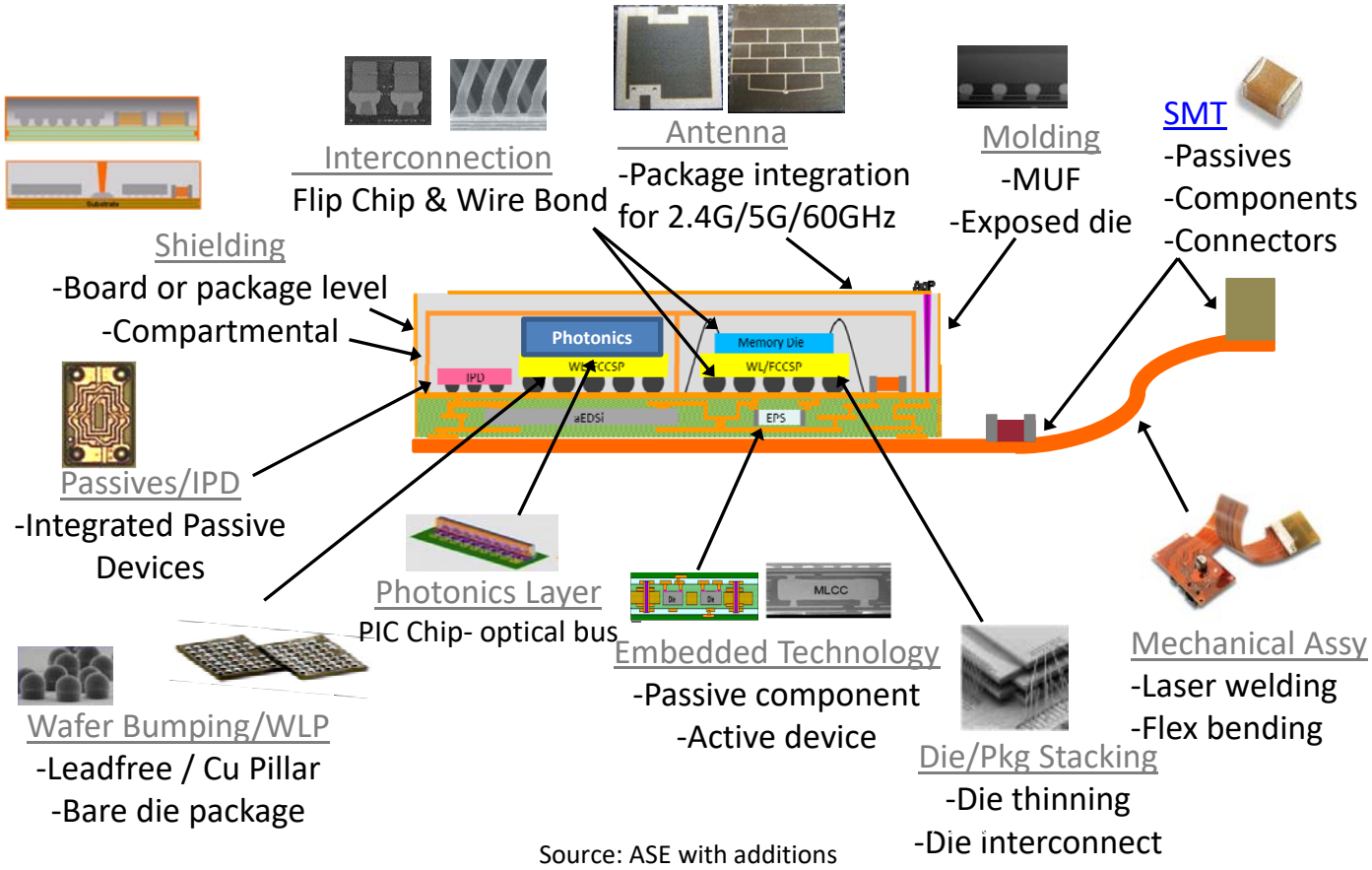
Over the next 15 years components incorporated into 3D packages include:

Each of these has there own packaging requirements for thermal, mechanical, optical and electronic properties that must co-exist in a single package.

This poses many new challenges for metrology and characterization.

- ✓ Passive components
- ✓ Embedded passives and actives
- ✓ New devices and new materials that will be developed over next 15 years

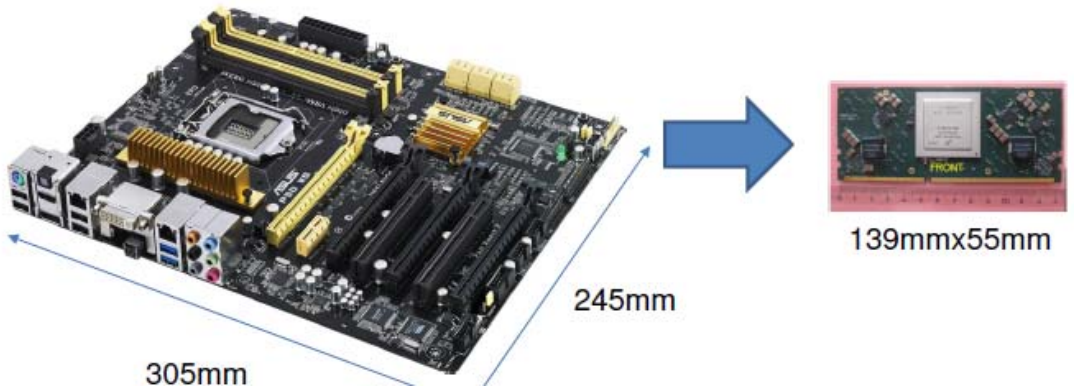
Electronic/Photonic SiP through Heterogeneous Integration



Source: ASE with additions

Micro-server Architecture Can Be Improved With Traditional Packaging

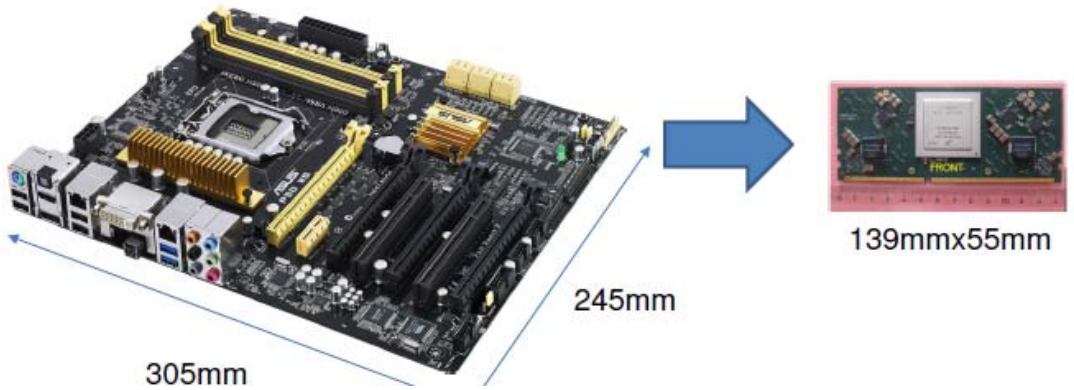
- ✓ The comparison with standard product is dramatic even with conventional PCB assembly and standard off-the-shelf components (Freescale T4240)
- ✓ Small size allows photonics to remain at rack unit edge



Source: Ronald P. Luijten MIT workshop 7/28/2015

Micro-server Architecture Can Be Improved With Traditional Packaging

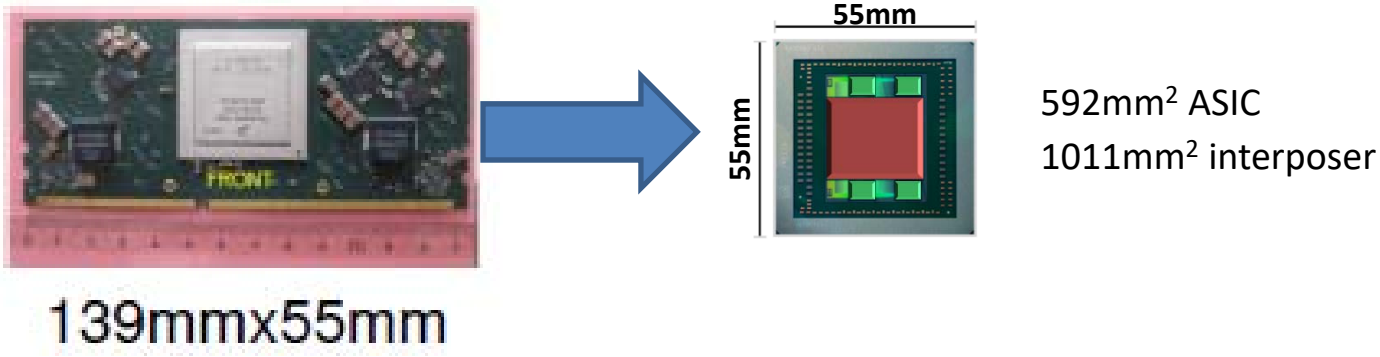
- ✓ The comparison with standard product is dramatic even with conventional PCB assembly and standard
  40% faster with 70% of Intel Xeon E3-1230l
- ✓ **power yields 2X the operations per watt, area reduced by 90% (some memory missing)**



Source: Ronald P. Luijten MIT workshop 7/28/2015

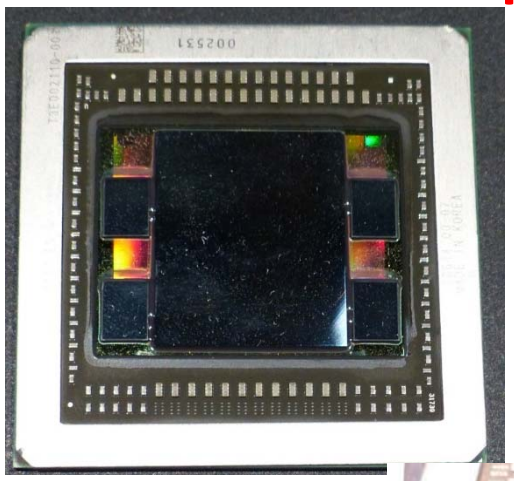
What Could We Do with 3D packaging?

- ✓ 60% smaller with 16Gb high bandwidth memory
- ✓ 4096 bit memory interface
- ✓ 512GB/s memory bandwidth
- ✓ Si interposer with TSV & µbump to package substrate
- ✓ Lower power
- ✓ 22 discrete die plus passive components

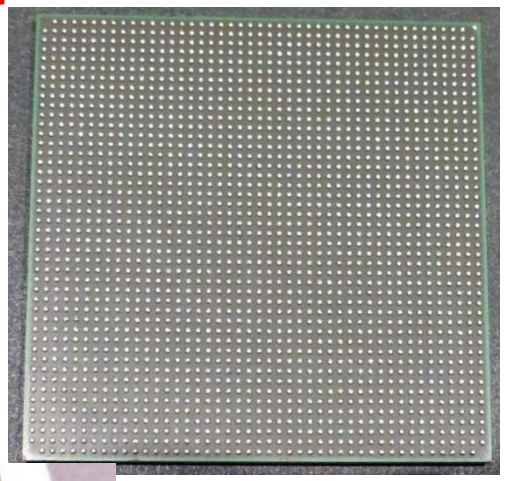


AMD “Fiji”

It’s in production today



Package Top
Cap removed



Package Bottom

Passive Components
Source: Home photography

Adding Photonics To The SiP Is Next

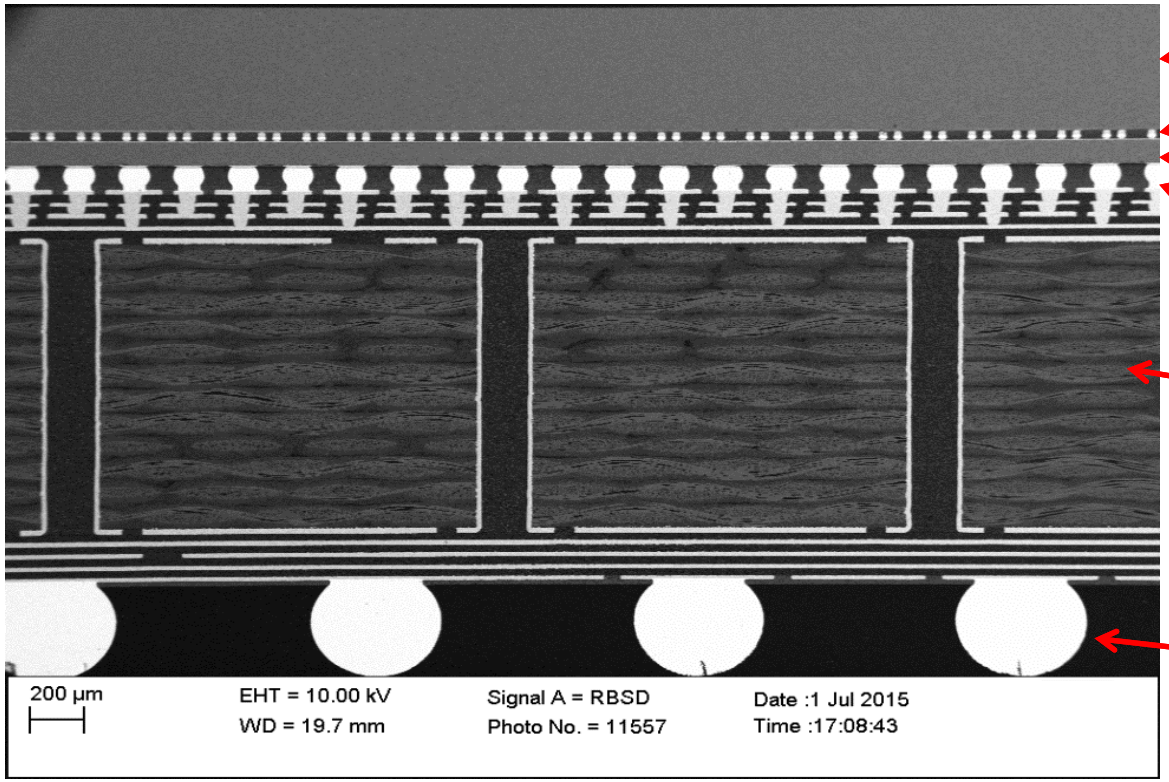
Adding a Silicon photonics chip to the stack would provide:

- ✓ Further reductions in power
- ✓ Further reductions in latency
- ✓ Decrease in total system size
- ✓ Increased physical density of bandwidth

This additional step in heterogeneous integration has difficult challenges including cost reducing silicon photonics, system test and thermal management with high thermal density

Some New Devices Are Here And More Are Coming

Future Interconnect For HI 3D-SiP Is Here Today

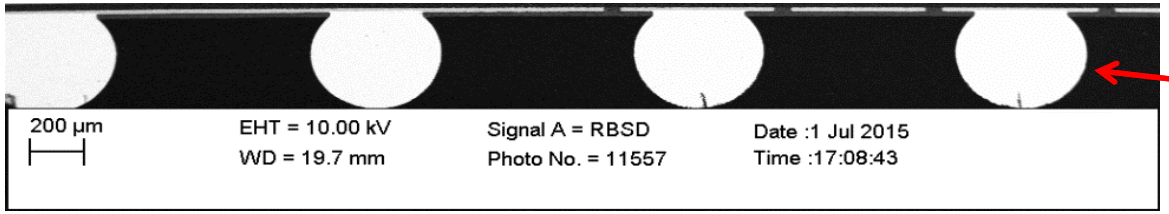


Future Interconnect For HI 3D-SiP Is Here Today

Complex 3D-SiP in volume production with high yield and reliability without known good die while transistors wear out.

Intelligent redundancy, continuous test while running, dynamic self-repair, and graceful degradation.

This has not yet been done with product that includes photonics but it will be during the life of this Roadmap



The Revolution In Packaging The Last 2 Years

Photonic ICs Are In High Volume Production

Intel's Silicon Photonics 100G PSM4 (Parallel Single Mode fiber 4-lane) QSFP28 is ***the first*** small formfactor [illegible]h speed, low power consumption Optical Transceiver.

- ✓ Optical links over single-mode fiber.
- ✓ Applications
  - Connectivity for large scale clou[illegible]nterprise data centers
  - Ethernet switch, router, and [illegible]side telecom interfaces
- ✓ Features
  - Compatibility with [illegible]node fiber connectors
  - Operating temp[illegible] range: 0 to 70°C
  - 3.5 W maxi[illegible]ower dissipation
  - Electric[illegible]ace IEEE 802.3bm
  - Rea[illegible]o 2 km

First Silicon Photonic Integrated Circuit Product

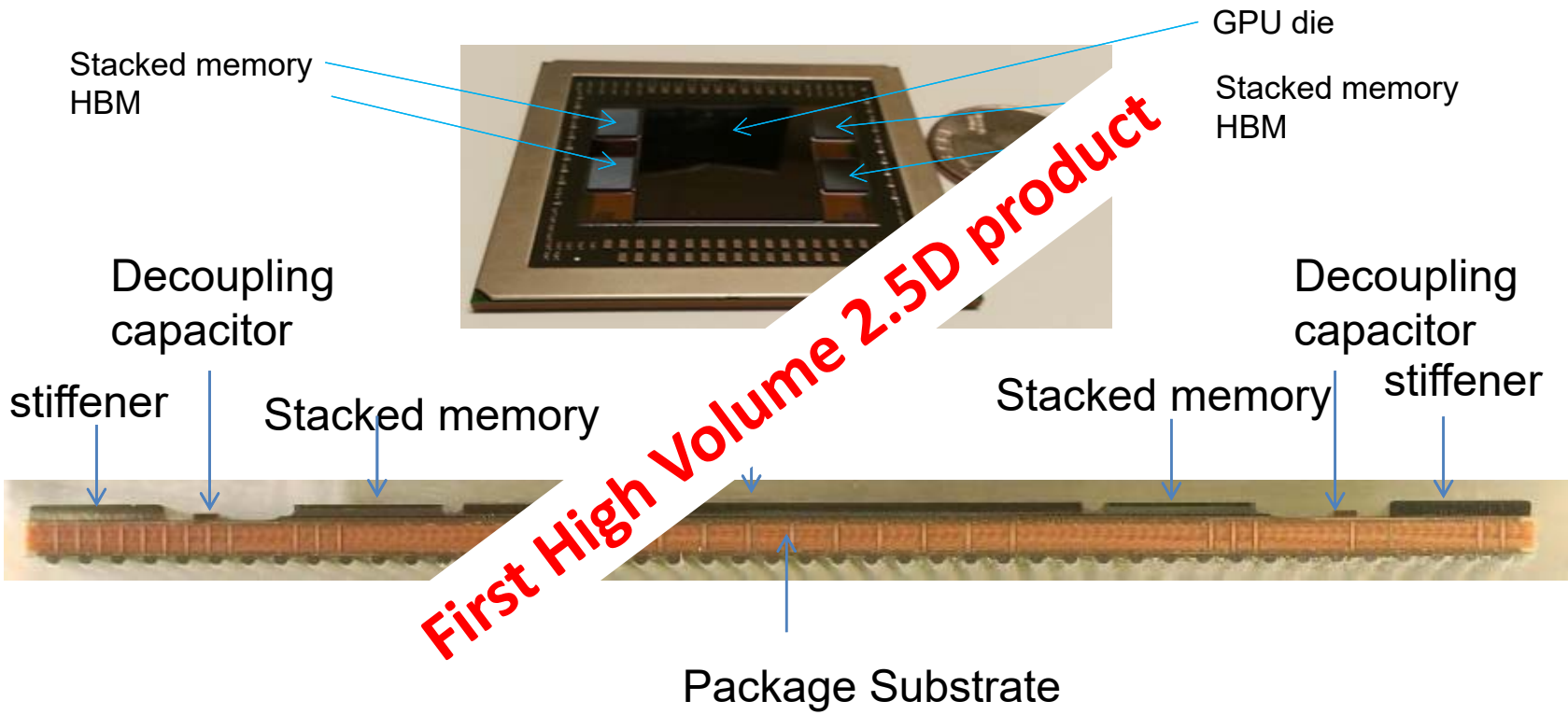
Intel's Product Line Is Moving To 400G And Range Up To 10km

Compliant with CWDM4 MSA or[illegible]al interface specification, with re[illegible]p to 500 m, 2 km, or 10 km depending [illegible]rsion

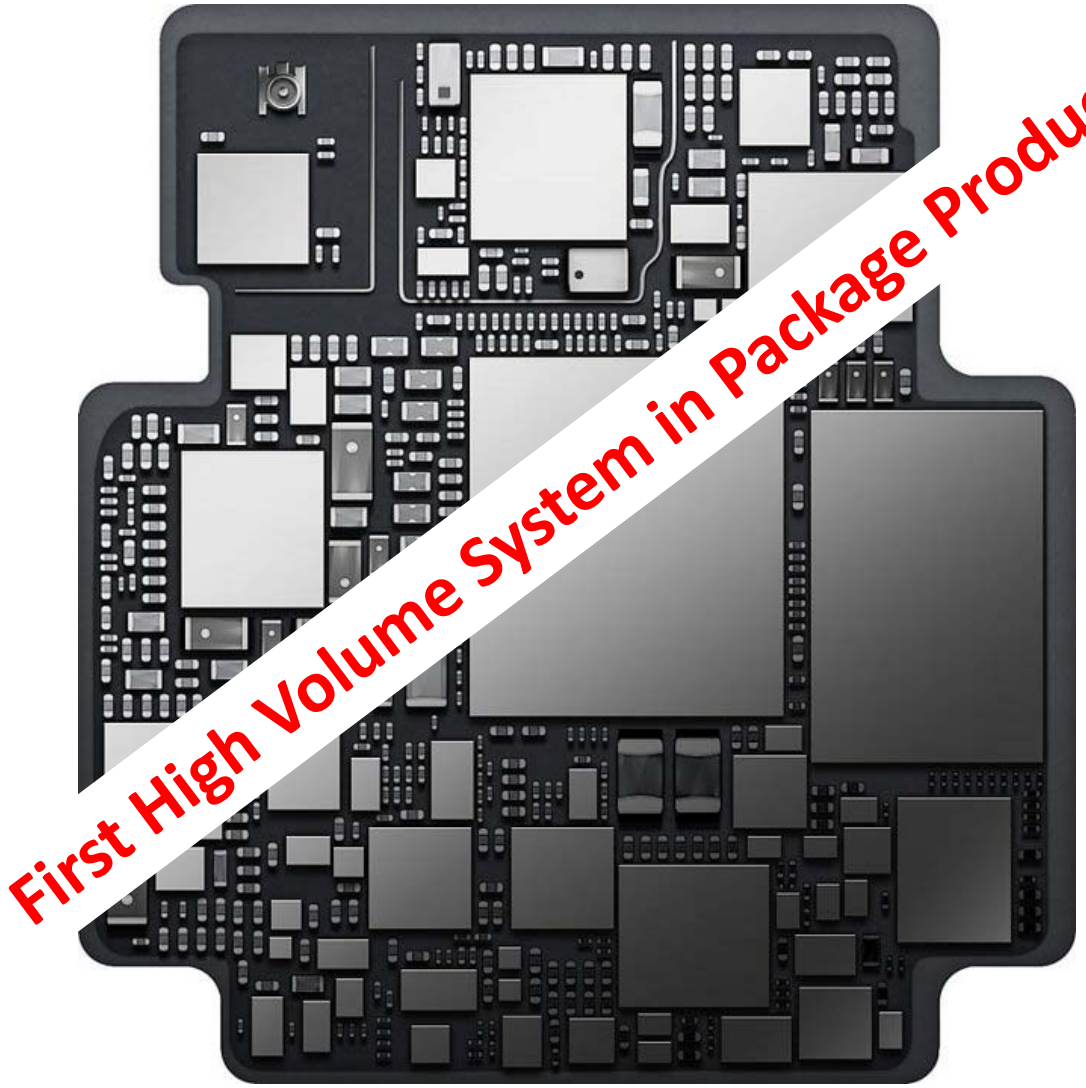
- ✓ CWDM wavelength g[illegible]1271, 1291, 1311, and 1331 nm) for [illegible]led operation
- ✓ Operating tem[illegible]ure range:
  - 2 km and [illegible]n versions: 0 to 70°C
  - 500[illegible]ion: 15 to 55°C

First Silicon Photonic Integrated Circuit Product

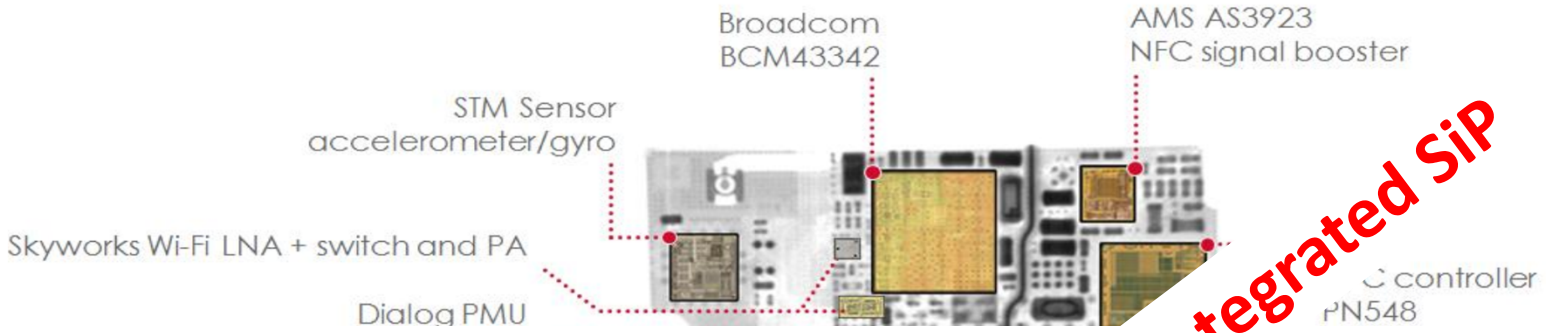
AMD Fiji product



Apple Watch S1 (Heterogeneous) SiP

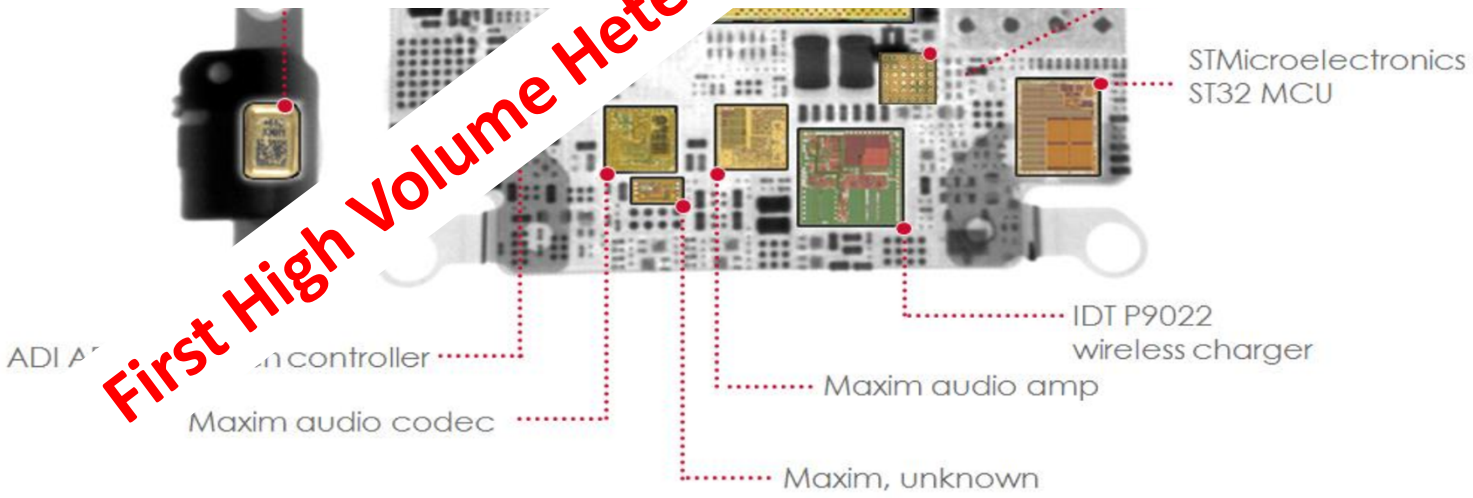


Apple Watch S1 (Heterogeneous) SiP



Complex, high perfo[illegible]ance, low cost and this is i[illegible]ne beginning

First High Volume Heterogeneous Integrated SiP

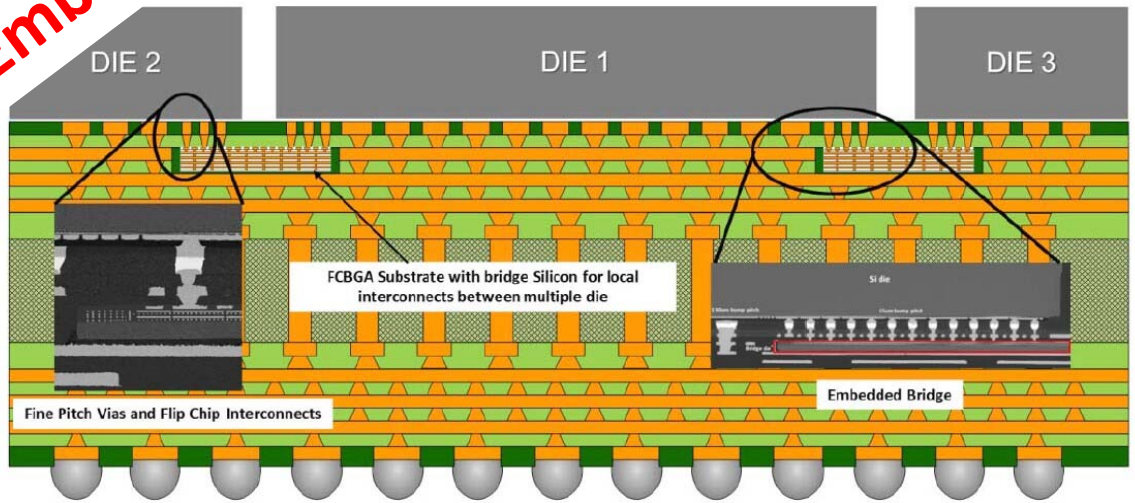


chipworks

Intel Embedded Multi-die Interconnect Bridge

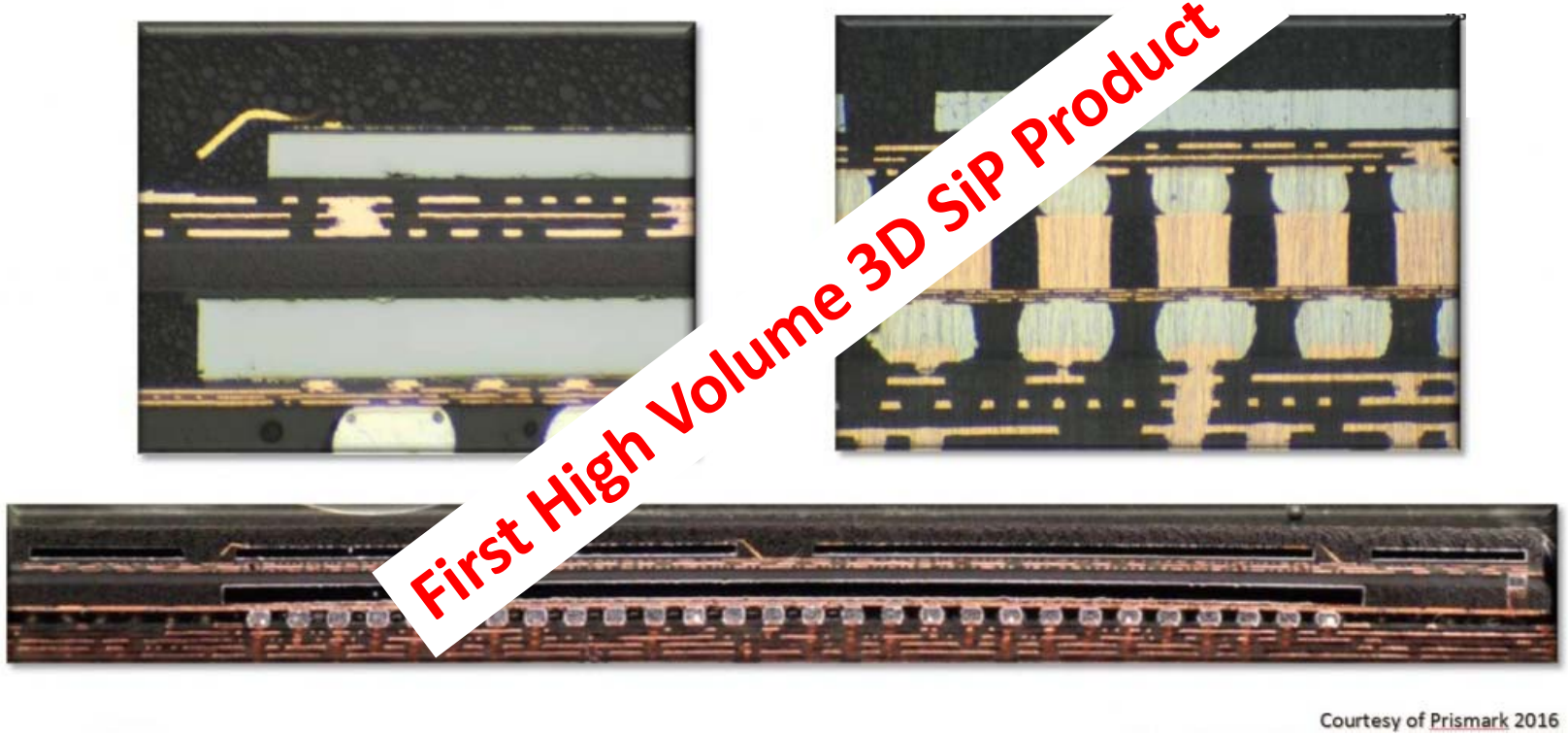
- ✓ EMIB uses thin pieces of silicon (< ...n) containing fine pitch interconn... 2um L/S) embedded in an organic su... e to enable dense die to die interco... between die on the BGA like lamin... ubstrate

First High Volume Embedded Interconnect bridge Product



Apple A10 Fan Out Package

TSMC Info



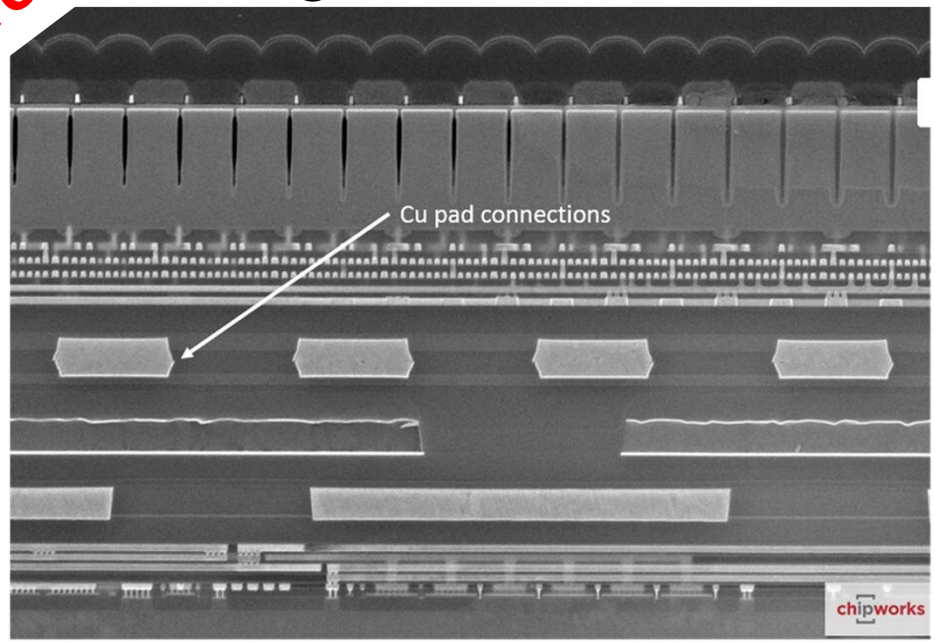
Courtesy of Prismark 2016

Direct Bond Interconnect Is Now In High Volume Production

Samsung's Galaxy S7 is the first high [illegible]me use of of the Ziptronix's DBI te[illegible]logy

- Bonding force is distributed over [illegible]ctric and conductor interfaces
- Near use case temperat[illegible]ocessing
- No under fill requi[illegible]

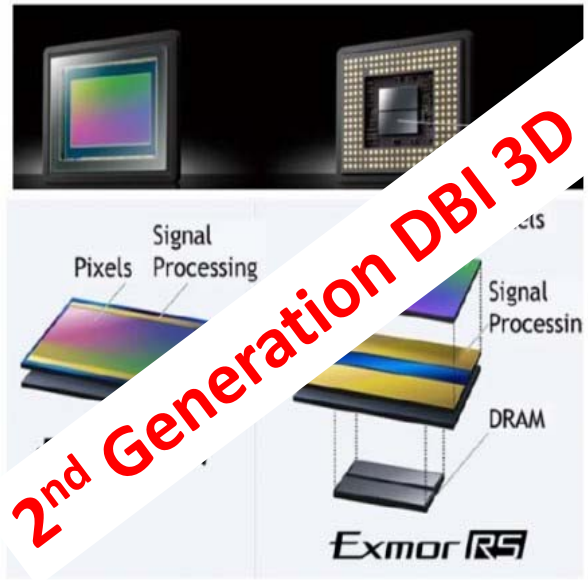
First High Volume DBI 3D process Technology Product



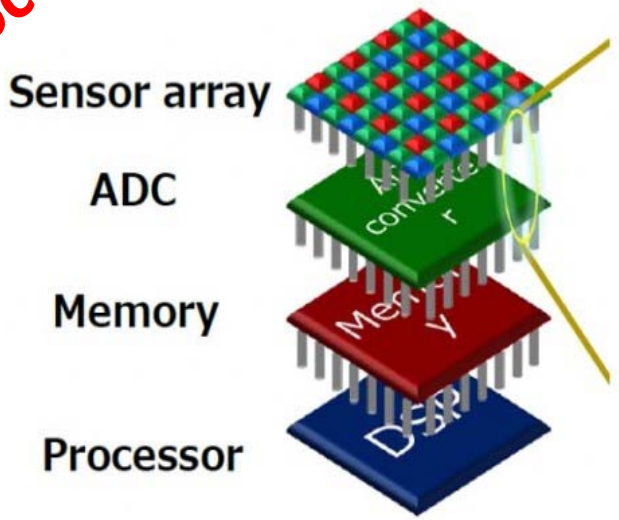
Chipworks cross[illegible] CMOS image sensor shows D[illegible]pper pad connections

Sony DBI Package is in Galaxy S7

Next generation will include stacked me y for 5X speed improvement and is proje o improve future robotics technol nd support robotics manufacturing

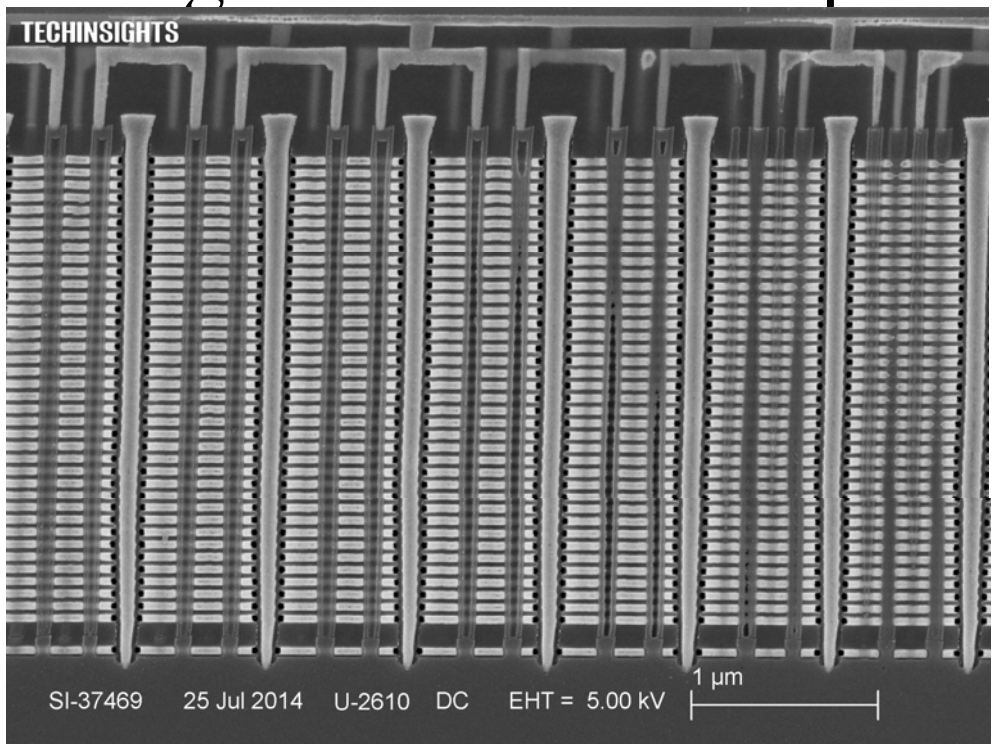


2nd Generation DBI 3D process Technology Product



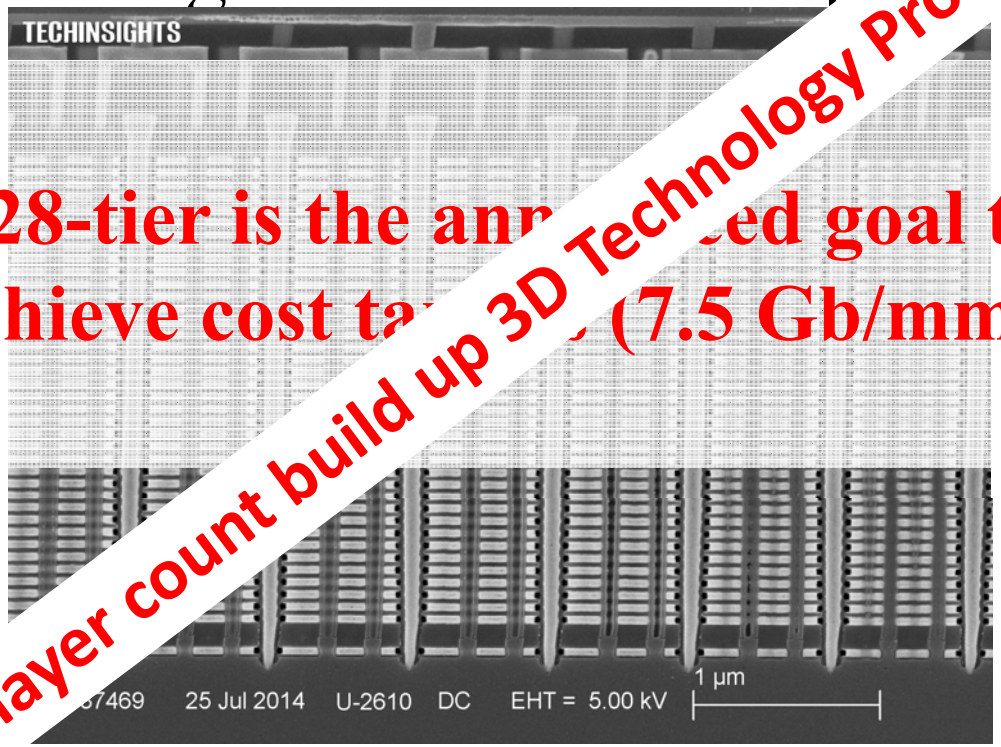
Fabricated 3D Memory
In Production

Samsung's 32-tier NAND product



Fabricated 3D Memory
In Production

Samsung's 32-tier NAND pr[illegible]ct

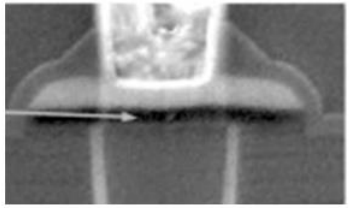


128-tier is the ann[illegible]ed goal to achieve cost ta[illegible] (7.5 Gb/mm²)

High layer count build up 3D Technology Product

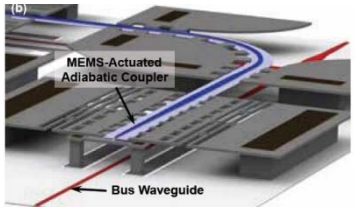
New Device Types Are Coming

These Devices And Their Packaging Will Use New Materials



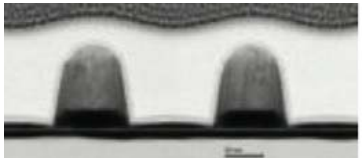
Carbon Nanotube Memory

Tolerant of temp and rad exposure



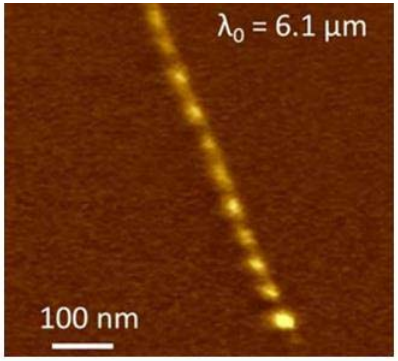
MEMS Photonic switch

Vertical coupler



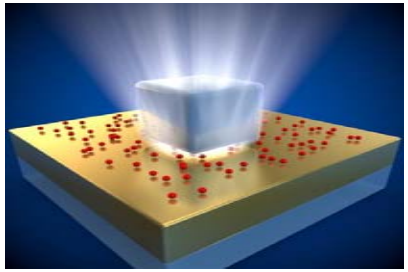
Spin torque devices

(2 magnetic junction pillars)



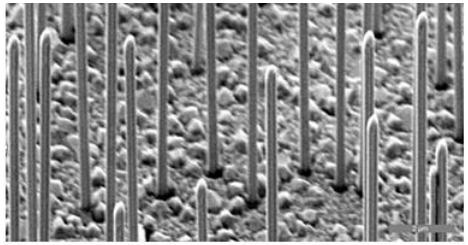
Plasmons in CNT Waveguide

1000 X smaller than photon



Plasmomic emission Source

(quantum dots and plasmons)

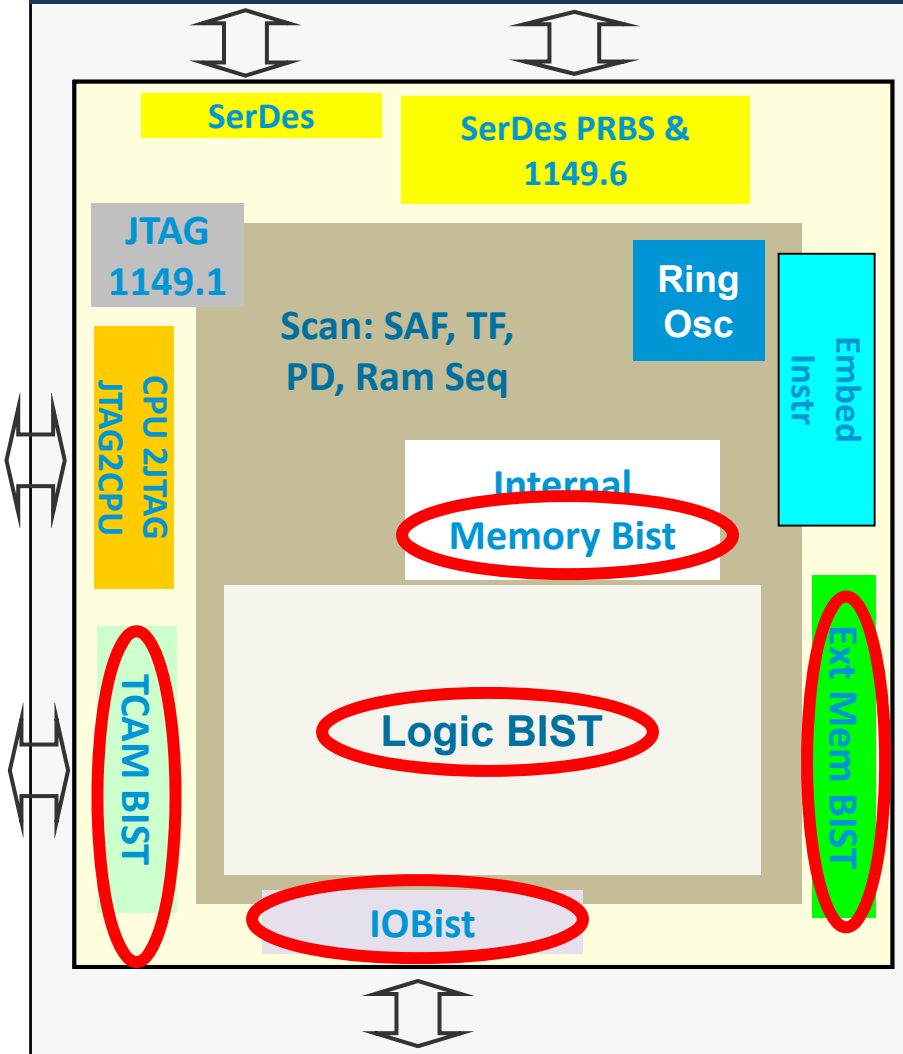


GaAs nanowire lasers

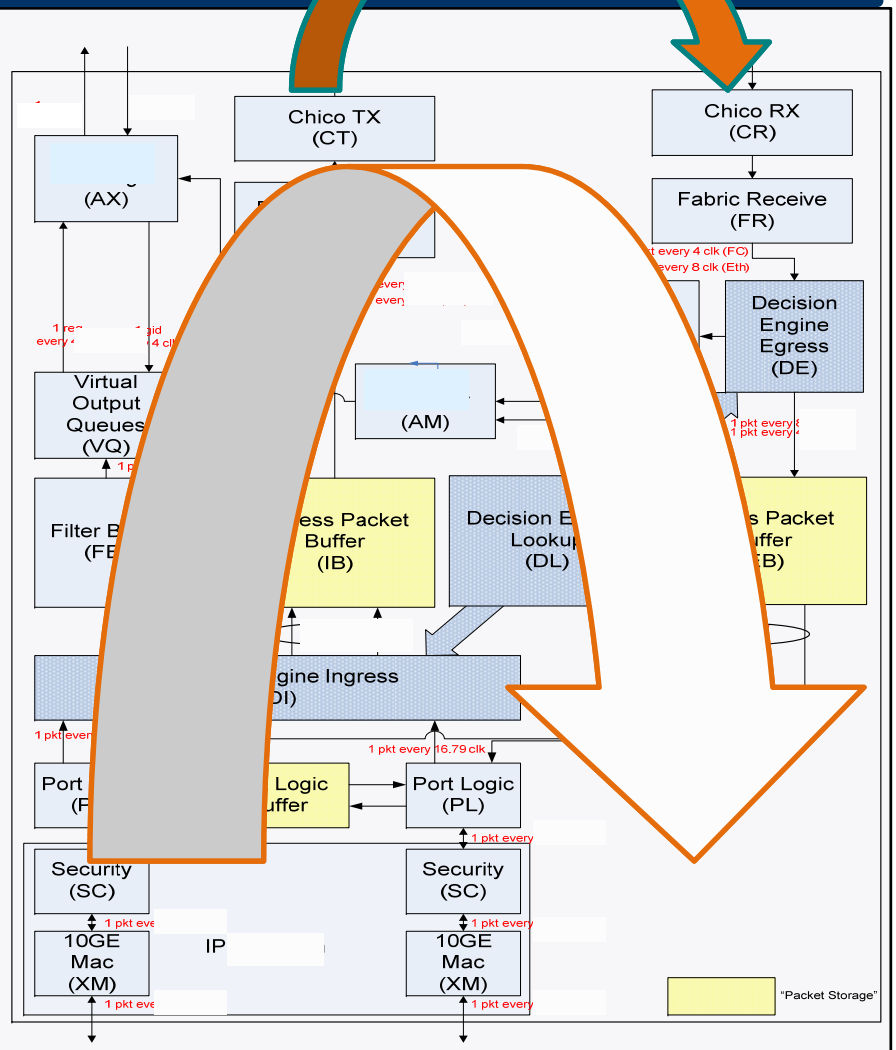
(grown on Si with waveguides embedded)

Ensuring Reliability At Low Cost Requires A Change In Test Strategy

Supplier Testing

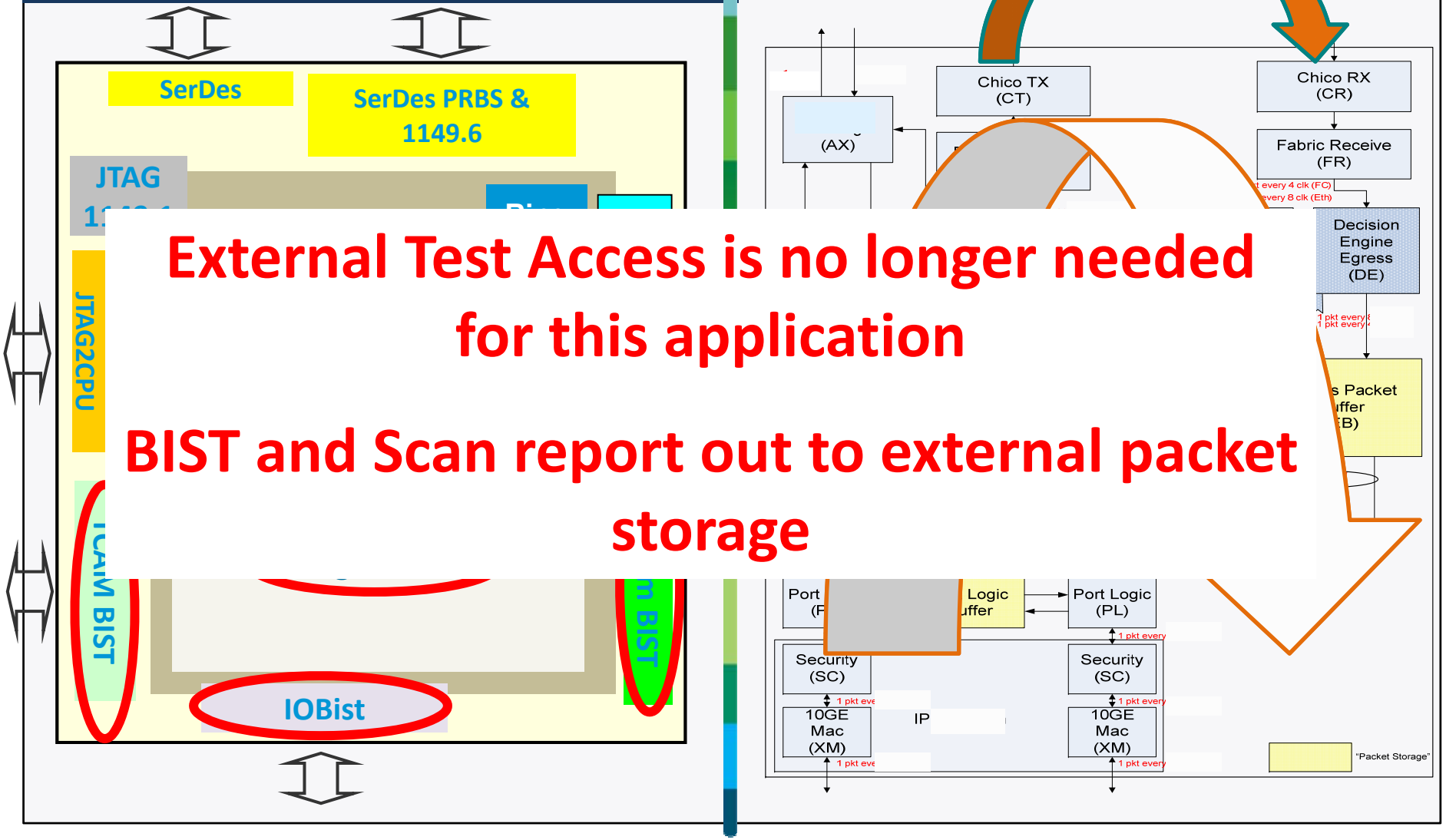


System Traffic Test



Supplier Testing

System Traffic Test



External Test Access is no longer needed for this application

BIST and Scan report out to external packet storage

Summary

The end of Moore's Law scaling has accelerated innovation in new architectures, new materials and new devices.

- ✓ **Atomic level tools that push device development to the limit of the physics are too expensive for use in production.**
- ✓ **2.5D and 3D packaging render many metrology and characterization techniques of the past inadequate.**
  - **Known good die are no longer available and have been replaced by intelligent redundancy and continuous test while running**
  - **Probe cards are being replaced by BIST and Scan techniques.**

We are at the beginning of a transition replacing Moore's Law scaling with new technologies that will enable continued progress for the next 50 years.

Thank You for Your Attention