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Non-destructive USJ characterization using Carrier Illumination™ measurements

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Outline

Description of measurement

- Motivation
- Method

Results on full NMOS and PMOS process flows

- NMOS on blanket and patterned wafers
- PMOS dose matrix
- Extension to PAI implant amorphous layer depth measurement

Gage capability (reproducibility, stability, system matching)

Acknowledgements

The Doping Group at International Sematech, under the direction of Dr. Larry Larson, including Dr. Billy Covington, Dr. David Sing, Clarence Ferguson, Dr. Bob Murto and Billy Nguyen

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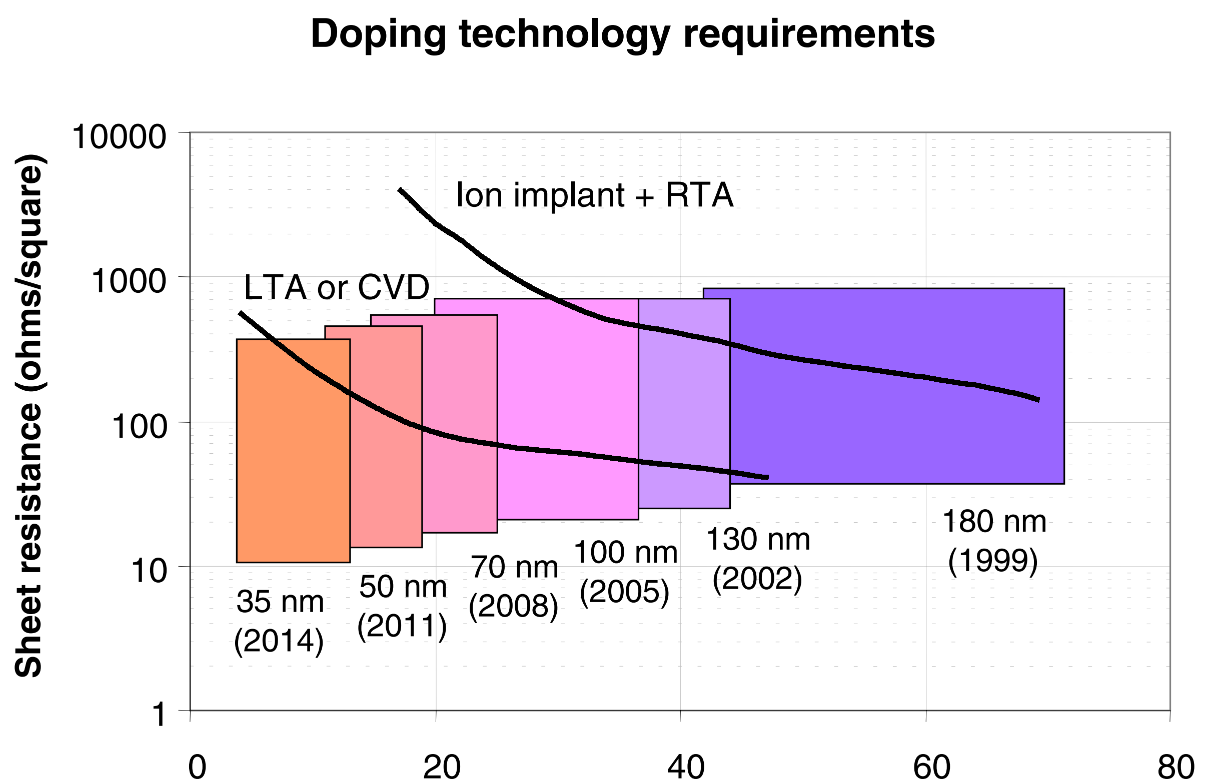
Drs. Jon Kluth and Bob Ogle of AMD SDC

Dr. Wilfried Vander Voorst, IMEC

The Development and Applications Groups at Boxer Cross Inc

Source/Drain layers test limits of doping technology



Source: ITRS'99

USJ processes will be limited to a very narrow process window for depth, active dose, and uniformity

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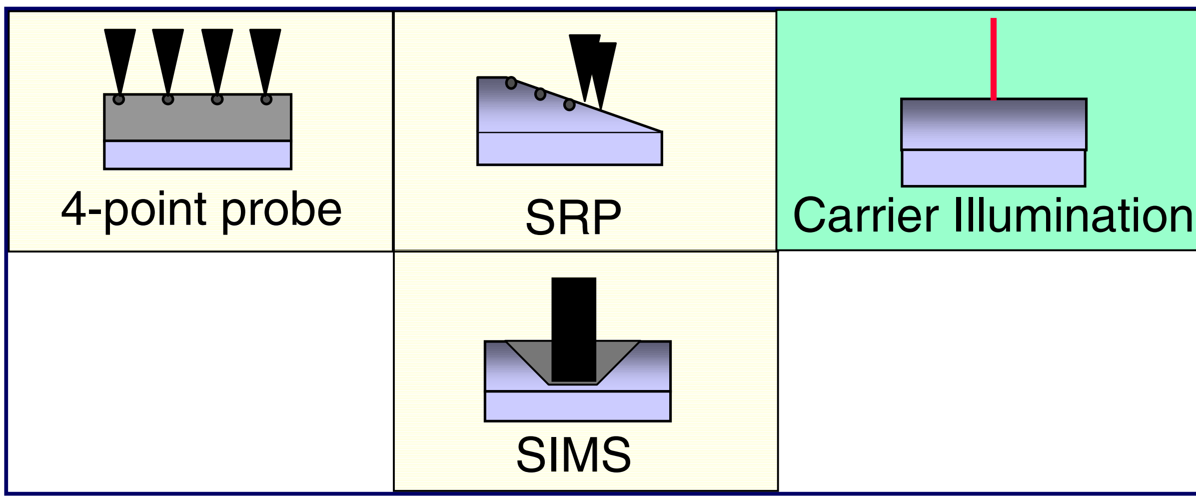
Metrology gap for activated shallow junctions

Measures:	Dose	Profile	Depth, dose
Need	All nodes	<250 nm	<180 nm
Where used:	In-fab	Analysis lab	In fab



Carrier Illumination (CI) measurement shortens control loop to tighten process control

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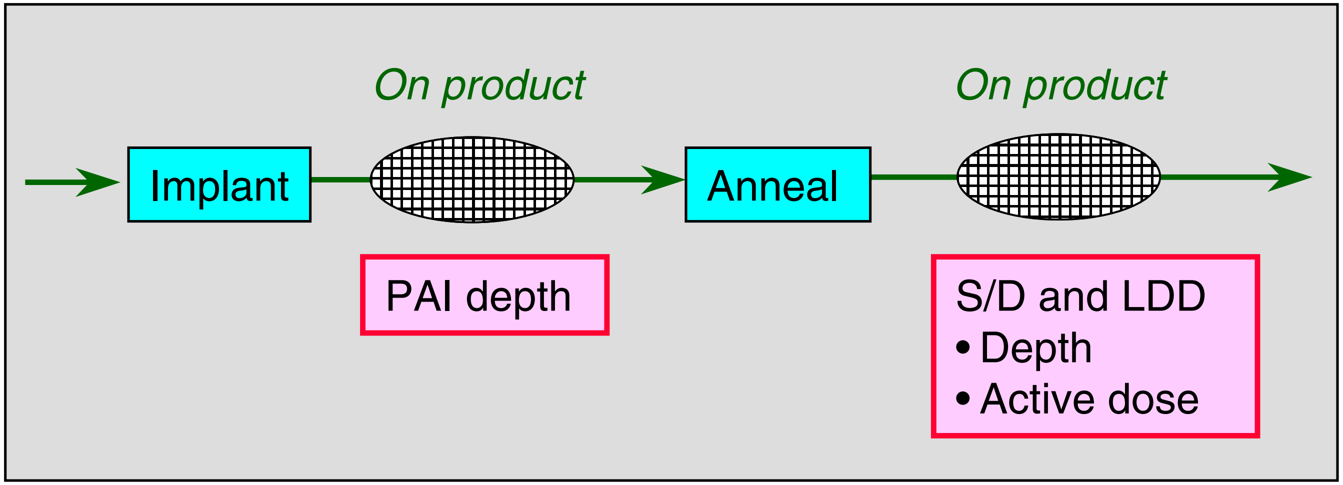
Characterize Source/Drain processes in the fab



- 2 μm spot size, nondestructive measurement for use on product
- Short measurement time allows high throughput, uniformity mapping

Aim: In-line characterization and control of USJ processes

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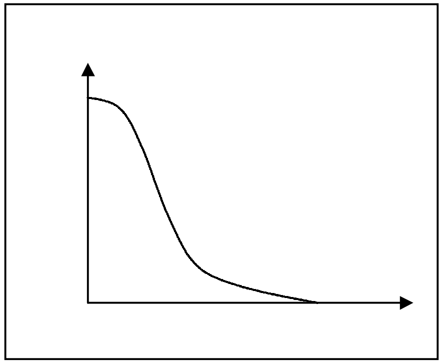
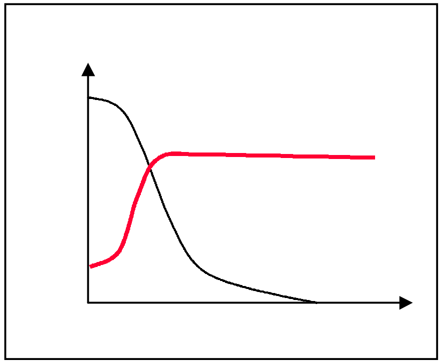
Carrier Illumination™ method - adding contrast to see the invisible



+ carriers



Optically generated carriers make transparent junction visible

Quasi-static measurement obtains high signal-to-noise ratio

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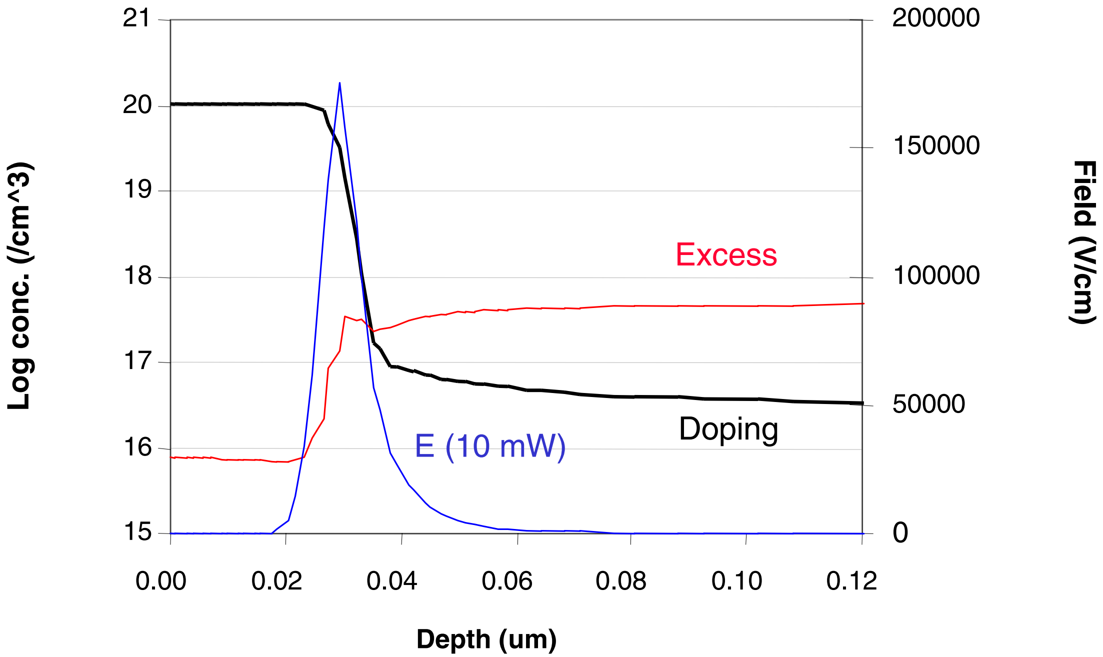
Simulation shows excess carriers build-up at junction



Steep rise in excess carrier concentration at junction edge.

Reflection signal comes mainly from this region, where gradient is largest.

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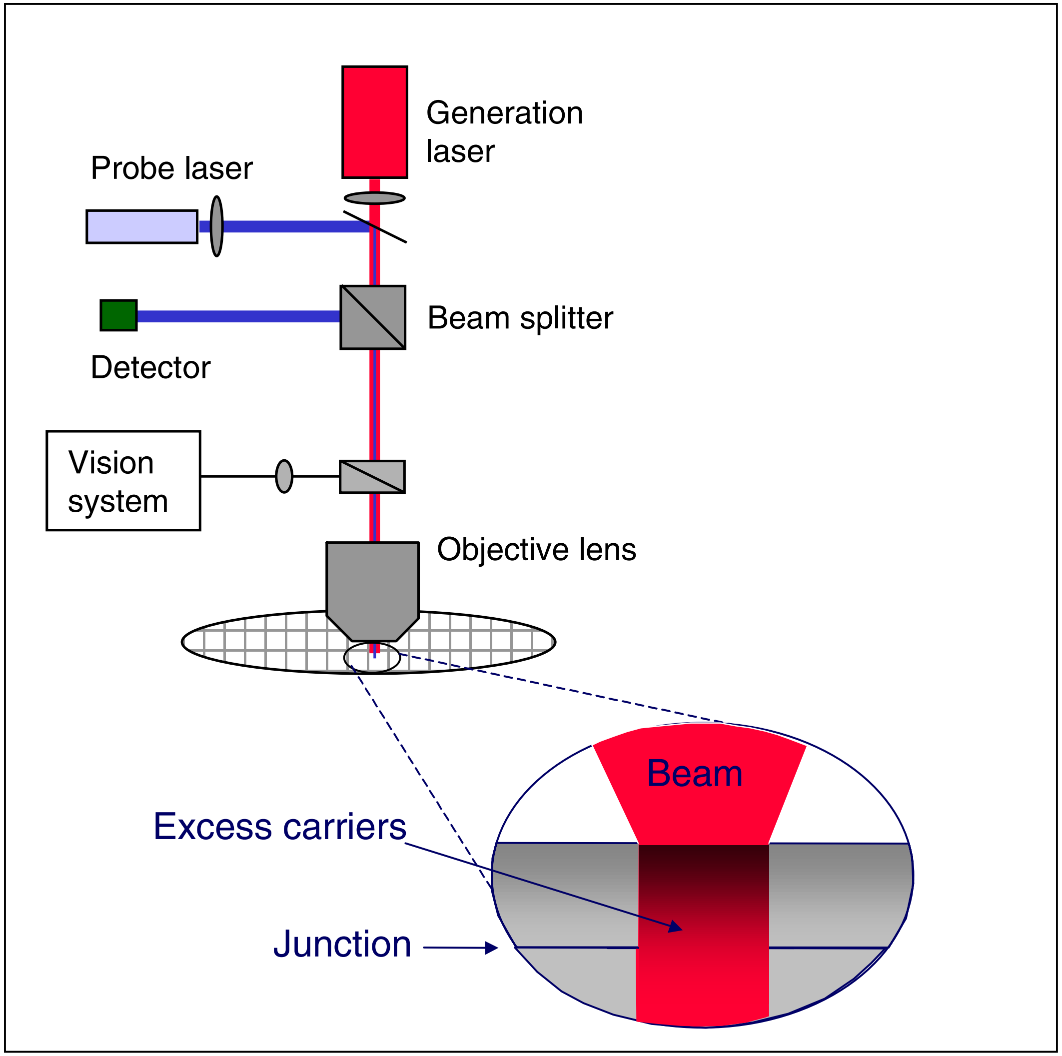
Non-contact measurement system



- Red laser induces excess carriers
- IR laser is used to measure wafer reflectance
- DC carrier distribution deduced from reflectance signal
- Patents issued and pending

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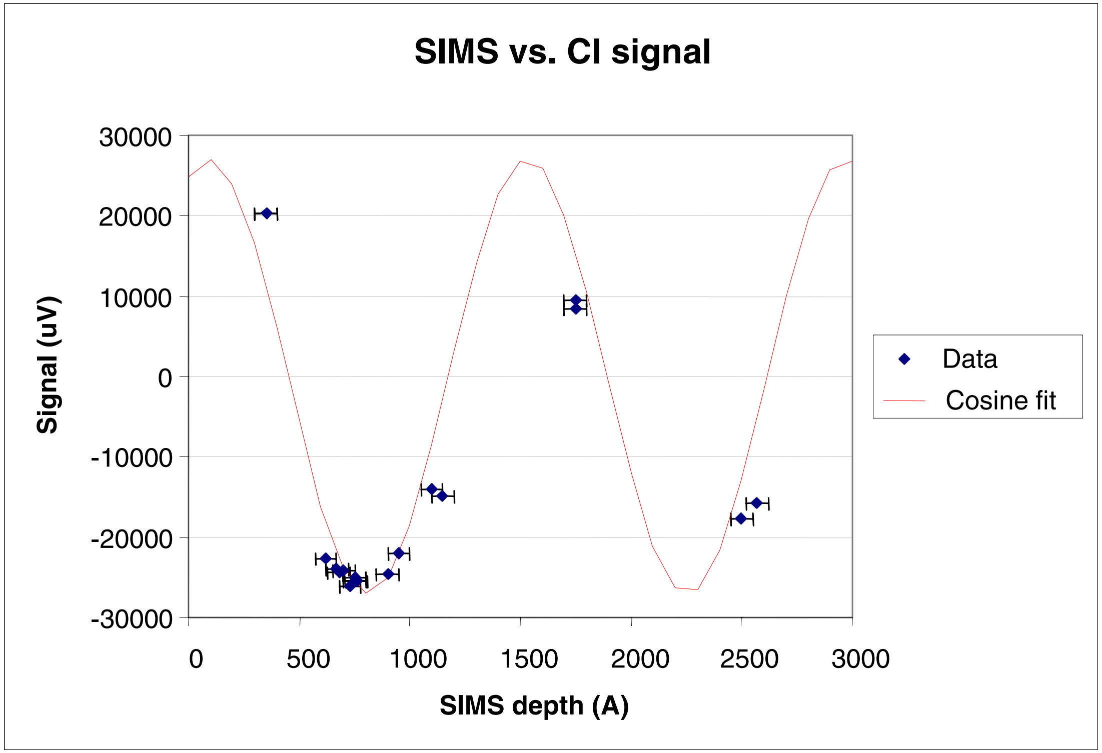
Measurement matches theory: As implants



1e16/cm^2 25 keV As

Annealed 950 to 1100 C

Source: Sematech.

Following theory, data fits cosine using 980 nm laser wavelength

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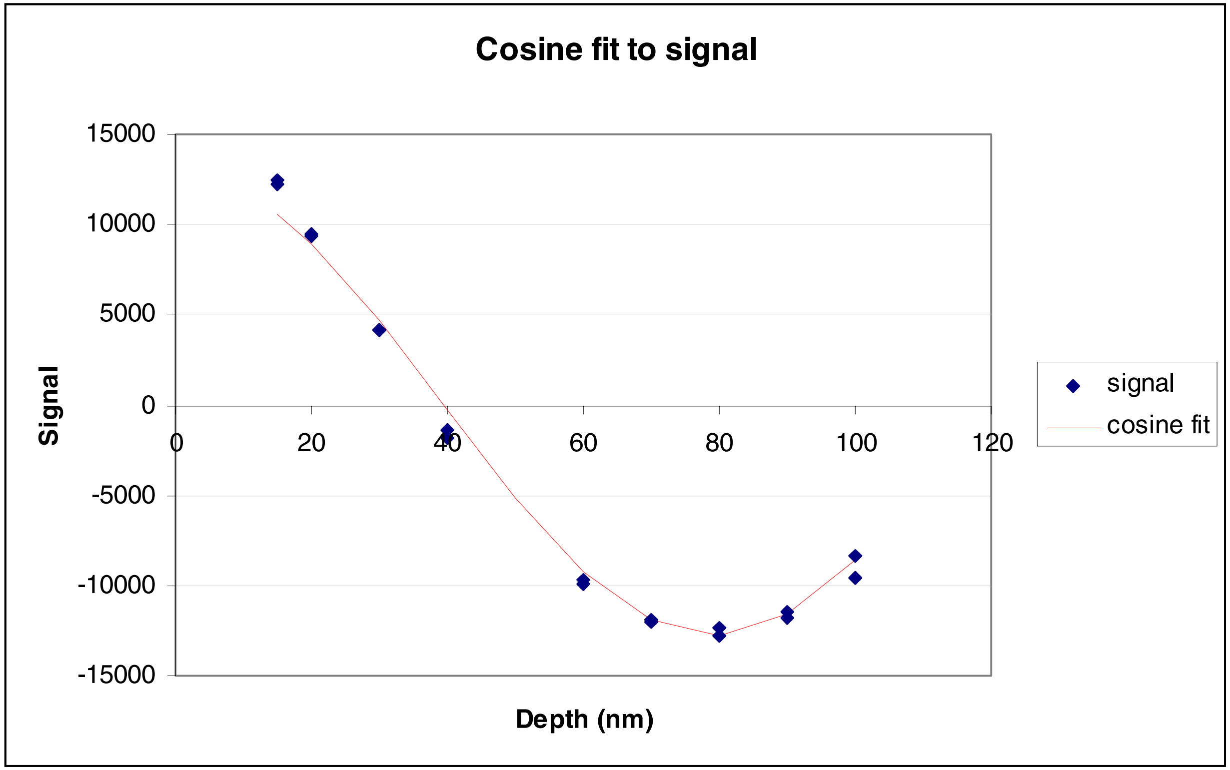
Measurement matches theory: B doped CVD Si layers



Source: IMEC, Sematech and Boxer Cross

CVD layers form well defined, box-like junctions of known depth.
Signal follows cosine fit predicted by theory to <20 nm.

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Characterization experiments

- As Source/Drain optimization, energy matrix
- As LDD optimization, retained dose matrix (180 nm NMOS)
- As Source/Drain DOE: energy, dose, anneal time, temp (patterns)
- B LDD optimization, implanted dose matrix
- Ge and Si PAI layers
- Gage study

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As S/D implants vs. energy with and without p-well

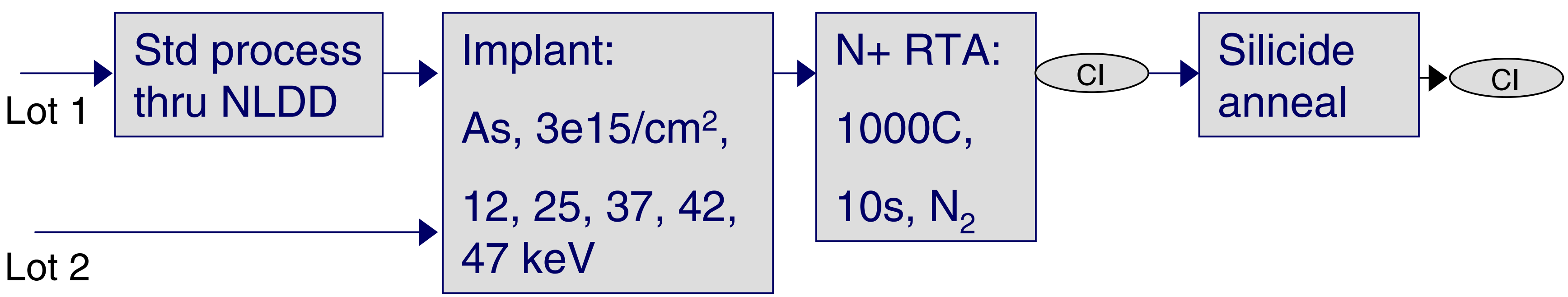
Depth trends as expected with energy, correlates to SIMS

DOE trends correlate to probing of test structures

P-well appears to have minimal effect

Found four mis-implanted wafers

- High CI signal indicates bad implant, not missed RTA
- Confirmed with re-anneal + 4-point probe and SIMS



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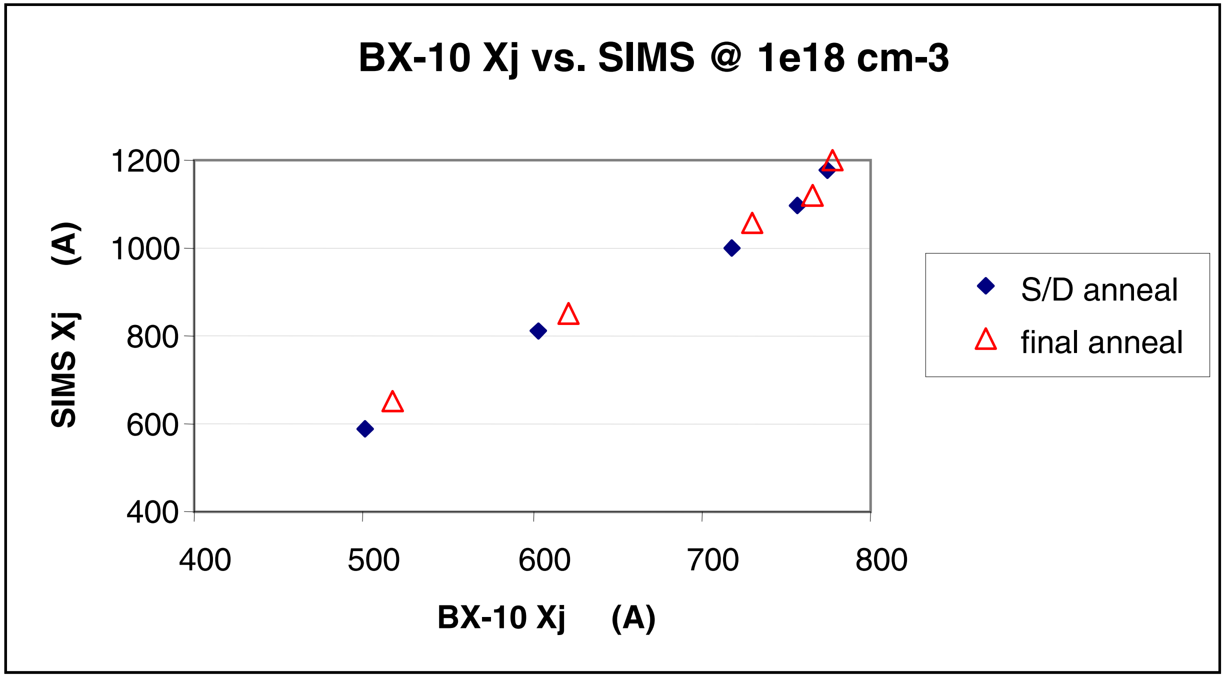
Junction depth trends with SIMS



Source: Sematech

CI measurement trends with SIMS over full range of energies

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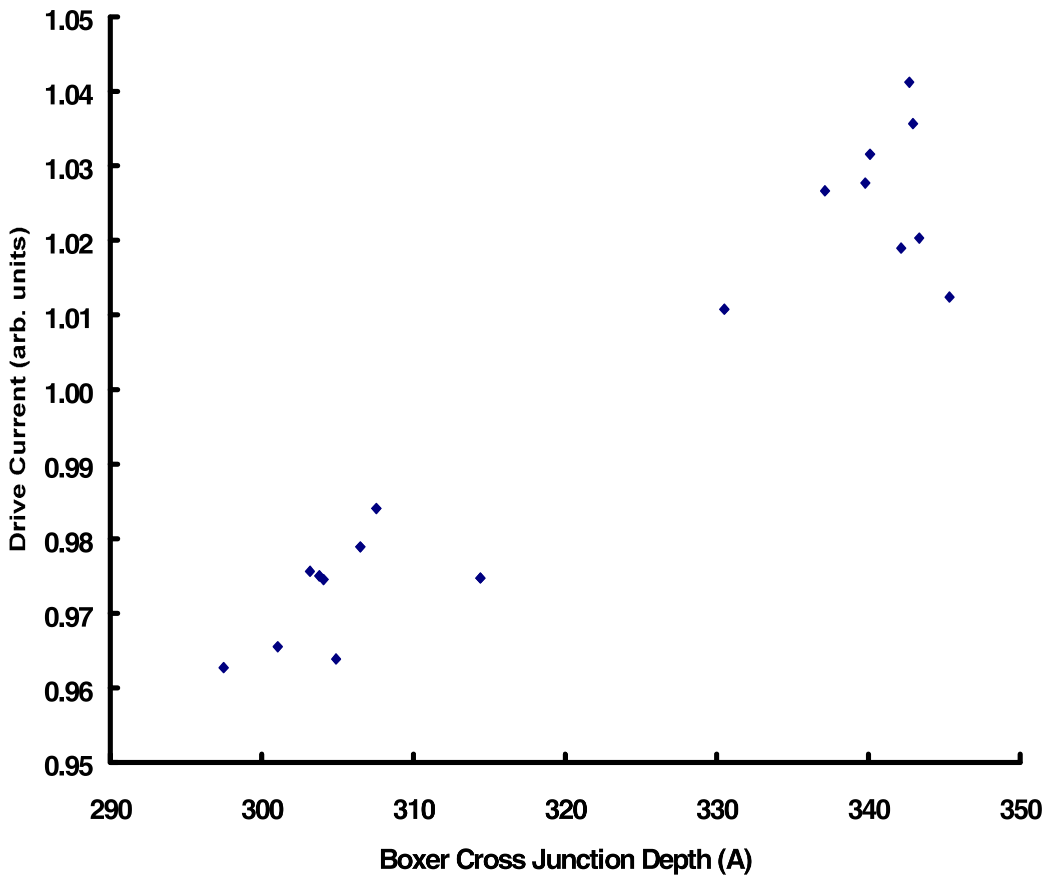
As LDD: Correlation to drive current (0.18 μm NMOS)



Source: AMD

NMOS extension depth measured in SIMS test structures after RTA

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NMOS Design of Experiment (DOE) matrix

S/D DOE evaluates CI measurement sensitivity to implant energy, dose, anneal time and temperature

	+	center	-
Dose (/cm^2)	3.60E+15	3.00E+15	2.40E+15
Energy (keV)	47	42	37
Temperature (C)	1025	1000	975
Time (sec)	10	6	2

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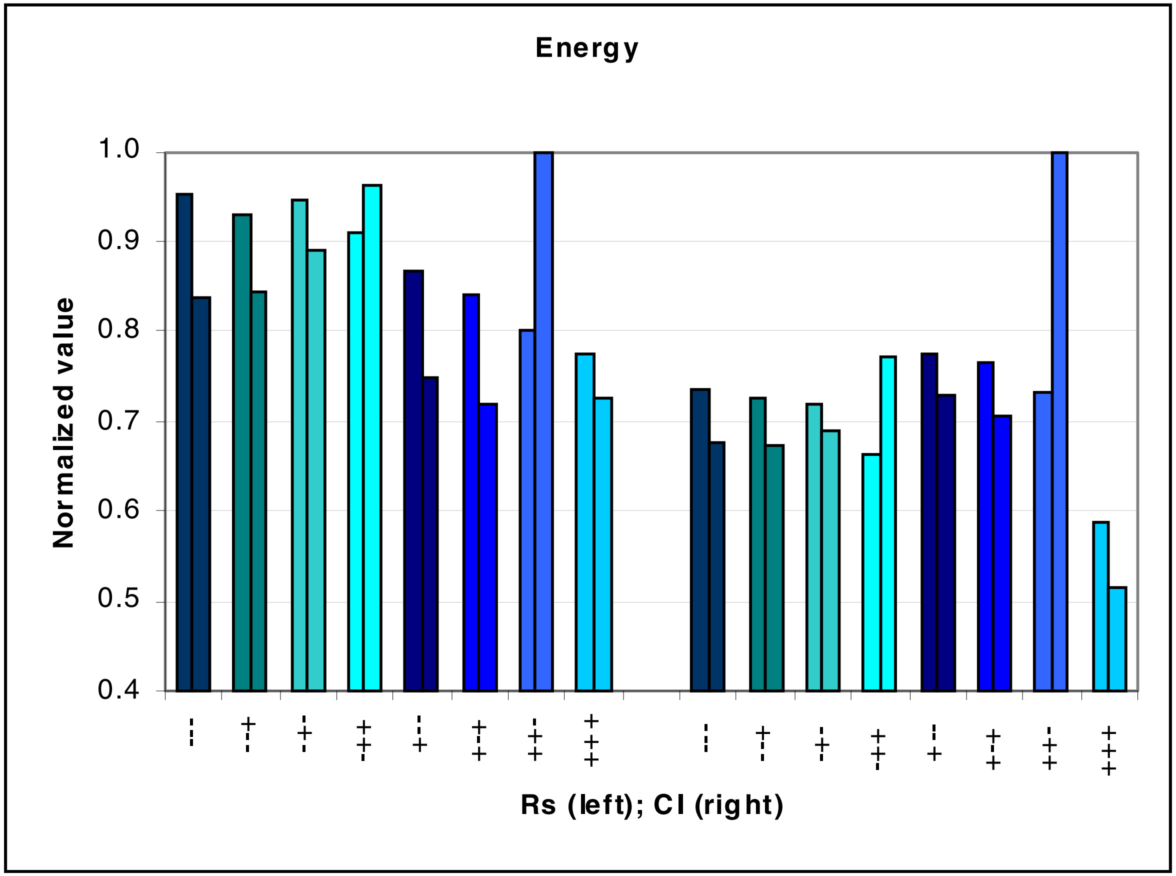
NMOS patterned wafer DOE result: correlation to energy



Source: Sematech

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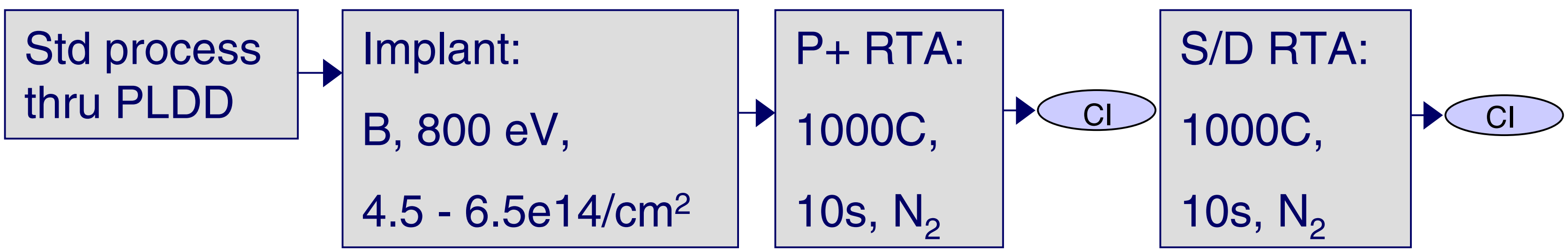
B^{11} LDD implants vs. dose

Depth trends with dose

Correlation to SRP, SIMS, 4PP

Noise limited resolution better than 2Å

N-well has minimal effect



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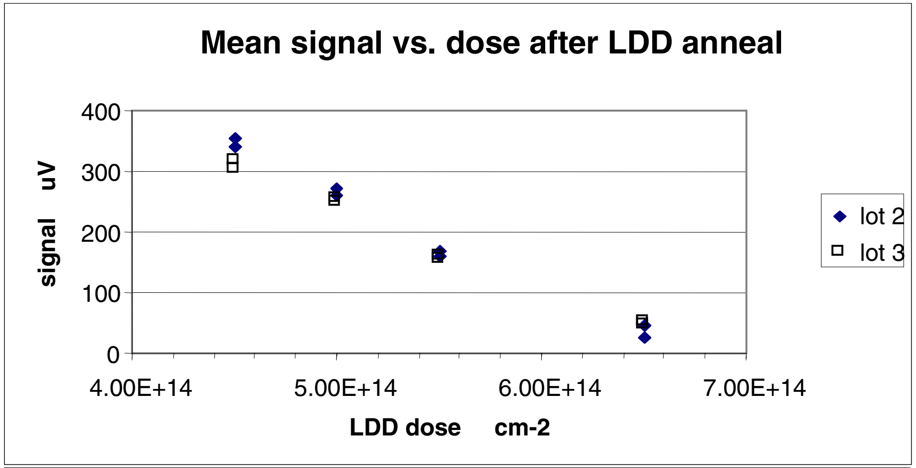
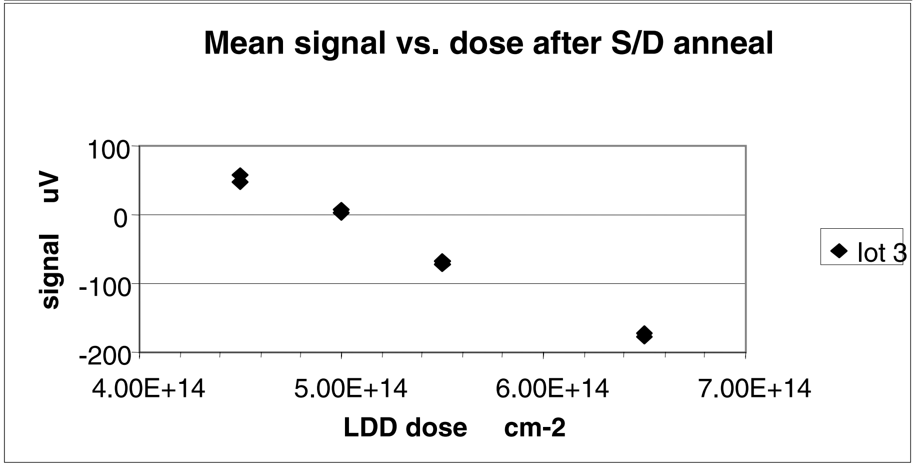
Post-anneal signal correlates to LDD dose



After LDD anneal:

Resolution of 5e12/cm^2
(1σ noise = 5 μV)



After LDD and S/D anneal:

Resolution of 6e12/cm^2
(1σ noise = 5 μV)

Source: Sematech

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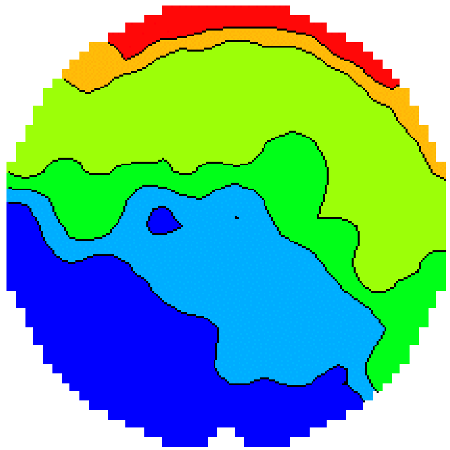
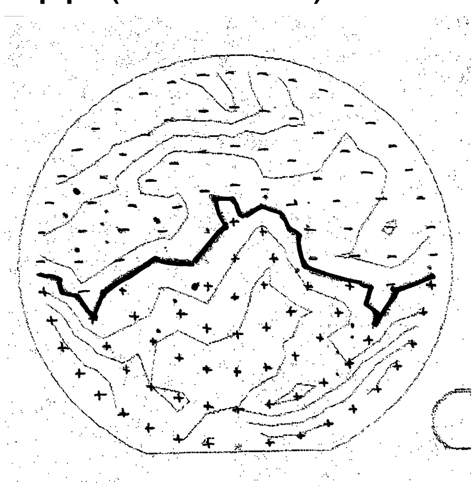
Correlation to 4PP map, SIMS, SRP

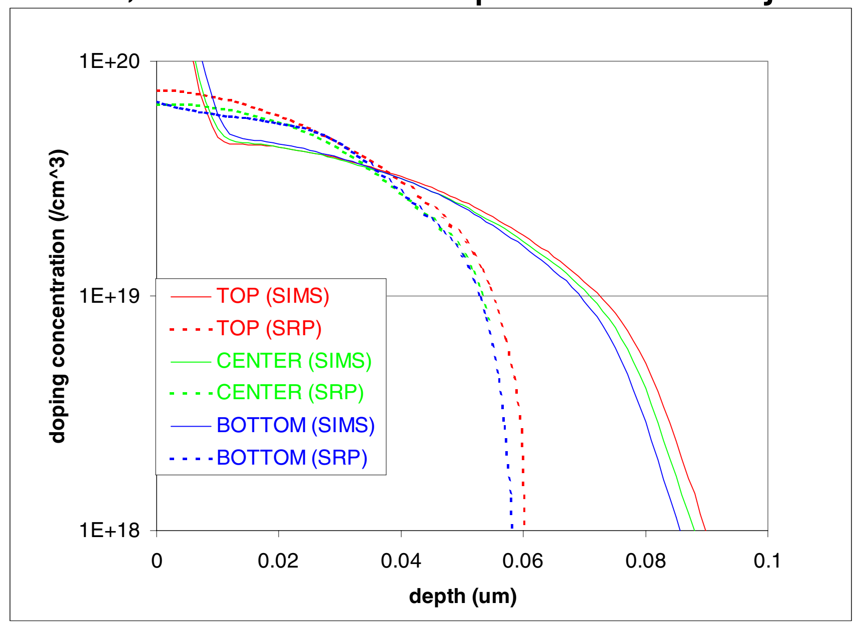
BX-10 (49 sites)

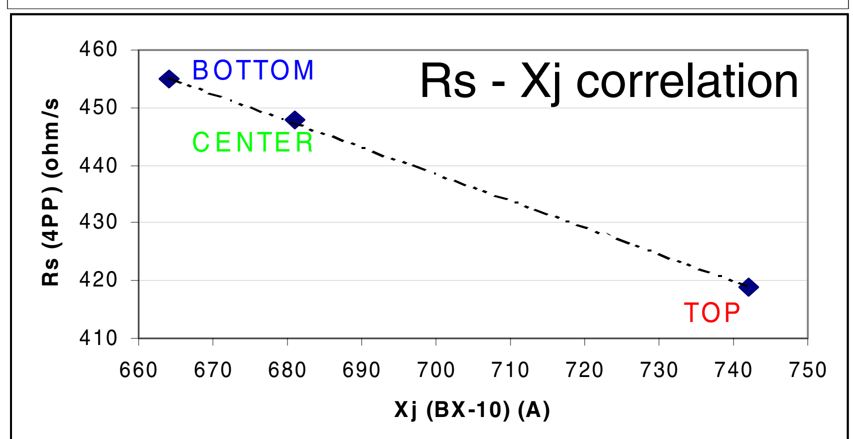


4pp (121 sites)



SIMS, SRP confirm top-to-bottom Xj trend





Source: Sematech

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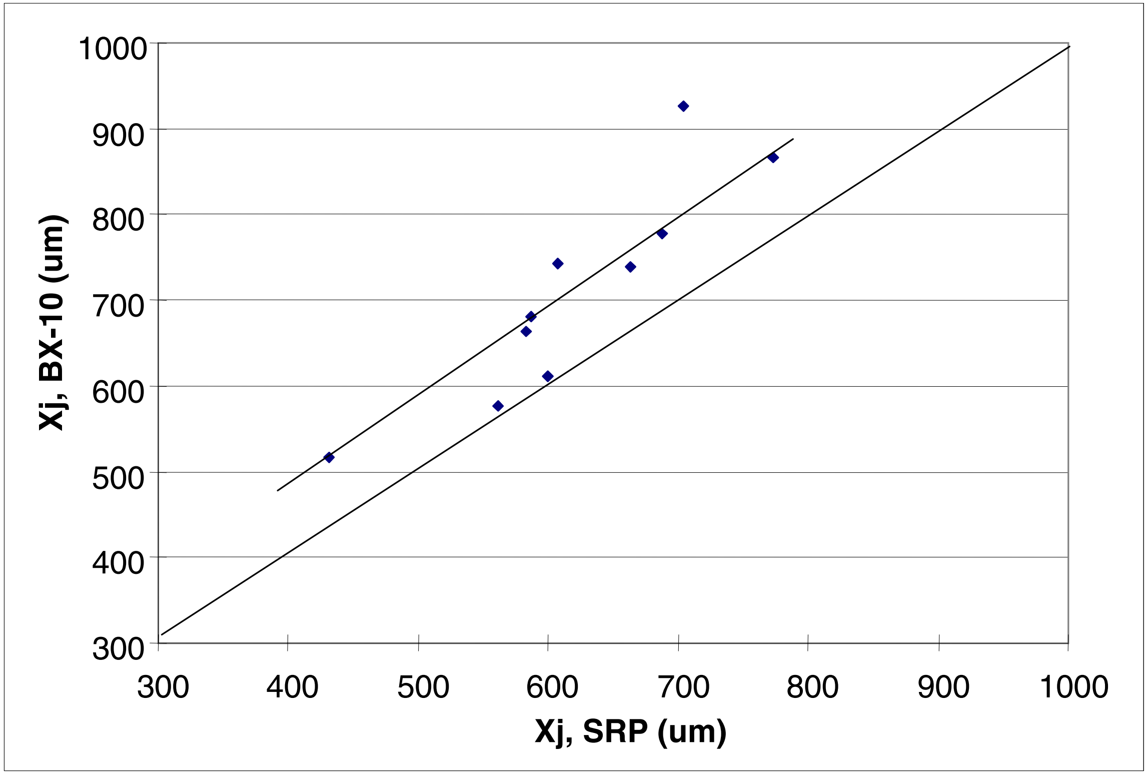
CI correlation to SRP measurements



800 eV B^{11}
into n-well

dose range
4e14 to 6.5e14/cm^2

Source: Sematech

- Offset due to use of p/p algorithm
- The three outlier SRPs trend opposite process (x_j drops with increasing dose)

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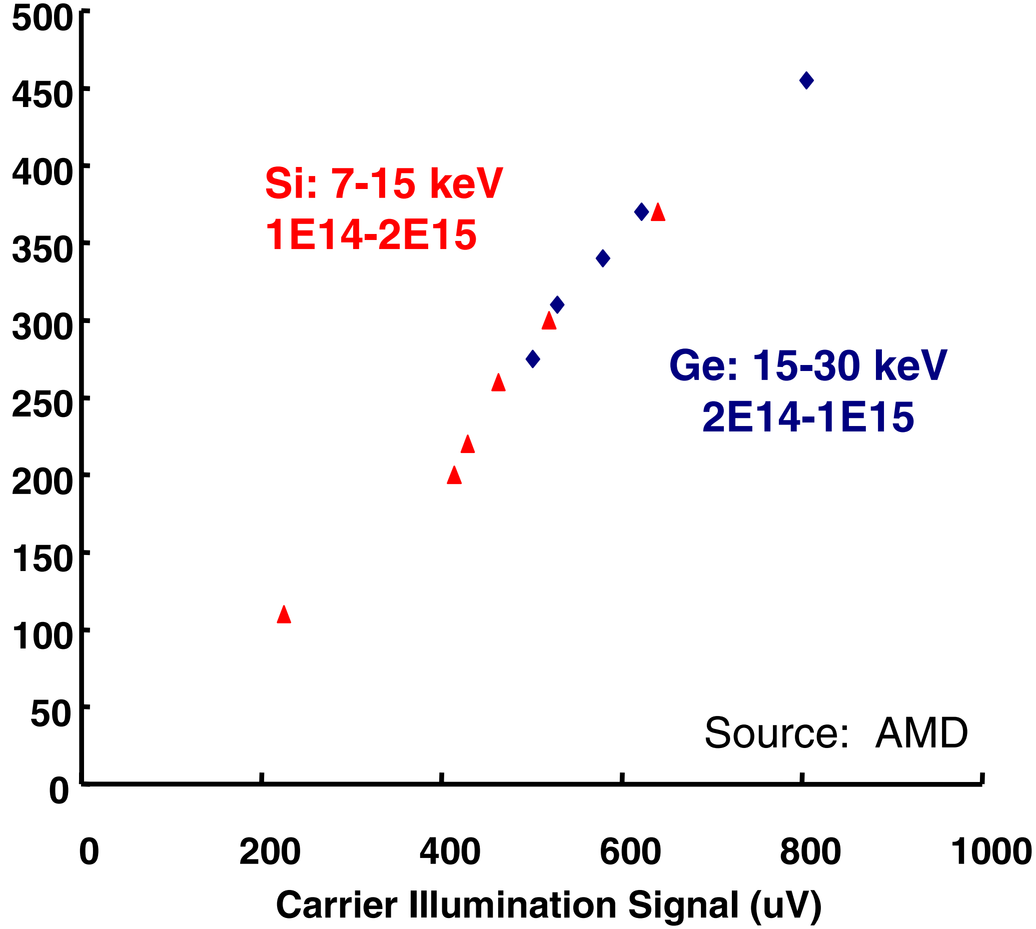
Pre-amorphization implant (PAI) depth measurement



Amorphization depth measured with TEM

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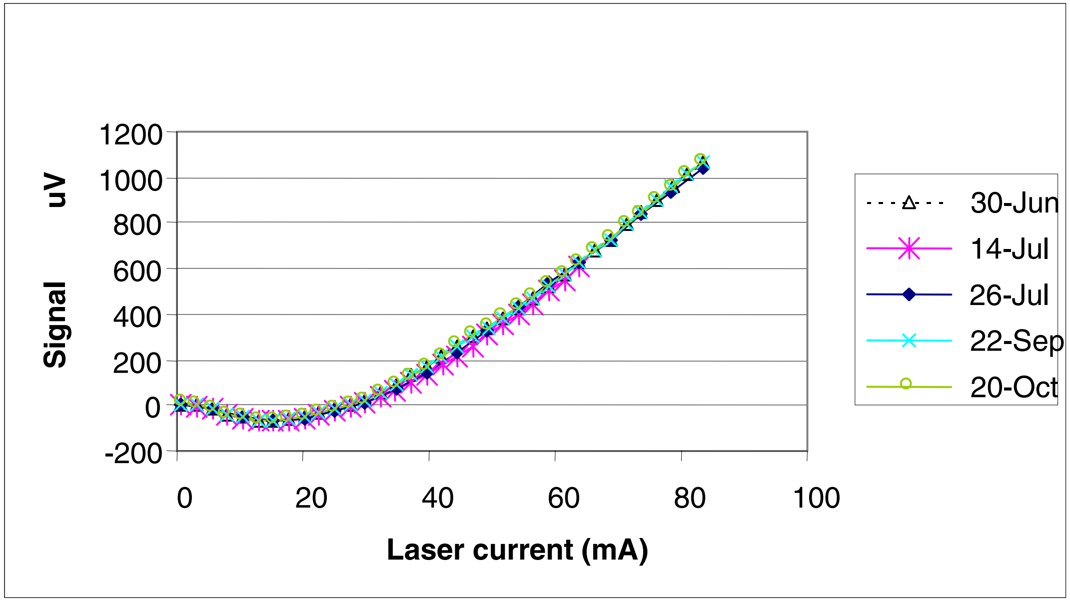
Good reproducibility and stability

- Wafer mean junction depth variation (1σ) for 9 sites, 30 runs, including load/unload:

  24 June: 0.63%

  28 June: 0.83%

- Graph shows measurements taken on reference sample over the four months following installation



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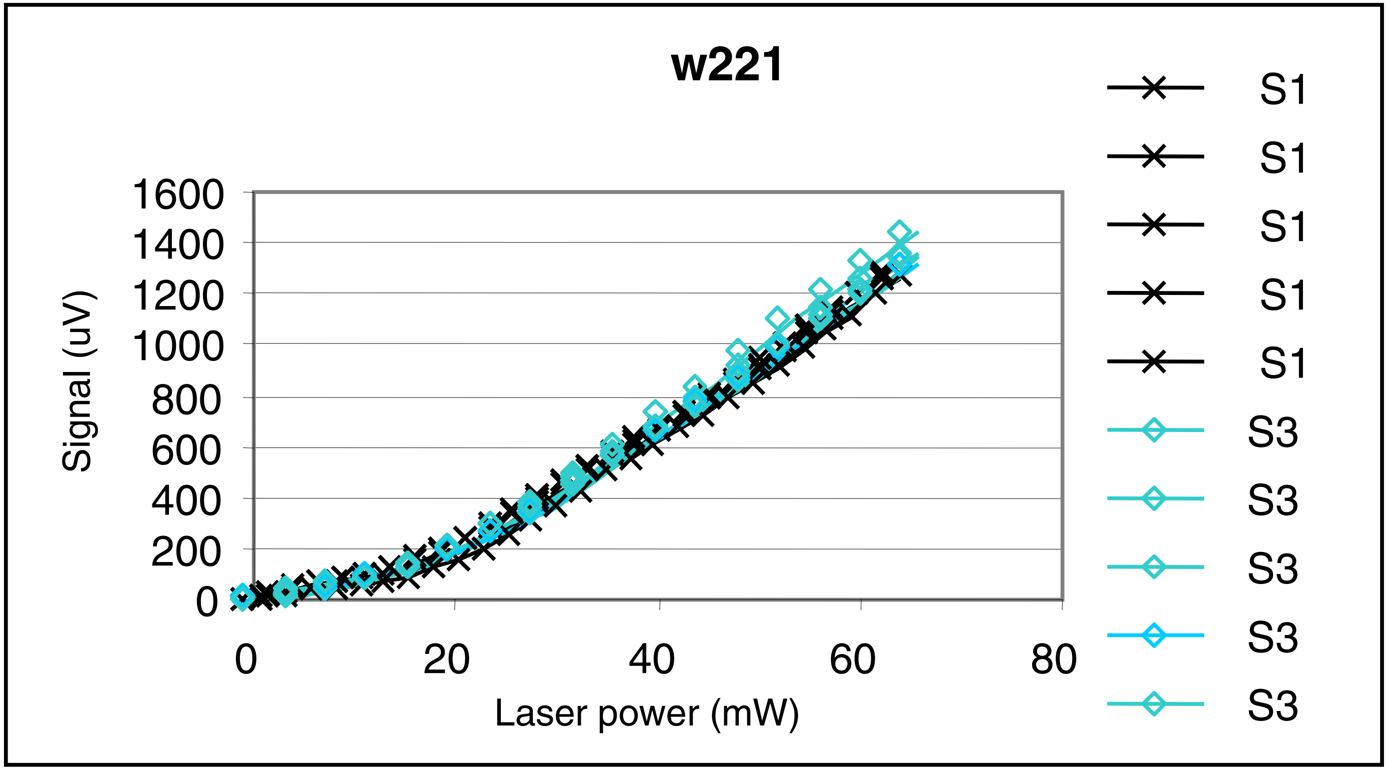
Matching of field systems



Measurements at 5 sites on same wafer, taken on field systems S1 and S3

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Conclusions

CI measurement characterizes critical sub-180 nm S/D processes (S/D, Extension, PAI)

- Provides non-destructive high resolution measurement on product
- Provides fast turn-around, suitable for in-line use or uniformity measurement
- Gage capability sufficient for in-line SPC

CI method enables tighter control required for current and future Source/Drain processes.

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