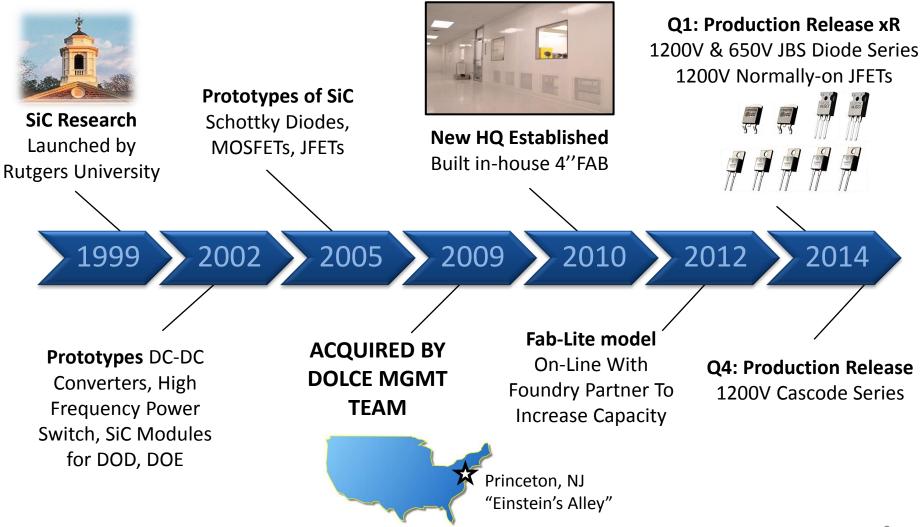




SIC MANUFACTURING IN THE FOUNDRY MODEL SEPTEMBER 2014

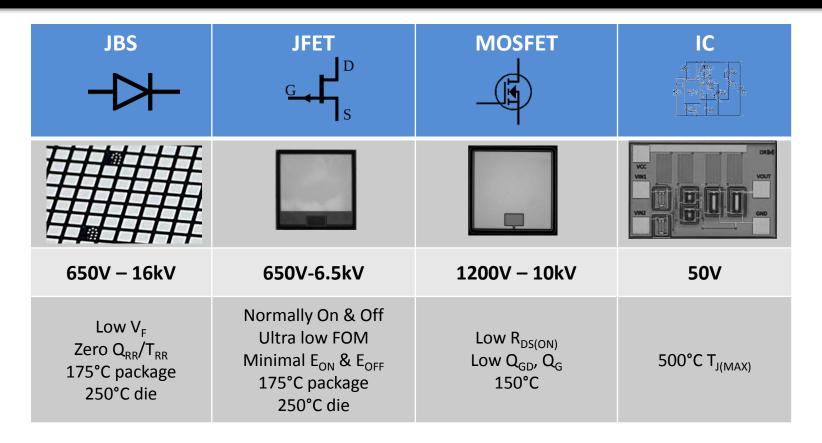


Company History



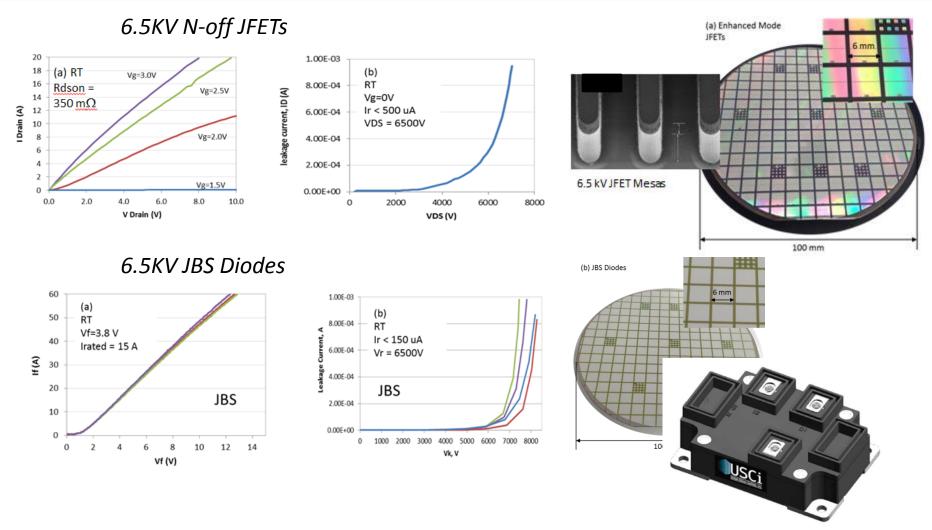


SiC Technology Focus Areas





USCI 6500V DEVICES PROTOTYPES





History of the foundry model in power devices

2008-today

Expansion to 12inch limited. New FAB investments small most suppliers trying to exploit overcapacity at 8inch. Outsourcing older tech to meet demand.

2005-2008

8inch Foundry model applied to FS-IGBTs and Superjunction technologies. Top suppliers still operate in-house FABs.

Late 90s-2000s

8inch Foundry model appears for low voltage MOSFETs – while most incumbents are still at 6inch

1970s-1990s

Power Discretes use custom processes and architectures. Fabs work with previous generation CMOS equipment. Top suppliers own their FABs (5in-6in)



The foundry model in SiC

PROS

- Silicon foundries bring a lot of established baseline expertise and manufacturing discipline
- High uniformity and high throughput processing equipment
- Foundries of sufficient scale with a solid (non-SiC) base business can offer reduced process costs
- By aggregating the SiC business from multiple companies, they can generate more economies of scale
- Capital efficient for ramping volume production

CONS

- Most foundries need consigned equipment to enable a SiC process
- Concerns about IP protection exclusivity can defeat the cost benefit from volume aggregation.
- Speed of technology development
- Volume projections in the near term 2-3 years are still too low to justify large investments
- Capacity and engineering resource allocation



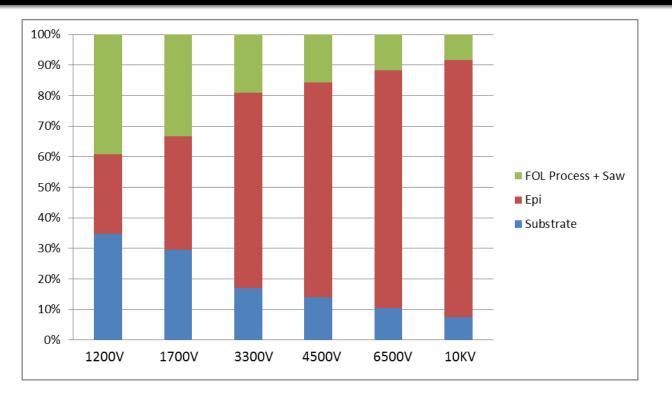
Economics of 6inch foundry process costs

Fab size	Fab	Monthly Running	Cost/Wafer at
Fab size	Outs/mo	costs	80% utlization
Small	1000	\$1,000,000	\$1,250
Small	10000	\$2,000,000	\$250
Medium	30000	\$3,000,000	\$125
Large	60000	\$4,000,000	\$83

- Total fab volume and utilization drive costs must find SiC volume drivers, or share the factory with other volume contributors
- High cost tools with limited throughput drive up costs SiC has several such bottlenecks in epi, implant, backgrind, saw. These are being rapidly improved.



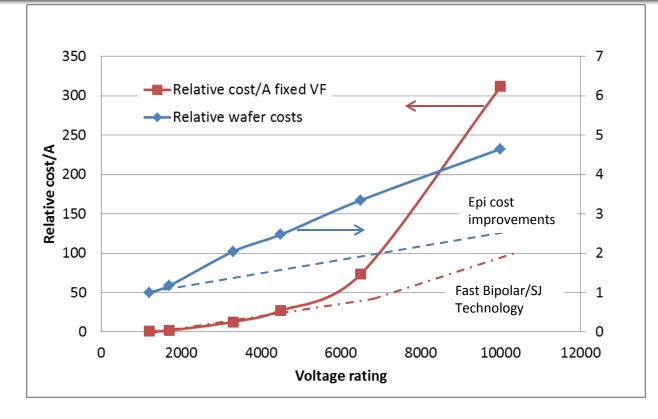
High voltage devices and their cost drivers



- Epi cost dominates present day SiC high voltage costs area needing rapid improvement in throughput without worsening quality
- For pure unipolar devices (JBS Schottky, MOSFET, JFET), several large chips needed for meet the current requirements.



Transistor/diode costs



- Unipolar device costs always increase with voltage rating since RdsA α BV $^{2.5}$
- Flattening the epi cost curve can drive down costs substantially
- Long term: need to get bipolar options to flatten the RdsA BV relationship





- The foundry model brings down wafer FAB costs, allow volume ramp with targeted capital expenditures, and brings Si high volume manufacturing capability to SiC.
- This translates both to stable high yields, as well as the ability to quickly deliver large volumes.
- Technological progress is needed and ongoing to drive down epitaxy costs for >3300V devices.
- Insertion of medium voltage diodes into IGBT modules can bring benefits in efficiency and improved operating lifetimes from lower operating temperatures.
- HV transistor solutions have a lot of promise, and initial products must be seeded to allow engineers to work on all the system issues with fast switching at 5-10KV.





Thank You!

USCi Welcomes Your Questions

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