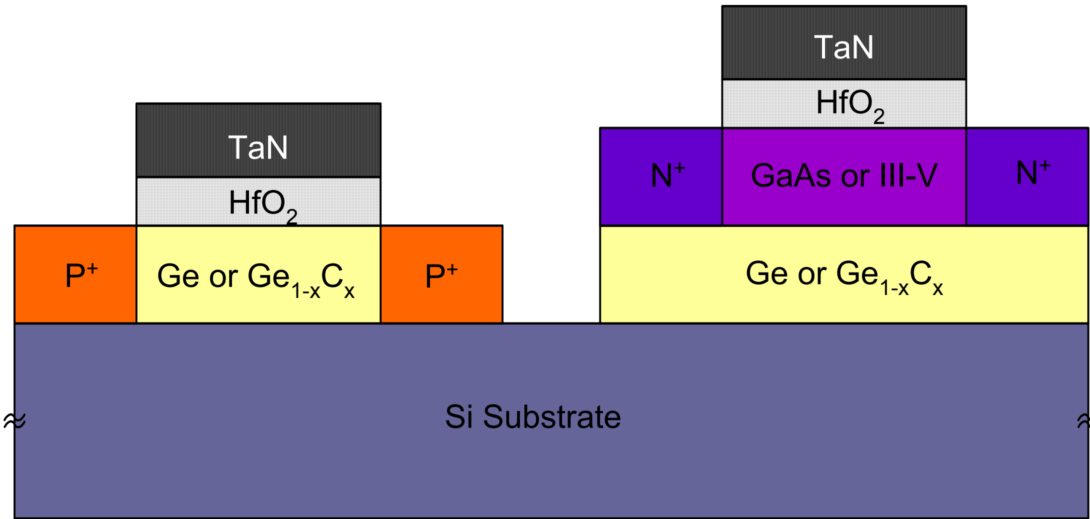
New Materials and Structures Based on Spin, Charge and Wavefunction Phase Control

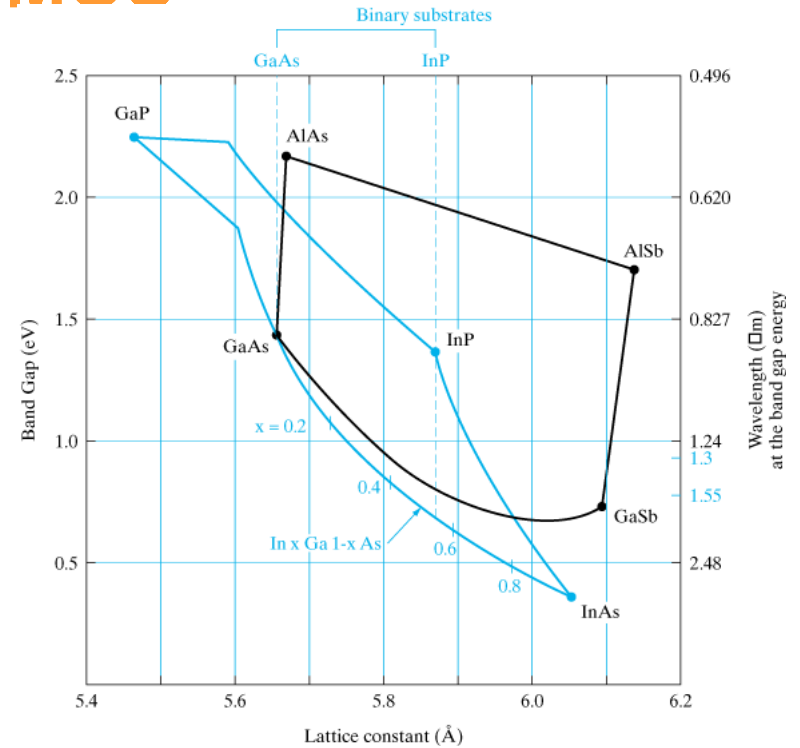
Sanjay Banerjee
Director, Microelectronics Research Center
Cockrell Chair Professor of Electrical & Computer Engineering
University of Texas at Austin

- Nanoscale Charge-based Transistors
- Nanoparticle Gate Flash Memory
- Spintronics
- Phasetronics

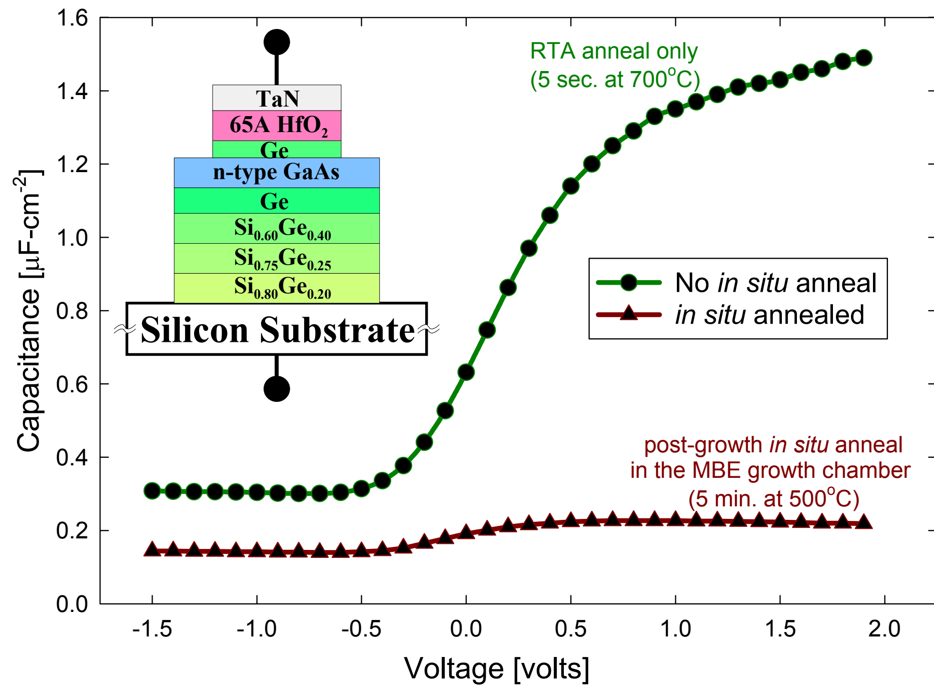
Acknowledgments: NRI-SWAN, DARPA-MARCO, NSF, SRC

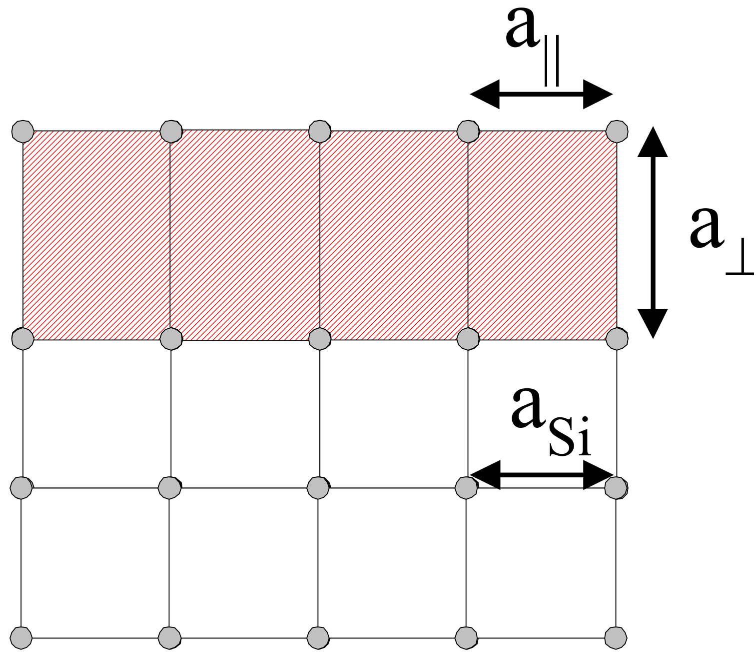
III-V and Ge CMOS

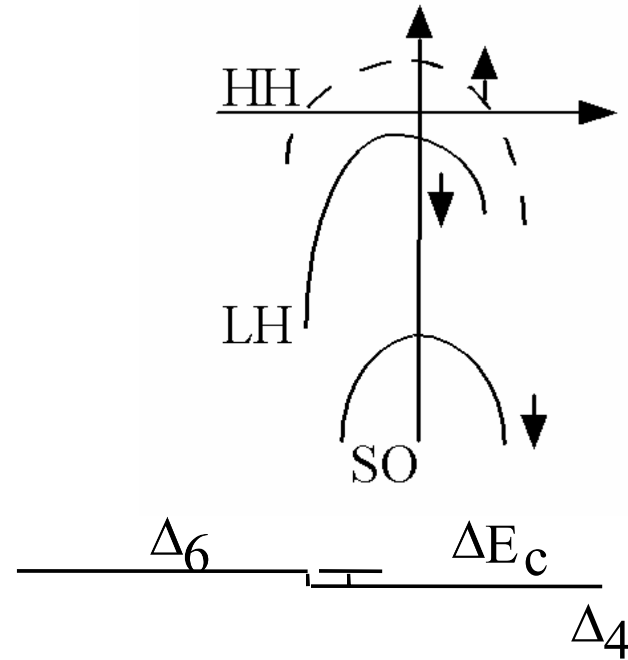




Ge

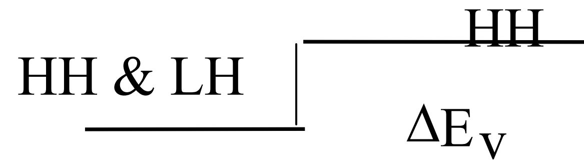


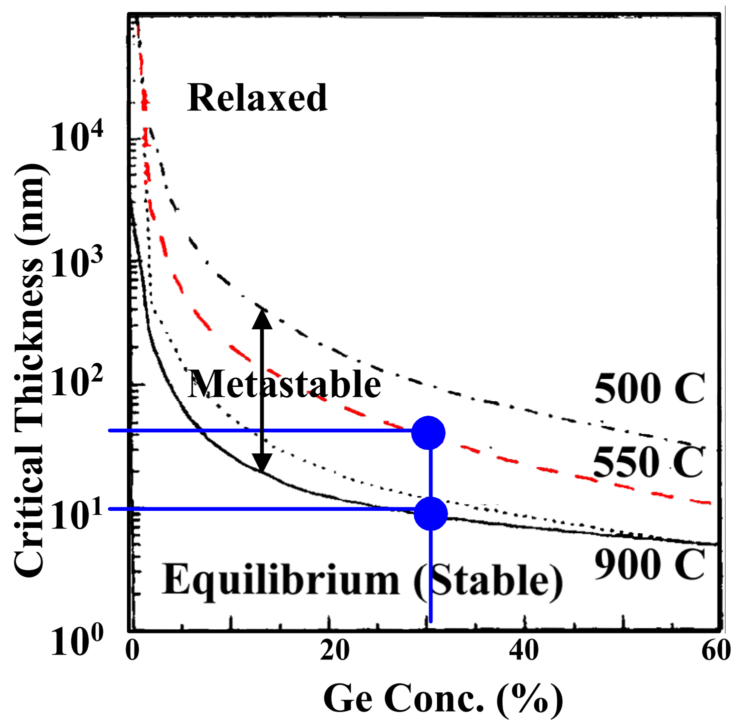




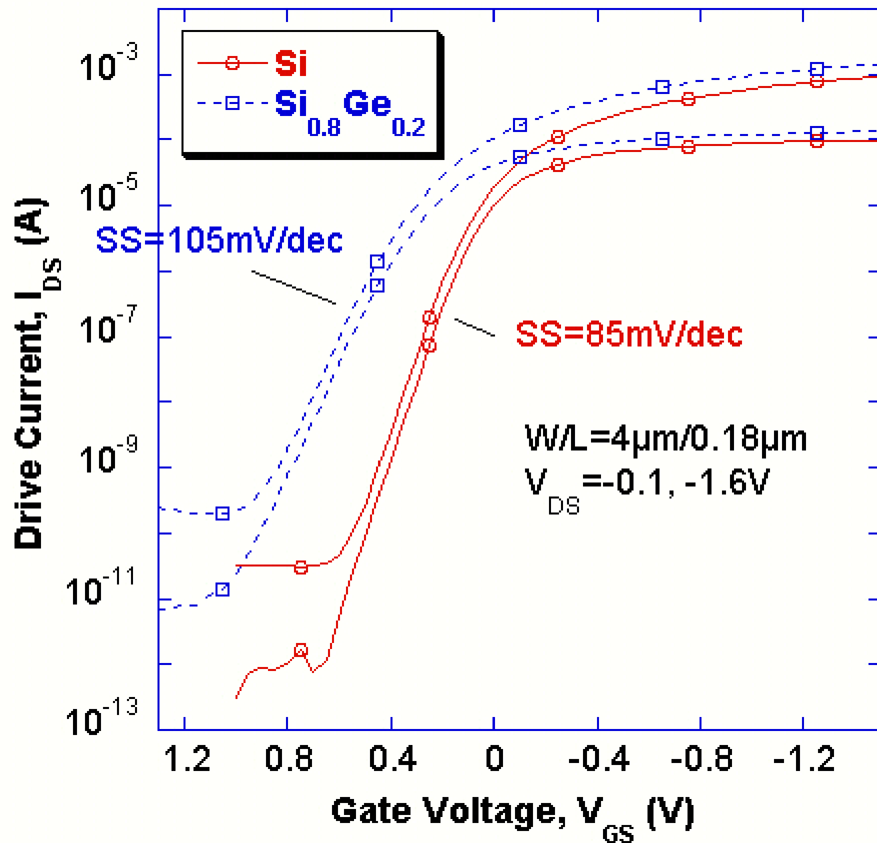
Relaxed Si

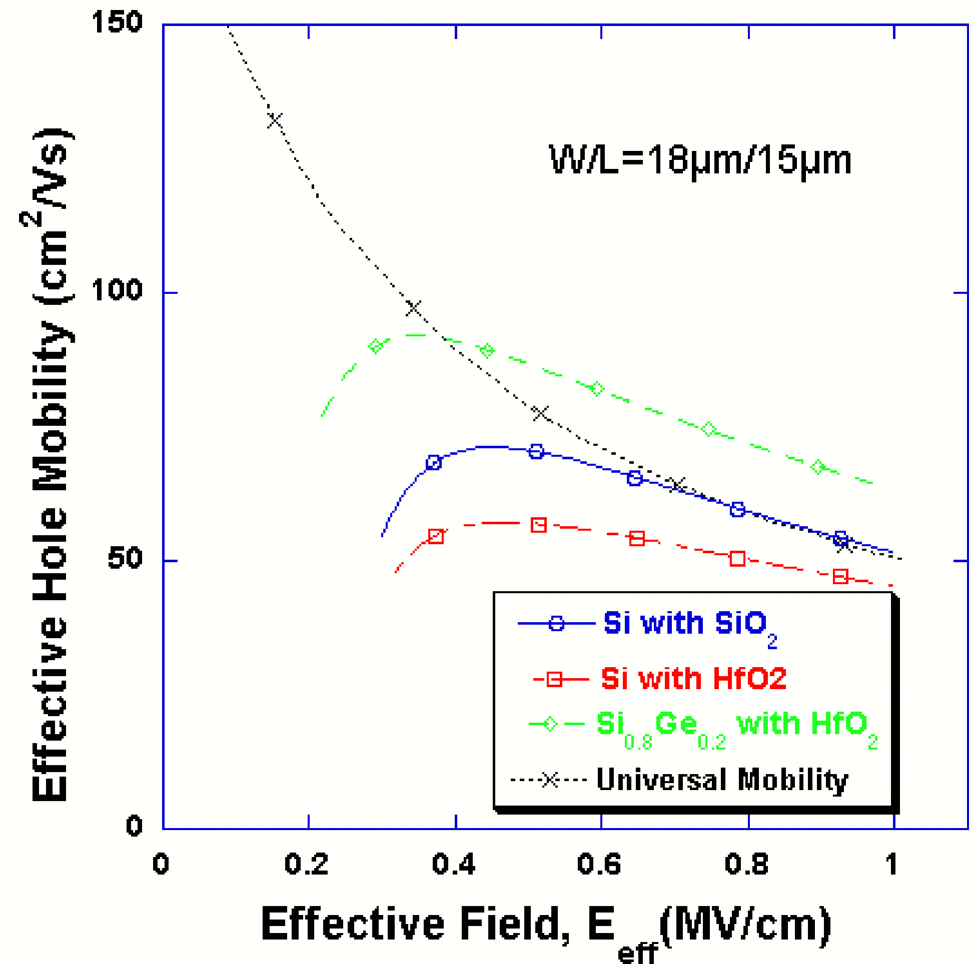
Strained $Si_{1-x}Ge_x$





Type-I (Compressive)



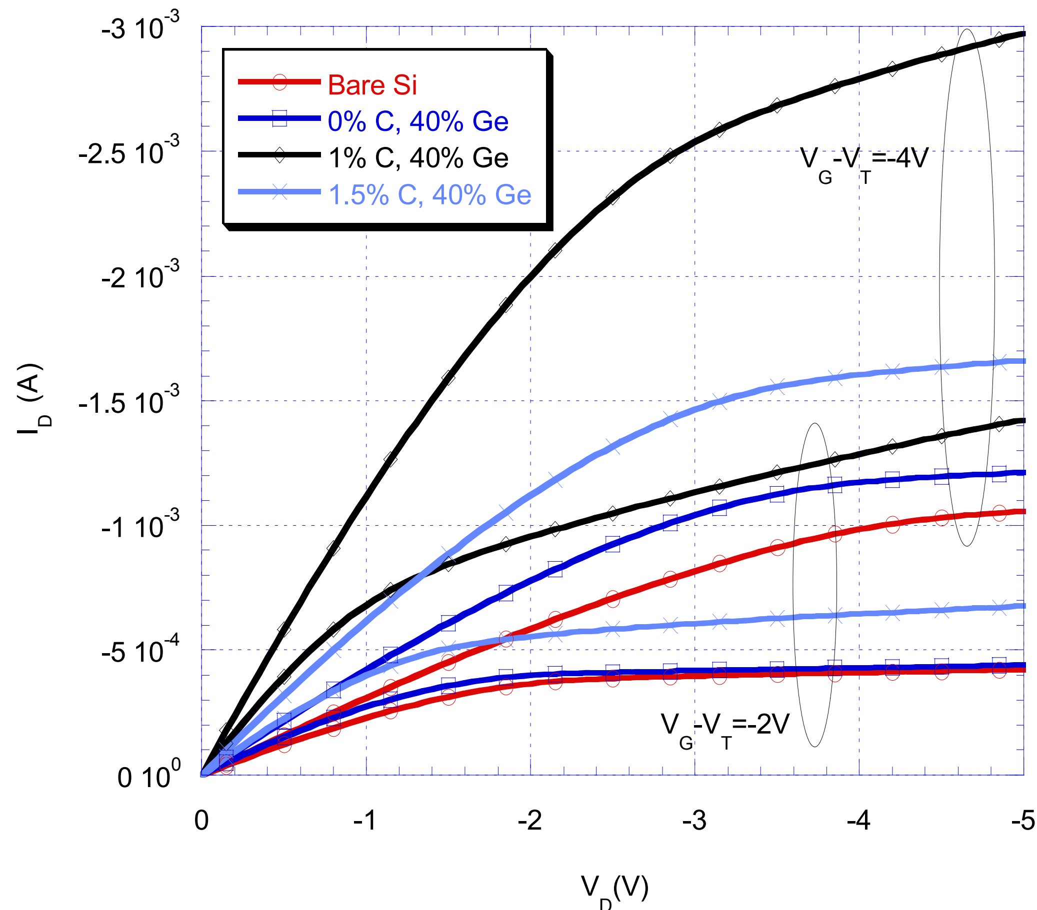


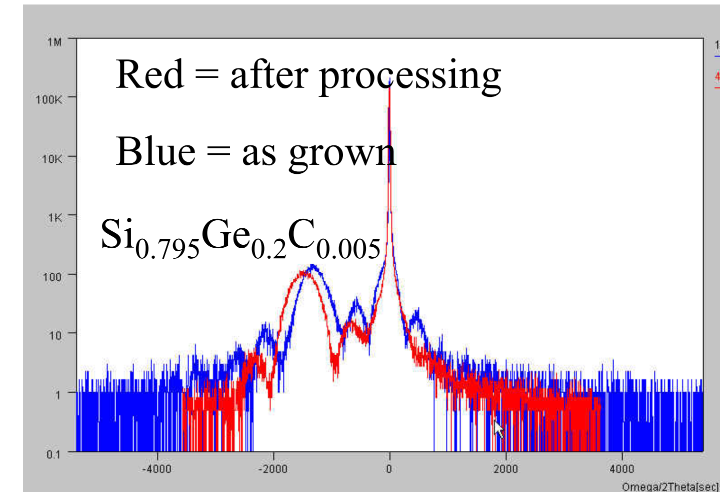
Subthreshold and mobility-field characteristics for 180nm $Si_{0.8}Ge_{0.2}$-HfO_2 PHFETs and control Si PMOSFET.

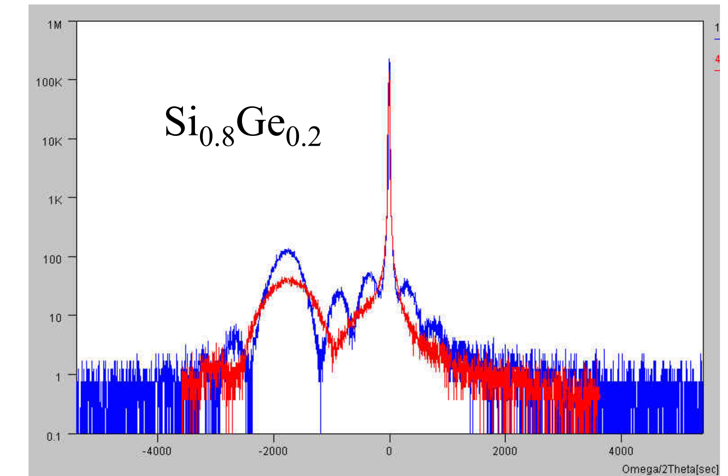
Recovery of mobility degradation for high-k gate dielectrics with enhanced-mobility channels: *(Onsongo,.., Banerjee)*

T.Ngai, J.Lee, S.Banerjee, "Electrical Properties of ZrO2 Gate Dielectric on SiGe," Appl. Phys. Lett., 76(4), p. 502, Jan. 2000.

Carbon Strain Compensation of Ge





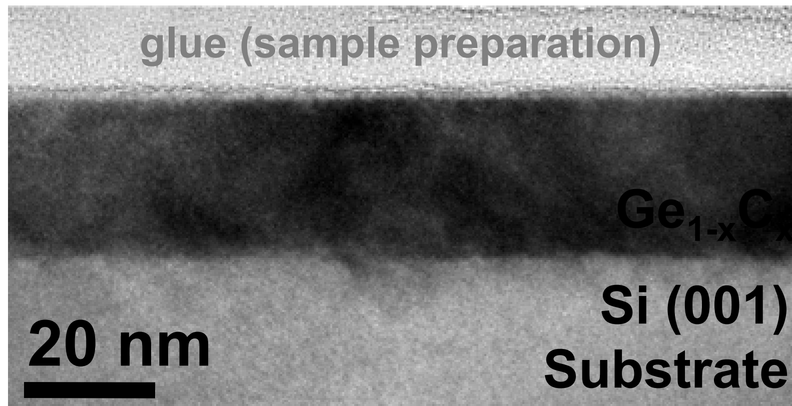


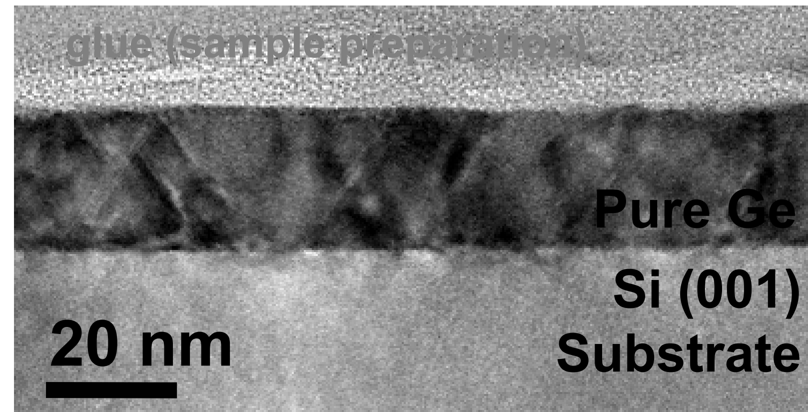
XRD Rocking Curves

- **Carbon has a smaller lattice constant than Si, Ge**
  - **Strain compensation of SiGe (~8:1 Ge-C ratio)**
- **Need low T for metastable C incorporation: low solubility ($5x10^{17}$ cm^{-3})**
- **C has different impact on strain than on bandstructure**

S.Ray, .. S.Banerjee, “Novel SiGeC Channel Heterojunction PMOSFET,” *Proc. of Int. Elec. Dev.Meet., 1996.*

XTEM Comparison of $Ge_{1-x}C_x$ on Si with pure Ge on Si

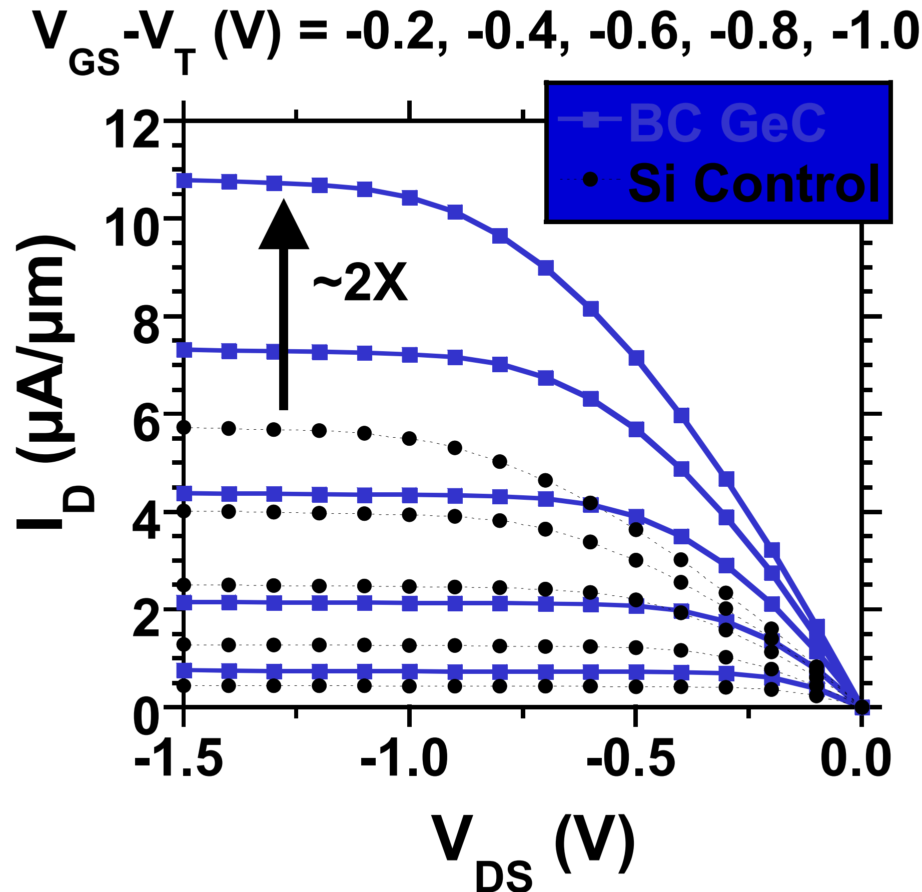


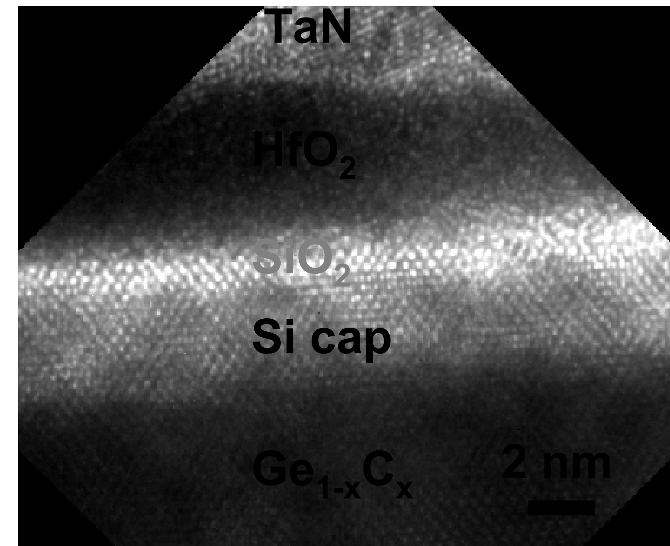


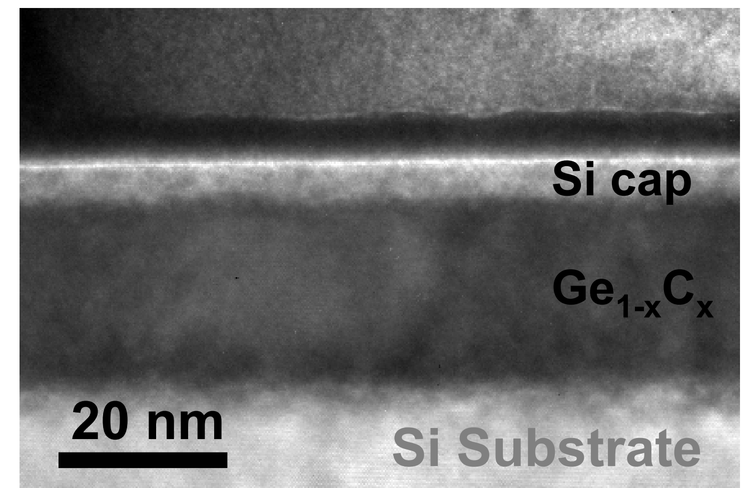
$Ge_{1-x}C_x$ **Pure Ge**

- **Pure Ge grown at low temperature directly on Si shows large number of threading dislocations**
- **Not present in $Ge_{1-x}C_x$ layer**
- **RMS Roughness > 3 Å**

$Ge_{1-x}C_x$ pMOSFET Devices





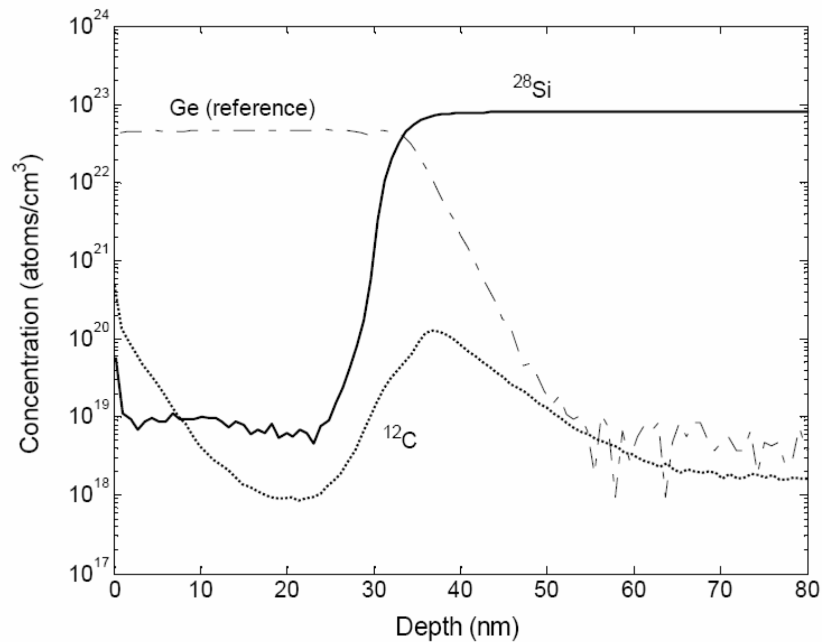


We have already demonstrated enhanced performance in high-k/metal gate pMOSFETs using $Ge_{1-x}C_x$ layers deposited directly on Si

- **Kelly, et al., IEDM 2005**
- **Kelly, et al., EDL 27(4) p. 265, 2006**

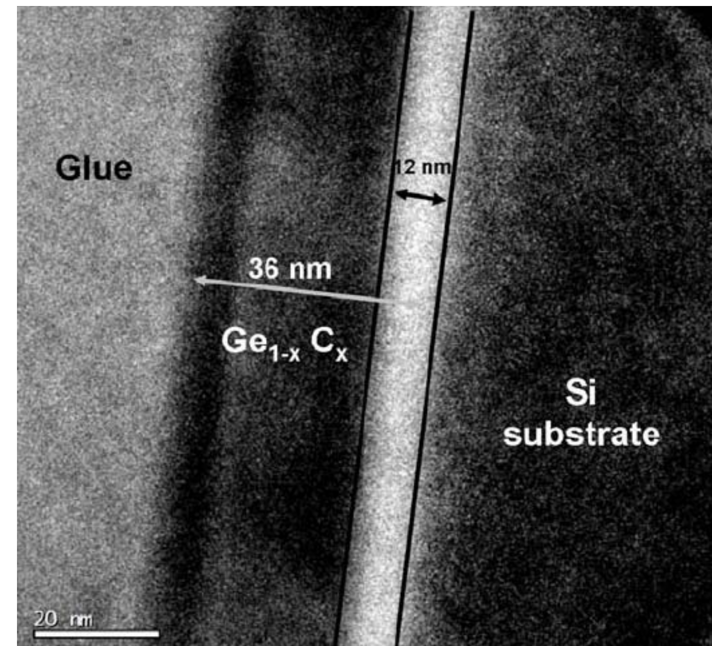
Carbon Incorporation (Yacaman)

SIMS



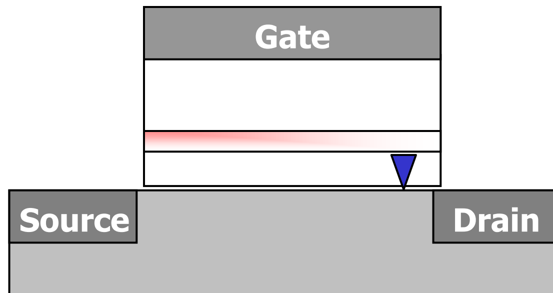
- SIMS measured using standard prepared by ion implantation
- Higher C level at interface

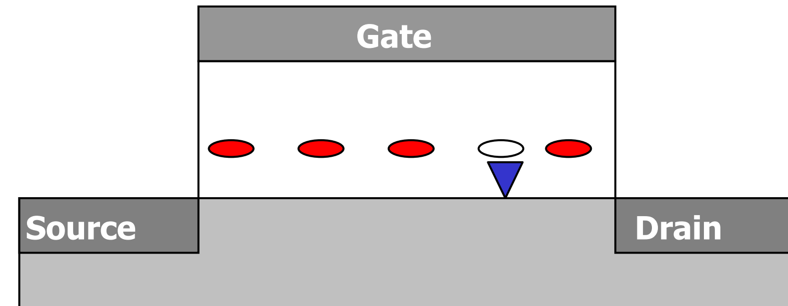
EFTEM



- Brighter regions correspond to higher C concentration
- Higher C incorporation has been observed at interface

Nanoparticle Gate Flash Memory





S. Tiwari et al, *Appl. Phys. Lett.* **68**, (1996)

Conventional Flash Memory

A defect totally discharges the floating gate

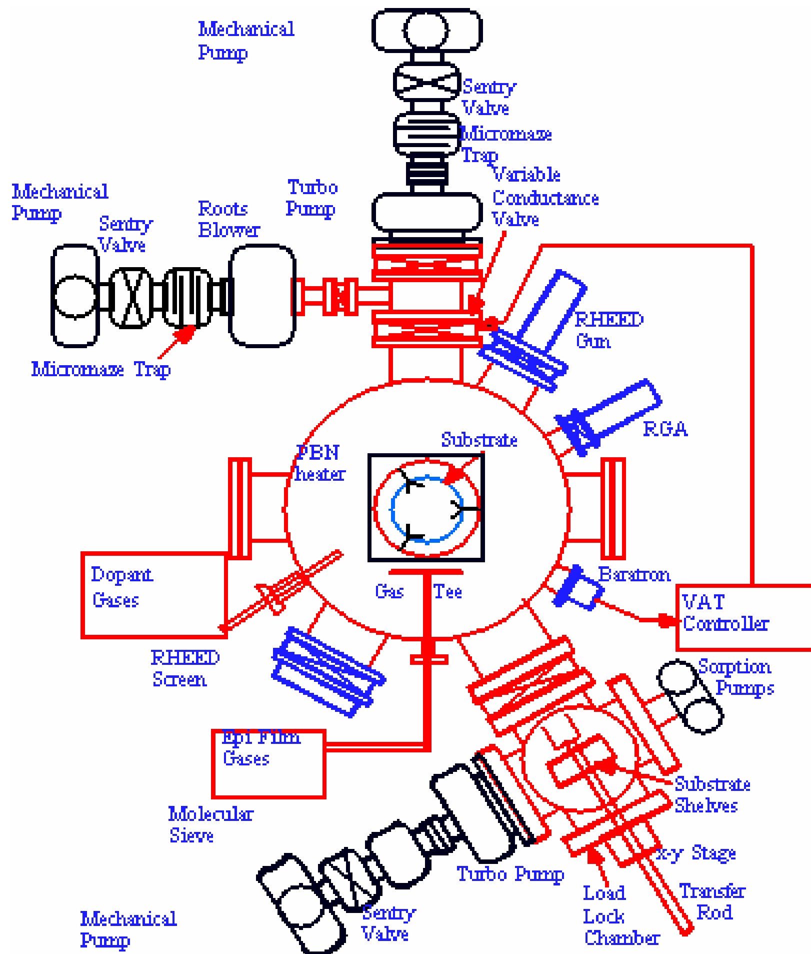
– Thick tunnel oxide
– High voltage/ power
– Low reliability/ speed

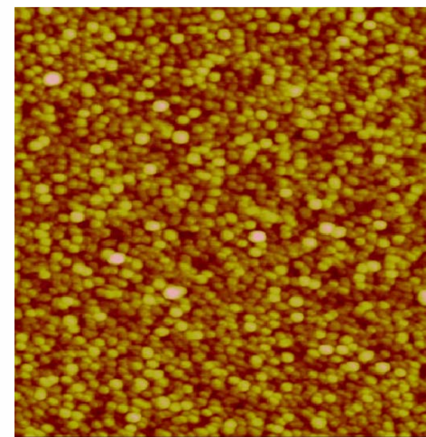
Nano-floating Gate Memory

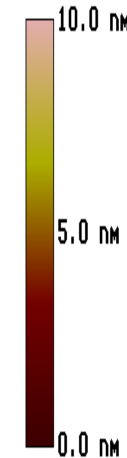
A defect discharges only one dot

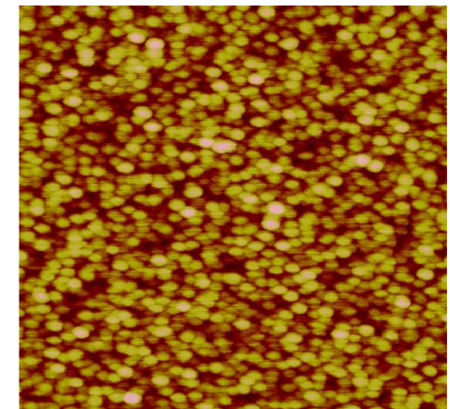
- High-k tunnel oxide
- Speed/ power/ density better
- Reliability improved
- *New phenomena*- self-assembly, Coulomb blockade, multi-level cells

SiGe Nanocrystals on High-K Dielectrics









HfO_2 SiO_2

AFM scans (1 micron x 1micron) showing SiGe dots grown at ~ 500ºC for 90 s with 0.75 gas ratio of GeH_4 to Si_2H_6.

Kim., Banerjee, Growth of germanium quantum dots on different dielectric substrates by chemical-vapor deposition, J VAC SCI TECHNOL B 19 (4): 2001

Band diagram of HfO_2 and SiO_2 dielectric at low program voltage

Channel

Dot

gate

Interface oxide

Tunneling oxide (HfO_2)

(HfO_2)

Si E_c

SiGe E_c

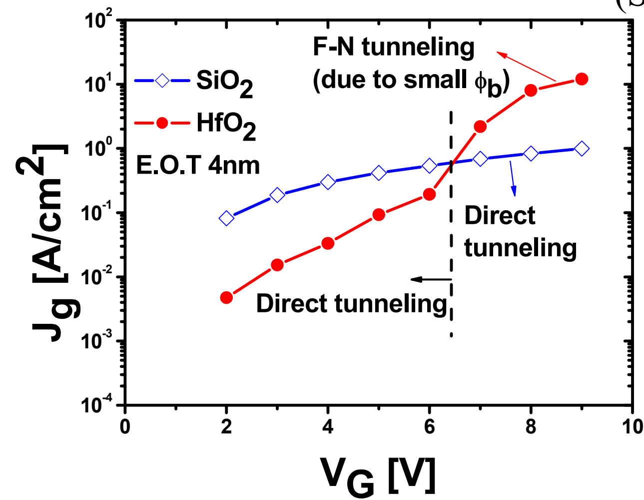
Channel

Dot

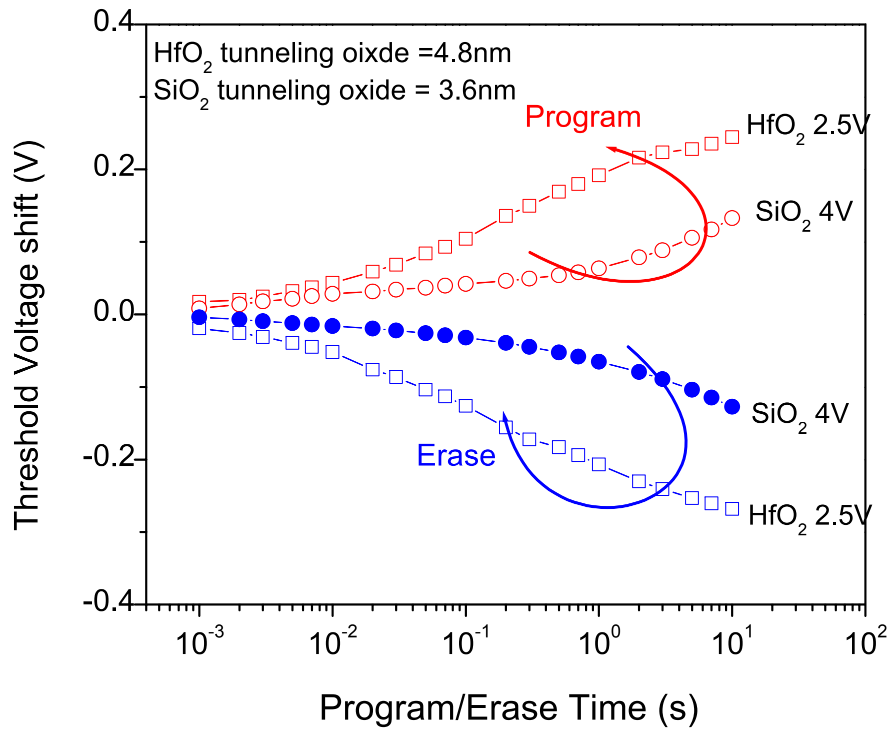
gate

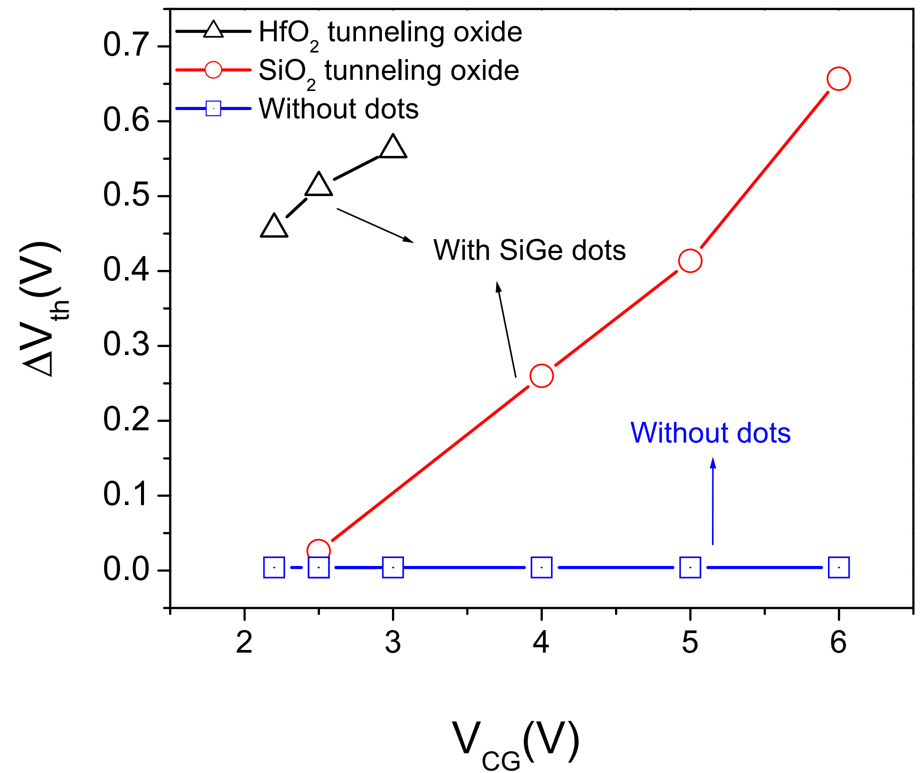
Tunneling oxide (SiO_2)

(SiO_2)



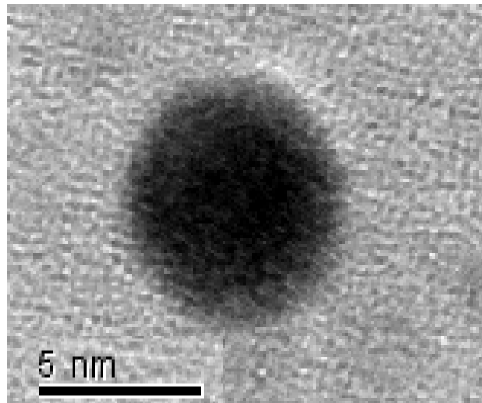
Program & Erase Transient Characteristics



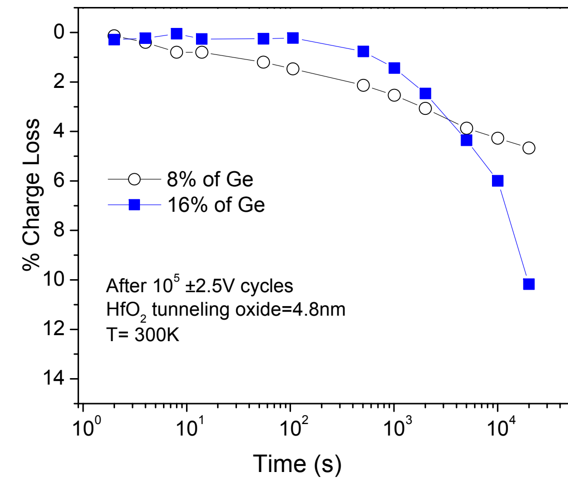


Kim DW, Kim T, Banerjee SK, ELECTRON DEV 50 (9): 1823-1829 SEP 2003

Coulomb Blockade in SiGe dot on SiO_2 and HfO_2

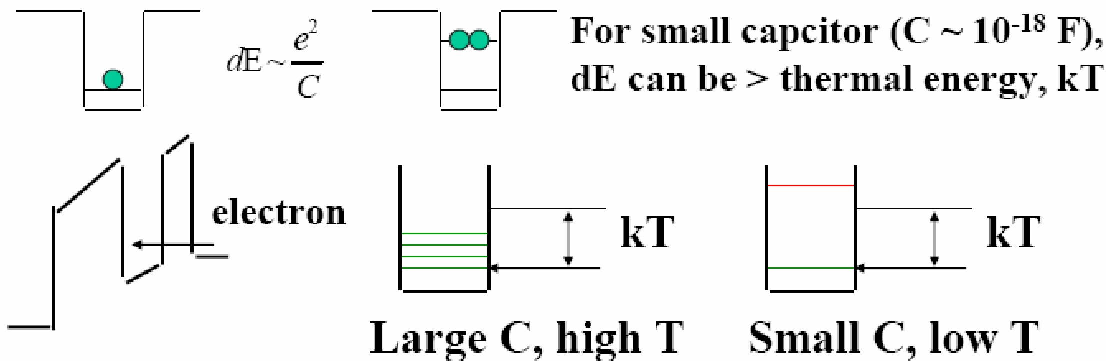


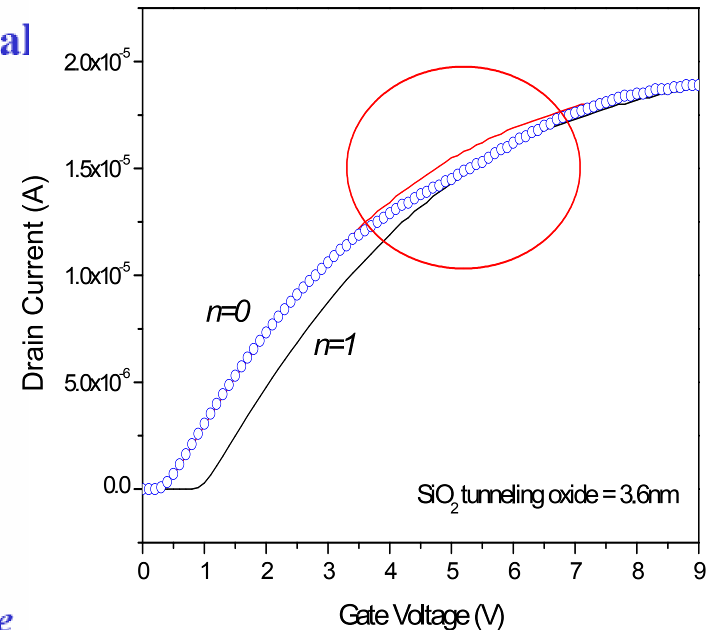
SiGe on SiO_2 @ 520 ºC



- **Limits programming by direct tunneling at low voltages**
- **Multiple electron storage reduces life-time in nanocrystal**

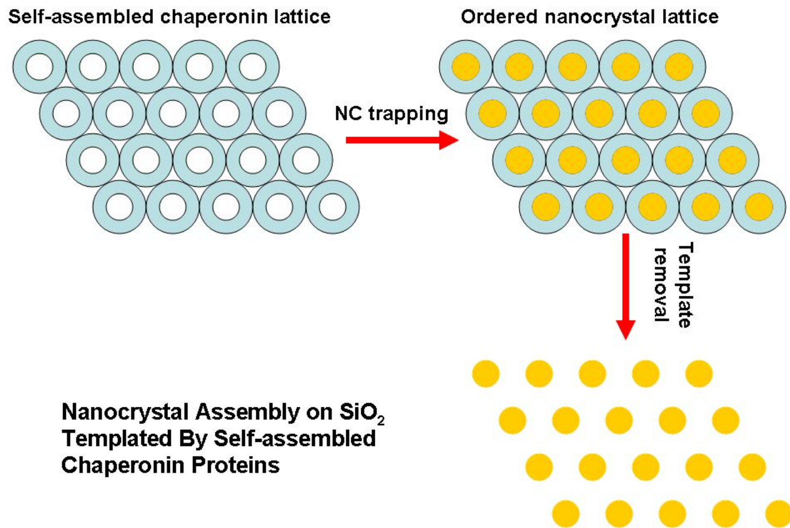
Putting an electron on nanocrystal raises other energy levels

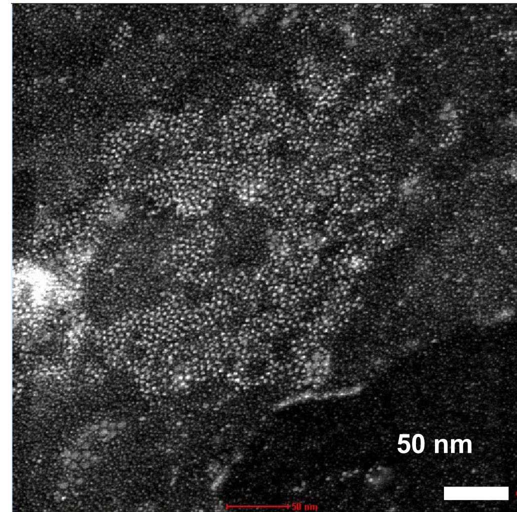


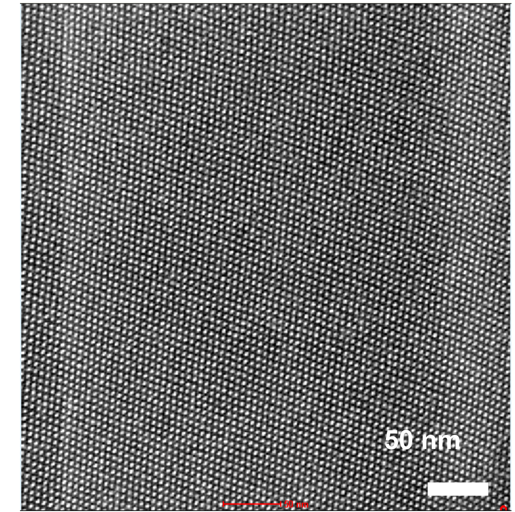


- *Low T: Given a Write voltage, fixed no. of electrons in nanocrystal*
- *For nanocrystals < 5nm, this effect is significant at room temperature*

Approach: Protein Assembly- FN P/E



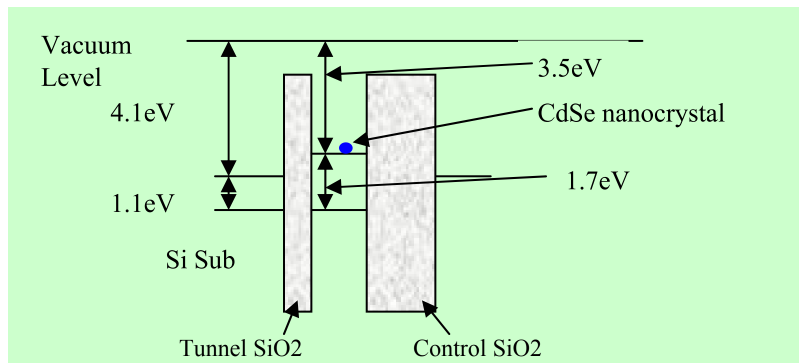


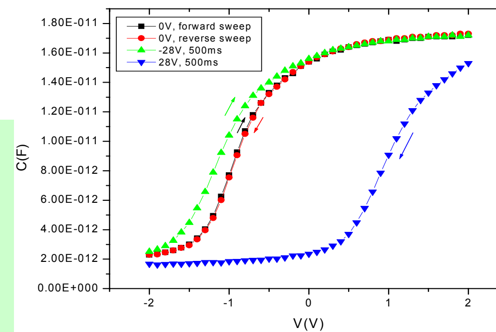


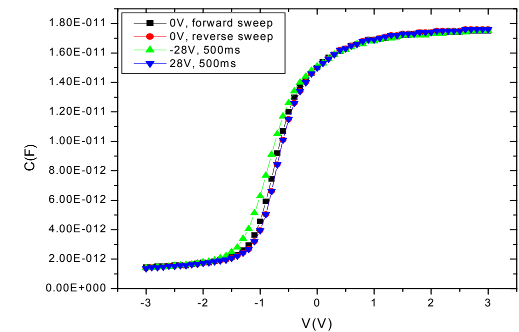
Trapping of Co, CdSe, PbSe nanocrystal on protein templates: w/o and with chaperonins ~ 10^{12} cm^{-2}

Cobalt is ferromagnetic

Chaperonin proteins to template CdSe nanocrystal assembly- 2005



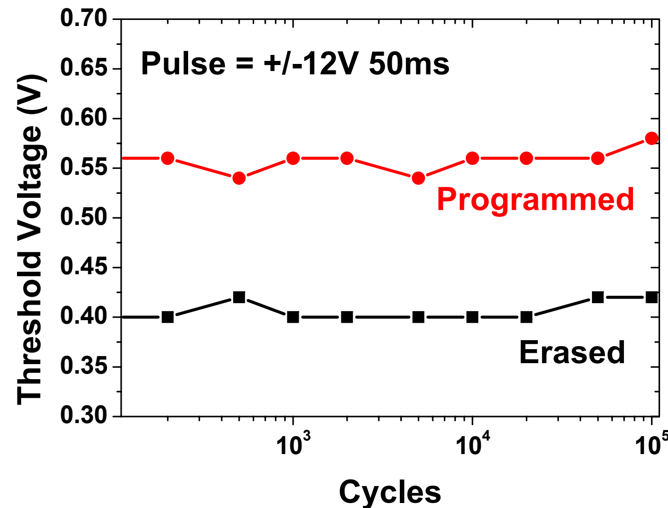




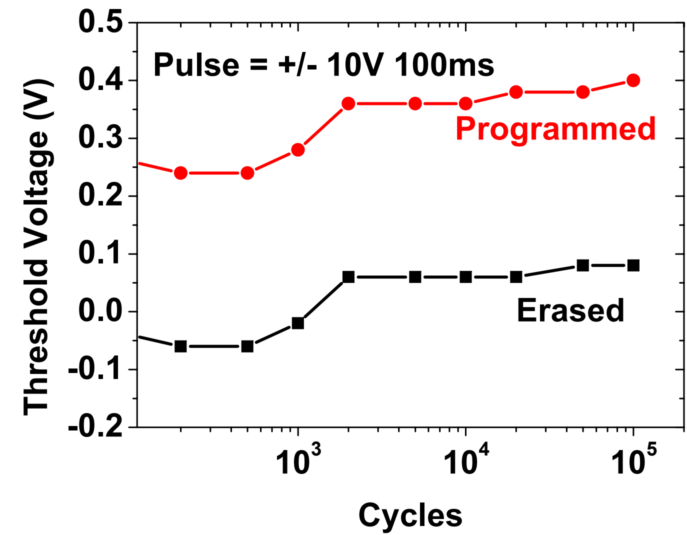
7nm tunnel oxide, 35nm control oxide, w/ and w/o protein-mediated CdSe nanocrystals (size: 7nm)
Problems with memory window closure after several write/erase cycles.

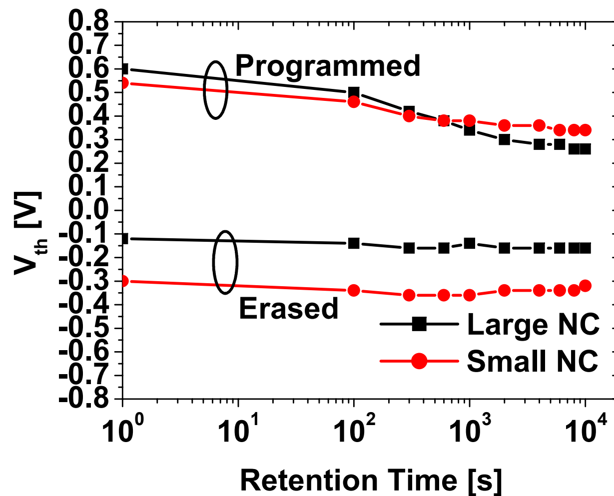
Endurance & Retention

Large NC



Small NC

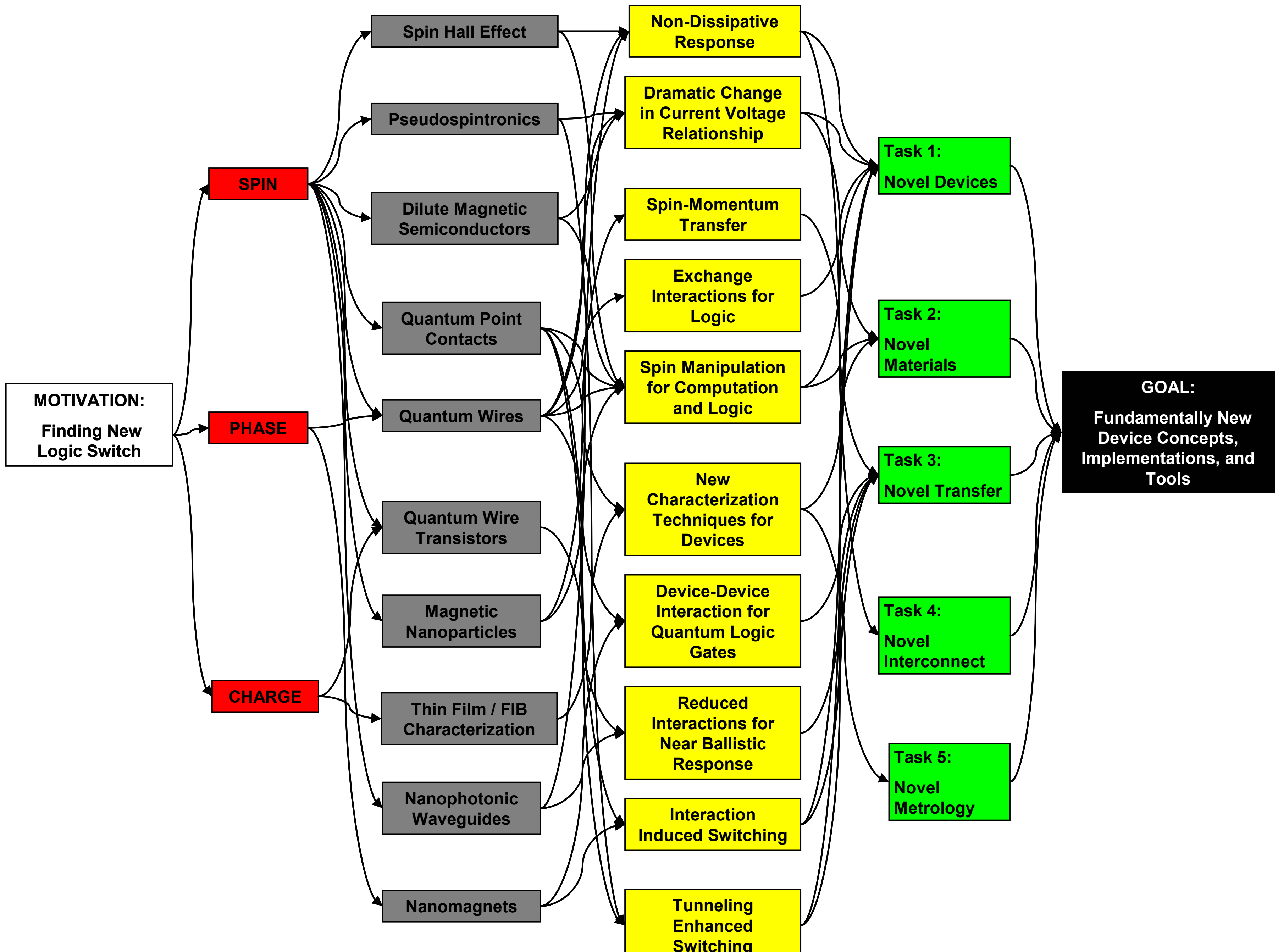




Temperature=85°C

10V ±200ms erase/program

SWAN- Novel Transistors Based on Electron Spin, Phase, Charge



Tasks 1-3: ITRS 2005, Emerging Research Devices

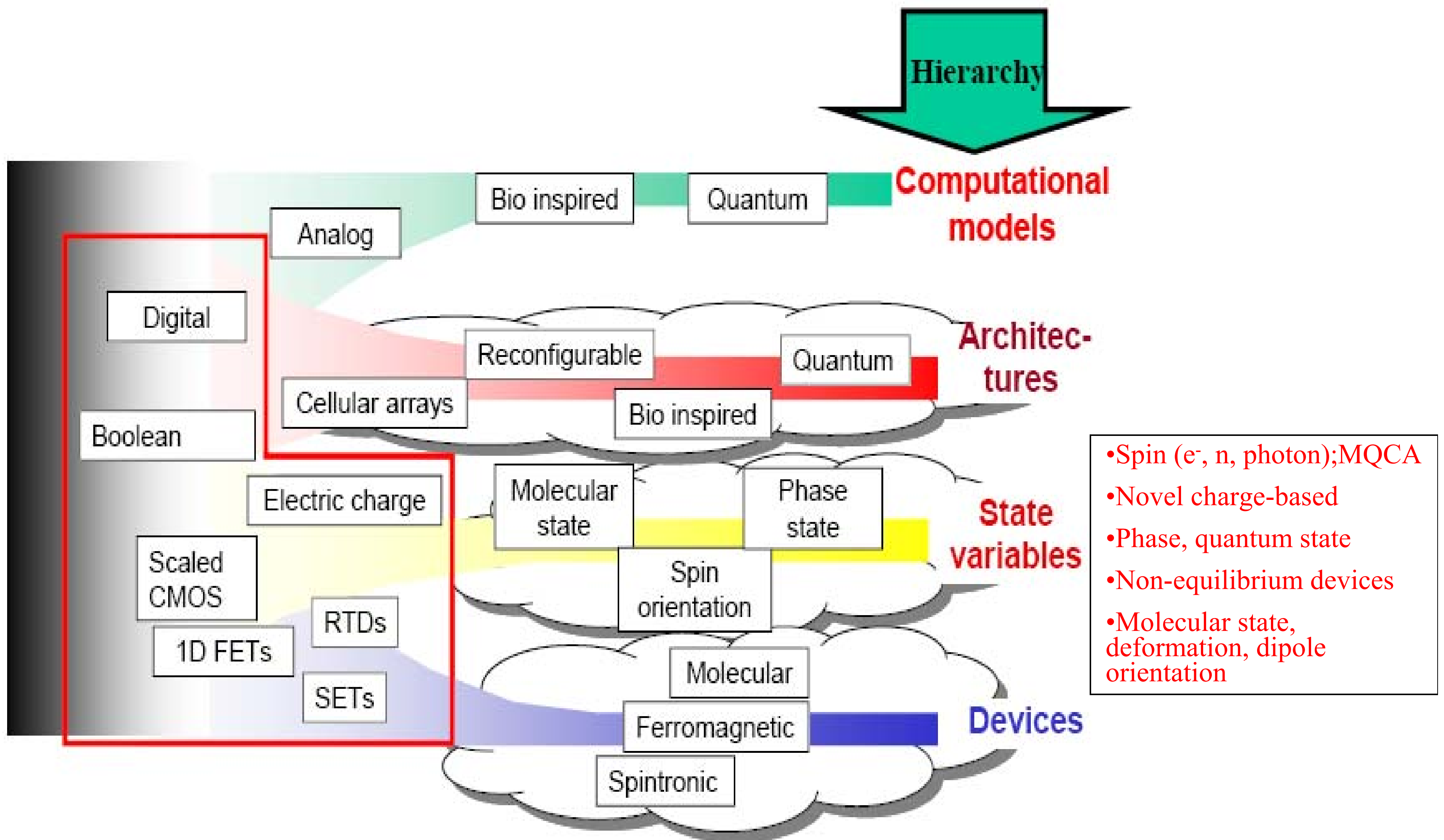
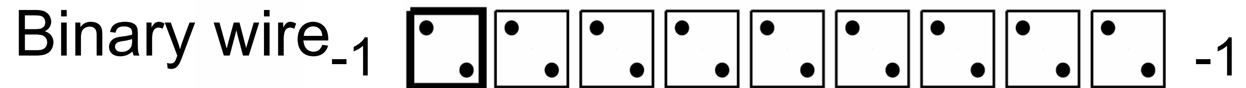


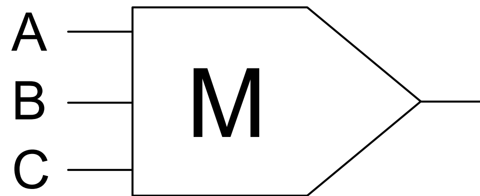
Figure 51 A Taxonomy for Nano Information Processing

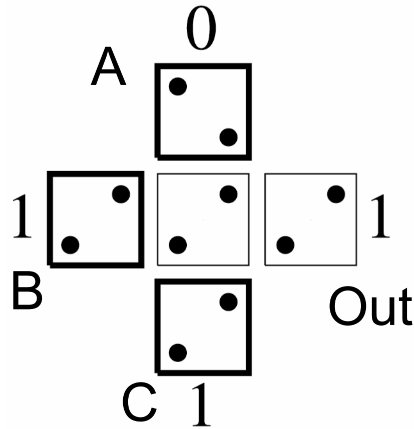
Nanomagnet-Based Logic- MQCA

Wolfgang Porod and Gary Bernstein, Univ. Notre Dame

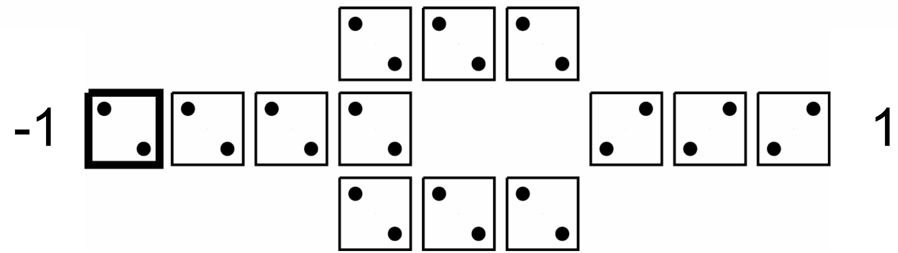


Majority gate

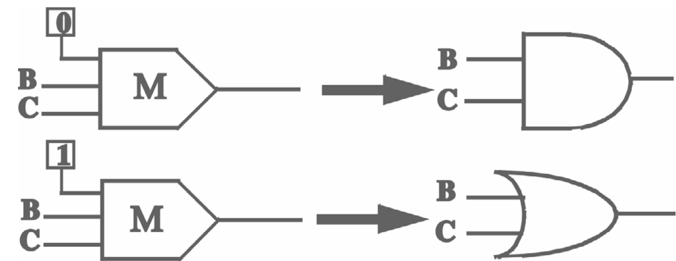




Inverter



	A	B	C	Output
AND gate	0	0	0	0
	0	0	1	0
	0	1	1	1
	0	1	0	0
OR gate	1	1	0	1
	1	1	1	1
	1	0	1	1
	1	0	0	0



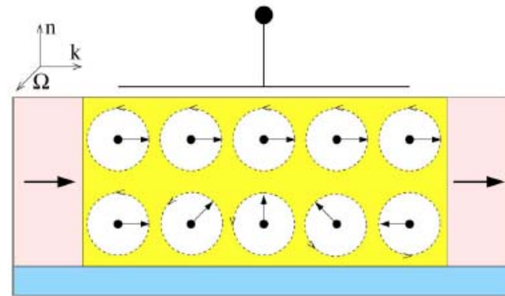
Programmable 2-input AND or OR gate.

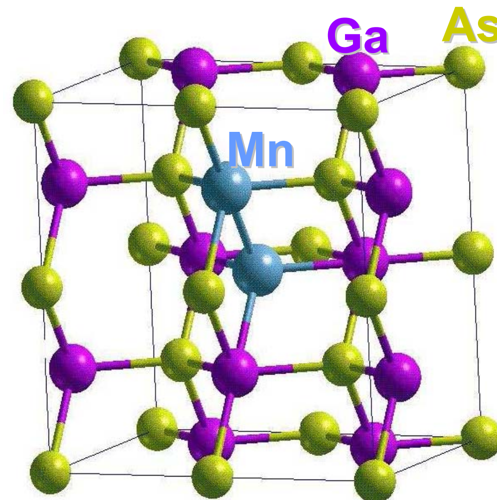
DILUTED MAGNETIC SEMICONDUCTORS (DMS)

Novel materials that coalesce ferromagnetism and semiconducting properties

Datta-Das Spintronic transistor –

magnetoresistance controlled by gate voltage by Rashba effect



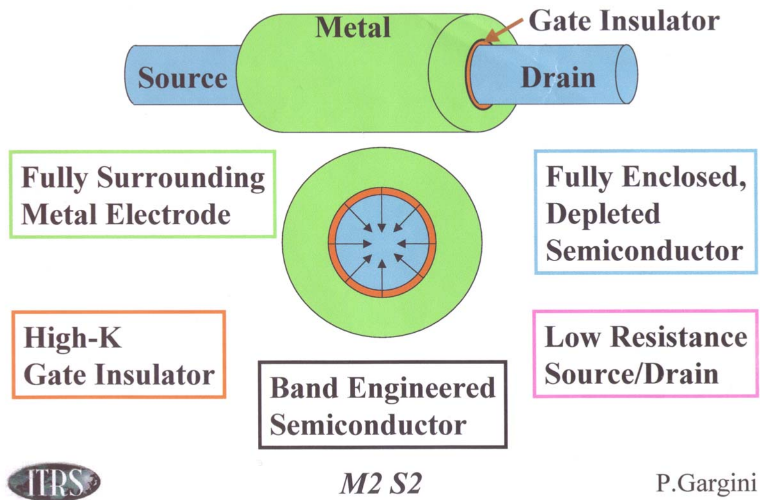


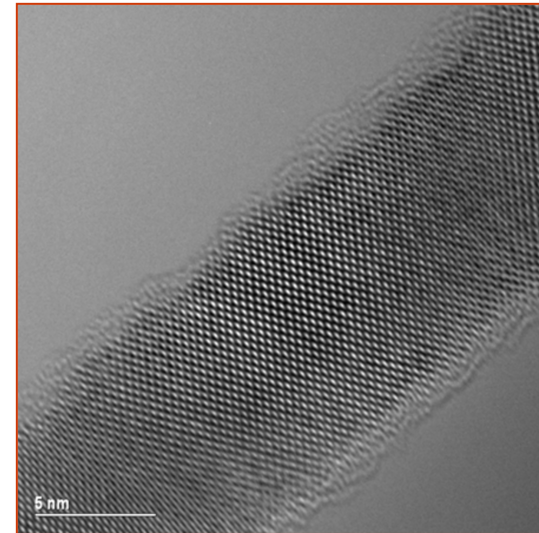
Mn - (~1-10%)
Mn has spin 5/2
and acts as acceptors:
Hole mediated FM

(Ga,Mn)As -excellent DMS except for record FM T_C ~ -100 ^oC

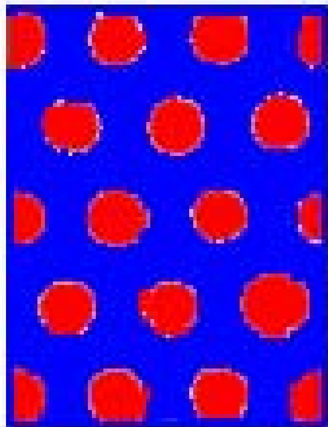
Jungwirth, Mašek, Sinova, MacDonald, Rev. Mod. Phys. in press

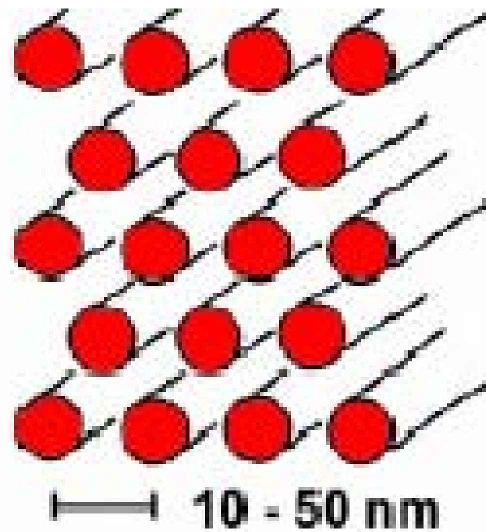
Phasetronics: Nanowire Bundle FETs- Quantum Interference Devices?

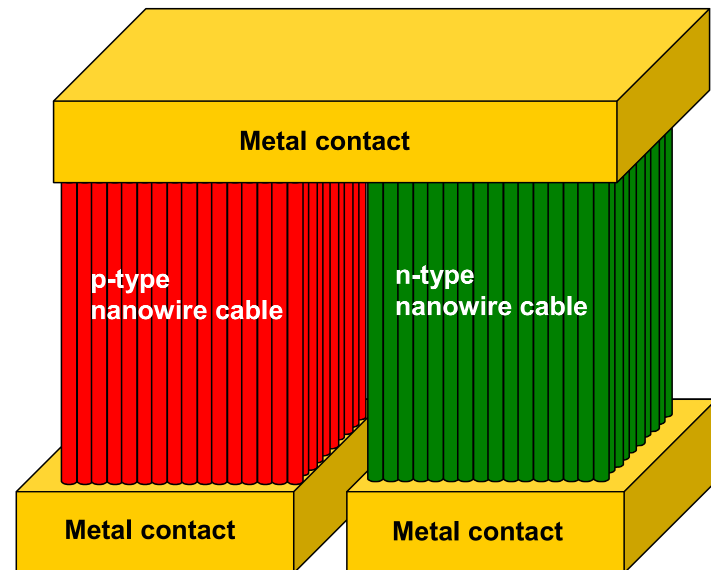




Ge nanowire with SFLS, Korgel







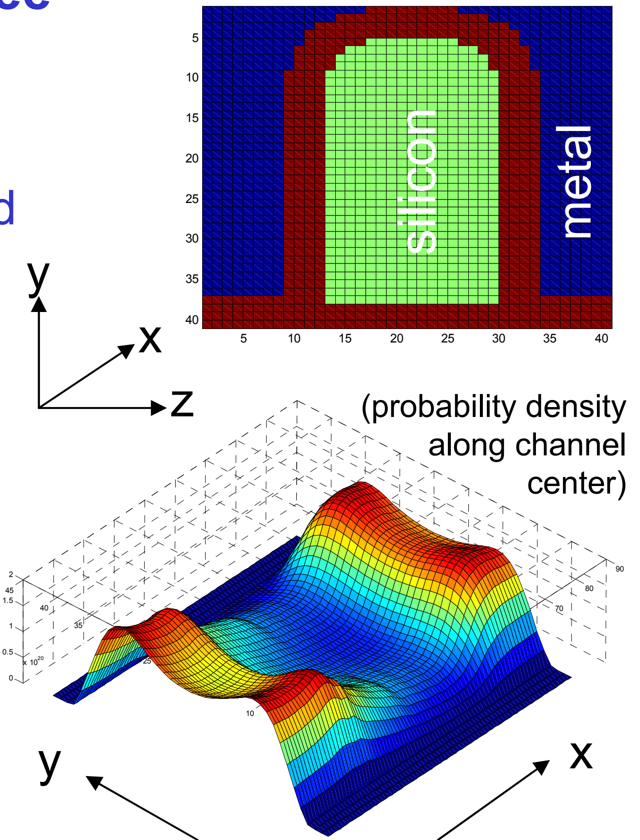
Green's Function Quantum Transport for "phasetronic" Devices

Register, Gilbert, Banerjee

- Foundation of existing first-principles semiclassical and quantum transport simulation tools **(SEMC)**
- Addition of novel device physics, e.g., spin & spin precession, spin scattering/relaxation mechanisms

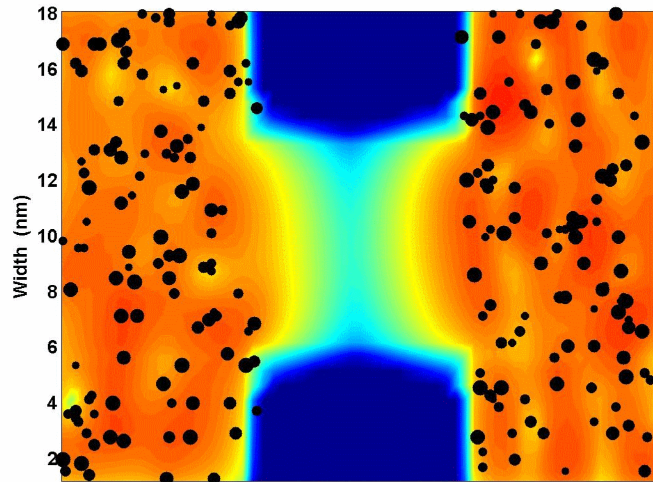
:

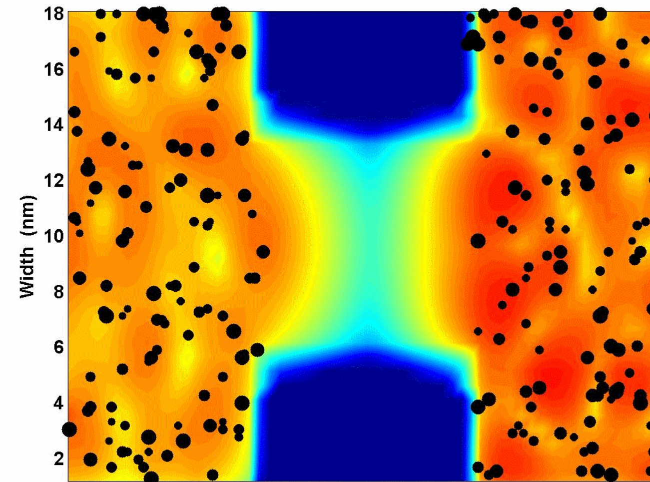
- Interplay of multiple complex physical effects in possible novel switching devices
  - momentum, energy and spin scattering
  - full band-structure
  - strain
  - quantum confinement



Self-consistent electron transport through quantum wire transistor *subject to acoustic and optical intravalley and intervalley phonon scattering*

SR Induced degradation



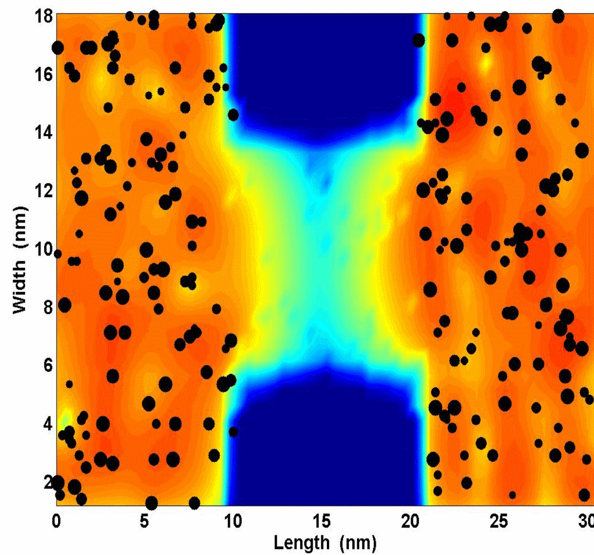


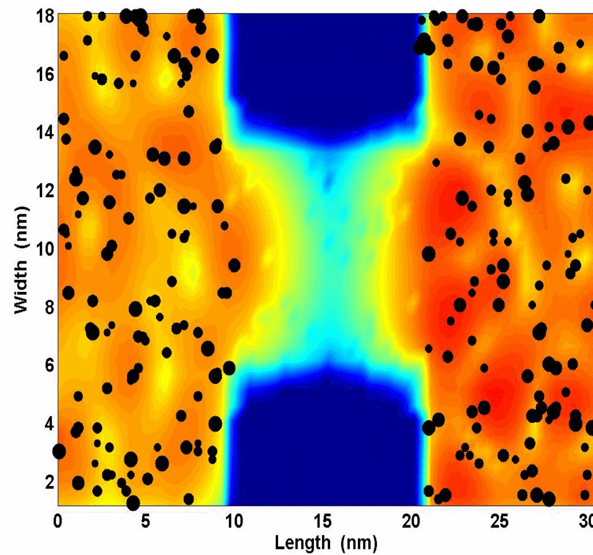
- 0.20 V

- 0.07 V

0.07 V

0.20 V





0.33 V

0.47 V

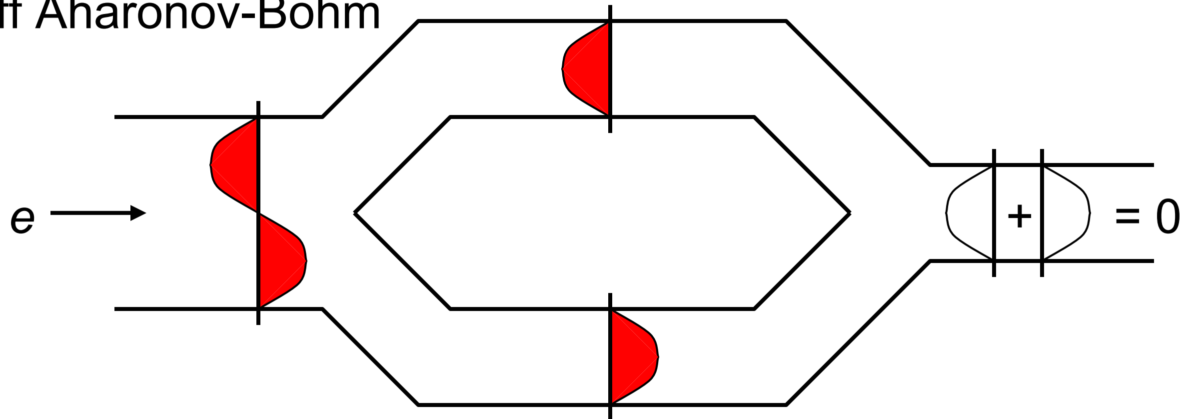
0.60 V

Nearly Ballistic Behavior

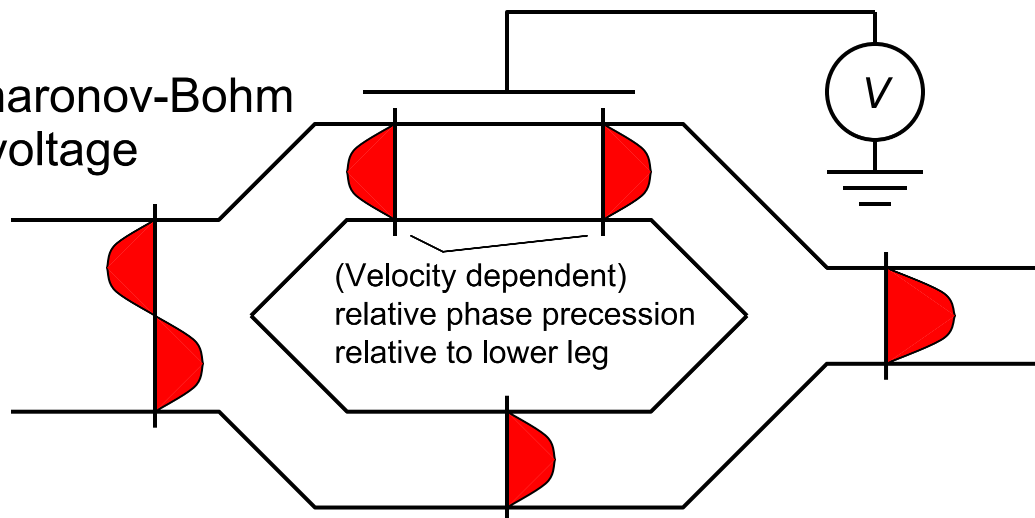
Severe Degradation

Normally-off Aharonov-Bohm device

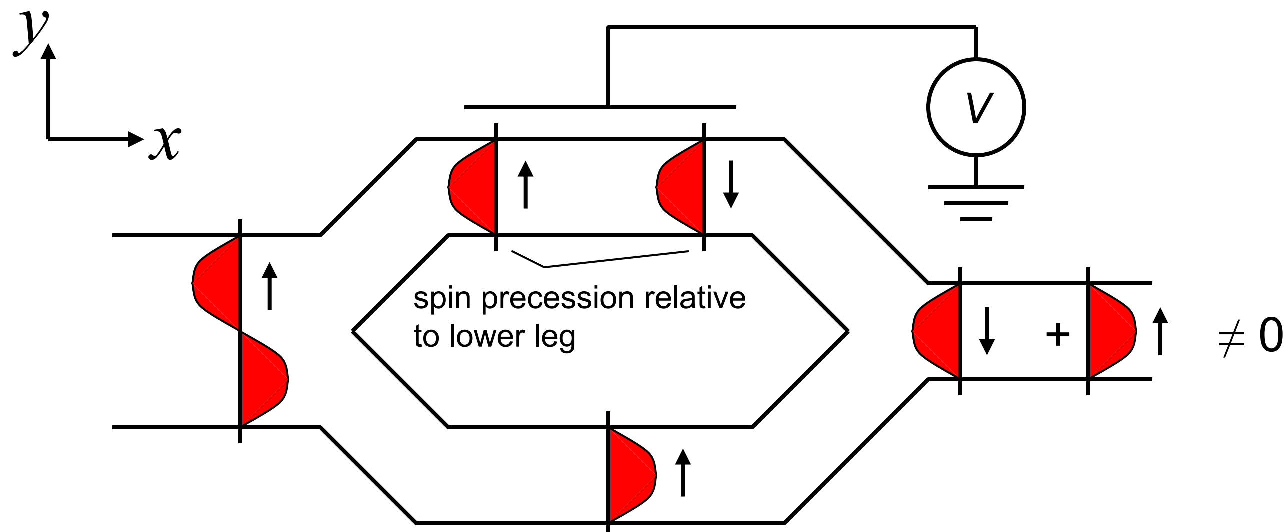
Normally-off Aharonov-Bohm Device



Normally-off Aharonov-Bohm Device + gate voltage



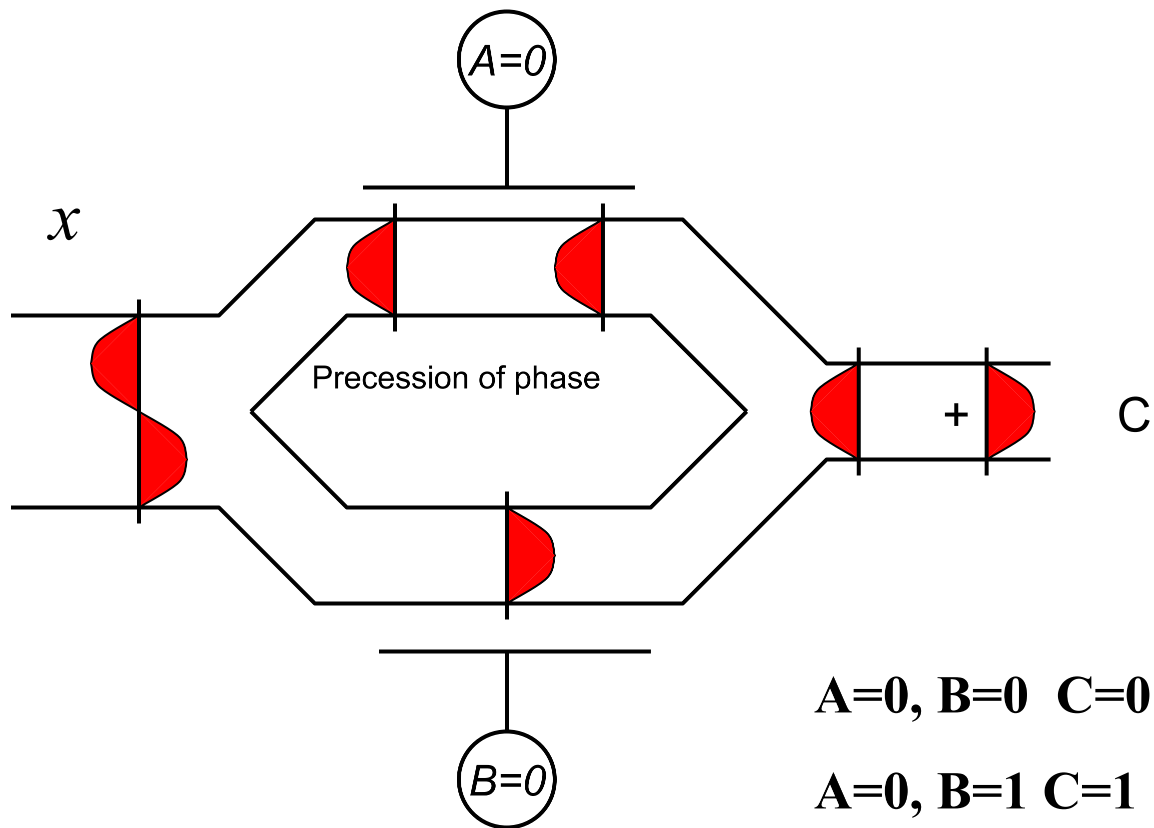
Spin (and spin precession about a magnetic field or due to the spin-Rashba effect)



$$\hat{H}_{Rashba} \cong \frac{\alpha_y}{\hbar}(\hat{\boldsymbol{\sigma}} \times \hat{\mathbf{p}})_y$$

$$\hat{H}_{Zeeman} \cong \frac{\mu_B g_s}{\hbar}(\mathbf{B} \cdot \hat{\boldsymbol{\sigma}})$$

EX OR Gates



A=0, B=0 C=0

A=0, B=1 C=1

A=1, B=0 C=1

A=1, B=1 C=0

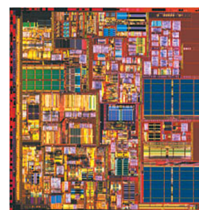
Task 4: Novel Interconnects- Plasmonics

(Massoud, Halas, Nordlander, Rice University, TX)

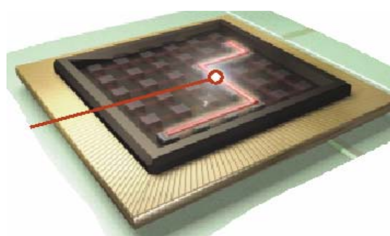
Continuing Need for High Performance Integrated Circuits

- Tomorrow's computing applications demand greater performance: processor speed, memory, low power, smaller size and portability
- Technology scaling required to meet demands

Nanoscale Integration Challenges



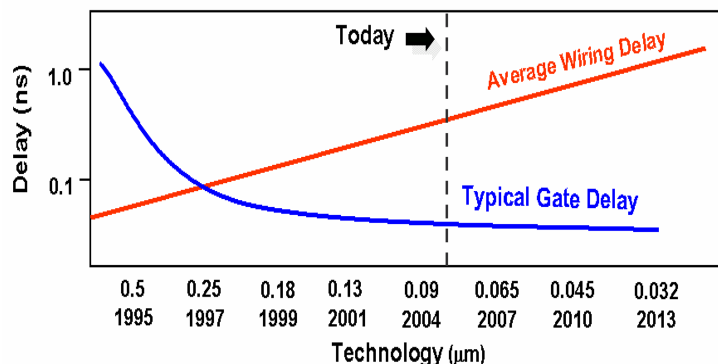
- Interaction between different physical domains: Analog, Digital, Photonic, and Spintronic Devices and interconnect
- Complex due to increasing number of devices per chip
- Need to capture complex phenomena at the nanoscale level
- Need efficient modeling to facilitate solutions for nanoscale ICs



Nanoscale On-Chip Communication Solutions

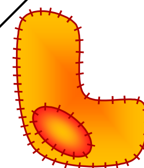
Scaling of Copper Interconnect Intractable for Future ICs

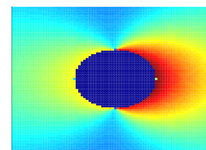
- Increase of delay and crosstalk
- Power consumption and electromigration



Nanoscale Modeling Solutions

- Nanoscale electronics will require new modeling paradigm
- Efficient Modeling Techniques (Fast and Accurate)
- Integrated Modeling Platform to efficiently characterize complex systems (analytical methods + fast computational techniques)
- Automate the design process to generate OPTIMUM and ROBUST designs
- Paradigm has already proven effective in traditional designs

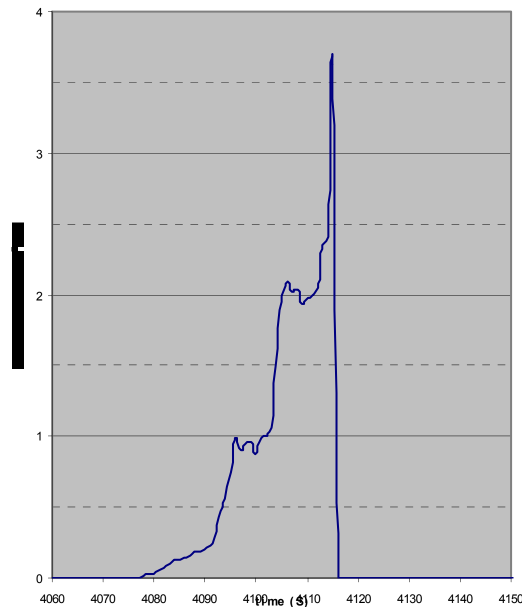


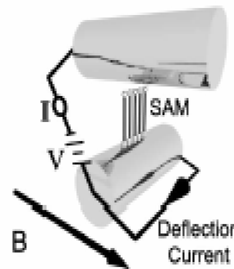


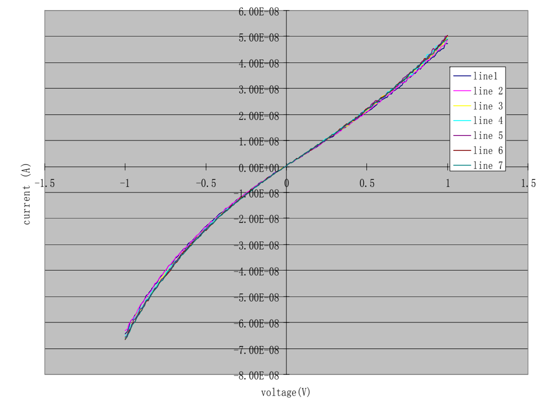
Task 5: Nanoscale Metrology

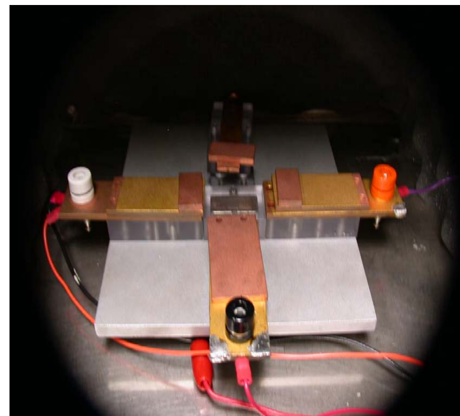
UT Dallas- Gnade, Kim, Wallace

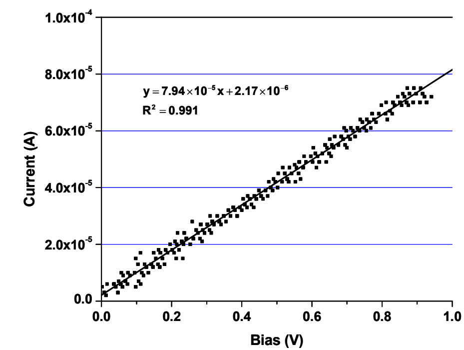
- Quantum contacts
  - Determine impact of material on quantum contact conductance
- Physical characterization
  - Determine spatial and strain limitations of CBED
- Electrical characterization
  - Determine limits for in-situ nano-probing







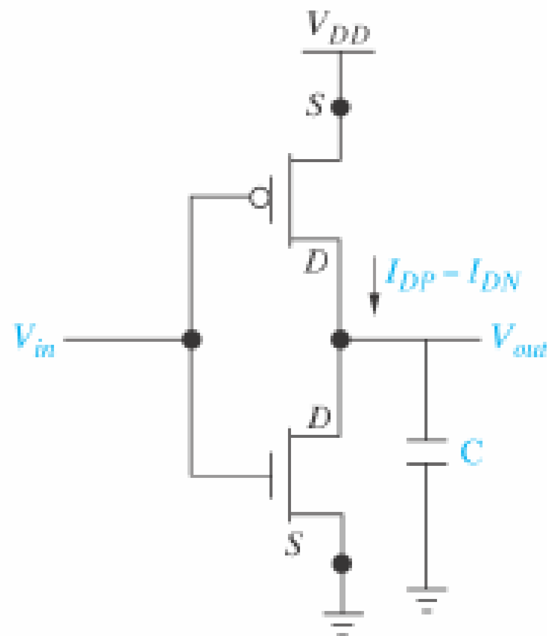




Ballistic transport through one single conduction channel

$$G_0 = 2e^2/h = (12.9\ K\Omega)^{-1}$$

What is needed in the new switch?



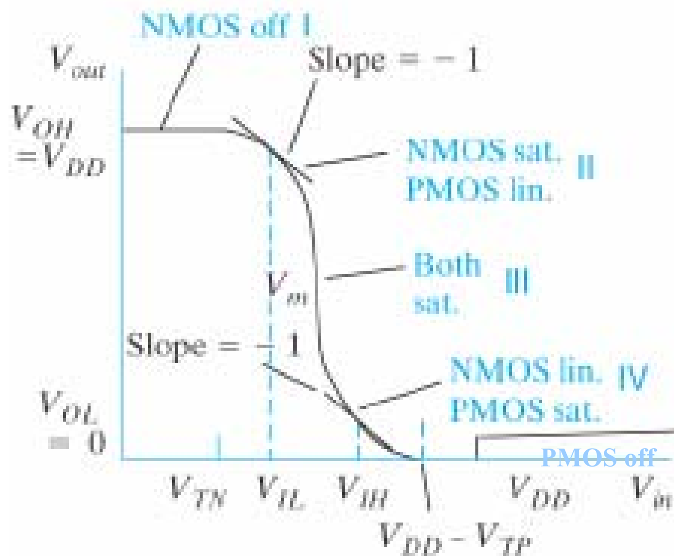
CMOS *ca* 2020

- ➢Energy ~ 10 aJ/op; power~ 10^7 W/cm^2
- ➢Speed ~ 0.1 ps/op (10 THz f_T; 100 GHz circuit)
- ➢Size ~ L_g 5 nm; cell ~ 100 nm, I_{DN}~ 3 mA/µm
- ➢Density ~ 10^{10} cm^{-2}; BIT ~100 GBit/ns/cm^2
- ➢Cost ~ 10^{-12} \$/gate

Speed = CV/I

Active Power = CV^{2}f

Stand-by Power = Sub-V_T, gate leakage



Desirable Attributes

- •Energy efficiency
- •Speed (performance, noise)
- •Room T operation (non-equilibrium devices?)
- •Size (device/ wafer): capacitance, fan-out
- •Gain; uni-directional signal flow (I/O isolation)
- •Reliability, manufacturability, cost
- •CMOS compatibility (process, topology)