Accelerating the next technology revolution

Frontiers Of Characterization and Metrology for Nanoelectronics

Overview Of 3D Integration Requirements

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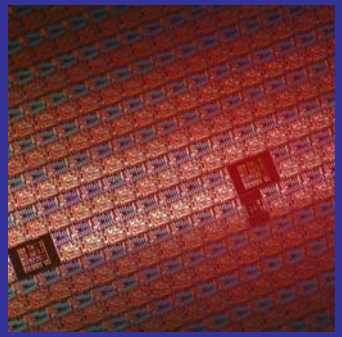
Andrew C. Rudack



3D Interconnect Development
May 13, 2009

Outline

- The Promise of TSVs
- Process & Integration Considerations
- Challenges
- The Need for Roadmaps
- Conclusions

IC Scaling – the Future

- Shrinks have driven density and performance
  - Lithography requires immersion, double exposure, double patterning and EUV to maintain shrink roadmap
  - Transistors require high k dielectrics, metal gates and 3D structures (FinFETS)
  - Metallization requires complex low k dielectric integration

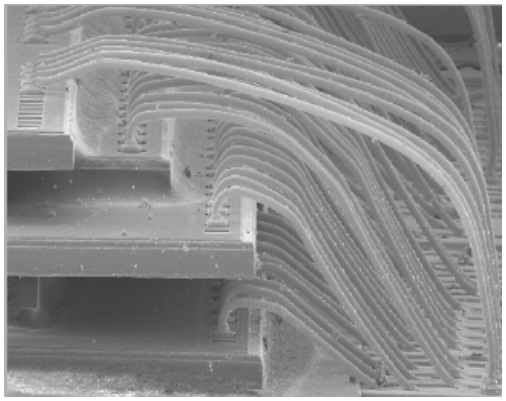
    ➔ Steadily rising Process Complexity
- 3D stacking can provide high density
  - With delayed introduction of above elements of conventional scaling
  - Without area driven yield penalty (stacking smaller die instead of a large 2D die)*
- Short Through Silicon/Substrate Vias (TSVs) can reduce interconnect delay compared to long lines in 2D**

  ➔ TSVs can contain rising complexity by extending technology lifecycles

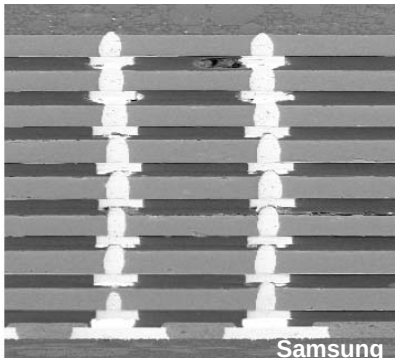
* L Smith (SEMATECH) - 3D Architectures for Semiconductor Integration and Packaging 2007

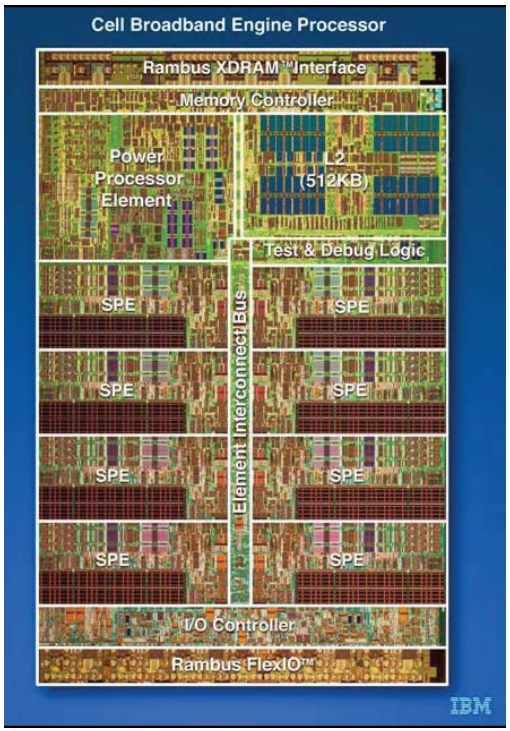
** S. Vitkavage (SEMATECH) – 3D Architectures for Semiconductor Integration and Packaging 2005

Through Silicon/Substrate Vias



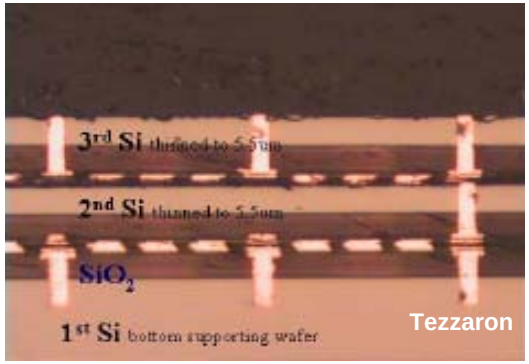
SiP:
- Low cost
- High Functionality





TSV:
- High Performance
- High Functionality
- Lower Power
- Lower Cost?

SoC:
- High Performance
- High Functionality



Benefits of 3D ICs With TSVs

- Improved form factor
  - Can provide smaller footprint and/or increased density
  - Can result in higher yield
- High Functionality
  - Improved integration of heterogenous technologies, materials and signals over SoC
- High Performance
  - High bandwidth and shorter wires (lower RC)
- Lower Power Consumption
  - Shorter wires and lower overall I/O count
- Cost Containment Potential
  - **Device level:** Addresses slowdown in productivity gain (from scaling)
  - **Die level:** Functionality, performance, power reduction (compared to SoC)
  - **Wafer level:** Parallelism of fab processing
  - **Factory level:** Optimizes cost structure for each “level” in 3D stack
  - **Market level:** Short Time To Market for products

3D Drivers

Product Needs/Applications	Technologies
Density/form factor	
– Memory stacking	Via-last Wafer-to-wafer or die-to-wafer
Functionality/Performance	
– Processor + SRAM cache	Two-level, face-to-face wafer-to-wafer or die-to-wafer
– Logic + SRAM + DRAM + Flash Memory – 3D equivalent of SoC – Beyond CMOS • Stacking CMOS “levels” with optoelectronics, MEMS, biosensors, etc.	Die-to-wafer heterogeneous integration

TSV Roadmaps (I)

(in Emerging Technologies section of 2007 ITRS Interconnect chapter)

Table INTC6 High Density Through Silicon via Draft Specification

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Minimum Interlayer HDTSV Contact Pitch (µm)									
High Density	3.2–5.0	2.9–4.4	2.6–3.8	2.2–3.4	2.0–3.0	1.6–2.6	1.4–2.2	1.3–2.0	1.0–1.7
HDTSV Diameter (µm)									
High Density	1.6–2.5	1.4–2.2	1.3–1.9	1.1–1.7	1.0–1.5	0.8–1.3	0.7–1.1	0.6–1.0	0.5–0.9
Maximum Via Density (cm^2)									
High Density	9.77E+0.6	1.21E+07	1.53E+07	1.99E+07	2.31E+07	3.91E+00	4.82E+07	6.10E+07	9.61E+07
Minimum Face-to-Face Pitch (µm)									
High Density	5.00	4.38	3.83	3.35	2.93	2.56	2.24	1.96	1.72
Maximum Layer Thickness (µm)									
High Density	7–25	7–25	7–25	6–20	6–20	6–20	5–15	5–15	5–15
Total Thickness Variation (µm)	<1			<0.75			<0.5		

"Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2007 Edition."

TSV Roadmaps (II)

(2007 ITRS Assembly & Packaging Section p 34)

Table AP7 Key Technical Parameters for Stacked Architectures Using TSV

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
Numbers of stacked die using TSV	3 – (8)	6	9	>9	>9	>9	>9
Minimum TSV pitch	10.0	8.0	6.0	5.0	4.0	3.8	3.6
TSV maximum aspect ratio**	10.0	10.0	10.0	10.0	10.0	10.0	10.0
TSV exit diameter(um)	4.0	4.0	3.0	2.5	2.0	1.9	1.8
TSV layer thickness for minimum pitch	50	20	15	15	10	10	10

***This applies for small diameter vias. The larger diameter vias will have a smaller aspect ratio.*

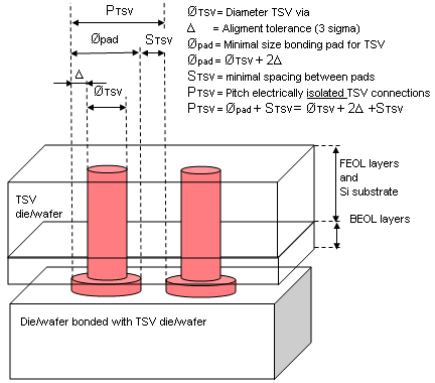
"Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2007 Edition."

ITRS 2008 HDTSV Update

- 2008 Update has been released on public website http://www.itrs.net/

Table INTC6 High Density Through Silicon Via Specification [1]

	2008	2009	2010	2011	2012	2013	2014	2015
HDTSV Diameter, ØTSV (µm) [2], [3]	1.6	1.5	1.4	1.3	1.3	1.2	1.1	1.0
Minimum Interlayer HDTSV Pitch (µm) [4]	3.2	3.0	2.8	2.6	2.6	2.4	2.2	2.0
Minimum Layer Thickness (µm) [5]	10	10	10	10	10	10	10	10
Bonding overlay accuracy, Δ (3 sigma) (µm) [6]	1.5	1.5	1	1	1	0.5	0.5	0.5
Minimum size bonding pad Øpad =ØTSV +2.Δ (µm)	4.6	4.5	3.4	3.3	3.3	2.2	2.1	2.0
Minimum pad spacing, STSV (µm) [7]	1	1	1	0.5	0.5	0.5	0.5	0.5
Minimum contact pitch, PTSV= Øpad + STSV (µm) [8]	5.6	5.5	4.4	3.8	3.8	2.7	2.6	2.5



- Addresses only wafer to wafer integration
- Assembly & Packaging Table has not changed
- Lack of electrical specs and corresponding links in other sections
  - Needs inputs from Design/System Drivers

"Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2008 Edition."

Key Process Elements of 3D ICs

- TSV Reactive Ion Etch
- Dielectric liner, barrier and Cu seed
- Void free TSV fill – process and materials
- Bonding of wafers or dies – process and materials
- Thinning and handling of wafers or dies

- Depending on the integration, certain process steps may be optional
- The order of processing can also change

3D Interconnect Toolset

- Many Familiar Processes/Tools used for 3D Interconnect:
  - Hardmask Deposition
  - Photolithography (typically i-line)
  - Hardmask Etch
  - Damascene/Dual Damascene process flow
    - Barrier/Seed (PVD/CVD)
    - Copper Plate
    - CMP
    - Probers/E-Test
- Metrology already in place (some challenges)
  - Reflectometers, CD-SEM, Dielectric Etchers, Sheet Resistance, Photo Overlay, Defect Detection, Defect Review, …

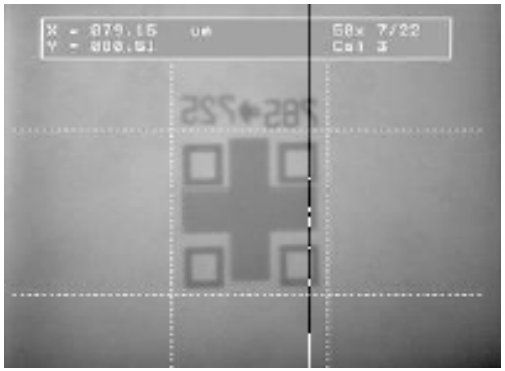
3D Interconnect Toolset

- New/Unique Processes/Tools used for 3D:
  - Wafer Aligners/Wafer Bonders
  - Through Silicon Via
    - High aspect ratio features >10:1 are challenging!
      - TSV Etchers
      - Barrier/Seed (PVD/ALD/CVD/Electro-grafting)
      - Copper Plating (Huge features to fill)
  - Wafer thinning (Backgrind/Chemical)
    - With wafer edge trimming to control chipping
  - Backside Wafer Lithography
    - Align to features at wafer interface
      - No visible alignment features – buried under Silicon

What are the 3D Metrology Challenges

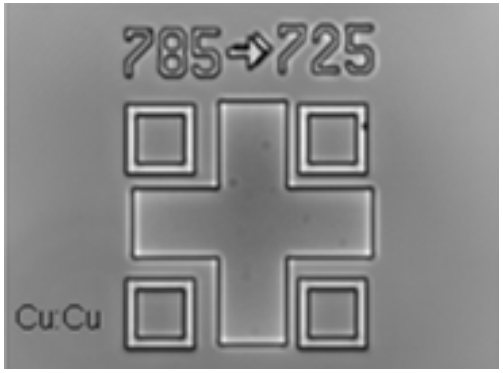
- Bonded Wafer Pairs
  - Silicon is opaque to visible light
- High Aspect Ratio Features
  - Challenge Optical Microscope techniques
- “New” 3D Metrology Techniques Are Indicated
  - Infrared Microscopy via 1310 nm IR (laser)
    - Bonded Wafer Pair Overlay, Defect Metrology
  - Scanning Acoustic Microscopy
    - Void Defect Metrology, Bonded Wafer Pair Overlay
  - Edge Bevel Inspection
  - X-ray Tomography

IR illumination technique improves resolution



Broad Band IR Scope

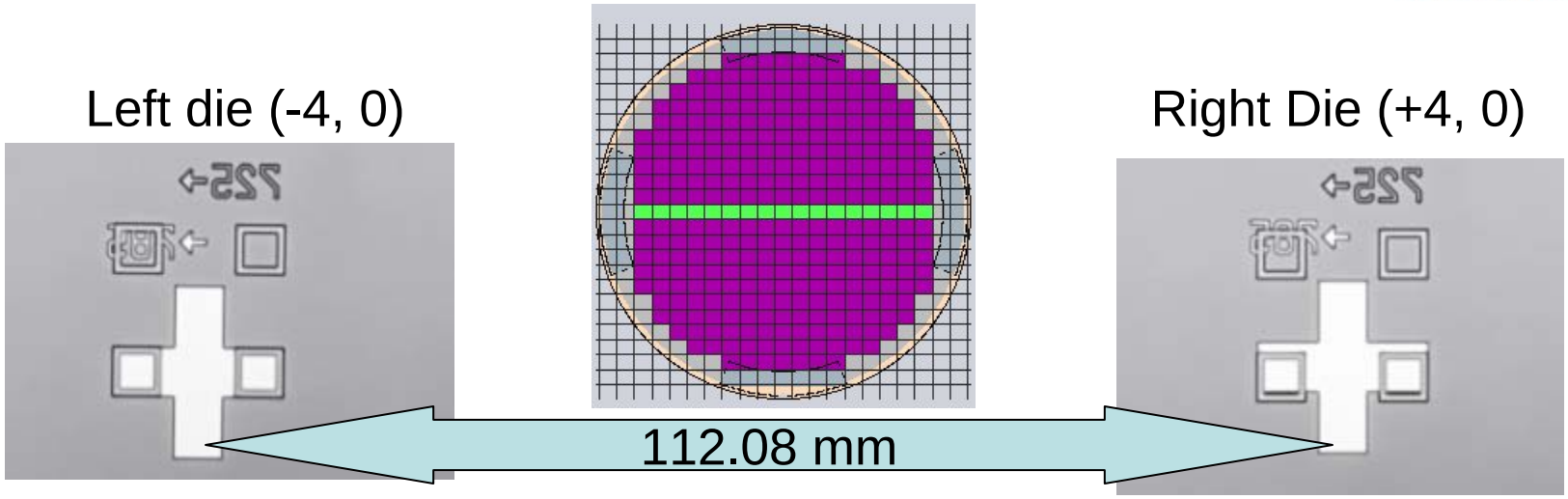
- Usually Halogen Lamp
  - "White" light + heat
- Broadband IR component for IR Illumination



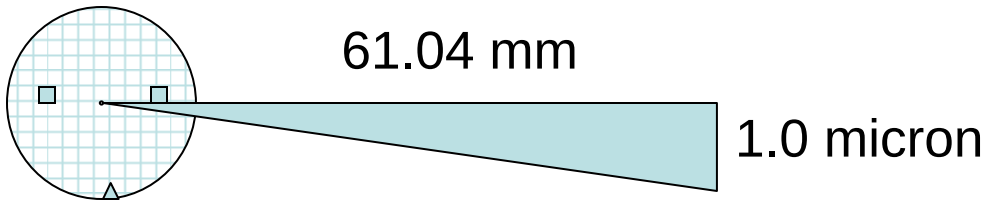
1310 nm Laser Infrared Microscope

- 1310 nm IR Laser for Illumination
- Resolution is improved

IR Scope – Overlay X/Y/Rotation

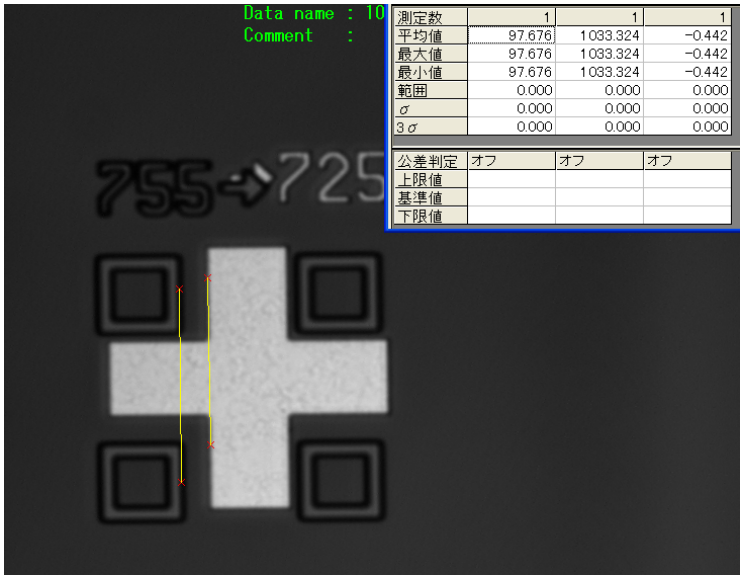


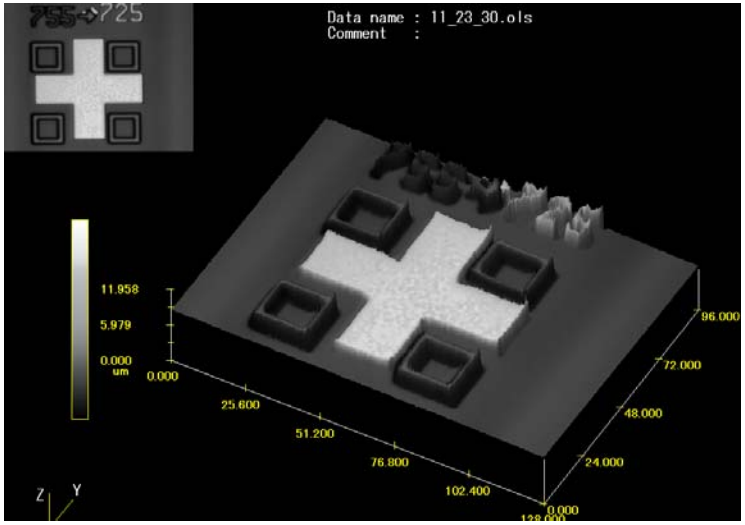
- Overlay measured through 775 microns Silicon!
  - shift in X=+0.2 micron, Y=+26.5 micron
  - apparent rotation can be calculated from wafer center, inducing another y overlay error of 1 micron



  - rotation = 0.939 degrees (clockwise)

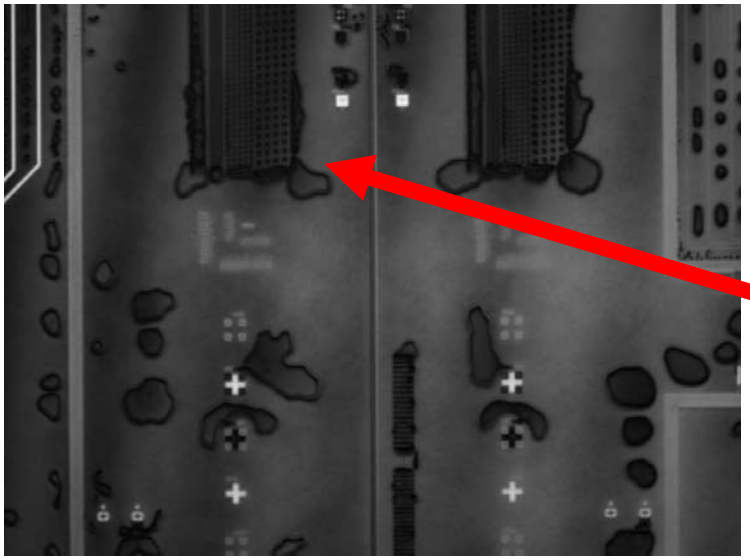
IR overlay





- Measure Overlay Alignment Fiducials
  - Cross on bottom wafer
  - Box on top wafer
  - Bonded Face to Face
- Pictures through 775 microns Silicon
- 3D reconstruction
  - explore wafer thickness remaining through IR confocal microscope techniques

Defects - IR Scope



IR view of bonded wafer
Surface through 775 microns Silicon

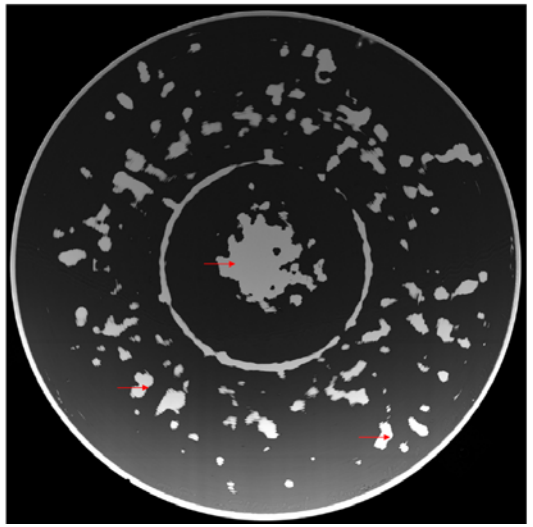
Incomplete bond material coverage over topography–

Conformal bond material flowing into over-etched alignment target

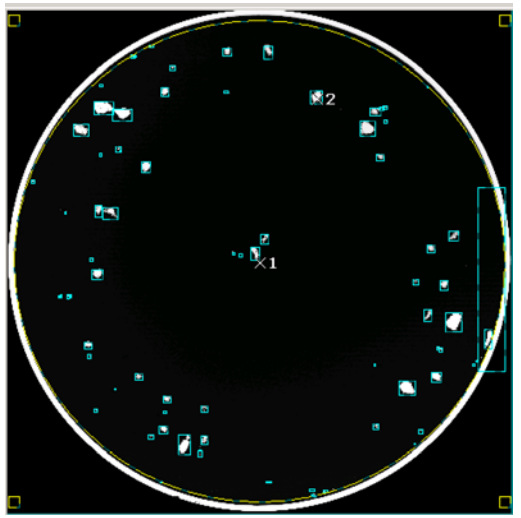
Scanning Acoustic Microscope (SAM) Bonder Process Development

Cu-Cu bond

- process improved by using scanning acoustic microscopy (SAM) for void detection, 13% voids decreased to < 1%



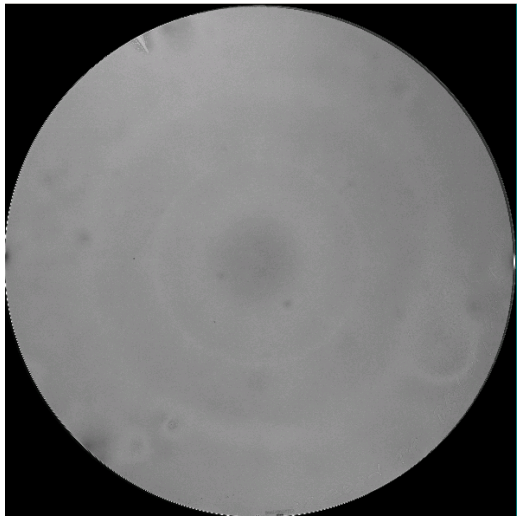
Cu-Cu in June 2008



Cu – Cu in August 2008

BCB bond

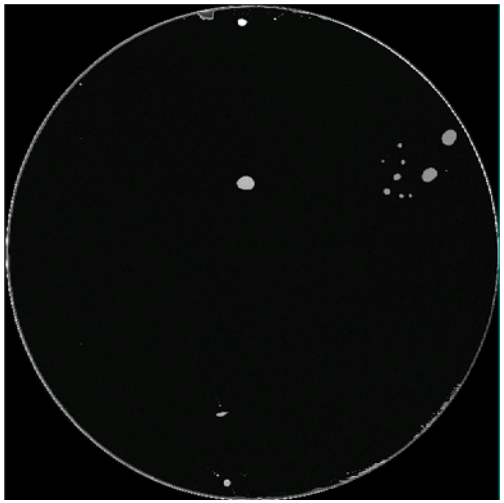
- Coat defects (pie slices) identified by SAM in the interface of a bonded wafer pair



BCB Bonding

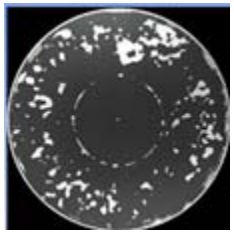
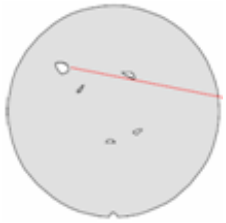
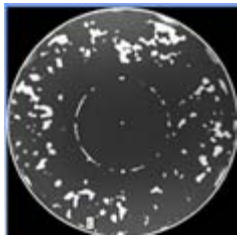
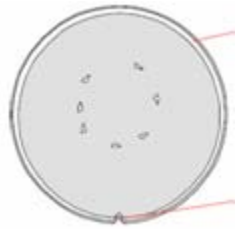
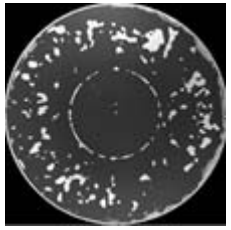
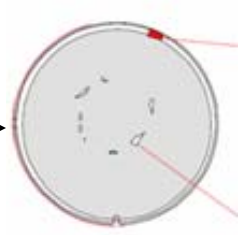
Oxide/oxide fusion bonds

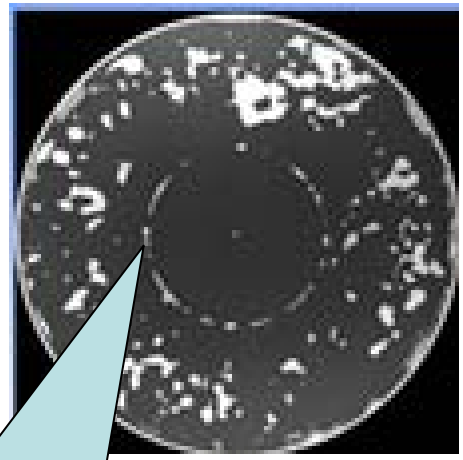
- Voids in the interface of a bonded wafer pair caused by particles, distinctive bulls-eye pattern



Oxide/oxide Bonding

SAM – Delamination Post Thinning

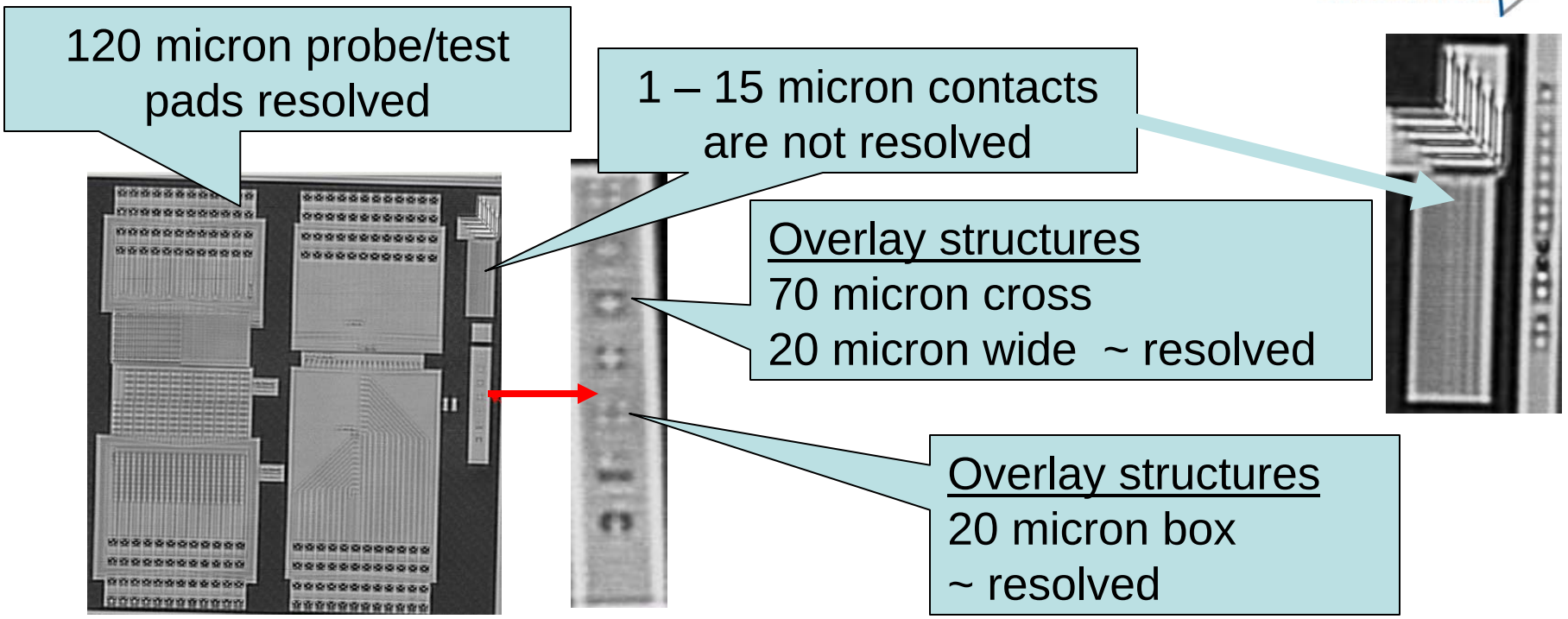
	Post bond SAM (Before Thinning)	Delaminations (Post thinning)
50 micron		
30 micron		
20 micron		



Center ring void defect is manifested as a delaminated ring after bonded wafer pairs are thinned.

Fix the bonder!

SAM as overlay metrology tool?

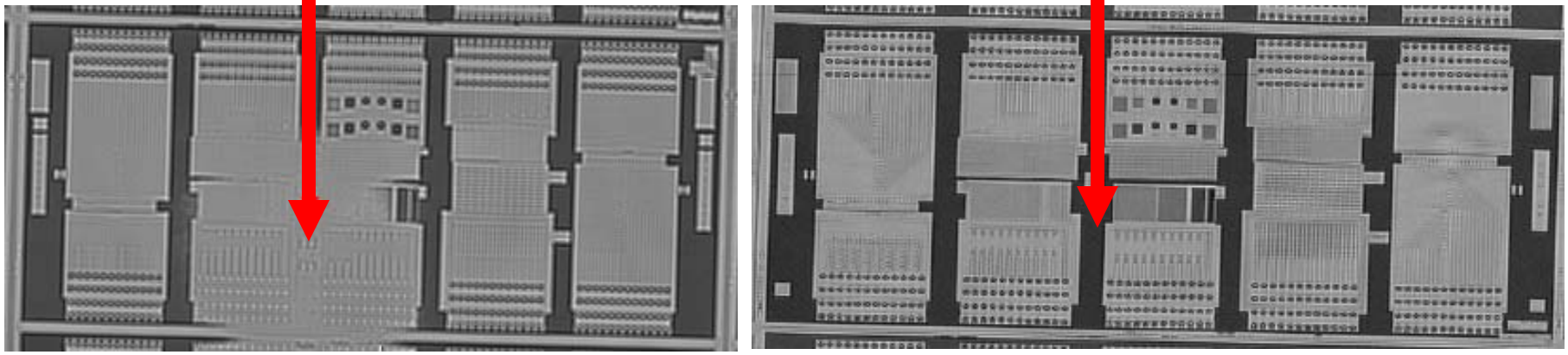


- Investigate improved SAM resolution
  - Post wafer thinning improvements
    - reduced attenuation
  - Higher frequency/shorter focal length transducers
    - Have in-house 110/230 MHz capability, and supports 300MHz

SAM - Pattern defects revealed in higher resolution mode

~ 2 mm Bond Defect in Copper Dummy Fill

Good Bonds in Copper Dummy Fill

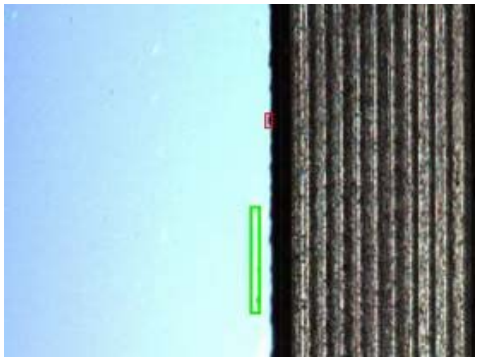


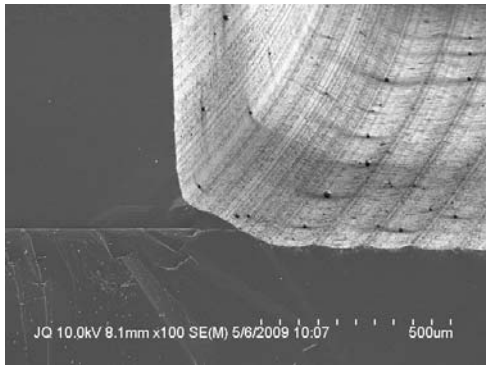
- SAM Metrology indicates voids:
  - Particulate Material between wafers prevented bond if isolated incident?
  - Bonder Hardware issue?
  - Surface contamination?

Edge Bevel Metrology

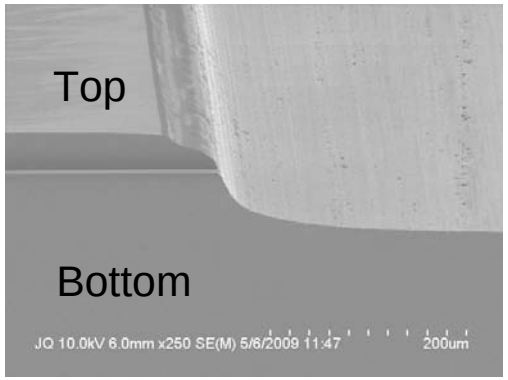
- Thinning Bonded wafer pairs:
  - top wafer edge trimming required to control chipping

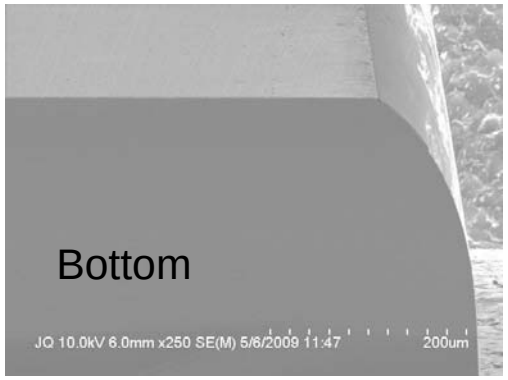
Saw marks/Chipping Evident Using Dicing Saw for ET





Grinding wheel reduced ET defects (saw marks/chips)





Summary

- 3D can be the new engine to keep the industry on the productivity curve
  - High performance
  - High functionality
- Product requirements and roadmaps are key to driving coherence and critical mass for 3D R&D
- 3D is not a single technology element
  - Productivity benefits can be realized at several levels
    - Requires industry wide coordination across technology, design and test
- 3D-specific metrology tools are indicated