



Accelerating Yield



Design for Manufacture in Overlay Metrology

Mike Adel

Optical Metrology Division,
KLA-Tencor Israel

Topics

- Introduction
- Uncertainty Contributors in Overlay Metrology
- Design for Manufacture in Overlay Metrology
- 2 Examples:
 - Sampling and Model Optimization
 - Target Optimization
- Summary

Introduction

- Overlay metrology has become a cornerstone requirement which enables modern lithographic patterning.
- The 2004 ITRS roadmap specifies only “precision” with the qualification that it includes tool to tool matching.
- Metrology engineers in the litho cell use various versions of *Total Measurement Uncertainty, e.g:*

$$TMU = 3\sqrt{\sigma_{precision}^2 + \sigma_{TIS}^2 + \sigma_{matching}^2}$$

Dynamic load unload
repeatability

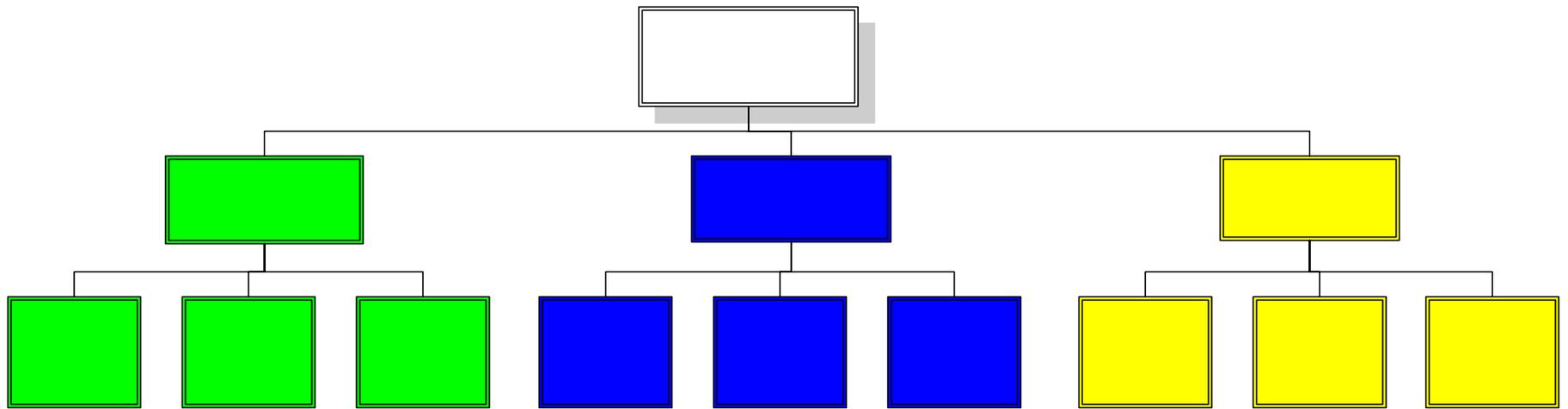
Tool Induced Shift
Variability across wafer

Site by Site matching
across wafer

Introduction cont:

- A wider scope in the definition of the overlay metrology process is required which views it as part of the greater IC manufacturing process.
- The standard contributors to the TMU metric mentioned above do not take into account many additional, ***non-negligible*** effects on the overlay metrology budget, e.g:
 - Unmodeled systematic errors
 - Overlay mark fidelity

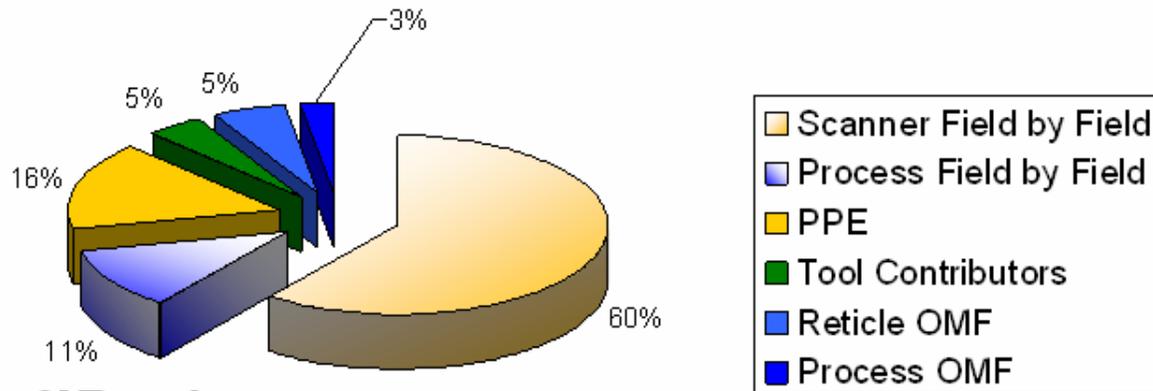
Overlay metrology uncertainty contributors



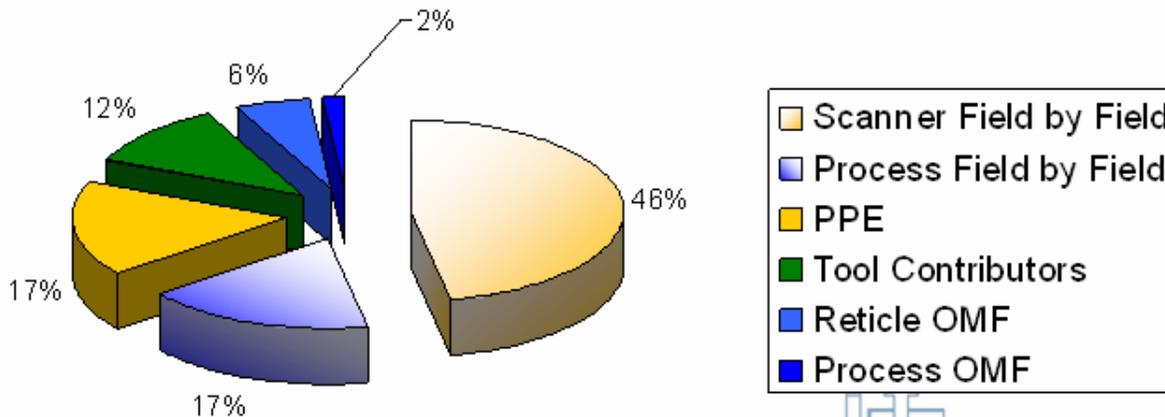
Sources of Residuals

Sources of overall residuals on standard wafer

*Poly-to-Active
FEOL process*



Sources of overall residuals on CMP+ wafer

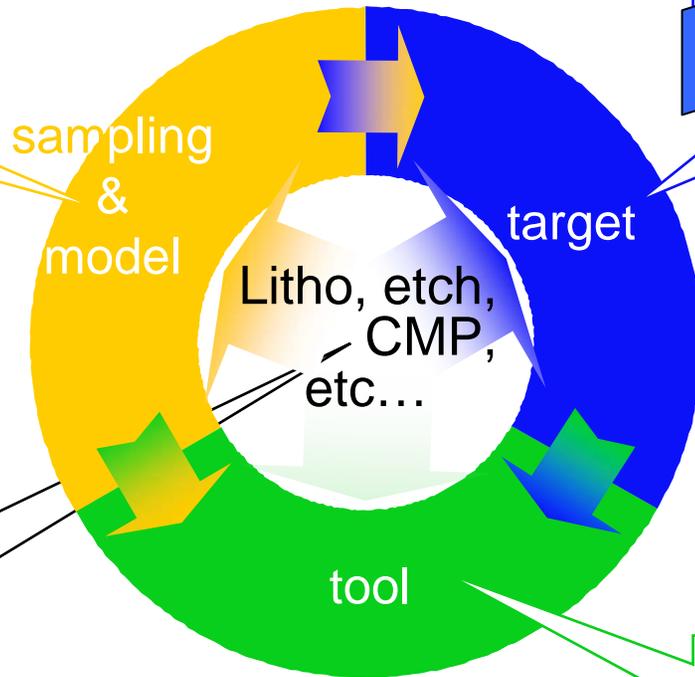


P. Leray, I. Pollentier, E. Kassel, P. Izikson, M. Adel, B. Schulz, R. Seltmann, J. Krause "In field overlay uncertainty contributors" SPIE Vol. 5752, Metrology, Inspection, and Process Control for Microlithography XIX, 2005

Design For Manufacture methodology

Example 1
1. Optimize sampling & model for alignment with manufacturing processes of variation.

Example 2
2. Optimize metrology target for compatibility with manufacturing processes.

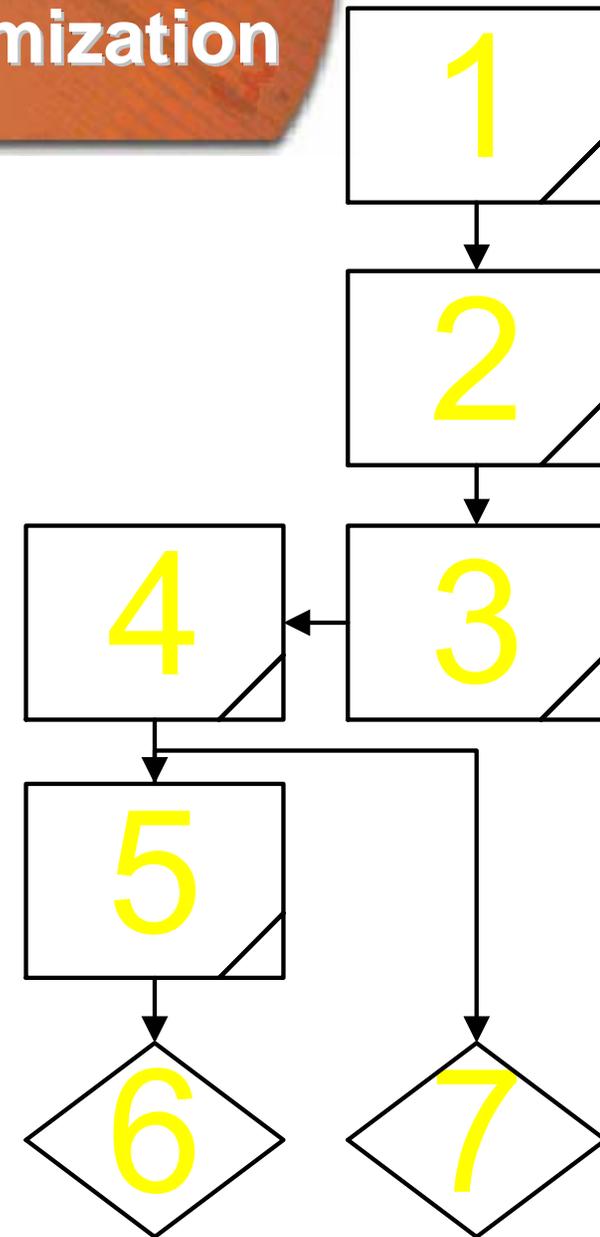


Semiconductor manufacturing processes

3. Optimize metrology tool for compatibility with 1 & 2.

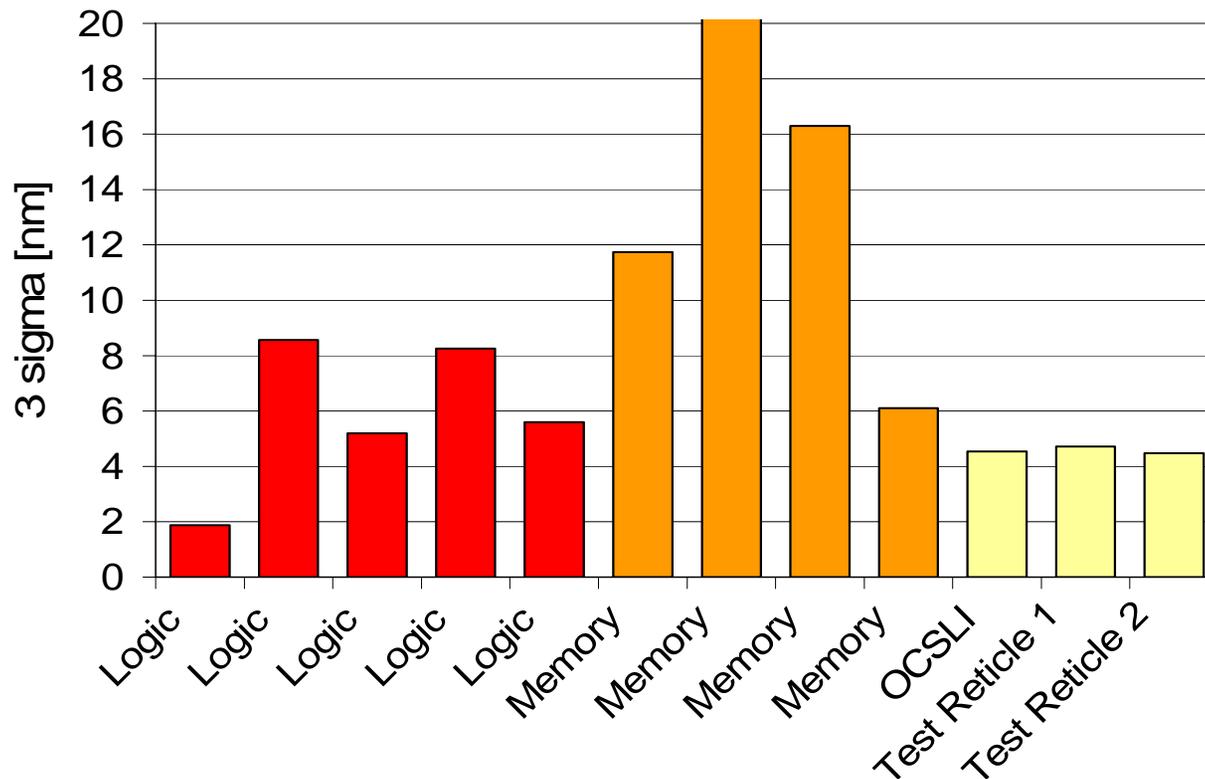
Example 1: Sample & Model Optimization

- Today, the standard method of overlay modeling is the “double pass” method described in the adjacent flowchart.
- Overlay metrology data may show significant *field to field variation* in the intra-field model terms.
- In such cases, an opportunity exists to improve lot dispositioning or correctibles accuracy....



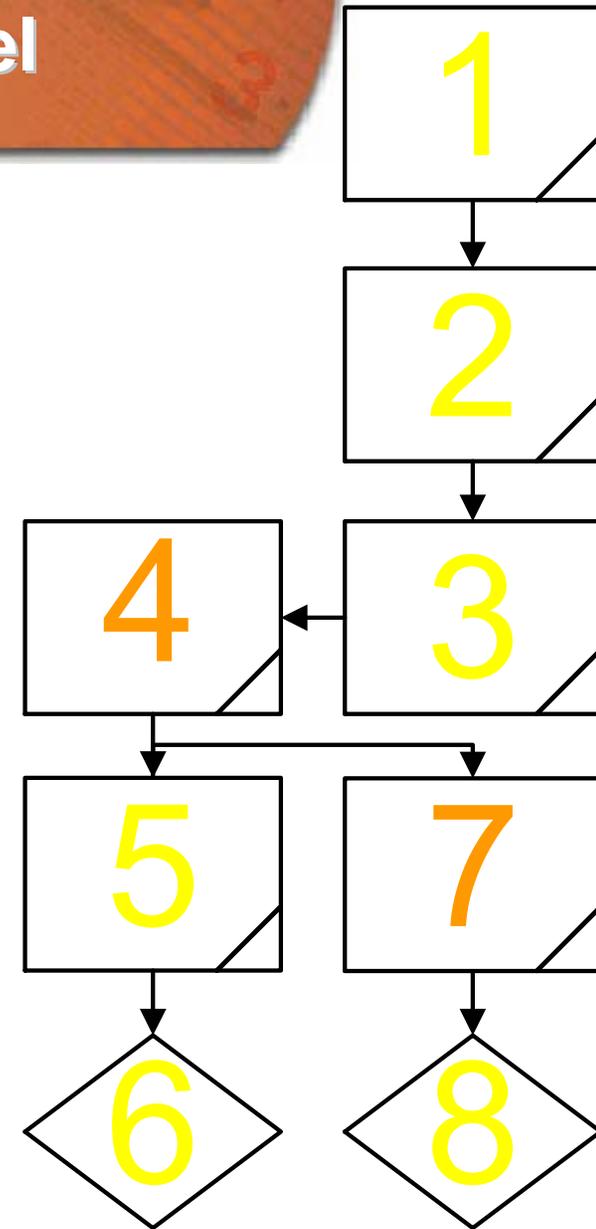
Example 1 cont: field to field variation in intra-field model

- 3 sigma overlay model uncertainty at the field corners due only to the field to field intrafield correctibles variability. Data from 130 and 90 nm processes in both production and R&D environments.



Example 1 cont: Alternative model

- An alternative model is now considered – see adjacent flowchart:
- Lot dispositioning is based on field by field intra-field modeling.
- Intra-field scanner correctibles may now be “field weighted”, instead of a simple average.
- Or a “higher order” correctibles model needs to be enabled.

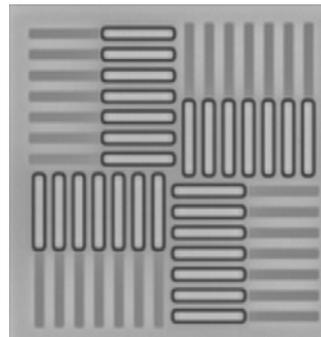
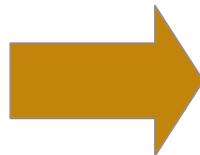
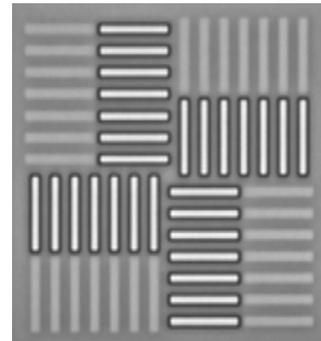
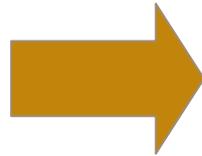
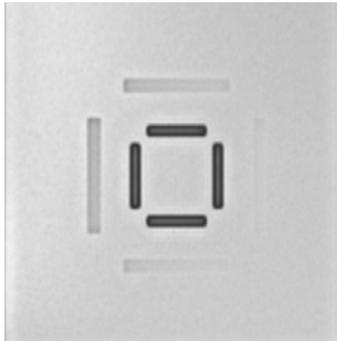


Example 2: Overlay target optimization

- Virtually all semiconductor manufacturers live with model residuals which are well beyond the level anticipated based on metrology tool or lithography process uncertainty contributors.
- Some manufacturers are forced to add costly process steps because the metrology tool/target interaction is negatively impacted by CMP, deposition or etch processes.
- Migration to grating structure targets increases robustness of the metrology process to process variation.

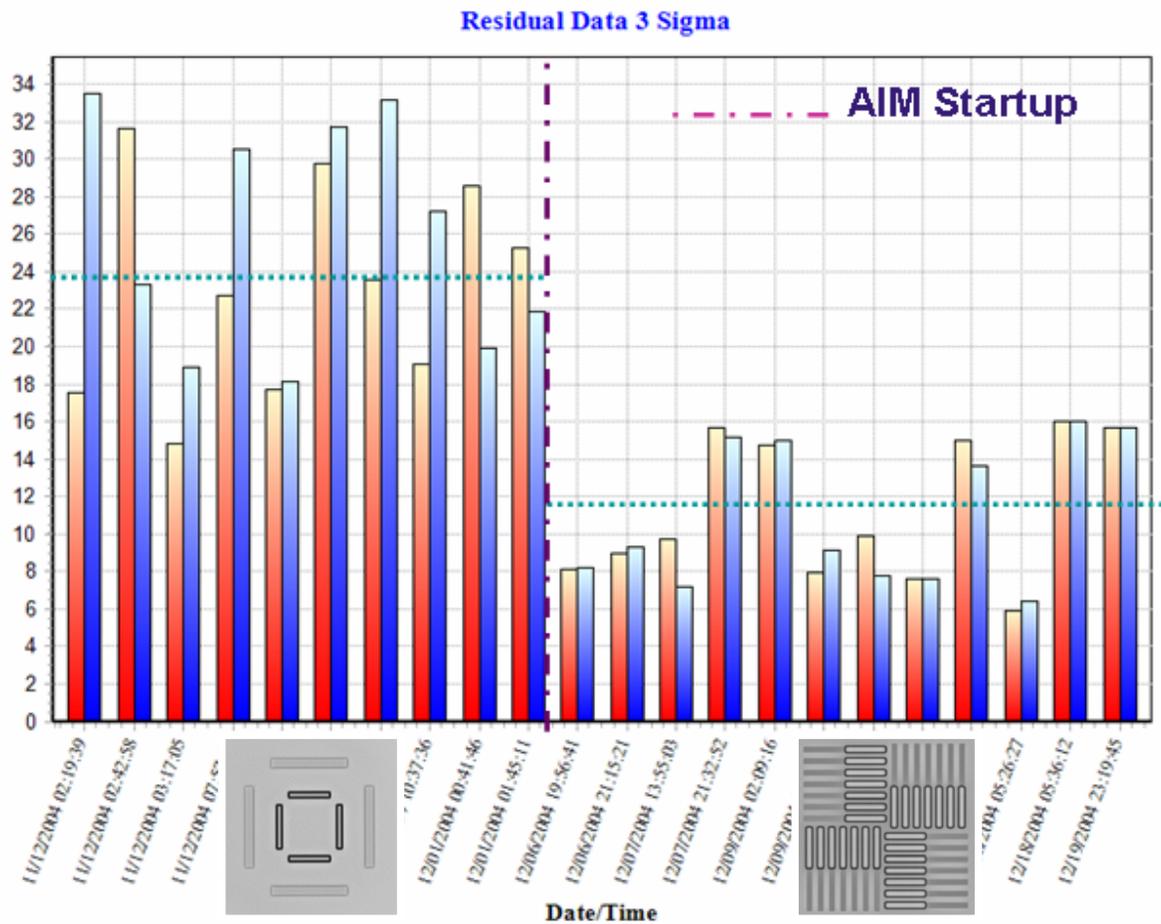
Example 2: 130 nm FEOL memory process

- BiB suffers from low contrast, contrast reversal, varying across wafer.
- AIM target more stable and uniform.



Courtesy of ST Microelectronics

Example 2 cont: overlay model residuals - target optimization



130 nm FEOL flash memory process

Residual Data X 3 Sigma Residual Data Y 3 Sigma

Courtesy of STMicroelectronics - R2 Technology Center - FTM - Lithography, Agrate B. Italy

A word on the metrology tool:

- What does DFM mean for the tool:
 1. Optimize for sample plan, and for the metrology target
 2. Reliability – *MTBF*
 3. Ease of use – *automated recipe setup & optimization**
 4. Peak performance – *all the time*

*"Complete Imageless Solution for Overlay Front-end Manufacturing" D. Herisson, V. LeCacheux, M. Touchet, V. Vachellerie, and L. Lecarpentier, STMicroelectronics, Crolles cedex, France; and F. Felten and M. Polli, KLA-Tencor Corporation, Meylan, France

Summary

- A DFM approach to overlay metrology dictates an optimization sequence as follows:
 1. Optimize model and sample plan for sources of variation.
 2. Optimize target for 1 above and for manufacturing process.
 3. Optimize tool for 1 & 2 and the obvious things...
- Examples of optimization from steps 1 and 2 have been shown:
 1. Model and sample optimization which accounts for significant field to field variation in intra-field model terms has been proposed.
 2. Target optimization for compatibility with manufacturing process, demonstrates reduced overlay model residuals.

Acknowledgments

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