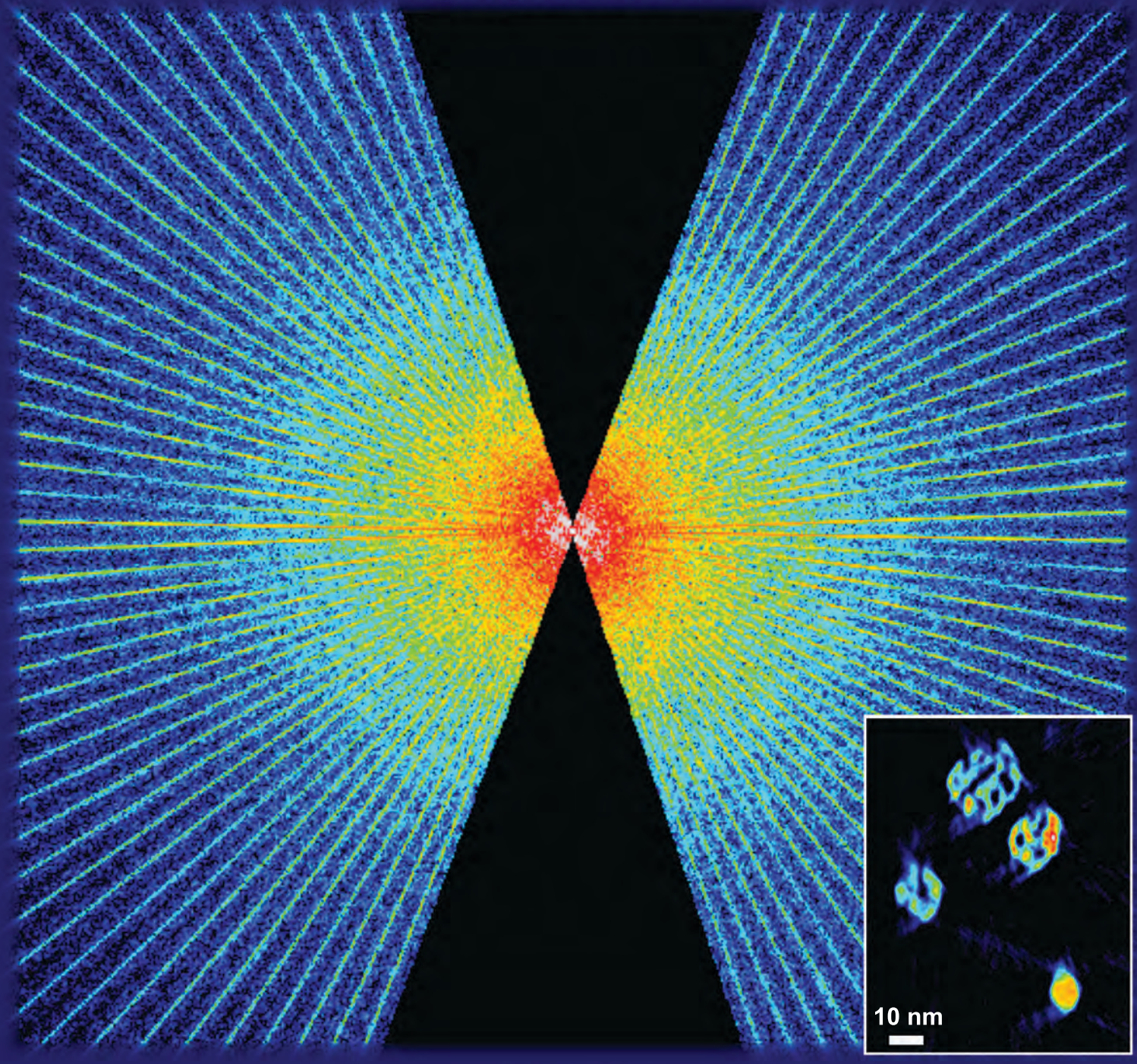
Frontiers of Characterization and Metrology for Nanoelectronics: 2013

March 25-28, 2013
NIST, Gaithersburg, Maryland
www.nist.gov/pml/div683/conference/



Editors:
E. M. Secula and D. G. Seiler

Committee Co-Chairs

David Seiler
National Institute of Standards and Technology (NIST)

Alain Diebold
College of Nanoscale Science and Engineering, SUNY Albany

Bob McDonald
formerly of Intel (Treasurer)

George Thompson
Intel

Amal Chabli
CEA-Leti

Committee Members

- **Luigi Colombo,** TI
- **Michael Current,** Current Scientific
- **Bob Havemann,** SRC
- **Dick Hockett,** Evans Analytical Group
- **Ajey Jacob**, Global Foundries
- **Toshihiko Kanayama,** AIST
- **David Kyser,** Applied Materials
- **Patricia Lindley,** Evans Analytical Group
- **Shifeng Lu,** Micron
- **Zhiyong Ma,** Intel
- **Ulrich Mantz,** Zeiss
- **Lori S. Nye,** Brewer Science, Inc.
- **Yaw Obeng,** NIST
- **Lothar Pfitzner,** Fraunhofer IISB
- **Erik Secula,** NIST
- **Sandip Tiwari,** Cornell University
- **Victor Vartanian,** ISMI
- **Wilfried Vandervorst,** IMEC
- **Usha Varshney,** NSF
- **Ehrenfried Zschech,** Fraunhofer Institute for Non-Destructive Testing

Cover Caption: A through-focal reconstruction demonstrated on porous PtCu nanoparticles with similar dimensions and details to a modern integrated circuit. The through-focal tomography provided a continuum of 3d information in Fourier space and a clear improvement in quality over traditional methods. Figure used with permission from Robert Hovden, Cornell University.

2013 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

Welcome to the 2013 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics (FCMN)! Our goal is to bring together scientists and engineers interested in all aspects of the characterization and measurement technology needed for nanoelectronic materials and device research, development, and manufacturing. All approaches are covered in this conference: chemical, physical, electrical, magnetic, optical, in-situ, and real-time control and monitoring. The conference summarizes major issues and provides critical reviews of important semiconductor techniques needed as the semiconductor industry moves to silicon nanoelectronics and beyond. It is hoped that the invited talks, contributed poster papers, and informal discussions will be a stimulus to provide practical perspectives, breakthrough ideas for research and development, and a chance to explore collaborations and interactions on a world-wide basis.

We are pleased to have Mike Mayberry, VP and Director of Component Research, Intel; Naga Chandrasekaran, VP of Process R&D, Micron; and Gyeong-Su Park, Leader of Analytical Science Group, Samsung Advanced Institute of Technology, as keynote speakers for the event. Over 30 other invited talks will offer overviews in the sessions that follow. Poster papers will supplement these overviews with the latest metrology-based research results. These poster papers represent significant contributions to the latest developments in characterization and metrology technology, especially at the nanoscale.

The 2013 FCMN is the ninth in a series that began in 1995. It emphasizes the frontiers and innovation in characterization and metrology of nanoelectronics. The proceedings for all eight previous conferences were published as hardcover volumes by the American Institute of Physics, New York. All but the 2011 proceedings are available to view for free on-line at www.nist.gov/pml/div683/conference/archives.cfm.

This year, the FCMN returns to the National Institute of Standards and Technology (NIST), Gaithersburg, MD, campus for the fifth time. Founded in 1901, NIST is a non-regulatory federal agency within the U.S. Department of Commerce. NIST's mission is to promote U.S. innovation and industrial competitiveness by advancing measurement science, standards, and technology in ways that enhance economic security and improve our quality of life. NIST employs about 2,900 scientists, engineers, technicians, and support and administrative personnel. Also, NIST hosts about 2,600 associates and facility users from academia, industry, and other government agencies.

It is our sincere hope that you find this conference stimulating and enjoyable!

With best wishes from the Committee Co-Chairs,

David Seiler, NIST;
Alain Diebold, College of Nanoscale Science and Engineering, SUNY Albany;
Bob McDonald, formerly of Intel (Treasurer);
George Thompson, Intel; and
Amal Chabli, CEA-Leti

Purpose and Goals

We bring together scientists and engineers interested in all aspects of the characterization and measurement technology needed for nanoelectronic materials and device research, development, and manufacturing. All approaches are covered in this conference: chemical, physical, electrical, optical, and in-situ. The conference summarizes major issues and provides critical reviews of important semiconductor techniques needed as the semiconductor industry continues its move in silicon nanoelectronics and beyond.

Contributed Posters

One of the major emphases of this conference is on the contributed posters. The extended poster abstracts selected by the committee represent significant contributions to frontier, state-of-the-art materials and device characterization and metrology.

Poster authors are responsible for setting up their displays, being present for posters sessions, and removing their displays at the end of the day.

Poster Sessions

Poster sessions with complimentary wine and cheese are scheduled for the end of Tuesday, Wednesday, and Thursday at NIST.

Special Session on Atom Probe Tomography

The FCMN committee is pleased to present a special session on Atom Probe Tomography, which will close the oral presentations on Thursday afternoon. Special thanks go to Cameca for sponsoring this session! This session will feature an interactive discussion on the research roadmap required to advance this technique from mostly early adopters to widespread use and acceptance as a routine metrology tool. This focused session will start with a view from an industrial user (Dr. K.Henry, Intel) providing an introduction to Atom Probe Tomography, its applications in semiconductor technology, and the challenges experienced in this work. Subsequent talks will provide quick overviews of state-of-the-art mixed with Q&A from the audience. The session will be chaired by Wilfried Vandervorst, IMEC.

Banquet

A dinner banquet will be held on Tuesday, Mar. 26th, at the host hotel, the Crowne Plaza Hotel in Rockville, MD. Bus transportation will be available to take you from NIST to the hotel starting immediately after the final poster session of the day.

Barbecue

An evening barbeque is planned at Smokey Glen Farm, Gaithersburg, Maryland, on Wednesday, Mar. 27th. Bus transportation will be available to take you from NIST to Smokey Glen Farm starting immediately after the final poster session of the day. Return bus service to the host hotel will be provided.

Gold Sponsors

Silver Sponsors

Bronze Sponsor

- Lake Shore Cryotronics, Inc.
- Metrologia

Exhibitor

- Angstrom Scientific, Inc.

Sponsors

About CEA-Leti

CEA is a French research and technology organisation, with activities in four main areas: energy, information technologies, healthcare technologies and defence and security. Within CEA, the Laboratory for Electronics & Information Technology (CEA-Leti) works with companies in order to increase their competitiveness through technological innovation and transfers. CEA-Leti is focused on micro and nanotechnologies and their applications, from wireless devices and systems, to biology and healthcare or photonics. Nanoelectronics and microsystems are at the core of its activities. As a major player in MINATEC campus, CEA-Leti operates 8,000-m² state-of-the-art clean rooms, on 24/7 mode, on 200mm and 300mm wafer standards. With 1,700 employees, CEA-Leti trains more than 240 Ph.D. students and hosts 200 assignees from partner companies. Strongly committed to the creation of value for the industry, CEA-Leti puts a strong emphasis on intellectual property and owns more than 1,880 patent families. For more information, visit www.leti.fr.

Press Contacts

CEA-Leti
Thierry Bosc
+33 4 38 78 31 95
thierry.bosc@cea.fr


weSRCH.com wishes to thank the researchers attending the
International Conference on Frontiers of Characterization
and Metrology for Nanoelectronics
for making the world a better place
by exploring ever smaller parts
of our world
weSRCH.com is a place to expand your career in new directions.
It is one of the top scientific sites in the world -- a virtual forum
where technologists present, learn and stay abreast
of advances in tech.
weSRCH.com
where technology equals opportunity

Tuesday, March 26

Registration

7:30 AM – 8:30 AM

Conference Opening

8:30 AM
Conference Opening
David Seiler, NIST, Conference Chair

8:45 AM
Introduction and Welcome to NIST
Willie May, Associate Director for Laboratory Programs/Principal Deputy, NIST

Keynote Talks

Session Chair: David Seiler, NIST

9:00 AM
Pushing Beyond the Frontiers of Technology 21
Mike Mayberry, VP and Director of Component Research, Intel

9:45 AM
Characterization and Metrology Challenges for Emerging Memory Technology Landscape 24
Naga Chandrasekaran, VP of Process R&D, Micron

10:30 AM
Coffee Break and Poster Viewing

11:00 AM
Advanced Metrology for Understanding Charge Transport Phenomena in Charge Trap Flash Memory 28
Gyeong-Su Park, Samsung Advanced Institute of Technology

General

Session Chair: Toshihiko Kanayama, AIST

11:45 PM
The Value Add of Metrology for the Semiconductor Industry 34
Dan Hutcheson, VLSI Research

12:15 PM
The 2012 ITRS Metrology Roadmap 36
Alain Diebold, SUNY Albany

12:45 PM
Lunch and Poster Viewing

Microscopy

Session Chair: Lori Nye, Brewer Science, Inc.

2:15 PM
Monte Carlo Simulations of Helium and Neon Ion Beam Induced Deposition 39
David Joy and Philip Rack, UT/Knoxville

2:45 PM
Limits of Aberration Corrected Electron Microscopy. 42
Ruud Tromp, IBM

3:15 PM
Coffee Break and Poster Viewing

3:45 PM
Aberration-Corrected Scanning Transmission Electron Microscopy 45
Ondrej Krivanek, Nion

4:15 PM
Three-Dimensional and Spectroscopic Characterization of Devices at the Atomic Scale Using Aberration-Corrected Electron Tomography 48
Robert Hovden, Cornell University

4:45 PM
A Mirror-Corrected Scanning Electron Microscope 51
Michael Steigerwald, Carl Zeiss

5:15 – 6:15 PM
Poster Session (with Wine and Cheese)

6:45 PM
Banquet at Hotel

Poster Presentation

TU-01, Real-Time Spectroscopic Ellipsometry in Atomic Layer Deposition Process 56
Han Wang, Xiaoqiang Jiang, and Brian G. Willis
Department of Chemical, Materials & Biomolecular Engineering, University of Connecticut, Storrs, Connecticut 06269

TU-02, Measure the Electron and Hole Contact Resistance in Gated Kelvin Structure 59
Hui Yuan[1,2], Curt A. Richter[2], Hao Zhu[1,2], Haitao Li[1,2], Oleg Kirillov[2], Dimitris Ioannou[1], and Qiliang Li[1]
[1]Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030
[2]Semiconductor and Dimensional Metrology Division, NIST, Gaithersburg, MD 20899-8120

TU-03, Transmission Electron Backscatter Diffraction (T-EBSD) for Characterizing Ultrathin Films in the SEM 62
Katherine P. Rice, Roy H. Geiss, and Robert R. Keller
Applied Chemicals and Materials Division, National Institute of Standards and Technology, Boulder, CO 80305

TU-04, Spatially-Resolved Dopant Characterization with a Scanning Microwave Microscope 64
T. Mitch Wallis, Atif Imtiaz, Alexandra E. Curtin, Pavel Kabos, Matthew D. Brubaker, Norman A. Sanford, and Kris A. Bertness
National Institute of Standards and Technology (NIST), 325 Broadway, Boulder, Colorado 80305

TU-05, Modeling Scanning Electron Microscope Measurements with Charging 67
John S. Villarrubia
National Institute of Standards and Technology, Semiconductor and Dimensional Metrology Division, Stop 8212, 100 Bureau Dr., Gaithersburg, MD 20899

TU-06, Automated STEM and TEM Metrology of Advanced Semiconductor Devices 70
Mark J. Williamson, Michael Strauss, and David Horspool
FEI Company, 5350 NE Dawson Creek Drive, Hillsboro, Oregon, USA

TU-07, Contamination-Free Scanning Electron and Helium Ion Microscopy 73
K.P. Purushotham, András E. Vladár, and Michael T. Postek
National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899-8212, USA

TU-08, Measurement of Silica Particles by Transmission Electron Microscope 76
F. Kole, Y. Guan, and P. Konicek
VLSI Standards, Inc., Five Technology Drive, Milpitas, California 95035 USA

TU-09, Applications of Electron Tomography to Advanced CMOS Process Technology. 79
Hugh L. Porter[1] and Jeremy D. Russell[2]
[1]SEMATECH and GLOBALFOUNDRIES, 257 Fuller Road, Suite 2200, Albany, NY 12203
[2]GLOBALFOUNDRIES, 400 Stone Break Extension, Malta, NY 12020

TU-10, Quantitative Characterization and Applications of 193 nm Scatterfield Microscope 82
M. Y. Sohn[1,2], B. M. Barnes[1], and R. M. Silver[1]
[1]National Institute of Standards and Technology (100 Bureau Drive, Gaithersburg, MD)
[2]Hyperion Biotechnology, Inc. (12002 Warfield, Suite 101, San Antonio, TX)

TU-11, 3-D Optical Metrology of Finite sub-20 nm Dense Arrays using Fourier Domain Normalization 84
J. Qin, H. Zhou, B. M. Barnes, R. Dixson, and R. M. Silver
Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, 100 Bureau Dr. MS 8212, Gaithersburg, MD USA 20899-8212

TU-12, Multi-Technique Approach for Determination of Crystalline Phase and Electronic Structure of Atomic Layer Deposited Hf1-xZrxO2 86
Relja Vasic[1], Steven Consiglio[2], Robert Clark[2], Kandabara Tapily[2], Manasa Medikonda[1], Gangadhara Raja Muthinti[1], Eric Bersch[3], Gert Leusink[2], and Alain Diebold[1]
[1]College of Nanoscale Science and Engineering, University at Albany, 257 Fuller Rd., Albany, NY 12203
[2]TEL Technology Center, America, LLC, 255 Fuller Rd., Albany, NY 12203
[3]SEMATECH, 257 Fuller Rd., Albany, NY 12203

TU-13, Quantification of Hafnium in Hafnium Oxide Film by
Isotope Dilution Neutron Activation Analysis 90
Toshiko Takatsuka, Kouichi Hirata, Kenji Ito, Naoko Nonose, and Tsutomu Miura
National Metrology Institute of Japan, National Institute of Advanced Industrial Science and Technology, Central 5, 1-1-1 Higashi, Tsukuba, Ibaraki 305-8565, Japan

TU-14, Complementary Metrology – aA Prerequisite for Reliable and
Traceable Characterization of Surfaces and Nanolayers 93
Andreas Nutsch[1,2], Burkhard Beckhoff[1], and Jaap Van Den Berg[3]
[1]Physikalisch-Technische Bundesanstalt, Abbestr 2-12, 10587, Berlin, Germany
[2]previously Fraunhofer IISB, Schottkystrasse 10, 91058 Erlangen, Germany
[3]University of Huddersfield, Huddersfield, HD1 3DH United Kingdom

TU-15, SIMS Correction and Depth Profiling of Ion Implantations Using Grazing Incidence XRF . . . 96
Philipp Hönicke[1], Burkhard Beckhoff[1], Yves Kayser[2], and Sven Kayser[3]
[1]Physikalisch-Technische Bundesanstalt, Abbestr. 2-12, 10587 Berlin, Germany
[2]Paul Scherrer Institut, 5232 Villigen PSI, Switzerland
[3]ION-TOF GmbH, Heisenbergstr. 15, 48149 Münster, German

TU-16, Towards Nanoelectronics Metrology with a Laboratory Set-Up in the Soft X-Ray Range 99
D. Grötzsch[1], B. Kanngießer[1], I. Mantouvalou[1], C. Herzog[1], K. Witte[1], M. Spanier[1], J. Lubeck[2], P. Hönicke[2], and B. Beckhoff[2]
[1]Technische Universität Berlin, Institut für Optik und Atomare Physik, Hardenbergstr. 36, 10623 Berlin
[2]Physikalisch Technische Bundesanstalt, Abbestr. 2-12, 10587 Berlin, Germany

TU-17, Local Tunneling Measurements of in-situ Gated Topological Insulators 103
Jeonghoon Ha[1,2,3], Niv Levy[1,2], Tong Zhang[1,2], Young Kuk[3], and Joseph A. Stroscio[1]
[1]Center for Nanoscale Science and Technology, NIST, Gaithersburg, MD 20899, USA
[2]Maryland NanoCenter, University of Maryland, College Park, MD 20742, USA
[3]Department of Physics and Astronomy, Seoul National University, Seoul, 151-747, Korea

TU-18, Comprehensive Characterization and Understanding of
Micro-Porous Low-κ Interconnects Using PALS, EP and XRR 105
D. Yang[1], R.L. Opila[1], G. Jiang[2], V. Pallem[2], D.W. Gidley[3], and N. Bhargava[4]
[1]Department of Materials Science and Engineering, University of Delaware, Newark, Delaware
[2]Delaware Research & Technology Center, Air Liquide America, Newark, Delaware
[3]Department of Physics, University of Michigan, Ann Arbor, Michigan
[4]Department of Electrical Engineering, University of Delaware, Newark, Delaware

TU-19, Direct Analysis of Undiluted Photoresist with
Inline Autodilution Inductively Coupled Plasma Mass Spectrometry. 108
Hyun-Kee Hong[1], J. S. Lee[2], Austin Schultz[2], Paul Field[2], and Daniel Wiederin[2]
[1]Samsung Electronics Co. Ltd., San #5, Banwol-Dong, Hwasung City, Gyeonggi-Do, Korea 445-701
[2]Elemental Scientific, 1500 North 24th Street Omaha, NE 68110, USA

TU-20, Extraction of Interfacial Doping Density in Metal/Silicon Contacts 110
Khaled Ahmed
Intermolecular, Inc., 3011 North First Street, San Jose, California 95134, USA

TU-21, Sub-Surface Metrology Using X-Ray Emitting AFM Probes 113
Faisal K. Chowdhury, H. Pourzand, and M. Tabib-Azar
Dept. of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT, USA, 84112

TU-22, Work Function Characterization Of Si1-xGex Heterostructure Using Kelvin Force Microscopy and Electron Spectroscopy 116
Sylvain Pouch, Nicolas Chevalier, Denis Mariolle, Eugenie Martinez, Pradeep Kumar, Olivier Renault, Julien Morin, Jean-Michel Hartmann, and Łukasz Borowik
CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France

TU-23, Measurement Uncertainties in MEMS Kinematics by Super-Resolution Fluorescence Microscopy 119
Craig D. McGray, Samuel M. Stavis, and Jon Geist
National Institute of Standards and Technology, Gaithersburg, MD 20899

TU-24, Sample Alignment of X-Ray Reflectometry Using Thickness and Density From Certified Reference Materials 123
Donald Windover[1], David L Gil[1], Yasushi Azuma[2], and Toshiyuki Fujimoto[2]
[1]National Institute of Standards and Technology, Gaithersburg, MD 20899, USA
[2]National Metrology Institute of Japan, National Institute of Advanced Industrial Science and Technology, Tsukuba 305-8568, Japan

1–1

PUSHING BEYOND THE FRONTIERS OF TECHNOLOGY

Mike Mayberry

Intel Corporation, Technology and Manufacturing Group, Hillsboro, OR 97124, USA

INTRODUCTION

Modern CMOS technologies are assemblies of complex three dimensional structures which incorporate precise layers of materials to enable the desired performance (Fig. 1). Metrology is essential to enable process control, calibration of process simulations, and debug of potential problems. Future devices, interconnects, and computational architectures will drive new challenges for metrology including the need to image in three dimensions with nanometer resolution and to characterize functionality with measurement of new material properties such as spin state and domain orientation.

THE NEAR FUTURE

Since about a decade ago, classical dimensional scaling has been replaced by both novel material and structural innovations which allow continued advancements in density and power-performance. Two general trends at the device level include 1) improving electrostatics in order to have precise control of switching behavior, 2) use of materials and materials engineering to improve effective mobility to improve efficiency. For interconnects, added complexity drives the need for more wiring resources as well as materials engineered for lower capacitance and resistance.

In the near future these trends of increasing structural complexity and incorporation of novel materials will continue [1]. An example of a proposed device with better electrostatics along with an example implementation of an ultimate CMOS device is shown in Fig 2 top.

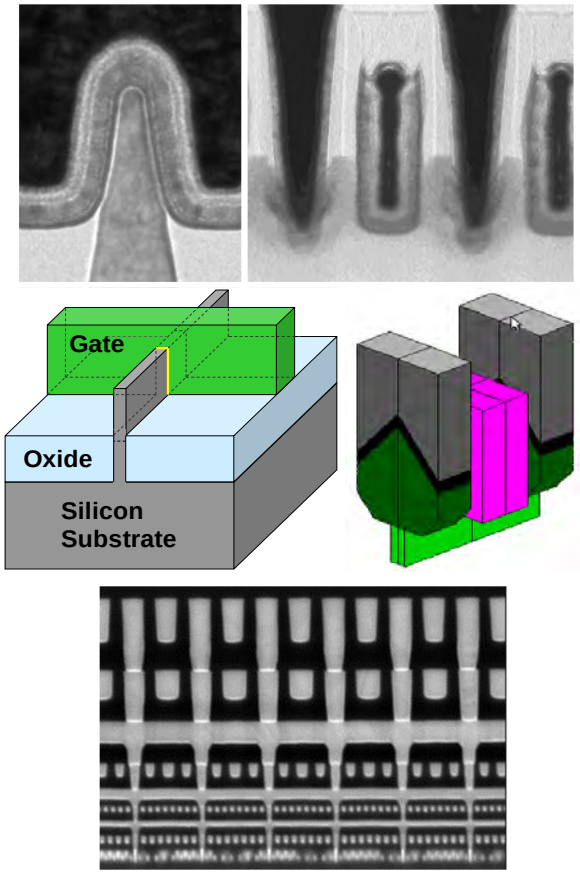


FIGURE 1. Modern CMOS technologies consist of multiple three dimensional structures. Intel's 22nm node trigate devices consist of fins with wrap-around gates. Wiring consists of nine or more metal layers.

At the same time, demand for increased interconnection of higher density devices will drive not only the addition of more layers but potentially

1–1

also a move to true 3D design where multiple device layers coexist with multiple wiring layers as shown in Fig 2 bottom [2].

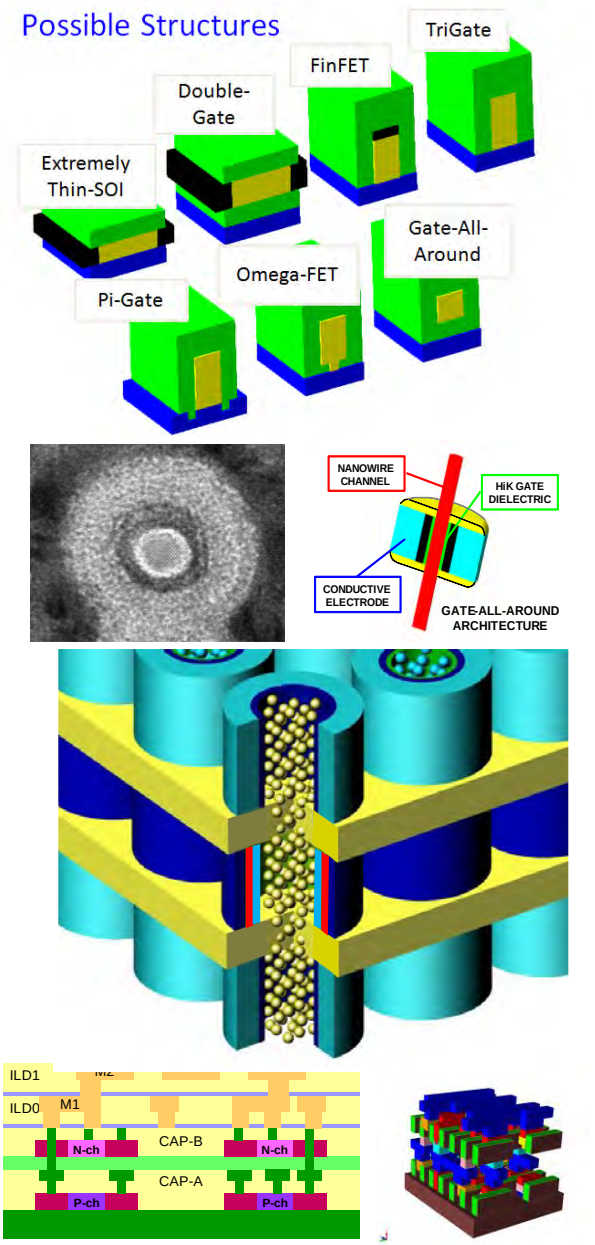


FIGURE 2. The gate-all-around device is projected to have the best theoretical electrostatic performance. However to realize the full potential of the device it is also necessary to precisely incorporate novel materials such as high mobility channels and high K-metal gates. Interconnection demands may also drive a move towards where multiple device layers coexist with multiple wiring layers. These structures and their small scale features pose new challenges for metrology and characterization.

THE LONGER TERM FUTURE

The search for beyond CMOS devices has led to a variety of candidates including both charge based and those relying on other physical phenomena, some examples shown in Fig 4 [3]. Some of these candidates, such as the tunnel FET, can replace CMOS devices with moderate changes to circuit design and interconnects while others demand more radical changes.

The spin torque devices use charge currents to produce a change in spin, either flipping of magnetic orientation or creation of a spin current. One example of a spin torque computational circuit is shown in Fig. 4. It consists of voltage inputs which induce charge current which pass through a spin filters. Spin currents are transported and combined in computational elements and finally charge currents are sensed at the outputs. This mixed domain circuitry contains multiple novel materials and detection of operation will require new measurement techniques.

Today's collection of metrology and characterization techniques is inadequate to the challenges that are coming. Destructive techniques will not allow verification of function while inline techniques may not have sufficient resolution to detect subtle shifts in processing. New ways to image in three dimensions in situ are vitally needed to meet the needs for these future processes and those demands will be much more varied than for today's CMOS baseline.

CONCLUSIONS

Metrology and characterization enable continued advances in electronics today and will become increasingly important as the scope of materials, structures, functions, and architectures broaden compared with the range of processes in production today. New metrology research is needed to be ready as these challenges unfold.

1–1

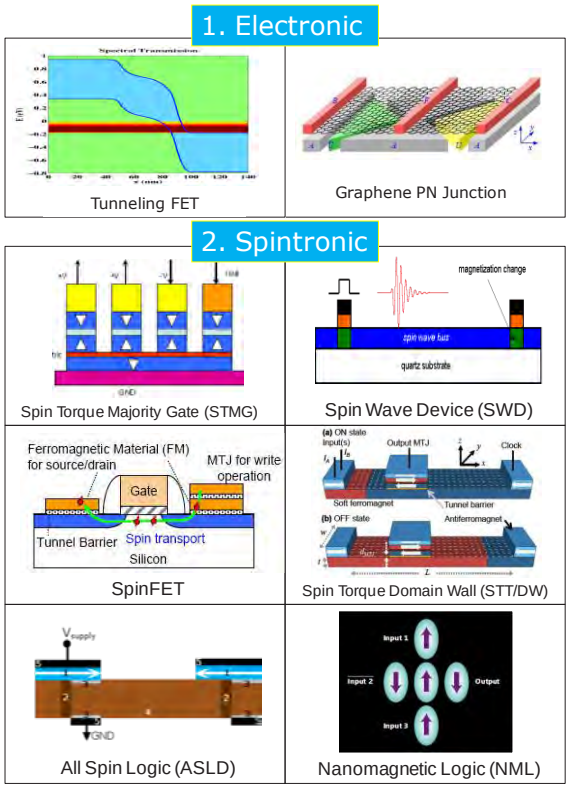


FIGURE 3. Multiple devices have been proposed as options beyond the end of CMOS scaling. Those based on charge can reuse interconnect materials and some circuitry while those based on spin will require more radical changes to materials and architectures.

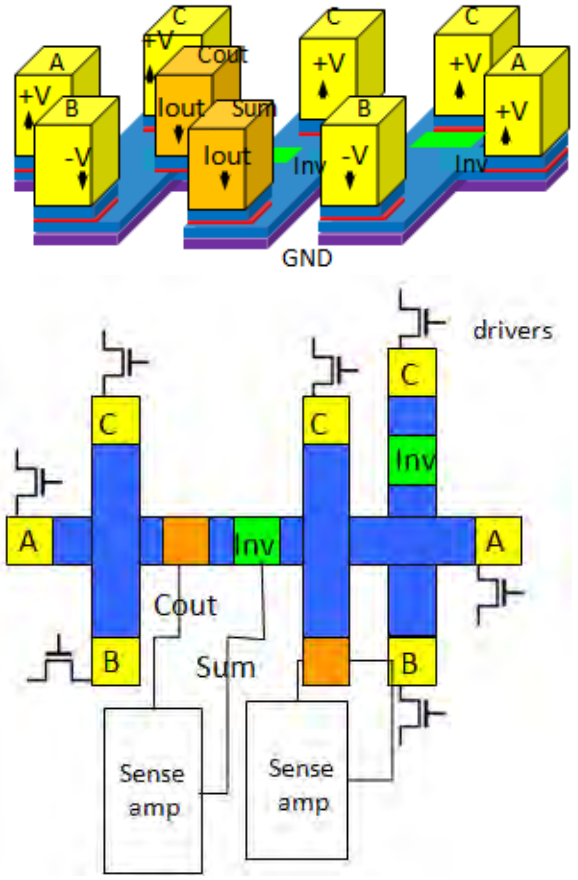


FIGURE 4. This is an example computational circuit based on spin torque devices that uses a mixture of charge current and spin current to carry out computation. Such circuits have the potential to be higher density than CMOS equivalents and also nonvolatile.

References

1. K. Kuhn, *IEEE Transactions on Electron Devices*, vol.59, no.7, pp.1813-1828, July 2012
2. M. Mayberry, *2012 International Interconnect Technology Conference*, pp.1-6, June 2012.
3. D. Nikonov, *2012 International Electron Devices Meeting*, pp. 573-576, Dec 2012

Keywords

Scaling, CMOS, computation, NonBoolean

1–2

Characterization and Metrology Challenges for Emerging Memory Technology Landscape

Naga Chandrasekaran, Steve Hues, Shifeng Lu, Du Li, and Chris Bishop

Micron Technology, 8000 Federal Way, Boise, Idaho, USA 83707

INTRODUCTION

Traditional Memory devices (DRAM, NAND, NOR) continue to broaden their application space enabled by a combination of density increase through technology shrink and performance improvements through materials innovation. At the same time, cadence of continued scaling for traditional memory devices is slowing down as they face critical limitations[1]. One of the primary limitations is due to the fact that these devices rely on charge (electron) trapping to hold memory information. In the case of NAND FLASH device, as the technology node shrinks from 4X nm to 1X nm [Figure 1], the numbers of electrons that may be stored in the floating gate diminish to the point where device reliability is degraded and continued scaling becomes difficult. In the case of DRAM, refresh performance requirements continues to challenge capacitor aspect ratio and material choices for the structure. Other factors limiting scaling include state of equipment technology to pattern smaller features and ability to achieve a competitive cost structure.

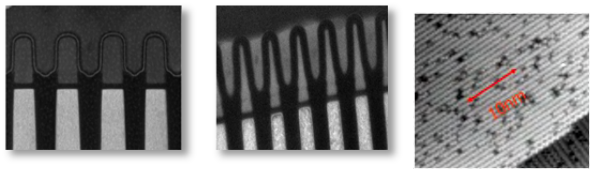


Figure 1: Transition of Planar NAND from (a) 4X nm to (b) 2X nm to (c) 1X nm showing 1X nm scaling approaching atomic scale.

Such critical limitations of traditional memories are being overcome by three parallel approaches: (1) Traditional 2-D memory technologies are starting to transition to 3-D structures (2) emergence of novel emerging memory technologies (PCM, STTRAM, Resistive RAM, to name a few) and (3) integration of multiple memory and CMOS technologies on board to facilitate multiple functions through innovative system architecture introductions. These innovative approaches are driving new and unique technology challenges in memory development space. One such area, which is exponentially challenged by such advances, is materials and structural characterization.

Evolution of Conventional Memory Technology

With increasing planar NAND challenges, the industry is starting to transition to Vertical NAND technology where the storage bits are now placed in 3-D structures. The complexity of a vertical NAND structure is as shown in Figure 2. Such structures incorporate tall thick stacks comprised of multiple thin layers, high aspect ratio channels, and recessed hidden structures, all of which needs to be controlled to high accuracy.

Figure 2: Vertical NAND (3-D) Structure Schematic

1–2

Stacking of DRAM memory and embedding such stacks with high speed logic layer is a fundamental change in how memory is used in system [Figure 3]. This has driven unique technology development in the form of Through Silicon Via (TSV), interconnects, and packaging technology.

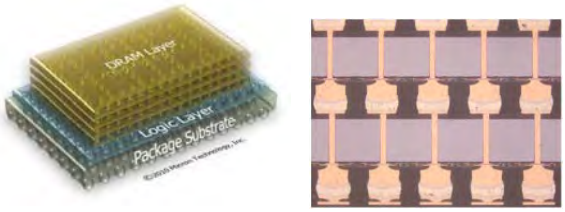


Figure 3: Fundamental Change in Memory System (a) Hybrid Memory Cube (HMC) and (b) TSV

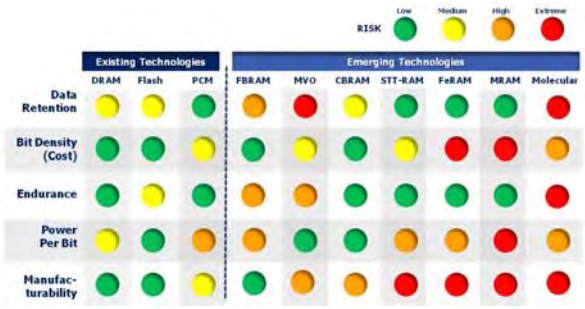
Vertical NAND and complex DRAM technology nodes present significant metrology challenges. Developing scatter models to measure Critical Dimensions (CD) for these structures involves complex mathematical modeling that results in long model development time. Even then, measuring CDs at the bottom of high aspect ratio structures and generating true profile measurements for such structures (e.g., capacitor, TSV, and V-NAND etch) are a challenge. Vertical NAND and emerging DRAM device architectures also present unique requirements to measure recess in vertical and horizontal directions, measurement of underlying layers, and buried defects. Multi tier modeling with tiers representing discrete thin and embedded layers poses optical measurement challenges. With more layers, we are pushing lambda to IR range.

DRAM and NAND technologies continue to drive stringent alignment requirements between patterning levels. Introduction of new materials and their integration methodology results in grainy and rough surfaces adding to overlay measurement variability. Tall structures with unique materials add to errors and fails driven by low contrast imaging, wafer shape changes, and back side uniformity issues. There is an ever increasing need to measure film stress and wafer shape changes.

Evolution of Emerging Memory Technologies

A large number of emerging memory technologies is being evaluated by the scientific community[2]. Table 1 shows a relative snapshot of performance metrics between alternate memory technologies. Most of these devices are non-volatile in nature targeting storage class applications in an attempt to mitigate the development and application space risks posed by traditional memory technologies (DRAM, NAND, NOR).

Table 1: Performance Comparison of Alternate Memory Technologies (Jan 2012)[2]



Phase Change Memory

Phase change memory[3] is a term used to describe a class of memory devices that utilize the ability of certain chalcogenide materials to rapidly change phase between two stable physical states, which have different material properties (e.g., resistivity) that may then be read as an indication of the bit state.

Resistive RAM

A resistive RAM memory device[4] incorporates a dielectric material which may be transformed between one or more resistive states (written) by the application of a voltage. The memory state of each bit is then read by measuring the resistance of the bit cell.

Spin-Transfer Torque RAM

1–2

Spin-transfer torque memory cell[5] consists of two ferromagnetic layers separated by an oxide layer. The resistance of the cell is determined by the relative magnetization directions of the ferromagnetic layers with that of one reference layer being held constant and the other switched from being parallel to the reference layer (low resistance) or anti-parallel (high resistance) by means of an applied voltage.

MATERIALS CHARACTERIZATION CHALLENGES

Emerging memory materials and the devices fabricated from them present material characterization challenges that are rapidly approaching the boundaries of our current metrology capabilities. The first challenge involves the necessity of examining very small volumes. With the profound shrinking of device dimensions, the large interfacial area to internal volume ratio has the potential to produce material properties within these small structures that may not be directly related to larger volumes which are readily measured with current methodologies.

A second challenge results from the nature of emerging memory materials themselves. Tertiary compounds, such as GST, not only have a much more complex phase and compositional space in which to exist than traditional semiconductor materials, but in an analogy to the Heisenberg effect, they can be changed simply by the act of measuring them with current techniques. Many materials exhibit phase segregation at the surface relative to the bulk. In order to accurately perform a compositional analysis of the bulk with a surface analytical technique, such as x-ray photoelectron spectroscopy, it is necessary to remove this surface layer with ion sputtering, which alters the surface layer by preferential sputtering in which the material components are removed at differing rates by the ion beam.

Two exciting areas for future metrology development are atom probe tomography[6], which holds the promise of 3D compositional analysis with atomic scale resolution and "benchtop" x-ray synchrotron sources[7], whose tunable high brightness sources hold the promise of transforming laboratory scale small volume x-ray based metrologies. Unfortunately, both of these are still in their infancy for semiconductor device applications and their development would prove a profoundly fertile ground for effective partnerships between academia and industry.

STRUCTURAL CHARACTERIZATION CHALLENGES

Process development for emerging memory devices is highly dependent upon a detailed knowledge of the structure of the component materials, particularly for PCM, where the structure is the very property that is used to store the bit information. Currently, two metrologies are being applied to these systems. Transmission electron microscopy (TEM) has the ability of performing direct atomic scale imaging of device structures [Figure 4] with the additional advantage of providing elemental mapping, albeit without the sensitivity required for traditional dopant-level concentrations, on the size scale of device features.

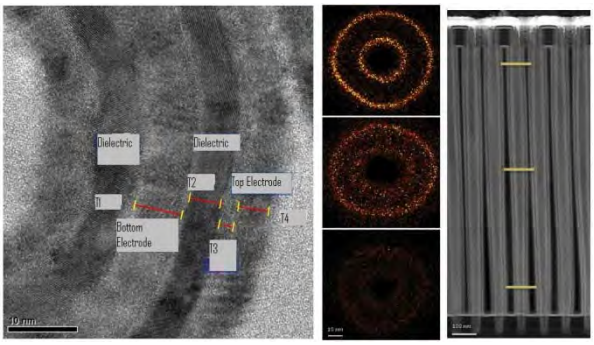


Figure 4: Atomic resolution TEM imaging (left) and elemental distribution mapping at three different heights (center) of a capacitor structure (right)

Another critical capability for emerging memory is the ability to measure phase information as a function of temperature. X-ray diffraction (XRD) coupled with a variable temperature hot stage provides this capability albeit on a dimensional

1–2

scale much larger than an individual memory cell, primarily due to the brightness limitations of conventional laboratory x-ray sources. An example where this capability would play a role would be use of Co/Pt superlattices in STTRAM applications. Metallic superlattices show properties that may be dramatically different than either metal by itself or in any conventional bulk alloy. Phase transitions in this system have been correlated[8] with magnetic property changes. Surface roughness [Figure 5] can also be an important factor. Advances in x-ray source brightness through the development of benchtop synchrotron sources, holds the promise of decreasing the size of the analytical area considerably, increasing the applicability of this technique to size scales more approaching device dimensions.

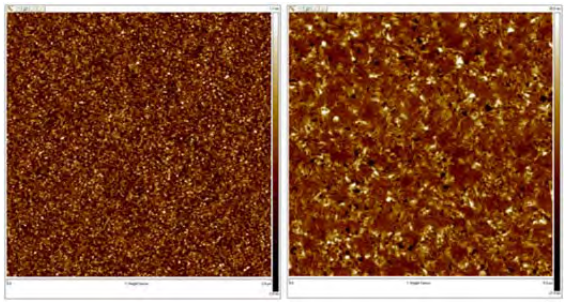


Figure 5. Surface roughness for as-deposited (Rq = 3 Å) and annealed (Rq = 47 Å) superlattice.

With many of these new memory devices we face two practical challenges. First, most of the techniques used to characterize materials and their performance is done in an offline lab. X-ray techniques or TEM data shown earlier, still lack the ability to perform elemental analysis at high throughput to use such techniques as line control measurements, which will be a requirement as emerging memory technologies find wider acceptance. Sensitivity, precision, and accuracy of such elemental analysis are still not well understood. Second, many of the characterization techniques still induce some amount of material state change or damage to the materials during characterization. Any such damage caused during characterization lead to ambiguity in interpreting failure states and characterizing emerging memory technologies.

SUMMARY

Emerging memory technologies present significant technological challenges in the area of materials and structural characterization. Furthermore, wide scale acceptance of such characterization techniques to be used in high volume manufacturing will require such metrology innovations to also be production worthy. It is possible we are entering a decade where scaling cadence, new memory technology development, and fundamental understanding of emerging memory technologies working aspects will be gated by our ability to characterize, measure, control, and improve unique materials and structures rather than lithography capability.

REFERENCES

1. D.J Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, and HS. P. Wong,, *Proceedings of the IEEE* **89**, 259-288 (2001).
2. Micron Technology Winter Analyst Presentation, 2012
3. G.W. Burr, M.J. Breitwisch, M. Franceschini, D. Garetto, K. Gopalakrishnan, B. Jackson, B. Kurdi, C. Lam, L.A. Lastras, A. Padilla, B. Rajendran, S. Raoux, and R.S. Shenoy, *J. Vac. Sci and Tech. B* **28**, 223-262 (2010).
4. T.Mikolajick, M. Salinga, M. Kund, and T. Kever, Adv. Eng. Mater. **11**, 235-240 (2009).
5. E. Chen, D. Apalkov, Z. Diao, A. Driskill-Smith, D. Druist, D. Lottis, V. Nikitin, X. Tang, S. Watts, S. Wang, S.A. Wolf, A.W. Ghosh, J.W. Lu, S.J. Poon, M. Stan, W.H. Butler, S. Gupta, C.K.A. Mewes, T. Mewes, and P.B. Visscher, IEEE Trans. Magn. **46**, 1873-1888 (2010).
6. T.F. Kelly and M.K. Miller, Rev. Sci. Instrum. **78**, 03110101 – 03110119 (2007).
7. M. Bech, O. Bunk, C. David, R. Ruth, J. Rifkin, R. Loewen, R. Feidenhans, and F Pfeiffer, J. Synchrotron Rad. **16**, 43-47 (2009).
8. T.K. Hatwar and T.N. Blanton, IEEE Trans. on Magnetics, Vol. 33, No. 5, Sept. 1997

KEYWORDS

Memory Devices, Emerging Memory, Metrology Challenges, Material Characterization, Vertical NAND

1–3

ADVANCED METROLOGY FOR UNDERSTANDING CHARGE TRANSPORT PHENOMENA IN CHARGE TRAP FLASH MEMORY

Gyeong-Su Park and Sung Heo

Samsung Advanced Institute of Science and Technology (SAIT), Gyeonggi-do 449-712, Korea

INTRODUCTION

Since various portable electronic devices have become popular consumer products, flash memory devices with charge-trapping layers, such as SONOS ($Si/SiO_2/SiN/SiO_2/Si$)-type [1] and TANOS ($TaN/Al_2O_3/SiN/SiO_2/Si$)-type devices [2], have attracted much attention due to lower programming voltage, better scalability, improved endurance, and high compatibility with standard CMOS technology [3]. However, the SONOS/TANOS devices have fundamental difficulties in controlling the trap density and the trap distribution, which are quite important in determining the programmed/erased bit distribution and data retention [4, 5]. The charge trap flash (CTF) memory device using nanocrystals (NCs) as a discrete charge-trapping layer was proposed as one of the most promising CTF devices, because the density and location of the NCs could be easily controlled by optimizing the process conditions [6, 7]. Although there are many reports on the NC-based CTF memory indicating various advantages including a low cost fabrication process, improved retention, and good reliability [8, 9], systematic analysis on the charge trap characteristics of the NCs has not been fully performed due to the capability of existing metrology and analysis techniques.

Tunneling barrier engineering with high-*k*/low-*k* dielectric stacks is in charge of the carrier injection efficiency by lowering the barrier height, and reducing the effective tunneling thickness and the interface trap generation [10, 11]. The high-*k* blocking layer also plays an important role in increasing the electric field across the tunneling oxide by hindering the transfer of the charge carriers to metal gate during programming/erasing operations (the back-tunneling current) [12]. The latest reports on both the tunneling oxide and the blocking layer have been focused on the physical mechanisms governing the erase speed and data retention of the CTF devices [13, 14] without comprehensive understanding of the close ties among their defect state, defect density, and atomic structure.

In this paper, we introduce new analytical approaches for closely examining the charge transport characteristics of the Si-NC based CTF memory shown in Fig. 1. We have used double layers of Si-NCs embedded in amorphous Si_3N_4 dielectric as a high density charge-trapping layer. A thin SiO_2 dielectric layer and an Al_2O_3 layer were also employed as a tunneling layer and a blocking oxide layer, respectively.

1–3

Analysis of charge trap distribution and charge injection

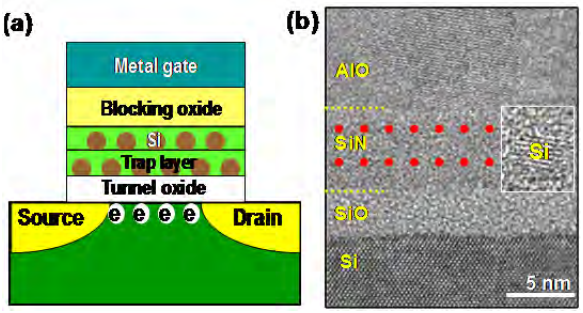


FIGURE 1. (a) Schematic illustration of the CTF architecture. (b) Cross-sectional TEM image of the Si-NC based CTF memory, where double Si-NC layers are embedded in a silicon nitride layer.

Since distribution and uniformity of Si-NCs in the Si_3N_4 dielectric layer influence the retention characteristics under elevated temperatures, detailed characterization of the Si-NC morphology and distribution in three-dimensional space is required. Figure 2(a) shows the top-view image of Si-NCs (2~7 nm), which are embedded in a Si_3N_4 matrix with the number density of 1.2 x 10^{12} cm^{-2}. In order to confirm the three-dimensional (3D) distribution of Si-NCs, we reconstructed an electron tomography image by combining plasmon-filtered microscopy (Fig. 2b-f) [15]. The electron tomography image reveals several key features, namely, (1) the Si-NC number density could be estimated even in the buried layer; (2) the Si-NC number density was higher in layer A than in other layers; (3) an additional Si-NC layer C was formed due to the diffusion of excess Si atoms; (4) larger Si-NCs in size were produced in the upper layers; (5) irregular shapes of Si-NCs were mainly formed in the diffused layer C.

To directly observe the distribution of charge traps both in the Si-NCs and in the SiO_2/Si interface, we carried out an electron holography [16] work in a transmission electron microscope (TEM) equipped with a field-emission gun and a biprism. Double layer structure of Si-NCs, used for this experiment, is shown in an energy-filtered TEM (EF-TEM) image of Fig. 3(a). Figures 3(b) and (c) show the corresponding electron hologram and its reconstructed phase image, respectively, obtained after irradiation of high energy electron flux (J=10 A/cm^2, electron bombardment for 10 s).

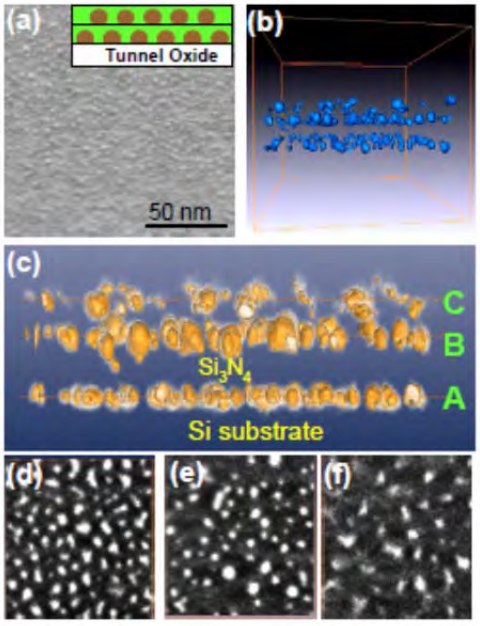


FIGURE 2. (a) Top-view SEM image of Si-NCs stacked on a tunnel oxide layer. (b-c) Tomographic reconstruction from a series of plasmon-loss images recorded at different sample tilts. (d-f) Distribution of Si-NCs at the layers A (d), B (e), and C (f) indicated in (c).

The reconstructed phase image of Fig. 3(c) directly shows electron traps in the Si–SiO_2 interface (a red dotted line) as well as in the double Si layers (yellow dotted lines). The phase shift into black contrast at three regions should be attributed to the electric fields of the trapped electrons. The interface trap was known to degrade the retention and endurance characteristics of the CTF memory [17]. To directly observe the electron injection from Si-NCs, we applied the *in-situ* electron holography technique of TEM with the experimental setup shown in Fig. 3(d). This setup ensures that the reference wave in the upper region of the Pt-Ir anode may not be perturbed by the applied voltage. Figures 3(e) and (f) show phase shift maps obtained when the voltages of 0 and 30 V, respectively, are applied between the Si substrate and the Pt-Ir anode. The accompanying *I-V* curve is also indicated in Fig. 3(g). The phase shift map shown in Fig. 3(e) demonstrates weak strength of the electric field concentrated on the exposed edge

of a Si-NC due to the electron traps. Moreover, the phase shift map of Fig. 3(f) demonstrates that the gradient equipotential lines are highly concentrated at the edge of a Si-NC when the applied voltage is 30 V. These observations strongly support that injection of trapped electrons occurs from the Si-NCs. In addition, it is evident from the *I-V* curve (Fig. 3(g)) that the electron injection starts from above 22 V and the injection current increases up to 250 nA at the applied voltage of 50 V.

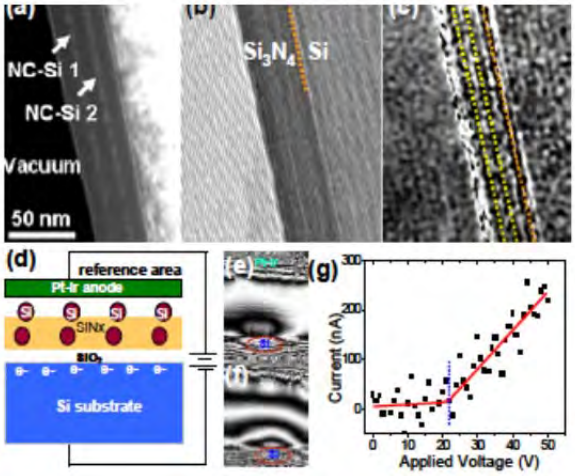


FIGURE 3. (a) Cross-sectional plasmon-loss image (filtered at 17 eV for Si) of double Si-NC layers embedded in a Si_3N_4 matrix. (b-c) Electron hologram (b) and reconstructed phase image (c) obtained from the same sample as (a). (d) Schematic illustration showing the experimental setup. (e-f) Reconstructed phase images obtained when the applied voltage is (e) 0, and (f) 30 V, respectively. (g) The accompanying *I-V* curve over the voltage range 0 to 50 V.

Measurements of band structure and defect states

Band-gap engineering of the *a*-Si_3N_4 and SiO_2 thin films, used as an alternative charge-trapping layer and a tunnel layer, is essential for improving the device reliability of CTF memory. In order to measure the band gap and valence band offset of the *a*-Si_3N_4 thin film, we have applied reflection electron energy loss spectroscopy (REELS) [18] and X-ray photoelectron spectroscopy (XPS), respectively. Figure 4(a) shows bandgap spectra of *a*-Si_3N_4 and SiO_2 films obtained by REELS. The estimated bandgap (Eg) values of the *a*-Si_3N_4 and SiO_2 films are 5.1 eV and 9.0 eV, respectively. Figure 4(b) shows a XPS valence band spectrum of *a*- Si_3N_4 in $Si_3N_4/SiO_2/Si$ heterostructure with the reference spectrum measured from the SiO_2 in SiO_2/Si structure. The valance band maximum (VBM) is determined by extrapolating the leading edge of the valance spectra to the base line. The VBM of the *a*-Si_3N_4 film (Fig. 4b) is about 1.6 eV. The valence band offset (ΔE_v) at the interface of *a*-Si_3N_4/SiO_2 is the energy difference between the VBM of SiO_2/Si and the VBM of *a*-$Si_3N_4/SiO_2/Si$ heterostructure. The resulting valence band offset of the *a*-Si_3N_4 film is 3.1 eV. Moreover, the band-gap and valence-band offset values allow us to determine the conduction band offset (Δ Ec) of the *a*-Si_3N_4 film using this relation: Δ Ec= Eg (SiO_2)-Eg (*a*-Si_3N_4)-ΔE_v (*a*-Si_3N_4/SiO_2).

The electronic property of the *a*-Si_3N_4 film as a trap layer is determined mainly by deep-level trap which is the center of electron and hole trappings. At the same time shallow-level trap enables the trapped charges to readily escape from the *a*-Si_3N_4 film, which degrades the CTF memory performances. In order to examine the defect states of the *a*-Si_3N_4 film for electron traps, we carried out thermally stimulated exo-electron emission (TSEE) [19] and deep level transient spectroscopy (DLTS) [20] measurements. TSEE spectra give information on the activation energies which correspond to the depths of defect centers below the conduction band minimum (CBM), whereas DLTS provides important information about deep-level defects. Figure 4(c) shows the TSEE spectrum for the *a*-Si_3N_4 film. The TSEE experiment was performed in the temperature range from 350 to 1050 K. The defect energy levels corresponding to the peak positions, which are obtained by Gaussian fitting, are at 1.25 (E_{t1}), 1.52 (E_{t2}), 1.90 (E_{t3}), and 2.22 eV (E_{t4}) below the CBM. The deep trap level at 1.90 eV is believed to originate from the hydrogen migration or the dangling bond, called the K center, in the silicon nitride [21].

DLTS measurement was carried out in the temperature range from 100 to 350 K. A DLTS spectrum for the *a*-Si_3N_4 film is shown in Fig. 4(d). The DLTS peak was observed at about 295 K, which is equivalent to the trap energy of 0.55 eV (E_d), above the VBM of *a*-Si_3N_4. In view of the above

1–3

results, band alignment and defect states of the *a*-Si_3N_4 film can be summarized in Fig. 4(e).

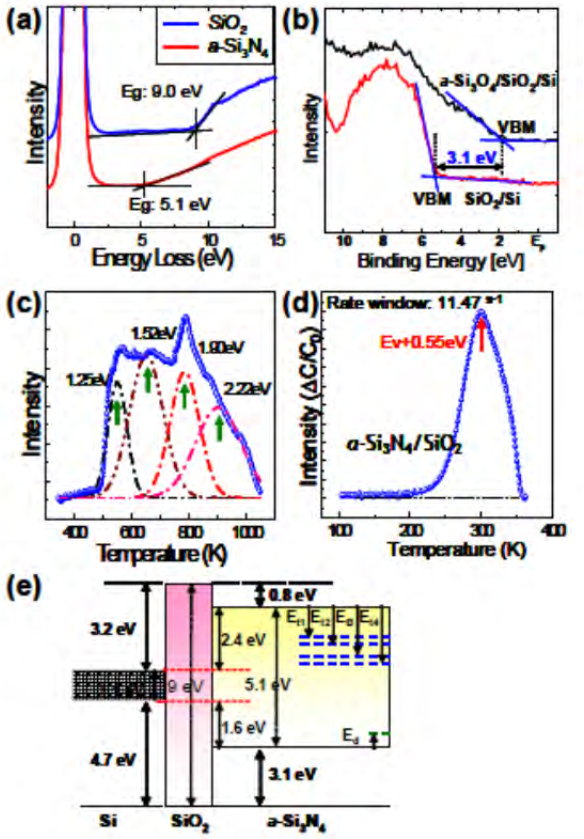


FIGURE 4. (a) REELS spectra for the *a*-Si_3N_4 and SiO_2 films at the primary beam energy of 3000eV. (b) Valence band spectrum of the *a*-Si_3N_4/SiO_2/Si heterostructure with a reference spectrum measured from the SiO_2/Si structure. (c-d) TSEE (c) and DLTS (d) spectra measured from the *a*-Si_3N_4 film. (e) Energy band diagram for the *a*-Si_3N_4 /SiO_2/Si system.

Analysis of charge leakage

Among the high-*k* materials, Al_2O_3 has been considered as an attractive candidate for the blocking oxide because it features a wide bandgap, a large value of conduction band offset, and a high-*k* value. While the performance of CTF memories with various Al_2O_3 stack structures has been widely investigated, less is known about the charge leakage problems through the Al_2O_3 film.

Figure 5 shows the structure characterization of the Al_2O_3 thin film deposited by atomic layer deposition (ALD) followed by thermal annealing at 1200 °C. We investigated the crystal structure and the electronic structure of the Al_2O_3 film using nano-area electron diffraction (NED) [22] and electron energy-loss spectroscopy (EELS) techniques, respectively. Figure 5(a) shows a high-resolution TEM (HRTEM) image of the Al_2O_3 film with a 7 nm thickness. The real space image of the incident beam probe (Fig. 5(b)) and corresponding NED pattern (Fig. 5(c)) obtained at the marked region (A) in Fig. 5(a) further show that the Al_2O_3 film consists of a polycrystalline structure.

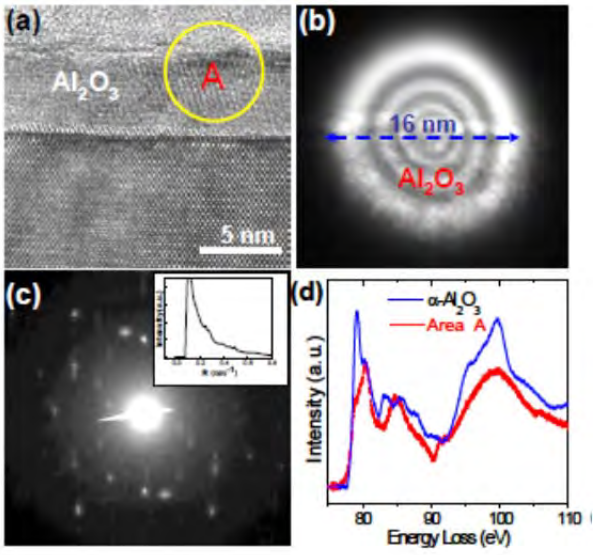


FIGURE 5. (a) Cross-sectional HRTEM image of the ALD-Al_2O_3 film. (b) An image of the electron probe with the Al_2O_3 film. The probe diameter is about 16 nm. (c) NED pattern from the marked region A of (a). (d) Core-excitation EELS spectra taken at region A as well as from the reference α-Al_2O_3.

The nano-area illumination enables the isolation of a single thin layer for electron diffraction. The radial intensity profile of the NED pattern shown in the inset of Fig. 5(c) indicates that the phase of the Al_2O_3 film is close to the γ-Al_2O_3, although there is some atomic displacement due to the defects. Figure 5(d) presents the core-excitation EELS taken at region A (in Fig. 5(a)) as well as at the reference α-Al_2O_3. With the Al-L_{23} energy-loss near-edge structure (ELNES) known to occur at the onset of 79.1 and 79.8 eV for α-Al_2O_3 and γ-Al_2O_3 [23], respectively, we confirm that the crystal phase of

the Al_2O_3 film is γ-Al_2O_3, in full accord with the NED result.

To crystallize the ALD-deposited Al_2O_3 film for lowering the defect density in the Al_2O_3 layer, post-deposition thermal annealing was performed at a series of temperatures (950 °C, 1050 °C, and 1200 °C). The crystallization behaviors during the annealing process were confirmed by X-ray diffraction (XRD) analysis. Fig. 6(a) shows the XRD spectra for the Al_2O_3 films. Obviously, XRD scan data taken from the Al_2O_3 films annealed at 950~1200 °C exhibit strong diffraction peaks of the γ-Al_2O_3 phase. Fig. 6(b) shows bandgap spectra obtained from the γ-Al_2O_3 films annealed at 950 °C, 1050 °C and at 1200 °C. The bandgap values are about 7.0 eV, regardless of the annealing temperatures. A higher bandgap of α-Al_2O_3 (8.9 eV) film can make a higher energy barrier than the γ-Al_2O_3 film that would block a back-tunnel to the gate electrode during the erase operation. However, there is a great deal of difficulty in making crystalline α-Al_2O_3 films using common deposition techniques.

Electron spin resonance (ESR) method [24] allows to measure the defect density in the γ-Al_2O_3 films. The ESR spectra of the as-deposited and annealed (1200 °C) γ-Al_2O_3 films measured at 15 K are shown in Fig. 6(c). Magnified ESR spectra are also shown in Fig. 6(d). They have a resonance at about 318.7 mT. The integrated intensity of ESR signal for the as-deposited γ-Al_2O_3 film is 1.4 times higher than that for the annealed (1200 °C) γ-Al_2O_3 film, indicating a 1.4 times higher defect density in the as-deposited γ-Al_2O_3 film. Thus the annealed (1200 °C) γ-Al_2O_3 film can lead to the retention enhancement of the CTF memory compared to the as-deposited γ-Al_2O_3 film due to the smaller electron traps of the blocking layer.

Analyses of the charge transport characteristics of Si nanocrystal-based memory are focused on the charge trapping, charge injection, and charge leakage phenomena. We demonstrated new TEM techniques, such as electron tomography with plasmon-filtered microscopy, *in-situ* electron holography, and NED, to characterize three dimensional distributions of Si-NCs embedded in the Si_3N_4 film, to directly observe the electron injection from the Si-NCs, and to determine the crystal structure of the Al_2O_3 thin film, respectively.

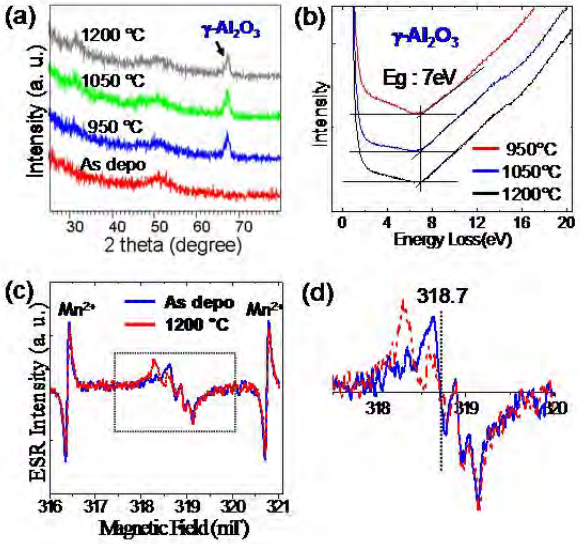


FIGURE 6. (a) XRD patterns of the ALD-Al_2O_3 films obtained after thermal annealing at 950~1200 °C. (b) REELS spectra of the ALD-Al_2O_3 films measured at the primary beam energy of 1500eV. (c) ESR spectra of the as-deposited and annealed (1200°C) γ-Al_2O_3 films measured at 15 K. (d) Magnified ESR spectra of the framed area shown in (c).

Furthermore, details of band alignment, defect states, and defect density were measured for the tunneling layer (SiO_2), charge trap layer (*a*-Si_3N_4), and blocking (Al_2O_3) layers using recently developed REELS, TSEE, DLTS, and ESR methods. We expect that the state-of-the-art analytical techniques described in this study will provide new pathways to disclose the nature of charge transport phenomena in CTF memories.

1–3

REFERENCES

1. J. Bu and M. H. White, *Solid-State Electronics* **45**, 113-120 (2001).
2. Y. Park , J. Choi, C. Kang, C. Lee, Y. Shin, B. Choi, J. Kim, S. Jeon, J. Sel, J. Park, K. Choi, T. Yoo, J. Sim and K. Kim, *IEDM Tech. Dig.*, 1 – 4 (2006).
3. M. Jung, K. Kim, G. Park and W. Cho, *Appl. Phys. Lett.* **94**, 053508 (2009).
4. W. J. Tsai, N. K. Zous, C. J. Liu, C. C. Liu, C. H. Chen, T. Wang, S. Pan, C. Y. Lu and S. H. Gu, *IEDM Tech. Dig.*, 719 – 722 (2001).
5. J. H. You, H. W. Kim, D. H. Kim T. W. Kim and K. W. Lee, *Simulation of Semiconductor Processes and Devices (SISPAD),* 199 – 2002 (2011).
6. M. L. Ostraat, J. W. De Blauwe, M. L. Green, L. D. Bell, M. L. Brongersma, J. Casperson, R. C. Flagan and H. A. Atwater, *Appl. Phys. Lett.* **79**, 433-435 (2001).
7. C. Lee, T. H. Hou and E. C. -C. Kan, *IEEE Trans. Electron Devices* **52**, 2697-2702 (2005).
8. H. I. Hanafi, S. Tiwari and I. Khan, *IEEE Trans. Electron Devices* **43**, 1553-1558 (1996).
9. J. S. Lee, Y. M. Kim, J. H. Kwon, H. Shin, B. H. Sohn and J. Lee, *Adv. Mater.* **21**, 173-183 (2009).
10. W. Chen, W. J. Liu, M. Zhang, S. J. Ding, D. W. Zhang and M. F. Li, *Appl. Phys. Lett.* **91**, 022908 (2007).
11. Y. C. King, T. J. King and C. Hu, *IEEE Trans. Electron Devices* **48**, 696-700 (2001).
12. Z. H. Ye, K. S. C. Liao, F. W. Shiu and T. K. Wang, *Microelectron. Eng.* **88**, 1194-1197 (2011).
13. Y. Seo, M. Y. Song, H. M. An, Y. S. Kim, B. H. Park and T. G. Kim, *J. Appl. Phys.* **112**, 074505 (2012).
14. Y. Seo, H. M. An, M. Y. Song and T. G. Kim, *Appl. Phys. Lett.* **100**, 173507 (2012).
15. A. Yurtsever, M. Weyland and D. A. Muller, *Appl. Phys. Lett.* **89**, 151920 (2006).
16. Y. Murakami, N. Kawamoto, D. Shindo, I. Ishikawa, S. Deguchi, K. Yamazaki, M. Inoue, Y. Kondo and K. Suganuma, *Appl. Phys. Lett.* **88**, 223103 (2006).
17. Z. Xia, D. S. Kim, J. Y. Lee, K. H. Lee, Y. K. Park, M. H. Yoo and C. Chung, *Simulation of Semiconductor Processes and Devices (SISPAD),* 233 – 236 (2010).
18. F. Paumier, V. Fouquet, M. J. Guittet, M. G. Soyer, R. H. French, G. Tan, Y. M. Chiang, M. Tang, A. Ramos and S. Y. Chung, *Mater. Sci. Eng. A* **422**, 29–40 (2006).
19. S. S. Hulluvarad, M. Naddaf and S. V. Bhoraskar, *Nucl. Instr. and Meth. in Phys. Res. B* **183**, 432-438 (2001).
20. C. Gong, E. Simoen, L. Zhao, N. E. Posthuma, E. V. Kerschaver, J. Poortmans and R. Mertens, *Photovoltaic Specialists Conference (PVSC)*, 858-862 (2010).
21. C. D. Valentin, G. Palma and G. Pacchioni, *J. Phys. Chem. C* **115**, 561–569 (2011).
22. J.M. Zuo, M. Gao, J. Tao, B.Q. Li, R. Twesten and I. Petrov, *Microsc. Res. Tech.* **64**, 347-355 (2004).
23. R. H. French, H. Müllejans and D. J. Jones, *J. Am. Ceram. Soc.* **81**, 2549-2557 (1998).
24. Y. H. Lee, D. H. Kim, Y. T. Jang, B. K. Ju and M. H. Oh, *J. Appl. Phys.* **87**, 7519-7523 (2000).

KEYWORDS

Charge trap flash memory, charge transport, Si-nanocrystal, band structure, defect states

2–1

THE VALUE ADD OF METROLOGY FOR THE SEMICONDUCTOR INDUSTRY

G. Dan Hutcheson

VLSIresearch inc., 2880 Lakeside Drive, Suite 350, Santa Clara, CA 95054

INTRODUCTION

The semiconductor industry spends upward of $5B per year on metrology equipment. That's about 2% of total revenues. Is it worth it?

VALUE ADD OR VALUE INSURE

Obviously it is; otherwise companies would not spend such huge sums. But some would argue that it doesn't add any value to the wafer. I once had a fab manager ask me what I thought of this and I answered that everything doesn't have to add value to be valuable. I asked what would happen if he shut down all the metrology tools in his fab. The answer was that there would be no yields. Hence at a minimum, metrology ensures the value of what has been made so it makes sense to add more value at the next step.

METROLOGY'S ROI

There is a second significant benefit: Metrology tools are the sense systems for yield learning in the fab. Without systematic decreases in defect density, yields would go down and Moore's Law would cease to work.

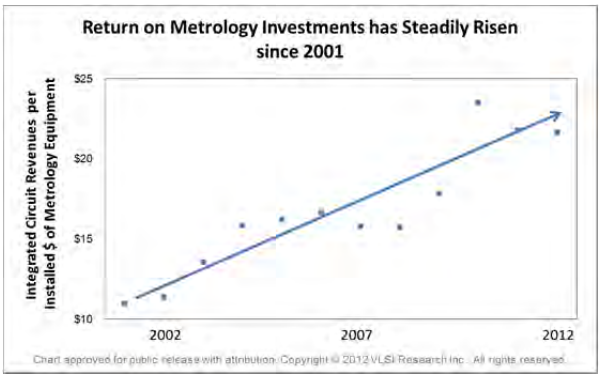


FIGURE 1. Return on Metrology Investments.

One way to measure that benefit is by calculating IC revenues from the installed metrology tools in the industry. From that perspective, revenues per dollar of installed metrology equipment have almost doubled over the last decade. In any given recent year, IC revenues are around twenty-one to twenty-four dollars per dollar of installed metrology equipment. That's up from around eleven dollars at the start of the millennium. That's quite an accomplishment.

THE VALUE OF YIELD

Metrology makes this possible by improving yield. A single percentage point in yield increases profits by around 8%. That is worth around forty billion dollars in additional shareholder value to the industry on an annualized basis.

2–1

Defect Density

If you look at any particular node, reducing defect density is the most important factor in driving a semiconductor company's profitability. During development defects must be cut by one-to-two orders of magnitude before a design can enter production. Once in production, there needs to be another defect density reduction of 50% or more to stay profitable.

Market Forces

This is because market forces drive chip prices down incessantly. But capital costs are fixed and material costs tend to rise with inflation. So the most immediate fix for a semiconductor company is to yield more die out of each wafer. Since they have already paid for the wafer, the only cost adder for the additional good die is packaging and final test. In other words, they have already paid for the bad die. If they can make future die good via reduced defect density they only have to pay packaging and final test cost to get to revenue. Packaging and final test cost is typically a fraction of wafer cost.

Time to money

All this must be done over relatively few quarters. A one quarter delay in defect reduction can cost almost half a billion dollars in lost revenues, given a normal high volume ramp. A four quarter delay in defect reduction can cost almost four billion dollars in lost revenues. Lose this much and it can cost a thousand or more jobs due to the lost production.

At the end of the day, metrology makes all this possible. The value of metrology comes in many forms: it's Return on Investment, increased revenues, faster time to money, greater profits, and the prevention of losses.

References

1. G. Dan Hutcheson, *The Chip Insider*®, Santa Clara: VLSIresearch, inc, October 11, 2012, pp. 1.
2. Robert Doering and Yoshio Nishi, *Handbook of Semiconductor Manufacturing Technology,* Boca Raton: Taylor & Francis Group, 2008, pp 35.1-35.20.

Keywords

Metrology, value-add, ROI, semiconductors

2–2

THE 2012 ITRS METROLOGY ROADMAP

Alain C. Diebold[1], Christina A. Hacker[2]

[1]College of Nanoscale Science and Engineering, University at Albany, 257 Fuller Road, Albany, NY
[2]Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899

INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) has provided a picture into the future technology requirements for integrated circuits for more than twenty years. The ITRS continues to project these technology requirements for transistor, memories, interconnect, and lithography with a fifteen year horizon. New materials and structures are described as potential solutions to circuit based requirements for future transistors, capacitors, and interconnect. Since the inception of the ITRS, metrology has been challenged by these requirements and the Metrology Roadmap captured these requirements and potential solutions.

2012 ITRS ROADMAP

The ITRS community recognizes that consumer electronics is now driven by much more than just computers. In an effort to understand this trend, "More than Moore" has become the accepted means of discussing the influence of RF, MEMS, sensors, Bio-chips and other technologies on the overall evolution of nanoelectronics. The ITRS maintains an overview of chip miniaturization through the Lithography, Front End Processes, Interconnect, Packaging, Metrology, and other roadmap sections.

2012 ITRS TECHNOLOGY PACING

The timing of the ITRS is now based on the ½ pitch of FLASH memory. The FLASH ½ pitch is expected to be 8 nm in 2024 and the gate length of a transistor in a logic device is 7 nm. Necessitating metrology methods near or at atomic scale dimensions which require a thorough understanding of nano-scale materials properties and of the physics involved in making the measurement. The complexity of the pacing of technology changes requires that different integrated circuit types be given separate scaling predictions. This information is summarized in Figure 1 along with the measurement technology requirements for Lithography Metrology.

		2013	2016	2019	2024
	Flash 1/2 pitch (nm)	*18*	*14*	*11*	*8.0*
	DRAM ½ Pitch (nm)	28	20	14	8.0
	MPU Printed Gate Length (nm)	28	20	14.0	6.0
	MPU Physical Gate Length (nm)	20	15.0	12.0	7
	Wafer Overlay Control (nm) - 20% DRAM	6.0	4.0	2.8	1.3
	Wafer Overlay Control Double Patterning (nm)	4	2	1	?
	Lithography Metrology				
Gate	Physical CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	2.1	1.6	1.2	0.7
Gate	Wafer CD metrology tool **uncertainty** (3σ, nm) at P/T = 0.2	0.42	0.31	0.25	0.15
Gate	Etched Gate Line Width Roughness (nm) <8% of CD	1.6	1.2	1.0	0.6
Dense Lines	Printed CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	1.9	1.5	1.1	0.8
Dense Lines	Wafer CD metrology tool **uncertainty** (3σ, nm) at P/T = 0.2	0.4	0.3	0.3	0.2
DP	*Double Patterning Metrology Requirements, Generic Spacer Patterning - Driven By Flash*				
DP	MetrOlogy Uncertainty for Core Gap (Carrier line)	0.4	0.3	0.2	0.1
Fin	*Fin Metrology*				
Fin	Metrology Uncertainty for fin top corner rounding radius (nm)	1.5	1.1	0.9	0.64

FIGURE 1. ITRS Metrology Roadmap Summary for Lithography Metrology showing the pacing of feature dimensions (CD=Critical dimension, P/T= precision to tolerance ratio).[1]

LITHOGRAPHY METROLOGY

Metrology for patterning processes is challenged by both feature shrinkage and the diverse requirements for potential future processes.[1] Near term multiple patterning processes such as double exposure, double patterning, and spacer double

2–2

patterning drive the need for advances in critical dimension and overlay measurement technology. Future patterning requirements for EUV lithography and directed self-assembly (DSA) using block co-polymers (BCP) drives additional requirements especially for mask (reticle) metrology for EUV. 3D device structures, such as FinFETs, provide additional challenges for CD metrology.

Critical Dimension Metrology

CD-SEM and scatterometry are expected to continue to provide viable measurement solutions, and with significant advances, may provide the necessary capability until the FLASH 14 nm ½ pitch.[1] New hardware such as Mueller Matrix Spectroscopic Ellipsometry is already enabling the application of Scatterometry to more complex features.[2] Advances in electron lens technology combined with use of frame averaging and advanced modeling of electron beam – sample interaction should provide next generation CD-SEMs capable of meeting measurement requirements to the 14 nm ½ pitch.

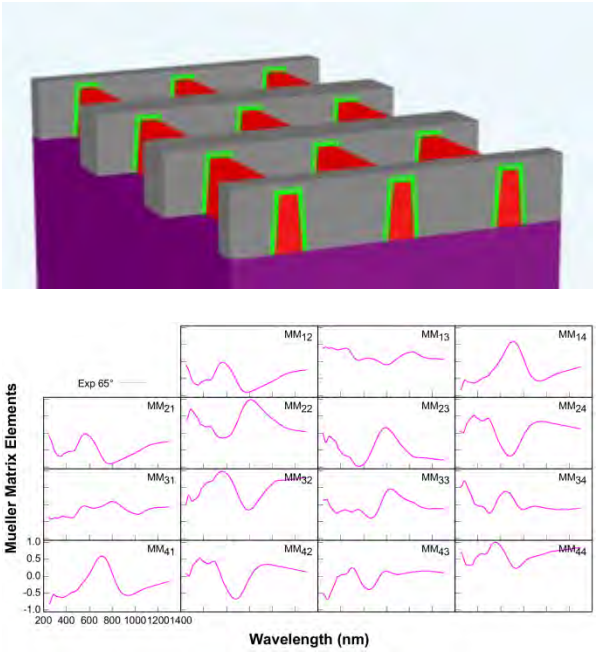


FIGURE 2. Mueller Matrix data for Fins with Gate on SOI. MMSE provides 16 MM elements vs the 2 for traditional Spectroscopic ellipsometry based scatterometry.

CD-Small Angle X-Ray Scattering

CD-SAXS measurements done using a synchrotron X-Ray source demonstrate a high potential for future technology nodes. Recently, the critical dimensions and feature shape of an array of DSA patterned BCP lines was measured using transmission small angle X-Ray scattering (t-CD-SAXS).[3] If transmission based CD-SAXS is going to be a viable metrology solution, transmission test structures must be accepted by the semiconductor industry. In addition, non-synchrotron based measurements must incorporate X-ray sources with sufficient brightness to enable high-throughput in-fab measurements.

Front End Processes

FEP metrology covers measurement needs for both transistor and memory devices. The key drives for transistor metrology are next generation high k, new channel materials and non-planar transistor structures. The switching mechanism of new memory devices is the subject of continued research.

New Channel Materials.

New channel materials such as silicon – germanium alloys, germanium, and III-V materials stacks all require measurements for process and defect control. While X-Ray methods already provide characterization of film composition and stress for blanket wafer samples, spectroscopic ellipsometry can be used to measure film thickness provided the stress state of the films is well known.[4] A key unmet requirement is for characterizing defects in the channel areas of patterned transistor structures. Here, the goal is to provide high throughput non-destructive methods.

Next Generation High K

Hf oxide based gate dielectric films are expected to continue scaling. This is driving the development of new processes that result in higher dielectric constants for hafnium oxide film stacks through inducing crystal phases or mixed phases with higher dielectric constants. The dielectric constant of

2–2

monoclinic (κ ~ 16), cubic (κ ~ 29) or tetragonal (κ ~ 70) crystal forms of hafnium oxide are well known.[5] Results from X-Ray characterization of some of these films is presented in Figure 3 and Figure 4. New optical models and an understanding of the variability of the grain texture are some of the metrology requirements for these higher κ materials.

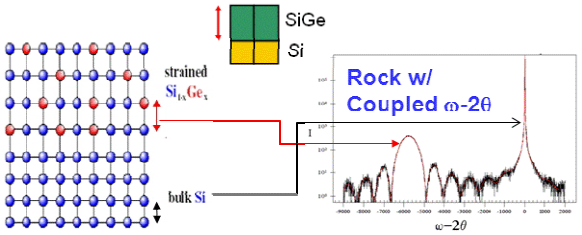


FIGURE 3. Omega- 2 theta X-Ray rocking curves combined with reciprocal space maps determine the Ge content of pseudomorphic Si(1-x)Gex alloys, film thickness, and prove that the films are fully stressed.[4]

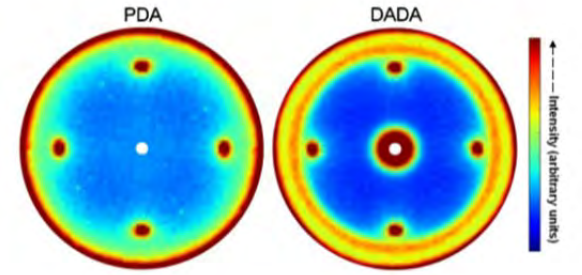


FIGURE 4. Pole figure analysis [d = 3.15 Å monoclinic (-111)] for two different high k deposition procedures. Figure from reference 5. [5]

New Memory

An understanding of the switching mechanism for RedOx memory will accelerate process and device development. Filaments are believed to form, and the reversibility of the filaments remains an open question. Considerable advances in metrology for through silicon vias (TSVs) include use of IR microscopy for wafer to wafer overlay measurement, ultrasonic microscopy for voids in bonding materials, and X-Ray microscopy for voids in filled TSVs.

INTERCONNECT

The possibility of new conductor metals may provide a new and largely unrecognized metrology challenge. Considerable advances in metrology for through silicon vias (TSVs) include use of IR microscopy for wafer to wafer overlay measurement, ultrasonic microscopy for voids in bonding materials, and X-Ray microscopy for voids in filled TSVs.

EMERGING RESEARCH MATERIALS AND DEVICES

Measurements for graphene based nanoelectronics continue to advance. One breakthrough study managed to measure the electrical impact of grain boundaries.[6] Future metrology demands will likely involve near-atomic resolution and measuring complex structures and properties (i.e. spin, resistance, stress, defect, etc) in 3-dimensions. An added bonus would be to achieve these results in real-time and nondestructively.

REFERENCES

1. International Technology Roadmap for Semiconductors, Semiconductor Industry Association, www.itrs.net.
2. Characterization of E-beam patterned grating structures using Mueller Matrix based Scatterometry, G.R. Muthinti, B. Peterson, R.K. Bonama and A. C. Diebold, Journal of Micro/Nano Lithography, MEMS & MOEMS, submitted.
3. C. Wang, et. al., SPIE Alternative Lithography Technologies IV, SPIE Advanced Lithography, (2012), abstract 8323-25.
4. G.R. Muthinti, M. Medikonda, T.N. Adam, A. Reznicek, and A.C. Diebold, J. Appl. Phys. **112**, (2012), 053519.
5. S. Consiglio, R. D. Clark, E. Bersch, J. D. LaRose, I. Wells, K. Tapily, G. J. Leusink, and A. C. Diebold, J. Electrochem. Soc. **159** (6), (2012), G80-G88.
6. A. W. Tsen, L. Brown, M. P. Levendorf, F. Ghahari, P. Y. Huang, R. W. Havener, C. S. Ruiz-Vargas, D. A. Muller, P. Kim, and J. Park, "Tailoring Electrical Transport Across Grain Boundaries in Polycrystalline Graphene," *Science* **336**, 1143 (2012).

KEYWORDS

Metrology, CD, Lithography Metrology, FEP Metrology, Interconnect Metrology

3–1

MONTE CARLO SIMULATIONS OF HELIUM AND NEON ION BEAM INDUCED DEPOSITION

P.D. Rack[1,2] and D.C. Joy
[1]*Department of Material Science and Engineering, University of Tennessee, Knoxville, TN 37996-2200, USA*
[2]*Center for Nanophase Materials Sciences Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831*

INTRODUCTION

The new Gas Field Ion Microscopes are able to deposit and etch material at the nanoscale in a highly controlled manner, but in order to exploit this capability it is necessary to have a detailed quantitative model of the process. A Monte Carlo simulation for He^+ and Ne^+ ion beam induced deposition (and etching) has been developed which provides data in excellent agreement with the observed experimental results over a wide range of experimental conditions. The ion beam induced nanoscale synthesis of PtC_x (where x~5) using the trimethyl (methylcyclopentadienyl)platinum(IV) ($MeCpPt^{IV}Me_3$) precursor is investigated by performing Monte Carlo simulations of helium and neon ions integrated with a gas handling routine to mimic the precursor adsorption and decomposition.

RESULTS

The simulation results [1] show that the helium beam leads to more lateral growth relative to the neon beam because of its larger interaction volume. Figure 1 depicts resting positions of 10,000 ions for both helium and neon simulations. It shows that much energy is dissipated in smaller volume for Ne ions as compared to that of helium ions. The lateral growth of the nanopillars is dominated by molecules deposited via secondary electrons in the both simulations. Notably, the helium pillars are dominated by SE-I electrons whereas the neon pillars by SE-II electrons as shown in Figures 2 and 3 respectively.

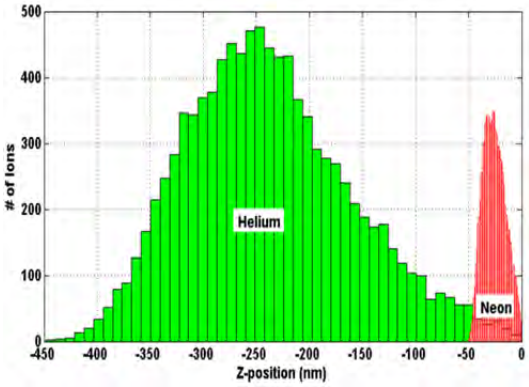


FIGURE 1. Histogram of resting position of Helium ions (green) and neon ions (red) in z-direction.

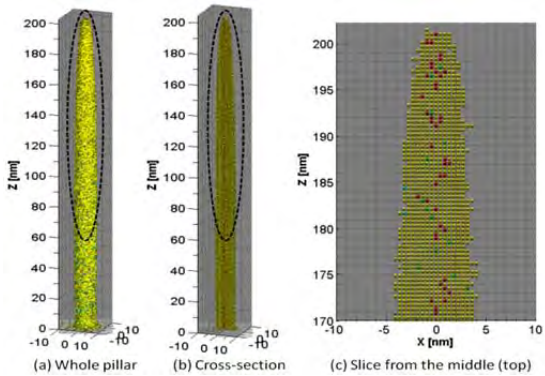


FIGURE 2. Deposited nanostructures of PtC_5 via Helium ion simulation at 70 µs precursor residence time.

3–1

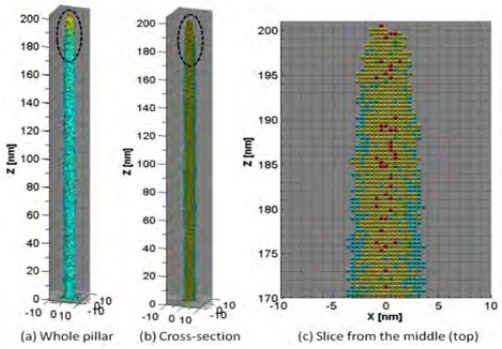


FIGURE 3. Deposited nanostructures of PtC_5 via Neon ion simulation at 70 μs precursor residence time.

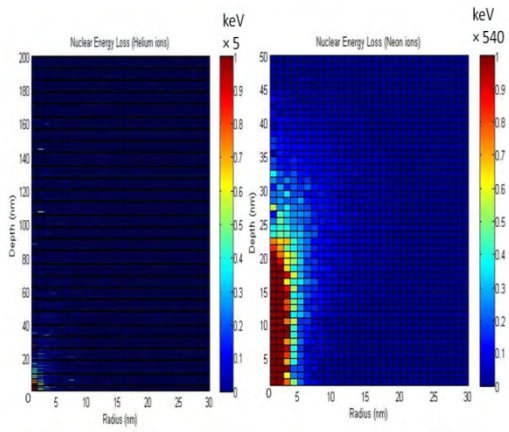


FIGURE 4. Deposited nanostructures of PtC_5 via Neon ion simulation at 70 μs precursor residence time.

Using a low precursor residence time of 70μs resulting in an equilibrium coverage of ~ 4%, the neon simulation has a lower deposition efficiency (3.5%) compared to that of the helium simulation (6.5%). At larger residence time (10ms) and consequently larger equilibrium coverage (85%) the deposition efficiencies of helium and neon increased to 49% and 21%, respectively; which is dominated by increased lateral growth rates leading to broader pillars. The nanoscale growth is further studied by varying the ion beam diameter at 10 ms precursor residence time. The study shows that total SE yield decreases with increasing beam diameters for the both ion types. However, the helium has the larger SE yield as compared to that of neon in the both low and high precursor residence time, and thus pillars are wider in all the simulations studied.

Finally, experimentally we have shown that He ion deposited material [2] has a larger room temperature resistivity (~$3.5x10^4$ - $2.2x10^5$ μΩ-cm) and temperature dependent transport behavior consistent with a granular material in the weak intergranular tunnel coupling regime. Conversely Ne ion deposited material has a much lower room temperature resistivity (~600 – $3.0x10^3$ μΩ-cm) and temperature dependent electrical behavior representative of strong intergranular coupling. The Ne ion deposited nanostructure has larger platinum nanoclusters, which is rationalized via Monte-Carlo ion-solid simulations that show the neon energy density deposited during growth is much larger due to the smaller ion range as shown in Figure 4. The plots depict the nuclear energy deposited via Helium and Neon simulations respectively. The observed platinum grain coarsening and subsequently lower resistivity for the Ne ions beam induced deposits is correlated to the enhanced platinum mobility via the enhanced nuclear stopping of the Neon ions.

Conclusion

We have explored nanoscale synthesis of platinum nanowires via focused helium and neon ion beam induced deposition. Monte Carlo simulations of the ion induced interactions reveal differences in the fundamental growth mechanisms due to the mass differences in the helium and neon mass and specifically the smaller ion range of the neon ions. Neon beam induced platinum deposits have much higher electrical conductivity than helium deposits. Characterization of the nanostructure reveal that the neon deposits have slightly larger platinum nanoclusters which is related to temperature dependent electrical measurements which suggest strong intergranular tunnel coupling. The grain coarsening is correlated to the nuclear energy density dissipated of the neon ions which enhance the platinum mobility via either binary collisions or a thermal spike.

Acknowledgement

We acknowledge experimental results were obtained in collaboration with H. M. Wu, L. Stern, J. H. Chen, M. Huth, C. H. Schwalb, M. Winhold, F. Porrati and C. M. Gonzalez. We also would like to acknowledge support of the Semiconductor Research Corporation (Bob Havemann program manager), Center for Nanophase Materials Sciences

3–1

at Oak Ridge National Laboratory by the Division of Scientific User Facilities, US Department of Energy.

References

1. R. Timilsina, D.A. Smith, P.D. Rack, Nanotechnology, (in press).
2. H. M. Wu, L. Stern, J.H. Chen, M. Huth, C.H. Schwalb, M. Winhold, F. Porrati, C.M. Gonzalez, R. Timilsina, P.D. Rack, Nanoscale (submitted).

Keywords

Gas Field Ion Microscope, Focused Ion Beam, Nanoscale Synthesis, Circuit Editing and Repair

3–2

LIMITS OF ABERRATION CORRECTED ELECTRON MICROSCOPY

R.M. Tromp[1,2], S.M. Schramm[2], and S.J. van der Molen[2]

[1]IBM T.J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598
[2] Leiden University, Kamerlingh Onnes Laboratorium, P.O. Box 9504, NL-2300 RA Leiden, The Netherlands

INTRODUCTION

The correction of spherical and chromatic aberrations constitutes one of the greatest breakthroughs in electron microscopy in the last 20 years[1]. In the Transmission Electron Microscope (TEM) resolution has improved[2] from the 0.1 nm level to 50 pm. In the Scanning TEM (STEM) the resolution has improved similarly, while at the same time imcreasing the current in the electron probe, facilitating powerful atom-by-atom spectroscopic imaging methods[3]. These microscopes make use of complex multipole optics to generate aberration coefficients that can compensate for the aberrations of the objective lens. In contrast, in Low Energy Electron Microscopy (LEEM) and Photo Electron Emission Microscopy (PEEM) aberration correction is achieved with much more compact cylindrically symmetric electron mirror optics[4] that can correct third order spherical and lowest rank chromatic aberrations over a broad range. While TEM and STEM usually operate at a fixed electron energy (at least in a single experiment), electron energy varies routinely in the range of 0-100 eV in LEEM and PEEM experiments, often over time periods of minutes or even seconds. The aberration constants, however, are strongly energy dependent, posing a significant challenge to the flexibility, reliability and accuracy of the aberration correction optics. The question then arises how accurately the aberrations must be corrected in order to achieve the full benefits afforded by these powerful new technologies.

ABERRATION CORRECTION

The aberrations of the cathode objective lens, the key component in a LEEM or PEEM instrument, depend strongly on the energy E_0 with which the electron leave the sample, and on the energy E gained in the electrostatic immersion field of the cathode lens. With a spacing L between the sample and the objective lens, the leading spherical and chromatic aberration coefficients C_3 and $_{Cc}$ of the electrostatic immersion field are given by[5] :

$$C_3=-C_c=L(E/E_0)^{1/2} \quad (1)$$

These coefficients are therefore strongly energy dependent, diverging at the low electron energies often used in PEEM experiments. As the start energy E_0 is frequently changed, both in LEEM and in PEEM in the course of a single experiment, the aberration correction optics must be able to adjust to these changing conditions 'on the fly', without significant and time-consuming operator intervention. In TEM and STEM such a requirement does not exist, as the electron energy –at least in a single experiment- is fixed. But even then aberration correction poses stringent requirements on the instrumental setup.

PARTIAL CORRECTION IN LEEM

This strong energy dependence in LEEM/PEEM poses a significant challenge on the aberration correction system, as the correction optics must be able to respond in real time to changes in E_0. It is important to establish the level of accuracy with which the aberration constants must be corrected.

3–2

Figure 1 shows an example[6] in which we plot the resolution as a function of the value of C_3, scaled to the value of the uncorrected system, for different values of the C_c from uncorrected (100%) to fully corrected (0%).

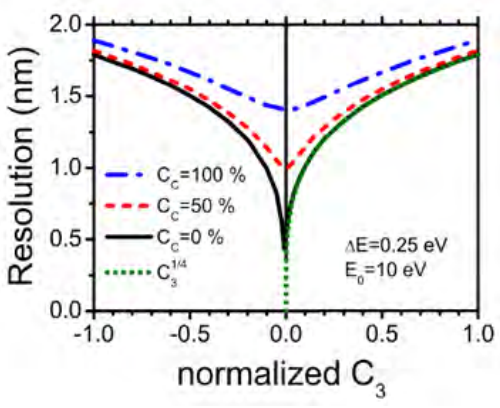


Figure 1. Resolution vs. the normalized value of C_3, for different settings of C_c (uncorrected = 100%, fully corrected = 0%). Start energy E_0 = 10 eV, ΔE_0 = 0.25 eV. Green dotted line: $C_3^{1/4}$ prediction

With C_c corrected we find a deep, cusp-shaped minimum near C_3=0. The green dashed line shows the $C_3^{1/4}$ power dependence of the resolution, predicted both by classical geometric optics and by a wave-optical treatment of the image formation process[6]. The figure shows a divergence in the change of resolution with respect to C_3 near the minimum, and a delicate dependence of the resolution on the accuracy and stability with which C_3 is corrected. With the derivative of the resolution diverging near the optimally corrected state, the system is intrinsically unstable. The higher the quality of the corrected state, the more unstable it is.

The Neighborhood Of The Corrected State In TEM

The neighborhood of the corrected state is shown in more detail in figure 2 for a 300 keV TEM, where the point resolution (defined as the spatial frequency at which the contrast transfer function first passes through zero) is plotted as function of C_3 and defocus C_1. The optimum resolution is achieved along the solid yellow line near the center of the figure[6,7]. When we deviate too far from the yellow line the resolution drops abruptly. Again, resolution is highly sensitive to the residual values of the aberration constants. For instance, a change in defocus of just 0.2 nm (the thickness of a single atomic layer), or in C_3 of 0.5 µm, already has a strong effect on resolution.

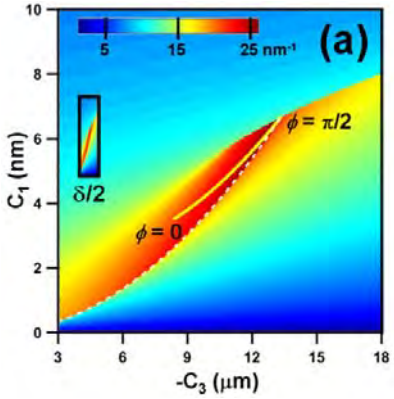


Figure 2. Point resolution for a C_3-corrected 300 keV TEM with the 5th order spherical aberration coefficient C_5=5mm. Optimum resolution is obtained for slightly negative C_3 and slightly positive defocus C_1. Small excursions from the optimum imaging conditions along the solid yellow line near the center can have strong effects on the achievable resolution. The inset labeled δ/2 shows the size of this map when a resolution improvement of a factor 2 is desired by additional correction of C_5.

If a further factor 2 improvement in resolution is desired, by correction of the 5th order spherical aberration coefficient C_5, the map shrinks even further, as shown by the inset labeled δ/2. Now the accuracy and stability with which defocus and C_3 must be set and maintained have shrunk to near-nothing, and it is unlikely that such an improvement could be realized experimentally in a phase contrast TEM instrument.

Other Factors

Of course, in addition to exquisite control of the electron-optical parameters many other factors are essential in obtaining the highest resolution, including mechanical stability, effective shielding against electromagnetic stray fields, stability of numerous power supplies, the laboratory environment, etc. The image detector also plays an key role. In LEEM and PEEM the detector used in

3–2

virtually all instruments consists of a channelplate image intensifier, a phosphor screen, and a lens-coupled CCD camera. The resolution of such a detector is very modest, about 130-150 μm across a 40 mm field (as measured in the detector plane). While it has been shown that Si-based detectors have the potential to be far superior[8], such image detectors have not been deployed in practice due to limited pixel count and low frame rates. We will present recent results obtained with a novel detector that delivers high pixel count, high resolution, and high frame rate at the same time, at a column electron energy of 15 keV.

The sensitivity of the corrected microscope to small inadvertent deviations in the microscope settings can have large effects on the achievable resolution as shown in figures 1 and 2. While corrected instruments have shown impressive gains in resolution, further improvements in resolution may be limited by these intrinsic sensitivities. As to the Low Energy Electron Microscope, the best resolution obtained without aberration correction is ~4 nm, at an electron energy of 3.5 eV. With correction the best resolution obtained to date is ~1.5 nm. We expect to improve this in the near future to 1 nm, just two times the wavelength of the electron. While a resolution of 0.5 nm is possible in theory, it is not clear that this can be realized in practice, due to the limiting factors discussed above.

References

1. P.W. Hawkes, Biology of the Cell **93** (2001) 432–439; Advances in Imaging and Electron Physics; Aberration-corrected Electron Microscopy, Volume **153** (P.W. Hawkes, editor) Academic Press, Amsterdam, 2008
2. C. Kisielowski, et al.; Microscopy and Microanalysis **14** (2008) 454; J. C. Meyer, C. Kisielowski, R. Erni, M. D. Rossell, M. F. Crommie, A. Zettl; Nano Letters, **8** (2008) 3582
3. See for instance S.J. Pennycook, M. Varela, A.R. Lupini, M.P. Oxley, M.F. Chisholm, J. Electr. Micr. **58** (2009) 87
4. R.M. Tromp, J.B. Hannon, A.W. Ellis, W. Wan, A. Berghaus, O. Schaff; Ultramicroscopy **110** (2010) 852; Th.Schmidt, et al.; Ultramicroscopy **110** (2010) 1358
5. R.M. Tromp, W. Wan, S.M. Schramm; Ultramicroscopy **109** (2013) 33
6. S.M. Schramm, S.J. van der Molen, R.M. Tromp, Phys. Rev. Lett. **109** (2012) 163901
7. R.M. Tromp, S.M. Schramm, Ultramicroscopy **125** (2013) 72
8. R. van Gastel, I. Sikharulidze, S.M. Schramm, J.P. Abrahams, B. Poelsema, R.M. Tromp and S.J. van der Molen, Ultramicroscopy **110** (2009) 33

Keywords

Electron Microscopy, Aberration Correction

3–3

ABERRATION-CORRECTED SCANNING TRANSMISSION ELECTRON MICROSCOPY

Ondrej L. Krivanek, Tracy C. Lovejoy and Niklas Dellby

Nion Co., 1102 8th St., Kirkland, WA 98075, USA

INTRODUCTION

Aberration-corrected Scanning Transmission Electron Microscopes (STEMs) are now able to image single atoms as light as boron; to determine the chemical type of single atoms using one of three different types of signals (annular dark field (ADF) image intensity, electron energy loss (EEL) spectrum, and X-ray spectrum); and even to probe the type of bonding holding a single atom in place, by analyzing the fine structure of its EEL spectrum. We review these advances and give a couple of recent examples of the progress. We then briefly describe another key advance presently taking place in aberration-corrected STEM: combining the ability to probe matter at atomic resolution with meV-level EELS resolution.

IMAGING AND ANALYSIS IN THE STEM

Aberration correctors that improved the resolution attainable by STEM instruments were developed in the late 1990s and early 2000s [1-3] (see [4] for a review), in parallel with correctors that improved the resolution of conventional TEMs [5]. They have since revolutionized the STEM's ability to image and analyze matter.

Present-day STEMs can resolve sample features spaced as little as 0.5 Å apart [6,7], and they can pack a nA-level beam current into an atom-sized electron probe [8]. At low primary voltages, they can perform imaging and spectroscopy with single atom sensitivity, in a way that is nearly damage-free in many types of samples [9-17].

EXAMPLES OF PRESENT-DAY STEM PERFORMANCE

Figure 1 shows STEM ADF images of single atoms of silicon embedded in monolayer graphene in two different configurations: (a) 4-fold, in which the Si atom replaces a C-C pair, and (b) 3-fold, in which it replaces a single C atom. The images were collected at 60 kV, with an electron dose of the order of 10^8 $e^-/Å^2$ for (a) and 10^7 $e^-/Å^2$ for (b), and there was no major sample damage.

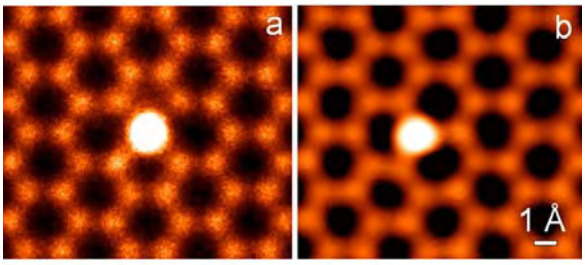


FIGURE 1. Annular dark field STEM images of single Si atoms embedded in monolayer graphene. a) Si in a four-fold site, b) Si in a 3-fold site. Courtesy Wu Zhou and Matthew Chisholm (see references [15] and [14]).

Figure 2 shows electron energy loss spectra obtained from the two types of Si atoms in a separate experiment also at 60 kV, and theoretical spectra modeled using density functional theory (DFT).

3–3

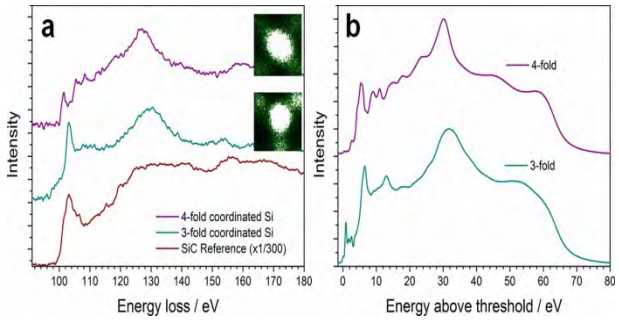


FIGURE 2. EEL spectra from the two types of individual Si substitutional atoms and from SiC. a) experimental spectra, b) simulations. Courtesy Quentin Ramasse (see reference [17]).

The dose for the experimental spectra was of the order of 10^{10} $e^-/Å^2$, and the Si atoms were liable to hop to neighboring sites in the graphene lattice while under observation. Although this did not change their atomic environment (3-fold Si atoms remained 3-fold coordinated and likewise for the 4-fold atoms), it would have made each atom move out of an atom-sized stationary beam. The resultant signal loss was prevented by scanning the beam over a small tracking window centered on each Si atom, and re-centering the window over the atom if it did hop to a neighboring site. The tracking windows used are shown as inserts in Fig. 2(a).

The agreement between the experimental and the simulated spectra is generally very good, with some small discrepancies remaining. The experiment has in fact been done independently in two different laboratories [16,17], and the agreement between the two sets of results is excellent. It is also worth noting that the best agreement for the 3-fold Si was only obtained if the Si atom was allowed to protrude about 0.5 Å out of the plane of the graphene, rather than being constrained to sit in the graphene plane [16, 17].

Because atoms are the basic building blocks of matter, it is clear that single atom imaging and analysis in the STEM are now reaching as fundamental a level of exploration as matter itself allows. It is also clear that an experimental technique that can examine individual atoms one-by-one, in their native environment, is not limited to looking at single atoms, and is in fact even more powerful when exploring the properties of the assemblies of atoms that constitute solid materials.

ULTRA-HIGH ENERGY RESOLUTION EELS

With aberration-corrected STEM now reaching down to the fundamental limits given by the materials rather than by the instruments, we are refocusing our energies on new instrumentation projects that are likely to bring as important benefits to materials research as aberration correction did.

Our first priority is improving the energy resolution of EEL spectra obtained with an atom-sized STEM probe, first to 30-40 meV, and ultimately to 10 meV and beyond. As the energy resolution improves, fundamentally new types of information will become available, starting with greatly improved inner-shell loss and low-loss spectral signatures, and moving onto, at 10 meV energy resolution and better, optical phonon spectroscopy. The second advance will amount to exploring a fundamentally new type of information: the interaction between the fast electrons and the atomic nuclei.

To attain these goals, we have designed and built a new type of an electron monochromator [18,19], which departs from previous designs in two fundamental ways. One, it monochromates the electron beam at the full primary energy, which helps to preserve the beam brightness by minimizing Coulomb interactions in the beam. Two, it employs stabilization schemes that make its energy resolution performance immune to variations in the high voltage of the microscope and in the monochromator main prism current [18-20]. The monochromator is fully dispersing-undispersing, i.e. it cancels the energy dispersion in the outgoing electron beam. At 60 keV primary energy, it has been able to produce monochromated beams ~1 Å wide [19].

Figure 3 shows EEL spectra obtained with the new system, with about 40 meV energy resolution

3–3

(i.e., with a 40 meV wide zero loss peak whose full height is 302 on the scale of Fig. 3 (a)) and about a 1 nm-sized probe [19].

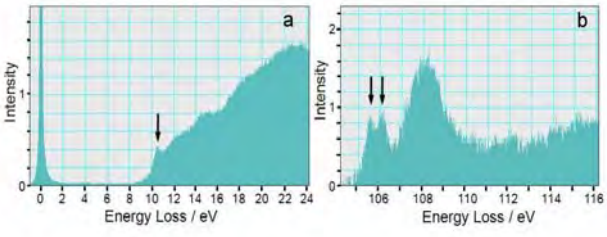


FIGURE 3. EEL spectra from SiO_2 in a MOSFET integrated circuit. a) low loss spectrum acquired in 0.2 s, b) background-subtracted Si $L_{2,3}$ edge acquired in 50 s.

The low loss spectrum shows an interesting sharp feature at about 10.5 eV (arrowed), which may be due to a band edge exciton. The Si $L_{2,3}$ edge shows a double peak at its threshold, at about 106 eV, split by 0.6 eV (two arrows).

Conclusion

Aberration-corrected STEM has introduced revolutionary new capabilities of great interest to materials science in general and semiconductor characterization in particular, and the revolution is by no means over yet.

References

1. O.L. Krivanek et al., "Aberration correction in the STEM", *Inst. Phys. Conf. Ser. (Proceedings 1997 EMAG meeting, J.M. Rodenburg, ed.)* **153**, 35–40 (1997).
2. O.L. Krivanek, N. Dellby and A.R. Lupini, "Towards sub-Å electron beams", *Ultramicroscopy* **78**, 1–11 (1999).
3. P.E. Batson, N. Dellby and O.L. Krivanek, Sub-Ångstrom resolution using aberration corrected electron optics, *Nature* **418**, 617-620 (2002).
4. O.L. Krivanek, N. Dellby and M.F. Murfitt, "Aberration Correction in Electron Microscopy", *Handbook of Charged-Particle Optics* (J. Orloff, ed., CRC Press, Boca Raton), 601-640 (2009).
5. M. Haider et al., "Electron microscopy image enhanced", *Nature* **392**, 768–769 (1998).
6. H. Sawada et al., "STEM imaging of 47-pm-separated atomic columns by a spherical aberration-corrected electron microscope with a 300-kV cold field emission gun", *J. Electron Microscopy* **58**, 357-361 (2009).
7. R. Erni et al., "Atomic-resolution imaging with a sub-50-pm electron probe", *Phys. Rev. Lett.* **102**, 096101 (4 pages) (2009).
8. N. Dellby et al., "Dedicated STEM for 200 to 40 keV operation", *Europ. Phys. J. Appl. Phys.* **54**, 33505 (11 pages) (2011).
9. O.L. Krivanek et al., "Gentle STEM: ADF imaging and EELS at low primary energies", *Ultramicroscopy* **110**, 935-945 (2010).
10. O.L. Krivanek et al., "Atom-by-atom structural and chemical analysis by annular dark-field electron microscopy", *Nature* **464**, 571-574 (2010).
11. K. Suenaga and M. Koshino, "Atom-by-atom spectroscopy at graphene edge", *Nature* **468**, 1088-1090 (2010).
12. T.C. Lovejoy et al., "Single atom identification by energy dispersive X-ray spectroscopy", *Appl. Phys. Lett.* **100**, 154101 (5 pages) (2012).
13. K. Suenaga et al., "Detection of photons emitted from single erbium atoms in energy-dispersive X-ray spectroscopy", *Nature Photonics* **6**, 545–548 (2012).
14. O.L. Krivanek et al., "Scanning transmission electron microscopy: Albert Crewe's vision and beyond", *Ultramicroscopy* **123**, 90-98 (2012).
15. W. Zhou et al., "Single atom microscopy", *Microscopy and Microanalysis* **18**, 1342-1354 (2012).
16. W. Zhou et al., "Direct determination of distinct atomic configurations and bonding of individual impurities in graphene", *Phys. Rev. Letts* **109**, 206803 (5 pages, 2012).
17. Q.M. Ramasse et al., "Probing the bonding and electronic structure of single atom dopants in graphene with electron energy loss spectroscopy", *NanoLetts* in press, DOI: 10.1021/nl304187e (2013).
18. O.L. Krivanek et al., "High-energy-resolution monochromator for aberration-corrected scanning transmission electron microscopy/electron energy-loss spectroscopy", *Phil. Trans. R. Soc.* **A 367**, 3683-3697 (2009).
19. O.L. Krivanek et al., "Monochromated STEM with a 30 meV wide, atom-sized electron probe", *Microscopy* **1** (inaugural issue), to be published (2013).
20. O.L. Krivanek and N. Dellby, "High resolution energy-selecting electron beam apparatus" *US patent application* #12/924,320 (2010).

Keywords

STEM, aberration correction, single atom imaging, single atom analysis, high resolution EELS

3–4

THREE-DIMENSIONAL AND SPECTROSCOPIC CHARACTERIZATION OF DEVICES AT THE ATOMIC SCALE USING ABERRATION-CORRECTED ELECTRON MICROSCOPY

Robert Hovden[1], Huolin L. Xin[2], Peter Ercius[2], Yi Jiang[3], Veit Elser[3], David A. Muller[1]

1 School of Applied and Engineering Physics, Cornell University
2 Lawrence Berkeley National Laboratory
3 Department of Physics, Cornell University

INTRODUCTION

With the development of aberration correction, scanning transmission electron microscopes (STEM) can probe sub-Angstrom features in a specimen. Semiconductor devices can be imaged in two-dimensions (2D) with atomic detail—revealing the underlying structure of defects and dopants in a material. In addition to enabling a high spatial resolution, the large convergence angles of aberration corrected instruments permit high-beam currents for chemical mapping. Electron energy loss spectroscopy (EELS) provides detailed information of composition and bonding information in devices and across interfaces. Constituent elements, such as Si, C, O, and N can be imaged down to atomic scales [1].

Accompanying the improved lateral resolution of such state-of-the-art machines is a greatly diminished depth-of-field (~6 nm) that poses challenges for nanocharacterization. Information outside of the focal plane quickly becomes blurred and less defined. It may not be possible to image a sample entirely in focus. Overcoming this limitation requires extended depth-of-field (EDOF) techniques that allow a single image, with all areas in-focus, to be extracted from a series of images focused at a range of depths [2]. Implemented from existing methods in the optical community, EDOF extracts the high-frequency information from a through-focal image stack in order to effectively extend the depth-of-focus in STEM. These methods are readily applied to extend the depth of focus of an aberration-corrected STEM for high-resolution imaging of devices over large fields of view.

Ultimately, these atomic resolution images are only 2D projections of a specimen. Modern structures in semiconductor devices have become smaller than the STEM sample thickness. In projection, information along the beam direction is averaged and lost. This includes information about liner-edge roughness and nanometer-scale reaction layers. Recovering the lost information requires 3D imaging [3]. Unfortunately, the resolution of a 3D STEM tomogram is hampered by missing information from the finite tilt range and the microscope's limited depth of focus—limiting volumetric resolutions to roughly 1 nm.

The current resolution limits of tomography can be overcome by collecting information beyond a

3–4

traditional tilt series. A novel through-focal tomographic technique utilizes depth sectioning at every specimen tilt and overcomes the limitations of aberration-corrected tomography, requires fewer tilt angles, and is less sensitive to initial focus determination. Comparisons of through-focal tomography with traditional tomography methods reveal improved contrast and resolution of extended objects over large fields of view.

Results

Chemical Mapping Of Devices

To study sidewall damage after etching of trenches in a porous low-k dielectric (Black Diamond IIx) the chemical distribution of elements was mapped using EELS. An EELS map (Fig. 1) shows non-uniformity in the etch where hardmask is undercut to 44 nm at the thinnest region. The porosity of the original SiCO layer can be seen as a splotchy pattern, showing a lower density of silicon in the EELS map. In this particular etch, the etching process has removed carbon at the etched surface creating an dense SiO_2 layer. Bonding information in the EELS signal shows that the SiO_2 interface layer matches that of bulk SiO_2 with a higher dielectric constant than the SiCO.

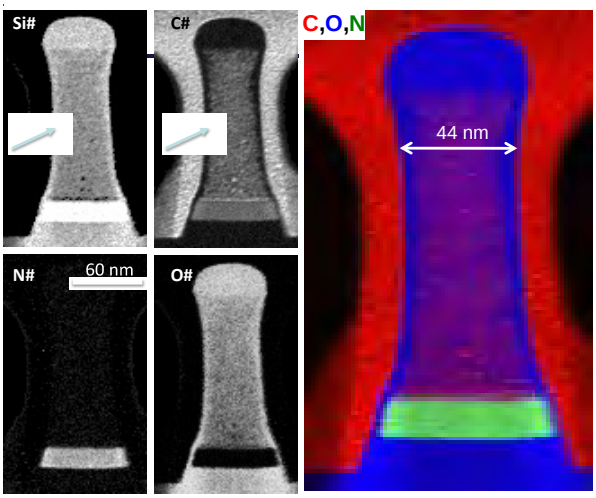


FIGURE 1. EELS map of 45 nm node NMOS device shows Si, C, N, O distributions. From an etching process, a silicon oxide layer has formed at the interface between the pillar and surrounding porous low-k SiCO material.

Extended Depth of Field For Devices

When imaging cross-sectional liftouts of semiconductor devices in an aberration-corrected microscope, the limited depth of field becomes immediately apparent. One region is in focus when another region is out of focus. The aberration corrected STEM image in Fig. 3a shows a gate oxide in focus while the drain contact of the same device is out of focus—and vice versa in Fig. 3c. Thus, only one region can be imaged with atomic resolution at a time. However, the small depth-of-field is overcome by acquiring a through-focal series of the specimen [2]. Then utilizing EDOF, the in-focus information out of each image in the series can be extracted and merged into a single (2D) image with an apparent extended depth-of-field [4]. Here we show that these algorithms are also applicable to atomic resolution imaging of semiconductor devices. Figure 3b. shows the reconstructed depth of field image of a transistor showing both gate-oxide and drain contact, where both regions are in focus with atomic detail.

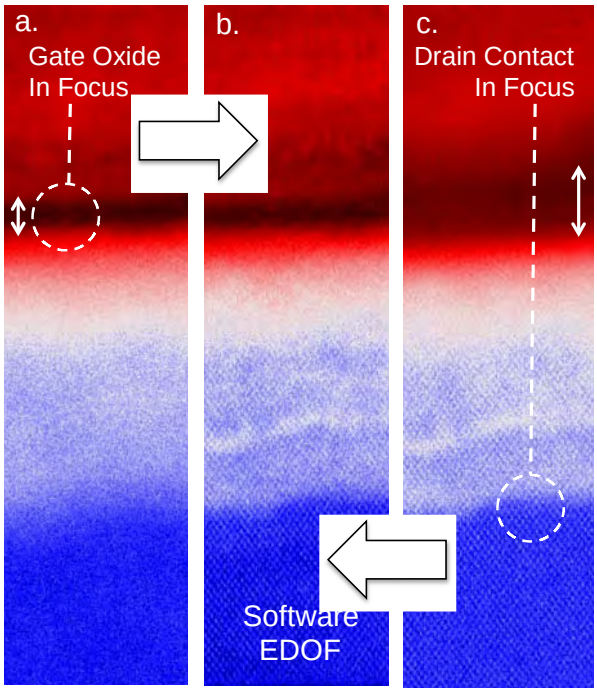


FIGURE 2. EDOF provides a single image of devices with all regions in focus (b). Normal imaging only permits either the gate oxide (a) or the drain contact to be in-focus (c). Out-of-focus imaging leads to incorrect

3–4

measurement of the oxide layer thickness (c). False colored dark field STEM image.

High-Resolution, Through-Focal Tomography of Extended Objects

A through-focal reconstruction was demonstrated on porous PtCu nanoparticles with similar dimensions and details to a modern integrated circuit. The pore structure provided a good metric for resolution of this novel technique. The through-focal tomography provided a continuum of 3D information in Fourier space (Fig. 3a) and a clear improvement in quality over traditional methods (Fig. b vs. d). The advantages of this technique are most dramatic over extended objects larger than the microscope's depth of focus (~5-10nm). In a traditional back projection, objects far from the center focal plane appear blurred and distorted (Fig. d)—leading to incorrect conclusions about morphology and certainly preventing any quantification. Through-focal reconstructions have an improved resolution and are free from these artifacts.

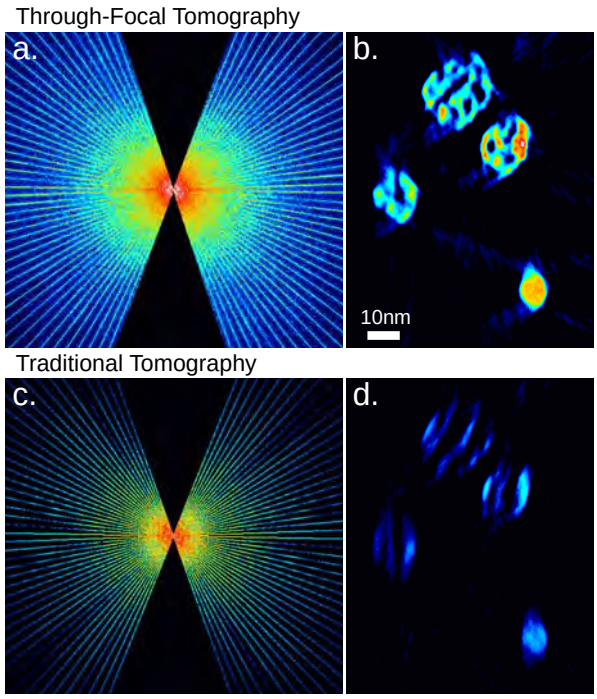


FIGURE 3. In Fourier space (a) through-focal tomography acquires a continuum of information throughout the microscope's tiltrange. In the real space reconstruction of porous nanoparticles, a cross section of several 3D particles shows clear presence of pores in the through-focal reconstruction (b); features that are missing or too heavily distorted in the traditional reconstruction (d)

Summary

Aberration corrected STEM provides high-beam currents with atomic resolution for EELS mapping of devices. The high-resolution comes with a small depth-of-field that can become problematic for specimen thicknesses larger than 5 nm. To overcome this problem when imaging devices over larger fields of view, extended depth of field algorithms can be utilized. For STEM tomography, the small depth of field can be used to enhance reconstructions by implementing through-focal tomography which acquires a through-focal image stack at every tilt.

Acknowledgements

Thanks to Phillip Stout who provided the BDIIx samples and Deli Wang who provided the PtCu nanoparticles. Supported by the Semiconductor Research Corp., the Cornell Center for Materials Research an NSF MRSEC (NSF #DMR 1120296), the Center for Nanoscale Systems at Cornell—an NSF NSEC (NSF #EEC-0117770, 0646547)—and Lawrence Berkeley National Laboratory supported by the U.S. Department of Energy (#DE-AC02-05CH11231).

References

1. D.A. Muller, et al, *Science*, **319**, 1073-1076 (2008)
2. R. Hovden, H. L. Xin, and D. A. Muller, *Microscopy & Microanalysis* **17**, 75-80 (2011)
3. P. Ercius, et al., *Microscopy & Microanalysis,* **15**, 244-250 (2009)
4. B. Forster, et al., *Microsc. Res. Tech.*, **65**(1-2), 33-42 (2004)

Keywords

Electron Microscopy, Tomography, Electron Energy Loss Spectroscopy, Aberration-Corrected

3–5

A Mirror-Corrected Scanning Electron Microscope

M. Steigerwald, C. Hendrich, D. Preikszas, and K. Schubert

Carl Zeiss Microscopy GmbH, Carl-Zeiss-Straße 56, 73447 Oberkochen, Germany

Introduction

In materials science and biological research the Scanning Electron Microscope (SEM) has a long tradition. In recent years the interest in the imaging of sensitive samples and the material contrast at a high lateral resolution has grown. Lowering the primary electron energy on one hand helps to reduce the sample damage. On the other hand the interaction volume is decreased, thus increasing the lateral information from the backscattered electron signal. Even in Transmission Electron Microscopy a very low acceleration voltage is desired to get lateral information on an atomic scale from samples which could not be imaged without dose-induced artifacts otherwise [1].

However, the low primary electron energy is extremely demanding to the electron optics, if not too much of the lateral resolution should be lost due to the increased wavelength of the electrons. In a suitable instrument typically the spherical and the axial chromatic aberration have to be corrected. Additionally, innovative detector schemes can provide enhanced analytic capabilities and can avoid limitations by signal noise and residual instrumental instabilities.

In our presentation we will discuss a mirror-corrected SEM, offering high-resolution analytics with efficient productivity to visualize even the most sensitive materials by use of electrons with energies far below 1keV. At these energies the resolution of conventional instruments is often very poor, but compensating for the primary aberrations of the objective lens can overcome this obstacle. The aberration correction by means of an electron mirror significantly increases the resolution especially for low energies; this has been proven in a unique spectro-microscope over the last 15 years [2, 3].

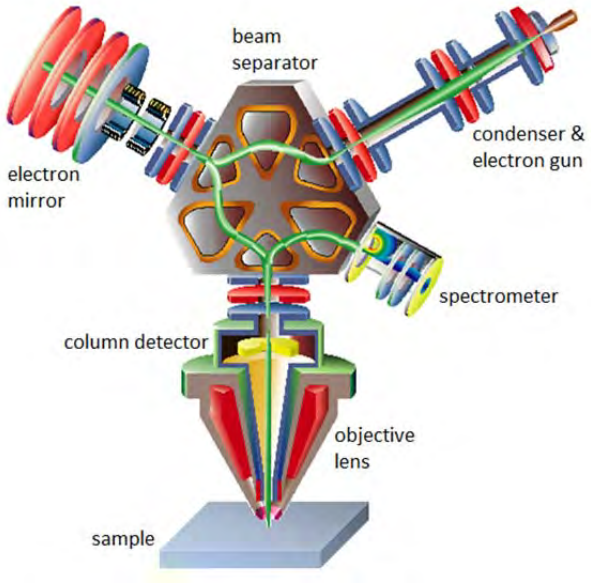


FIGURE 1. Schematic view of the mirror-corrected scanning electron microscope.

Electron Column

The mirror-corrected SEM roughly resembles the schematic view in Fig. 1. A low-aberration beam separator, which is especially free of dispersion, astigmatism, and distortion, is used to incorporate the electron mirror to the column. The primary

3–5

beam starts form the electron source, is prepared in the condenser, and deflected to the electron mirror by the beam separator. There the necessary negative spherical and axial chromatic aberration is produced, and the beam separator leads the reflected beam to the axis of the objective lens. After passing the objective lens the primary aberrations have been compensated, so that a high lateral resolution is possible even when the numerical aperture of the beam is large. In this way, for example, a resolution well below 2nm at a primary energy of 100eV should be possible.

Condenser Optics

The condenser focuses the electrons that leave the thermal field emission gun at the entrance plane of the beam separator with a certain probe current and under a certain illumination angle. This is done by three electrostatic condenser lenses. The first condenser lens changes the illuminated area of the beam-limiting aperture, thus adjusting the probe current. The subsequent condenser lenses form a zoom system, that is capable to vary the magnification at a constant intermediate image plane.

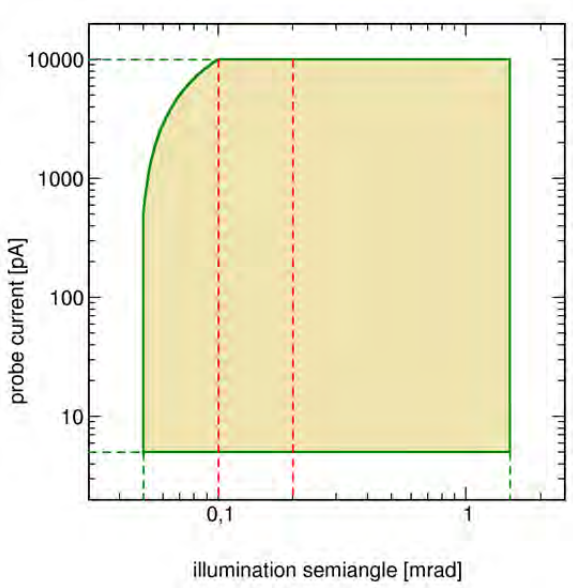


FIGURE 2. Accessible variation range of the condenser. The illumination semiangle is measured in the beam separator entrance plane.

An electron microscope that should be suited for imaging and analysis purposes aims for a probe current range from some pA up to some nA. If it makes use of an aberration corrector, the illumination angle has to be increased gradually at a constant focus and position condition of the beam while the corrected state is adjusted.

Fig. 2 illustrates the parameter range for our system. The probe current can be varied from 5pA to 10nA, whereas we expect the best results at 50pA. The optimum illumination semiangle at the beam separator entrance plane for the best resolution with the uncorrected objective lens lies between 0.1mrad and 0.2mrad. A smaller illumination angle can be chosen to get a large depth of focus. For the corrected mode, the illumination angle can be sufficiently increased to reach the maximum resolution that is theoretically possible. While doing so, a constant intermediate image plane and a stable optic axis can easily be achieved due to the absence of hysteresis effects in the electrostatic optics.

Mirror Corrector

The beam separator images one-to-one from its entrance plane to its exit plane, which are both situated in the near of the respective edges of the pole pieces, like shown in Fig. 3. Due to the composition of positive and negative magnetic dipole fields the overall dispersion cancels out in any plane: Electrons with slightly differing kinetic energies leave the beam separator at nearly the same position and at nearly the same angle.

Like in the whole column, the average kinetic electron energy in the beam separator is fixed at a constant value. The electrons are decelerated just at the end of the objective lens to reach the chosen landing energy. In this way the hysteresis effects in the ferromagnetic pole pieces of the beam separator do not harm the adjustment when switching between different landing energies.

After the first passage of the beam separator, the electron mirror reflects the beam while simultaneously imaging the exit plane of the beam separator onto itself. Therefore, the electrons pass

3–5

the beam separator a second time with an identical path of axial rays. Due to this symmetry the aperture aberration of second order cancels out, at least in theory. In practice, this aberration is at least largely reduced.

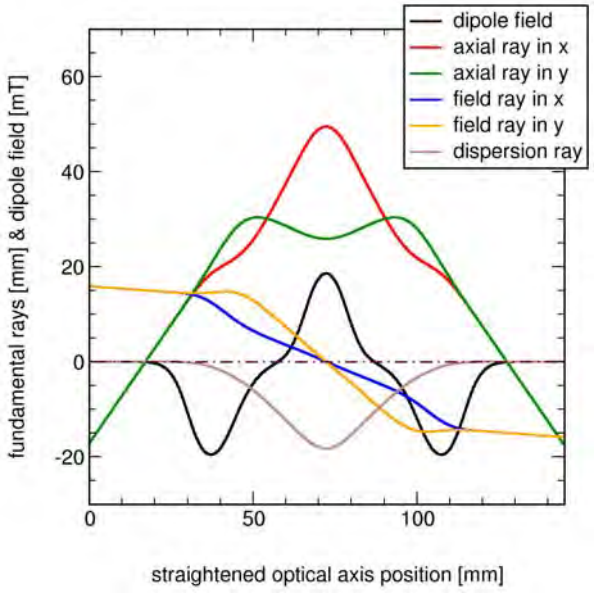


FIGURE 3. Dipole field (oriented in y) and fundamental rays in the beam separator, plotted along the straightened optic axis.

The electron mirror depicted in Fig. 4 consists of four electrodes. The electrode facing the beam separator is formed by the housing and connected to column potential. The remaining three electrodes are used to adjust the focal length, the spherical aberration, and the axial chromatic aberration. For these aberrations appropriate negative values are chosen, so that the aberrations of the objective lens and, to a very small part, the condenser lenses are compensated. As mentioned above, the focal length is determined by the imaging conditions of the beam separator.

While the corrected state is adjusted, all three variable potentials of the mirror have to be changed. This should not lead to an inacceptable shift or tilt of the optic axis, so the mechanical alignment of the mirror electrodes must be very precise. We met this requirement by special fittings and machining on an ultra-precise tool. The thermal expansion coefficients of the involved materials (titanium and ceramics) are similar, so that the thermal stability is sufficiently good. Additionally, two electrostatic deflection elements enable to steer the electron beam on the proper axis into the mirror.

FIGURE 4. Electron mirror with the three electrodes on variable potential. The fourth electrode is hidden inside the lower insulator.

A further prerequisite for imaging electron optics is a small sensitivity to magnetic stray fields. Due to the longer optic axis and the better resolution the magnetic impact on a corrected microscope compared to a conventional one is even larger. Therefore, the whole column of our microscope is covered by a threefold Mu-metal shielding.

Signal Detection

The electric field that decelerates the primary electrons at the end of the objective lens just in front of the sample simultaneously accelerates the signal electrons [4]. Nearly all secondary electrons (SE) and a good part of the backscattered electrons (BSE) are transferred back to the column by the objective lens. Due to the larger distance from the optic axis and the different kinetic energy of most of the signal electrons compared to the primary electrons a reasonable fraction of them is detected by the annular column detector (see Fig. 1).

3–5

But when approaching low landing energies, especially below 200eV, the difference between primary and signal electrons gradually vanishes and the signal detected by the column detector gets smaller: More and more signal electrons pass the central hole in the detector and usually are lost. However, in the mirror-corrected microscope the beam separator, that separates the incoming beam from the outgoing beam in the electron mirror, also separates the signal electrons from the primary beam. We modified the magnetic configuration of the signal path of our beam separator in a way to transfer as many signal electrons to the spectrometer position as possible, even when their kinetic energy differs strongly from the average value.

FIGURE 5. Grids for generating the retarding electric field in the spectrometer.

The spectrometer is realized by the retarding field generator shown in Fig. 5 with a subsequent combination of scintillator, light-pipe, and photo-multiplier. However, there is enough space to implement more sophisticated arrangements like magnetic or electrostatic sector field analyzers in the future.

With no retarding field, the arrangement works like a simple electron detector. With increasing retarding field, first the SE, then the BSE with large energy loss, and then the low-loss BSE are blocked from the detector. Taking subsequent images with different retarding fields and subtracting them shows significant contrast changes. This technique can be extended to measure whole spectra with a high lateral resolution.

RESULTS

Within the scope of a funded project [5] a corresponding technical demonstrator was developed and built. In the following we will present our first results.

HIGH-RESOLUTION IMAGING

After some exciting time of system integration, error analysis and search for the best adjustment we got reasonable images from our test samples.

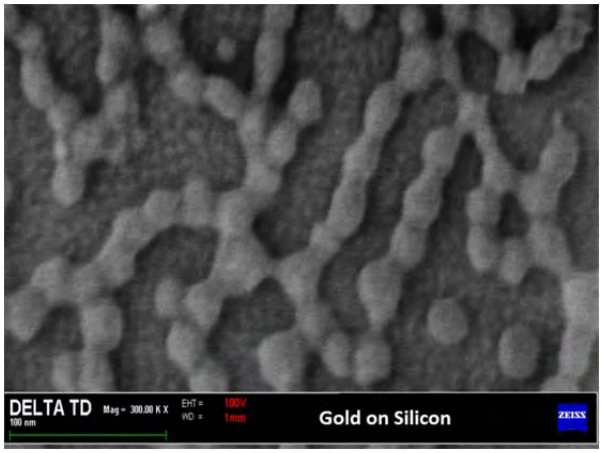


FIGURE 5. Gold on Silicon at 100eV landing energy and 1mm working distance.

For getting best contrast and resolution, Gold-on-Silicon samples proved to be superior to Gold-on-Carbon samples. Fig. 6 shows such a Gold-on-Silicon sample at a short working distance and at a landing energy of 100eV. The automatic resolution evaluation procedure that routinely works with conventional SEM results in a lateral resolution of 0.9nm ± 0.2nm.

HIGH-RESOLUTION ANALYSIS

3–5

For the test and the characterization of the spectrometer we must prepare signal electrons with well-defined energy distribution. This is done by biasing the sample to a negative voltage, so that the primary electrons are reflected in front of the sample. When increasing the retarding potential in the spectrometer, measured with reference to the cathode potential, from negative to positive values, the signal rises from zero to maximum. The 25-75% width of this rise amounts to 60V.

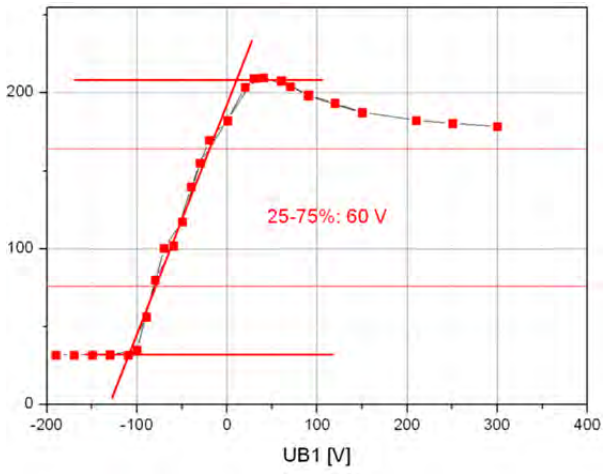


FIGURE 6. Signal of elastically reflected electrons versus the difference between the retarding potential in the spectrometer and the cathode potential.

The energy resolution of 60eV is limited by the lateral distribution of the signal electrons after passing the objective lens and the signal path of the beam separator. A better preparation of this lateral distribution would immediately result in a better energy resolution. For example, this can easily be achieved by an aperture within the beam separator and in front of the spectrometer that can be changed in size and location, but at the drawback of losing signal.

Conclusion

First very promising results of a mirror-corrected SEM with analytical detection capabilities were presented. It was shown that the instrument is best-suited for high-resolution imaging and analysis at very low landing energies, possessing the potential to cover important measurements addressed by the semiconductor roadmap.

Additional results which are expected to be collected in the near future will be presented at the conference. Information about the ultimate resolution, system stability and ease-of-use will be demonstrated, as well as application examples from semiconductor and materials science.

References

1. U. Kaiser et al., *Microscopy and Microanalysis* **16 (Suppl. 2),** 1702-1703 (2010).
2. R. Fink et al., *Journal of Electron Spectroscopy and Related Phenomena* **84**, 231-250 (1997).
3. T. Schmidt et al., *Ultramicroscopy* **110,** 1358-1361 (2010).
4. H. Jaksch et al., *Microscopy and Microanalysis* **9 (Suppl. 3),** 106-107 (2003).
5. This research was supported by the *German Federal Ministry of Education and Research* under contract **13 N 9430**.

Keywords

Scanning electron microscope, mirror corrector, high-resolution imaging, high-resolution analysis

TU–01

Real-Time Spectroscopic Ellipsometry In Atomic Layer Deposition Process

Han Wang, Xiaoqiang Jiang, and Brian G. Willis

Department of Chemical, Materials & Biomolecular Engineering, University of Connecticut, Storrs, Connecticut 06269

Introduction

Atomic layer deposition (ALD) has attracted much attention due to its capability for accurate thickness control and superior conformal growth [1]. Ellipsometry is an all-optical, nondestructive method, and *in-situ* real-time spectroscopic ellipsometry (RSTE) provides a simple and fast way to optimize and diagnose ALD processes [2, 3]. In this work, we investigate strontium oxide (SrO) as a model system to better understand temperature-dependent growth behaviors and complex substrate effects in ALD process [3, 4].

Experimental

ALD System

SrO thin films were deposited in a warm wall stainless steel reactor. The Sr-metal precursor was the THF adduct of $Sr(C_5{}^iPr_3H_2)_2$ (Air Liquide) [3]. H_2O vapor (Millipore 18 MΩ) was used as the oxidizer. The solid Sr source compound was heated to 140–145 °C in a glass container where it becomes a light yellow liquid. The temperature of the H_2O container was 25 °C. Both inert gas purging and vacuum were used between reactant exposures. Argon was regulated to maintain 1 Torr reactor pressure using leak valves; vacuum pumping was to below 10 mTorr. The whole ALD system was heated to a temperature higher than 150 °C to prevent precursor condensation on the reactor and tubing walls. Typical purging and pumping times were 40 and 30 s due to the relatively large reactor volume.

Spectroscopic Ellipsometry

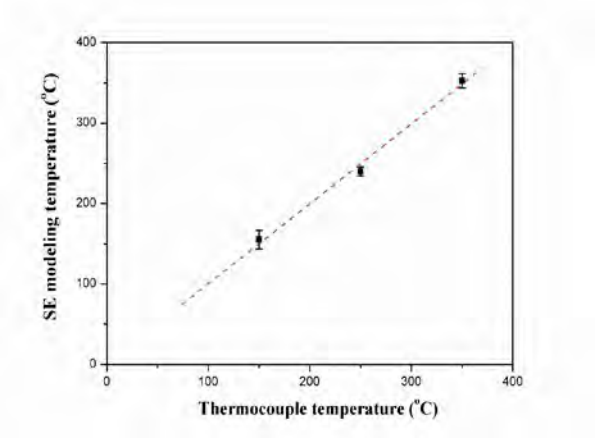


FIGURE 1. SE modeling temperature change as a function of thermocouple temperature

The whole ALD process was monitored via an M-2000 V™ spectroscopic ellipsometer with the COMPLETE EASE 4.32 data analysis software from J. A. Woollam Co., Inc. Ellipsometric Ψ and Δ data were acquired at a fixed angle of incidence (68°) over the spectral range 370–1000 nm (1.2–3.34 eV). Crystalline strontium oxide has an indirect band gap of approximately 5.7 eV and is transparent (k=0) over the whole photon energy range of our ellipsometer. A simple Cauchy model can be applied to extract the information of thickness and refractive index of thick SrO layers [2]. Because

TU–01

optical properties of silicon are temperature-dependent, they should be simulated by fitting Si substrate temperature before any ALD process. As shown in Fig. 1, the simulated silicon temperature is quite consistent with the one measured by thermocouple with 10 degree difference.

RESULTS

REACTION MECHANISM

RTSE measurements contribute useful information about reaction mechanisms, as shown in Fig. 2 [3]. Thickness versus time curves acquired at 200 and 250 °C show similar characteristics, where the apparent thickness abruptly increases during an Sr precursor feeding step and decreases after switching to water feeding. Following each Sr precursor pulse, the change in thickness during purging is negligible at 200 °C, but a small continuous decrease is discernible at 250 °C.

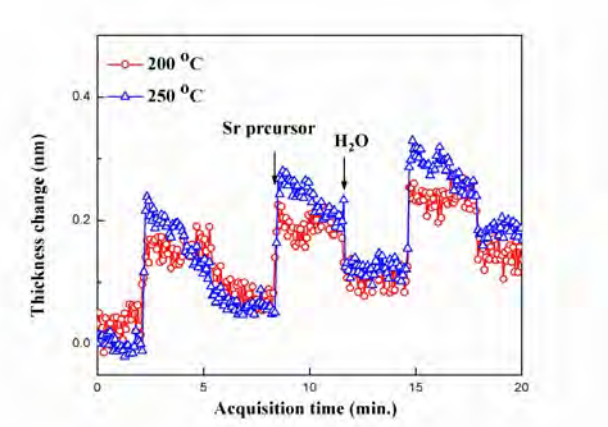


FIGURE 2. Apparent thickness change as a function of acquisition time at different deposition temperatures.

The ligand-exchange model, where hydrogen from the surface OH sites reacts with precursor organic ligands to eliminate the protonated ligand, is consistent with both the SE data shown in Fig. 2 and previous work by Rahtu et al [3, 5].

NUCLEATION EFFECT

Hydroxyl groups have been widely identified as the main reactive sites for the adsorption of metal precursors in metal oxide ALD processes [1]. Thus, the GPC is partially dependent on the number of OH groups on the surface and for a specific ALD process any non-linear growth behavior may result from the variation in the number of reactive sites.

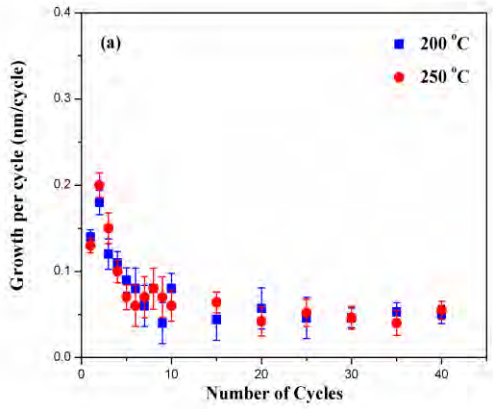


FIGURE 3. Growth per cycle (GPC) as a function of number of ALD cycles on ALD-grown Al_2O_3 surface at 200 and 250 °C

As shown in Fig. 3, SrO growth is promoted during the first few cycles compared to later ALD cycles on ALD-grown Al_2O_3 surface. The substrate-enhanced growth on Al_2O_3 surface probably indicates that the concentration of OH groups on SrO is less than on Al_2O_3 at both 200 and 250 °C. Also, the slowly decline of GPC during the first few cycles means a full coverage of SrO film is not achieved after the very first cycle probably due to the steric hindrance from the relatively large cyclopentadienyl complex. Steady growth characteristic of SrO homo-ALD is observed after 5-7 cycles.

TU–01

In Fig. 4, a more persistent substrate effect is observed for growth on SiO_2 surface. On SiO_2, the initial GPC also shows enhanced growth similar to Al_2O_3, but the effect is steady for a full 10 cycles. After 10 cycles, the GPC steadily decreases until reaches its final value after 30 and 25 cycles at 200 and 250 °C, respectively.

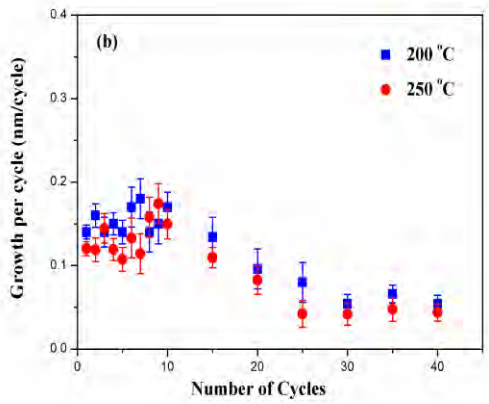


FIGURE 4. Growth per cycle (GPC) as a function of number of ALD cycles on SiO_2 surface at 200 and 250 °C

TEMPERATURE EFFECTS

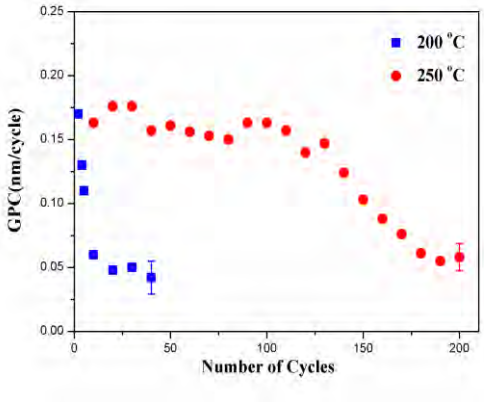


FIGURE 5. Annealing effect on GPC of SrO films grown at 200 and 250 °C.

We observed an unusual effect of annealing on the GPC of SrO films grown at 250°C and 200°C, as shown in Fig. 5. We firstly deposited a 3.5 nm film (about 40 cycles) on native SiO_2 substrates for both 250 and 200°C, followed by *in-situ* annealing of each sample at 350 °C under 1 torr Ar flow for 30 min. Prior to annealing, the samples reached the normal homo-SrO GPC of 0.6 nm/cycle. After annealing, additional SrO was deposited at the original deposition temperatures of 250 or 200°C.

As seen in Fig. 5, the annealing process has a large effect on the growth rate. At both temperatures, the first post-anneal GPC is more than a factor of 2 higher than normal growth. The effect is short lived for films deposited at 200 °C, but persists for more than 120 cycles for growth at 250°C. Eventually, the effect decays back to normal growth for both temperatures. The observations show that the GPC is sensitive to the changes of the substrate induced by the in-situ annealing treatment.

CONCLUSIONS

In-situ RTSE was applied to the SrO ALD process. The surface reactions between precursors and the surface could be monitored via noninvasive ellipsometry with robust submonolayer sensitivity. Initial growth is strongly affected by the choice of substrates and *in-situ* annealing leads to unusual effect with significant enhancement of the growth rate.

REFERENCES

1. R. Puurunen, *J. App. Phys*. **97**, 121301 (2005).
2. E Langereis, et al*., J. Phys. D: Appl. Phys*. **42,** 073001 (2009).
3. H. Wang, X. Qiang, and B. Willis*, J. Vac. Sci. Technol. A* 30, 01A133 (2012).
4. H. Wang, X. Qiang, and B. Willis, submitted.
5. A. Rahtu, T. Hanninen, and M. Ritala*, J. Phys. IV* **11**, 923 (2001).

KEYWORDS

in-situ, spectroscopic ellipsometry, real-time, atomic layer deposition

TU–02

MEASURE THE ELECTRON AND HOLE CONTACT RESISTANCE IN GATED KELVIN STRUCTURE

Hui Yuan †,*, Curt A. Richter *, Hao Zhu †,*, Haitao Li †,*, Oleg Kirillov *,

Dimitris Ioannou † and Qiliang Li †

† Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030
** Semiconductor and Dimensional Metrology Division, NIST, Gaithersburg, MD 20899-8120*

INTRODUCTION

Si nanowire (SiNW) has been considered as one of the most attractive nanomaterials for future Field Effect Transistor (FET) as it represents one of the ultimate, one-dimensional mediums with effective electron conduction. We have previously been engaged in the research of bottom-up Si nanowire FETs with gate-all-around (GAA) structure for high performance. [1-2] GAA structure provides excellent electrostatic gate control over transistor channel even when channel length is scaled below 10 nm. [3] However, the small contact area between SiNW and source/drain metal leads to large contact resistance which could dramatically degrade the device performance. In multiple-gate FinFETs, the contact resistance dominates the parasitic resistance due to the narrow width of their S/D regions. [4] Therefore the study of contact resistance in nanoelectronics becomes very important. However, the conventional methods, such as transfer length method and Kelvin structure, may not be precise enough as the channel become very low doped (even intrinsic) and very small.

In this work, we have designed and fabricated a gate-assisted Kelvin test structure which is based on two FETs integrated on a single SiNW to measure contact resistance. The two single SiNW FETs with 50 nm channel length are connected in symmetry with a metal/SiNW contact in the middle. The SiNW FETs are ambipolar, so the carrier type in the conducting channel can be selected by applying positive and negative gate bias. Therefore, the contact characteristics for electron transport and hole transport can be separated and measured.

FABRICATION

The SiNW was grown from Au catalyst by low pressure chemical vapor deposition at 420°C with SiH_4 as precursor. The nanowires were harvested into a methanol and dispersed on a p-Si substrate with 300-nm dry SiO_2. Then the nanowires were oxidized at 750 °C for 5 minutes in O_2 flow with rapid thermal oxidation (RTO) to achieve 2 nm ~ 3 nm thermal oxide. As shown in Figure 1,

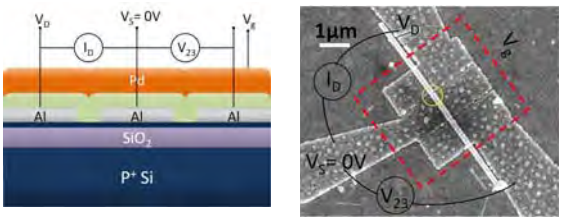


FIGURE 1. Device structure and measurement set-up: (Top) schematic diagram, (Bottom) SEM image of the nanowire and channel in the yellow circle in middle image. Yellow circle indicates a FET.

the devices were fabricated with conventional

TU–02

methods used in semiconductor technology including e-beam and photo lithography, metal deposition and lift-off. Al metal with 1 μm in width and 100 nm in thickness was deposited to form a Kelvin test structure so that the contact resistance on the middle electrode can be characterized. Then, 20-nm HfO_2 was deposited by atomic layer deposition (ALD) at 300 ℃ followed by 100-nm Pd deposited as the gate. In the last step, the samples were annealed at 200 ℃ in Ar for 2 minutes to improve roughness and defects metal contacts around the nanowires. We believe the part of SiNW surface underneath the contact has been easily doped to p-type by Al atoms because one dopant atom in such a small nanowire body will induce significant doping concentration. [7]

RESULTS AND DISCUSSION

Before the characterization of contact resistance, current-voltage (IV) properties of the SiNW FETs were measured. As shown in Figure 2(a), such

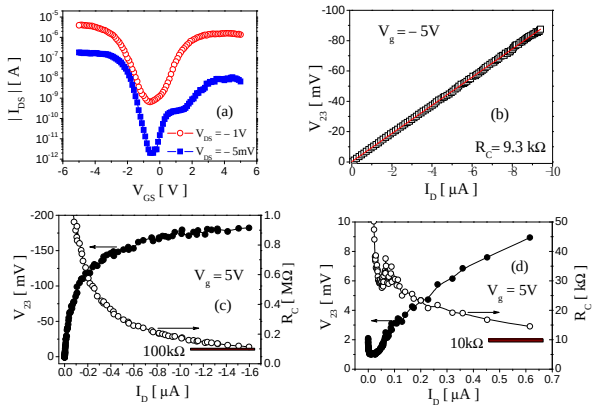


FIGURE 2. Electric characterization: (a) Ambipolar I_{DS} vs. V_{GS} characteristics. (b) hole-transport contact characteristics selected by negative V_{GS}. (c) and (d) electron-transportation contact characteristics selected by negative V_{GS}. (c) electrons injected from SiNW channel; (d) electron injected from metal.

short-channel SiNW FETs exhibited ambipolar characteristics with electron conductance lower than hole.

These ambipolar IV characteristics indicated both hole and electron conductance could be selected in the SiNW FET channel by negative or positive gate bias, respectively. Our SiNW was not intentionally doped and was intrinsic in the channel. The part of SiNW surface under Al contact was doped to p-type making the devices more like p-type FETs. However we can still see electron current at positive gate bias. This is because gate electric field penetrates in the gate-to-source/drain overlap region and helps building electron channel from source to drain in such a short distance.

For the characterization of contact resistance with measurement set-up hown in Figure 1, the Kelvin test structure includes three parallel electrodes on the same Si nanowire with two gates of 50 nm in length in between. We connected the middle electrode as the sources and an electrode on two sides as drains of the FETs. Source and bottom p^+-Si were grounded. The channel current (the source-to-drain current, I_{DS}) is driven by V_{DS}. Therefore the direction of carrier flow through the middle contact was controlled by selecting positive or negative drain voltage (V_D). The non-local voltage, V_{23}, between the source and an extra electrode on the other side of the SiNW is measured as the voltage drop across the source contact. And the contact resistance is given by [9]:

$$R_C = \frac{V_{23}}{I_D}$$

Under negative gate bias, the SiNW channel is accumulated with holes. The nonlocal voltage V_{23} is linear with I_{DS}, as shown in Figure 2(b), indicating Ohmic-contact like contact resistance for hole transport. The linear fitting gave a contact resistance of 9.3 kΩ. Roughly assuming that the Si nanowire is 100 nm in diameter and the contact is 1μm in width, the specific contact resistivity is about 2.9×10^{-5} Ω.cm^2.

For the electron conduction selected by positive gate bias, the contact resistance is much higher, and more interestingly it is sensitive to the electron's flow direction. The I_{DS}-V_{23} dependence is similar to I-V characteristics of a pn junction (see Figure 2c and 2d). Such a pn junction was formed under the

Al metal contacts during the deposition of HfO_2 and annealing, as discussed in fabrication section. [7] It should be noted that this pn junction could be formed and tuned by field effect which is different with a conventional two-terminal pn junction. As shown in Figure 3, the energy band bending is controlled by the gate to source voltage, V_{GS}, rather than the bias on the junction. When V_{DS} < 0,

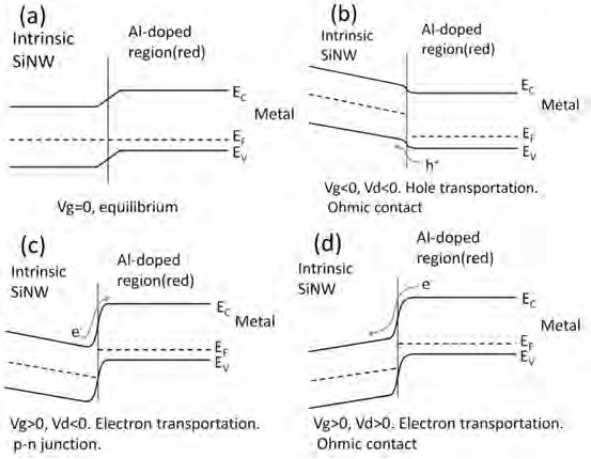


FIGURE 3. Band diagram of the contact area at different bias. (a) Vg= 0, equilibrium situation; (b) Vg< 0, VDS< 0. Hole transportation, Ohmic contact; (c) Vg> 0, VDS< 0. Electron transportation, Schottky barrier; (d) Vg> 0, VDS> 0. Electron conductance, Ohmic contact.

electrons flow from channel to metal, vice versa for V_{DS} > 0. Electron climbing up a barrier hill to reach metal contact (c) will experience higher resistance than electron going down the hill (d). We found that the contact resistance at condition (c) saturated at about 120 kΩ, while the contact resistance at condition (d) saturated at 10 kΩ. That means the contact resistance of electron flow at condition (d) finally saturated at that of hole conduction. We believe that this 10 kΩ is due to the intrinsic resistance of the contact materials in both sides. In addition, negative differential resistance appeared when I_{DS} is very low at (c) V_{DS} > 0. We believe this is due to the charging and discharging of the interface states at the contact.

CONCLUSION

In summary, we have designed and fabricate the gated Kelvin test structure based on SiNW FETs. The test structure helped us to study the contact resistance and junction property in nanoelectronics. This structure is very attractive as it is able to select the carrier type in the same contact by switching the gate voltage. We believe this new characterization metrology will lead to new application in nanoelectronics.

REFERENCES

1. M. P. Brown and K. Austin, *The New Physique*, Publisher City: Publisher Name, 2005, pp. 25-30.
2. M. P. Brown and K. Austin, *Appl. Phys. Letters* **85**, 2503-2504 (2004).
1. Q. Li, X. Zhu, Y. Yang, D. E. Ioannou, H. Xiong, D. Kwon, J. S. Suehle, and C. A. Richter, Nanotechnology **20**, 415202 (2009).
2. X. Zhu, Q. Li, D. E. Ioannou, D. Gu, J. E. Bonevich, H. Baumgart, J. S. Suehle, and C. A. Richter, Nanotechnology **22**, 254020 (2011)
3. J. P. Colinge, "Multiple-gate SOI MOSFETs" in Solid State Electron., vol. 48,no. 6, pp. 897-905, 2004
4. J. Yu, S. Chung and J. R. Heath, J. Phys. Chem. B **104**, 11864-11870 (2000)
5. W. T. Lynch and K. K. Ng, IEEE Int. Electron Dev. Meet. Digest, **1988**, 352-355 (1988)
6. D. K. Schroder, "Semiconductor material and Device Characterization" 3rd Ed. Hoboken, New Jersey: John Wiley and Sons, Inc., 2006, pp. 143.
7. J. R. Heath and M. A. Ratner, Physics Today 56, 43 (2003)

KEYWORDS

Contact resistance, silicon nanowire, Kelvin structure

TU–03

TRANSMISSION ELECTRON BACKSCATTER DIFFRACTION (T-EBSD) FOR CHARACTERIZING ULTRATHIN FILMS IN THE SEM

Katherine P. Rice, Roy H. Geiss, Robert R. Keller

Applied Chemicals and Materials Division, National Institute of Standards and Technology
Boulder, CO 80305

INTRODUCTION

Transmission electron backscatter diffraction (t-EBSD) is a new technique of materials characterization using a standard scanning electron microscope (SEM).[1] By changing the sample-detector geometry so that electrons pass *through* a thin specimen prior to entering a commercial EBSD detector, an interaction volume significantly smaller than that typically associated with conventional EBSD can be achieved. As a result, electron diffraction data in the form of Kikuchi patterns can be collected from extremely fine-scale films and particles, down to the sub-10 nm dimensional scale. In conventional EBSD, incident electrons are thought to undergo Kikuchi scattering in the top 10 to 40 nanometers of a film [2], thereby requiring a film at least that thick to produce a diffraction pattern, while achieving a lateral spatial resolution in the typical range of 20 nm to 35 nm parallel to the tilt axis and 80 nm to 90 nm perpendicular to the tilt axis. Here we present recent results and electron scattering simulations associated with probing the sampling limits of the t-EBSD technique for semiconductor industry-relevant films as thin as 5 nm, while maintaining single-nanometer lateral spatial resolution.

ULTRATHIN FILMS

Ultrathin high dielectric constant (k) layers are desired to make nanoelectronic devices smaller and more efficient. Hafnium oxide, a high-k dielectric important in the industry for capacitor and memory applications, has properties that are crystal structure-dependent [3]. However, characterization of increasingly thinner films presents challenges, as less material is available for established crystallographic techniques such as x-ray diffraction. Cross-sectional TEM is not only time-consuming, but it provides only limited information about the planar uniformity of the film; furthermore, direct crystallographic data by TEM methods are not easily collected for material volumes with characteristic dimensions smaller than 10 nm due to the low scattering cross sections associated with ~ 200+ keV electrons. Transmission EBSD, performed at ~ 20 keV, provides information from large areas of ultrathin films, while requiring only little material volume, by capturing forward-scattered electrons in transmission with standard EBSD equipment (Figure 1).

TU–03

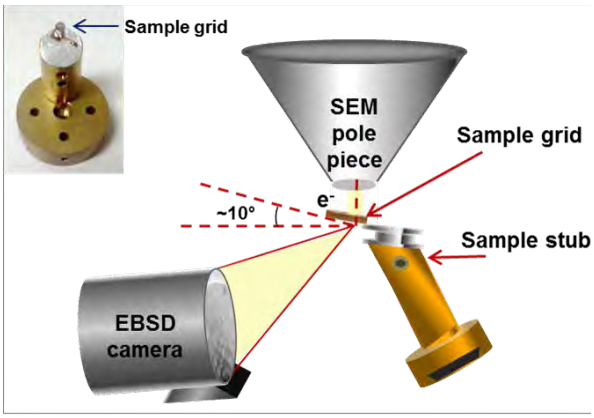


FIGURE 1: Sample geometry for t-EBSD technique

To examine samples, we typically use a standard carbon- or nitride-membrane copper TEM grid, where the films can be deposited directly on the grid by sputtering, thermal evaporation, or atomic layer deposition, or they can be picked and placed with micromanipulator methods.

Atomic layer deposition is an ideal technique for probing the efficacy of the t-EBSD method because of the high degree of uniformity and thickness control of the film. However, the films are typically deposited amorphously and need to be processed with high-temperature anneal to induce crystallinity. Figure 2 shows t-EBSD patterns obtained from annealed (3min. at 500 °C) HfO_2 films of thicknesses (a) 10 nm and (b) 5 nm deposited by ALD.

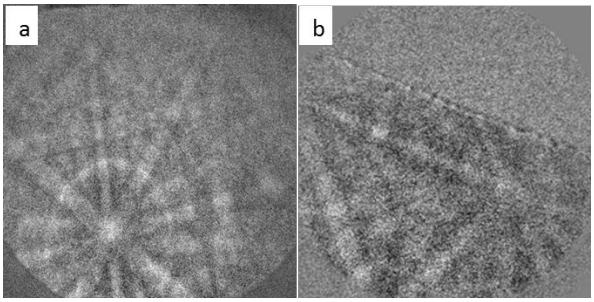


FIGURE 2. Kikuchi patterns from (a) 10 nm HfO_2 film and (b) 5 nm HfO_2 film.

A variety of other materials and thicknesses will be shown as well, in addition to direct comparisons between reflection and transmission mode EBSD.

Transmission EBSD is not limited to ultrathin films and nanoparticles. Thermally evaporated copper films of thickness up to 400 nm have been shown to generate indexable Kikuchi patterns.

Monte Carlo Simulations

Monte Carlo simulations of electron scattering provide first-order insight on how transmitted electrons achieve greater spatial resolution than backscattered electrons, while providing enough scattering to produce diffraction patterns. Simulations from transmitted electrons through a 40nm Ni film show a spatial resolution of an average of 12 nm in transmission, compared to about 70 nm in reflection[1]. This 5-fold increase enables the technique to be extended to nanoparticles and nanostructured films, as well as more accurate orientation mapping of the sample.

References

1. Keller, R. R.; Geiss, R. H., Transmission EBSD from 10 nm domains in a scanning electron microscope. *Journal of Microscopy* **2012,** *245* (3), 245-251.
2. Dingley, D., Progressive steps in the development of electron backscatter diffraction and orientation imaging microscopy. *Journal of Microscopy-Oxford* **2004,** *213*, 214-224.
3. Hausmann, D. M.; Gordon, R. G., Surface morphology and crystallinity control in the atomic layer deposition (ALD) of hafnium and zirconium oxide thin films. *Journal of Crystal Growth* **2003,** *249* (1-2), 251-261.

Keywords

Electron backscatter diffraction, thin films, semiconductors, Kikuchi patterns.

TU–04

SPATIALLY-RESOLVED DOPANT CHARACTERIZATION WITH A SCANNING MICROWAVE MICROSCOPE*

T. Mitch Wallis, Atif Imtiaz, Alexandra E. Curtin, Pavel Kabos, Matthew D. Brubaker, Norman A. Sanford, and Kris A. Bertness

National Institute of Standards and Technology (NIST), 325 Broadway, Boulder, Colorado 80305

INTRODUCTION

The scanning microwave microscope (SMM) is a tool for spatially-resolved microwave characterization of nanoelectronic materials and devices. The microscope incorporates a sharp, near-field probe, which measures local changes in reflected microwave signals from a device under test (DUT). With proper calibration and modeling, a variety of parameters can be extracted from the measurements, including impedance,[1] absolute capacitance,[2,3] and dopant concentration.[4,5] Here, we describe two additional capabilities of the SMM related to dopant profiling. First, we discuss the capability to tune the contrast in $d(S_{11})/dV$ images of variably-doped samples by adjusting the SMM operating frequency. Second, we demonstrate capabilities to locate a p-n junction within a GaN nanowire (NW) and observe changes in the junction morphology as a function of applied SMM bias.

The commercial SMM used in these experiments is illustrated in Fig. 1(a) and described elsewhere.[2] The SMM incorporates a broadband (DC to 18 GHz) signal path with an atomic force microscope (AFM), effectively forming a one-port microwave network in which the DUT acts as a load. With the AFM operating in contact mode, the complex scattering parameter for the reflected microwave signal, S_{11}, is measured by use of a vector network analyzer. Thus, the system simultaneously acquires topographic data along with images of S_{11}. Additionally, by applying a small, low-frequency modulation bias to the SMM probe, a lockin technique can be used to extract the derivative $d(S_{11})/dV$, which is proportional to the absolute capacitance.[2] In addition to the modulation bias, a variable DC bias (V) may be applied to the probe tip, allowing for measurement of the dC/dV versus V curve. In turn, measurements of the voltage dependence of dC/dV enable quantitative determination of dopant concentration.[4]

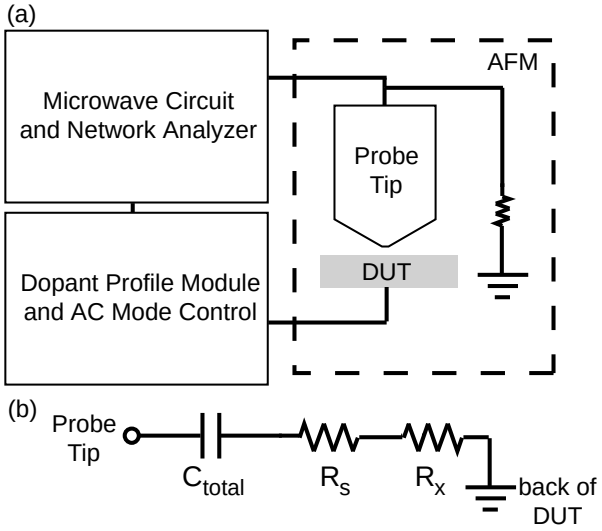


FIGURE 1. (a) Simplified schematic of the commercial SMM (b) Simple circuit used to model probe-DUT interactions. Both figures based on Reference 7.

TU–04

Frequency-Dependent Sensitivity of SMM

SMM measurements can be used to extract calibrated, spatially-resolved dopant profiles.[4] Such measurements require well-characterized reference samples with regions of known dopant densities. Here, we measured samples produced by the IMEC Center for Advanced Metrology Solutions.[6] The samples are p-type doped Si, topography-free and comprise a series of parallel dopant density regions with densities varying in decade increments (10^{16} cm^{-3}, 10^{17} cm^{-3}, 10^{18} cm^{-3}, and so on). Each region is a stripe about 1.5 µm wide and many mm long.

In Fig. 2, $d(S_{11})/dV$ images of the reference sample are shown at three operating frequencies: 2.20 GHz, 13.37 GHz, and 17.86 GHz. Regions of constant dopant density run vertically through the image as indicated by dashed lines in Fig. 2. The DC SMM bias was adjusted from 0.00 V to -3.00 V during image acquisition. Beginning at the topmost horizontal scan lines, the data was acquired with a bias of 0.00 V. Throughout the scan, the bias was adjusted sequentially until the bias was -3.00 V in the bottommost scan lines. In the 2.20 GHz image, maximum contrast is observed in the 10^{16} cm^{-3} and 10^{17} cm^{-3} stripes. In the 13.37 GHz image, the contrast is altered, though both the 10^{16} cm^{-3} and 10^{17} cm^{-3} stripes still show significant contrast. Finally, in the 17.86 GHz image, maximum contrast is confined to the 10^{17} cm^{-3} stripe.

One simple approach to understanding the frequency-dependent contrast is to model the path from probe to ground with a lumped element circuit, shown in Fig. 1(b).[7] The total capacitance, C_{total}, is a series combination of the depletion layer capacitance, C_D, and the oxide capacitance, C_{ox}. C_D is calculated via a standard MOS model, with the probe tip acting as the metal, the Si acting as the semiconductor, and the Si oxide in between. R_s is the local sheet resistance and R_x is the resistance of the Si sample between the local region under the probe and the ground connection. Both C_{total} and R_s depend on local dopant density. Thus, for a given dopant density, a selection frequency $(\tau_{sel})^{-1}$ may be calculated from $\tau_{sel} = \xi(Rs + Rx)\ C_{total}$, where ξ is a dimensionless factor that depends on probe geometry. The existence of a selection frequency for each dopant density enables the SMM to enhance sensitivity and image contrast by an adjustment of operating frequency.

Imaging p-n Junctions

In addition to the SMM's frequency-dependent sensitivity to the magnitude of the dopant density, the SMM is also capable of locating p-n junctions within a device. In order to demonstrate this, we imaged axial p-n junction GaN NWs with the

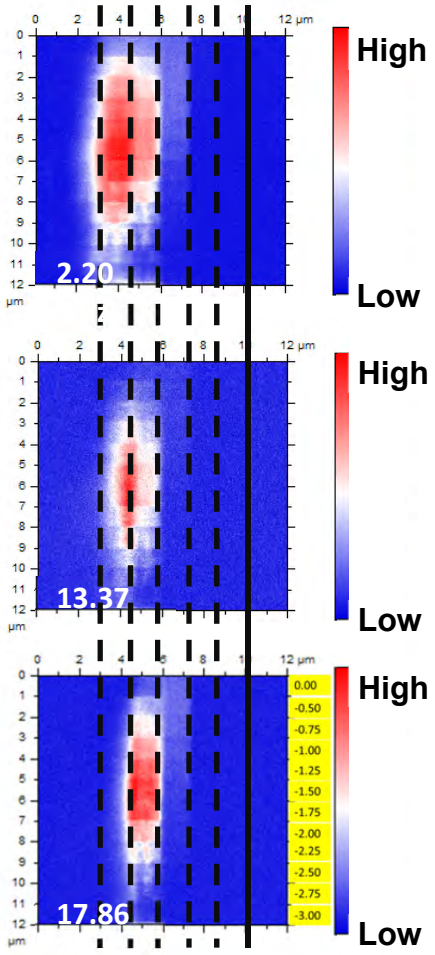


FIGURE 2. d(S11)/dV images of the variably doped Si sample taken at SMM operating frequencies of 2.20 GHz, 13.37 GHz, and 17.86 GHz. Vertical dashed lines indicate boundaries between differently doped regions. Solid line indicates sample edge. DC probe bias sequence indicated at the right side of the 17.86 GHz image.

SMM. The GaN NWs were synthesized by plasma-assisted molecular beam epitaxy and doped *in-situ* during growth to produce axial p-n junctions.[8] The thinner NW root was doped p-type, for approximately 40% of the overall growth duration and the thicker NW tip was doped n-type. Single NWs produce diode-like I-V characteristics, although the individual p-sections exhibited low conductivity.

Fig. 3 shows images of GaN NWs dispersed on SiO_x / Si. The topography image is consistent with other studies of these NWs, displaying maximum apparent diameter on the order of 200 nm and a gradual taper in the diameter over the length of the wire. The apparent length of the structure is about 6 µm. However, the apparent length decreases to about 4 µm in simultaneously acquired *dC/dV* amplitude and phase images (phase image shown in Fig. 3, middle panel). In other words, only the n-type segment of the NW shows a response in the *dC/dV* images. To study bias-dependent morphology of the p-n junction, additional NWs were dispersed on a TiAl metal layer supported by SiO_x / Si. In the bottom panel of Fig. 3, the apparent length of the n-type segment increases by about 200 nm when a bias of -5 V is applied to the SMM probe. While a full theory of these phenomena is still under development, it is clear that SMM is capable of locating p-n junctions in devices and enables bias-dependent study of the morphology of such junctions.

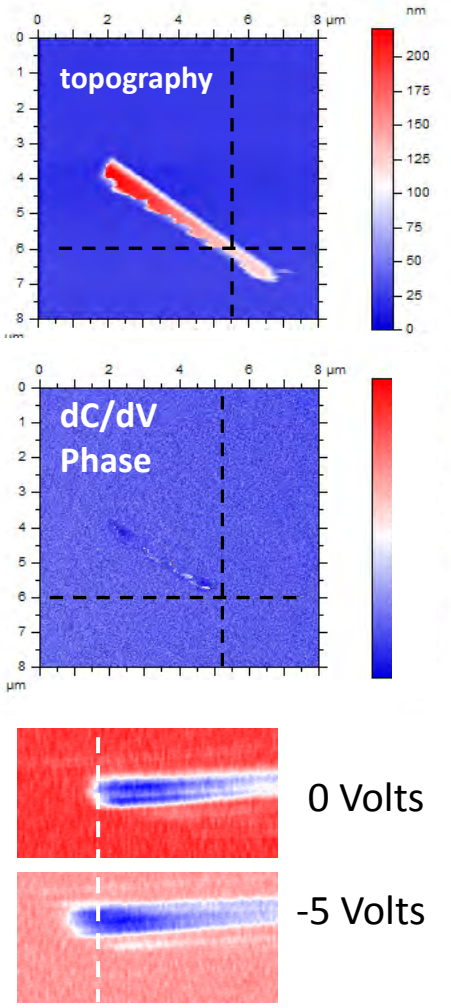


FIGURE 3. (Top) Contact AFM topography of GaN NW (12 µm X 12 µm). (Middle) *dC/dV* phase image, operating frequency 18.5 GHz. (Bottom) *dC/dV* amplitude images of p-n junction at 0 Volts and -5 Volts. Note that the color scale is reversed in the bottom panel.

REFERENCES

* Contribution of an agency of the U.S. government; not subject to copyright.

1. M. Farina, D. Mencarelli, A. Di Donato, G. Venanzoni, and A. Morini, *IEEE Trans. Microwave Theory and Techn.* **59**, 2769-2776 (2011).
2. H. P. Huber, *et. al.*, *Rev. Sci. Instrum.* **81**, 113701 (2010).
3. A. Karbassi, *et. al.*, *Rev. Sci. Instrum.* **79**, 094706 (2008).
4. H. P. Huber, *et. al.*, *J. of Applied Phys.* **111**, 014301 (2012).
5. J. J. Kopanski, J. F. Marchiando, and J. R. Lowney, *Mater. Sci. Eng. B-Solid State Mater. Adv. Tech.* **44**, 46 (1997).
6. Trade names are used to provide clarity and do not imply endorsement by NIST or the U.S. government.
7. A. Imtiaz, *et. al. J. of Applied Phys.* **111**, 093727 (2012).
8. K. A. Bertness, A. Roshko, N. A. Sanford, J. M. Barker, and A. V. Davydov, *J. of Crystal Growth* **287**, 522 (2006).

KEYWORDS

Dopant profiling, Nanoelectronics, p-n junctions, Scanning microwave microscopy

TU–05

Modeling Scanning Electron Microscope Measurements with Charging

John S. Villarrubia

National Institute of Standards and Technology, Semiconductor and Dimensional Metrology Division†
Stop 8212, 100 Bureau Dr., Gaithersburg, MD 20899

Introduction

Some of the more challenging measurement problems in integrated circuit manufacture involve samples with mixed insulators and conductors. For example, it is often desirable to make critical dimension measurements on resist (an insulator) prior to etching or to ascertain whether an unfilled contact hole through an insulating oxide is unobstructed all the way to its bottom or to determine whether the metal in a filled hole has made the desired electrical contact with the under-layer. In the scanning electron microscope (SEM), insulating regions charge. The resulting electric fields affect subsequent incoming and outgoing electrons. The effect may be to the detriment or to the benefit of the attempted measurement. Quantitative measurements can be made provided the effect of charging on the image is sufficiently understood. Even a qualitative understanding of charging phenomena can guide the design of more nearly optimal measurement procedures.

Additional charging-related capabilities have been added to our JMONSEL (Java Monte Carlo simulation for Secondary Electrons) SEM simulator. JMONSEL computes the image given the sample and instrument. Metrology problems are the inverse of this; we must determine the sample shape (and maybe certain instrument parameters) for a measured image. When the forward (simulation) capability is available, we have already demonstrated some success on this inverse problem with a model-based library method.[1,2] Thus, the ability to simulate SEM signals under charging conditions has been the missing piece of this metrology solution. Implementation of such a capability is described in the next section. Its application to charging during the imaging of a contact hole will be treated in the final section.

†. Official contributions by the National Institute of Standards and Technology are not subject to copyright.

The Simulator

JMONSEL is a single-scattering Monte Carlo simulator. It already had a flexible hierarchical constructive solid geometry (CSG) method to describe complex three-dimensional samples.[3] Electron scattering from atomic nuclei is simulated using Mott scattering cross sections interpolated from NIST standard reference database 64.[4] Secondary electron generation in materials for which the relevant input data are available is modeled using a dielectric function theory approach.[5, 6] When such data are unavailable, a simpler parametric model[6] based on the ideas of Salow[7] as recently applied by others[8,9] may be used. The simulator also accounts for refraction caused by the potential energy difference between dissimilar materials and can account for both beam size (finite spatial resolution) and divergence (finite depth of focus).

It was necessary to make some additions to model insulators and charging. In insulators the absence of electronic inelastic modes below the band gap makes phonon scattering important. JMONSEL now uses a phonon scattering implementation similar to that of Llacer and Garwin.[10] The previous CSG sample description can economically describe large sample regions, but its use is not permitted for charging simulations. Instead, the sample is subdivided into a tetrahedral mesh with Gmsh,[11] a publicly available

TU–05

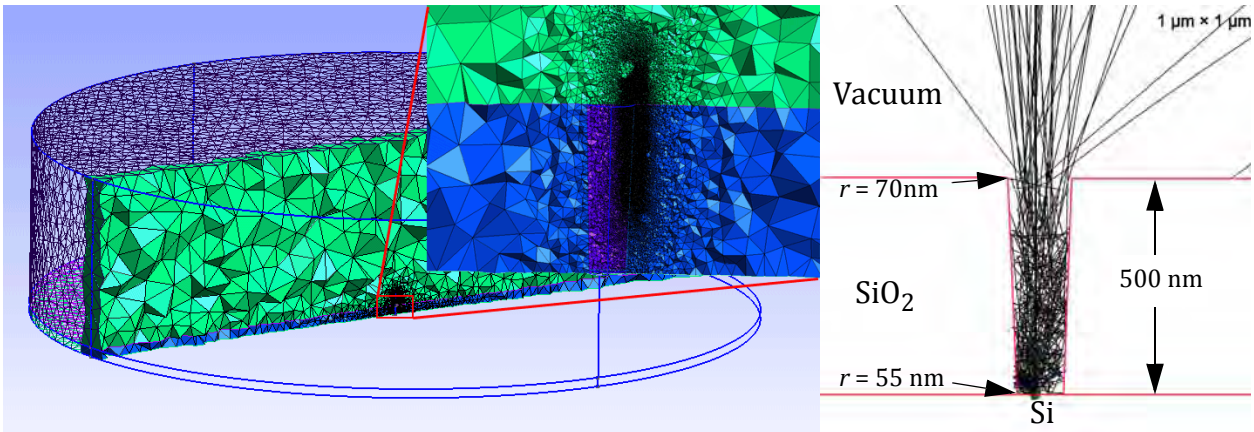


Figure 1. Left: Cutaway of meshed contact hole and surrounding volume. Tetrahedra that intersect a plane through the axis of the hole are rendered as solids. Oxide is blue, the vacuum above the hole is green, and (inset) the vacuum in the hole itself is purple. Right: Geometrical schematic showing dimensions, composition, and simulated electron trajectories in the neighborhood of the contact hole. (Color on-line only.)

software. A typical mesh is shown in Fig. 1. Mesh elements vary in size. For this sample their sizes are approximately 1 nm to achieve the required accuracy in the region of interest but then increase with distance to accommodate large-volume samples with reasonable computer memory.

When the scattering code indicates that an electron stops in an insulating region, the corresponding tetrahedron's net charge is changed by $-e$. When a secondary electron is generated, the charge of the tetrahedron from which it comes changes by $+e$. After every N electrons (N a user-settable parameter) the electric fields that result from these charges is computed by finite element analysis (FEA) using GetDP.[12] The scattering code was modified to account for the effect of the electric field on the direction and energy of electrons.

An Example: Charging during Imaging of a Contact Hole

Evolution of the System to Equilibrium

A simulation was performed on the sample shown in Fig. 1. This sample is a conical contact hole (70 nm radius at the top, 55 nm at the bottom) through 500 nm of SiO_2 on a Si substrate. All potentials are referenced to the wafer potential, which is therefore at 0 V. The sample rests in an externally imposed electric field of 5×10^6 V/m, directed in the $-z$ direction so that electrons generated at the sample are drawn up toward the detector.

In the simulation the electron beam is raster scanned with 3000 linescans 5 nm apart. Within each linescan there are 15000 landing positions 1 nm apart. The resulting 15 μm square raster is centered on the contact hole. Electrons reach the Si wafer with 500 eV landing energy. A "frame" consists of 1 electron at each landing position in this raster.

In the first frame the average potential in the raster area at the oxide surface evolves as shown in Fig. 2. At this landing energy the total yield is initially greater than 1. That is each beam electron causes on average more than one sample electron to be ejected,

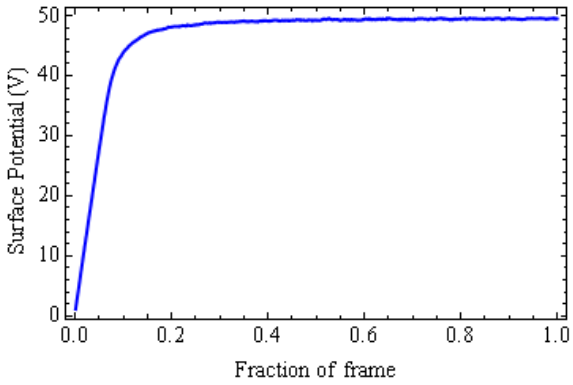


Figure 2. The surface potential near the contact hole increases rapidly at first and saturates well before the first scan frame completes.

TU–05

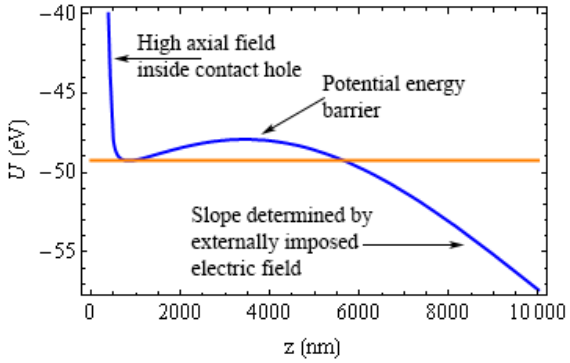


Figure 3. Electron potential energy ($U = -e\varphi$) along the axis of the contact hole, from the grounded wafer at $z = 0$.

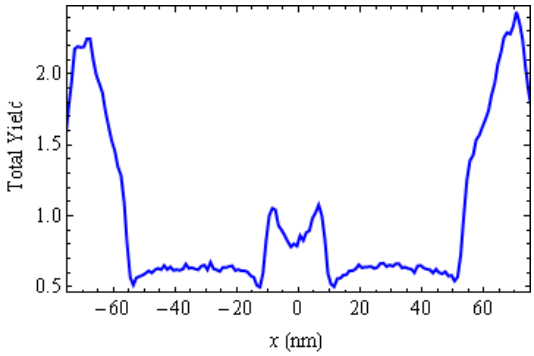


Figure 4. Simulated linescan across the contact hole with a cylindrical (10 nm radius, 10 nm height) Si marker particle at the bottom.

so the surface develops a positive charge. Charging is initially rapid, but the rate slows and saturates under these conditions at a fraction of the first frame. The reason for this is seen in Fig. 3, which shows the potential energy ($-e\varphi$ with φ the electrostatic potential) for $0\ \text{nm} < z < 10000\ \text{nm}$ along the axis of the contact hole. The wafer is at $z = 0$ nm. The positive charge results in a local minimum near the oxide surface at $z = 500$ nm. This positive charge is attractive to escaping electrons, resulting in a potential energy barrier. Electrons without enough energy to overcome the barrier return to the surface. Thus, increasing charge increases the barrier and reduces the yield until its average value is one, at which point steady-state is reached. This is how insulating samples can develop a stable imaging condition. Because many of the ejected electrons have only a few electron volts, a small barrier is enough to produce this condition.

Visibility of Contact Hole Bottoms

After charge saturation, simulated scans across the hole can be performed to determine the yield. A simulated linescan is shown in Fig. 4 (trajectories in Fig. 1 right). A false Si "marker" particle[13] at the hole center tests whether the signal truly carries information about the bottom. The clear presence of contrast in the simulated linescan indicates that the bottoms of holes this size should be visible in the SEM. An earlier linescan when the surface potential was a factor of 10 smaller exhibited a factor of roughly 5 lower signal.

Charging enhances the signal in this case because electrons at the bottom are attracted toward the top of the hole. At large z in Fig. 3 the slope corresponds to the externally imposed field. Inside the contact hole at $z < 500$ nm the slope has the same sign, tending toward escape, but at 100 MV/m a factor of 20 larger magnitude. Signal from the bottom of a given hole is maximized by maximizing the surface potential. This can be done, up to a limit set by leakage current in the dielectric, by increasing the size of the charged area.

References

1. J. S. Villarrubia, A. E. Vladár, and M. T. Postek, *Surf. Interface Anal.* **37**, 951-958 (2005).
2. J. S. Villarrubia, A. E. Vladár, J. R. Lowney, and M. T. Postek, *Proc. SPIE* **4689**, pp. 304-312 (2002).
3. J. S. Villarrubia, N. W. M. Ritchie, and J. R. Lowney, *Proc. SPIE* **6518**, 65180K (2007).
4. A. Jablonski, F. Salvat, and C. J. Powell, NIST Electron Elastic-Scattering Cross-Section Database - Version 3.1, National Institute of Standards and Technology, Gaithersburg, MD (2002), http://www.nist.gov/srd/nist64.cfm
5. Z.-J. Ding and R. Shimizu, *SCANNING* **18**, 92-113 (1996).
6. J. S. Villarrubia and Z. J. Ding, *J. Micro/Nanolith. MEMS MOEMS* **8**, 033003 (2009).
7. H. Salow, Phys. Z. **41**, 434-442 (1940).
8. H. Seiler, J. Appl. Phys. **54**, RI (1983).
9. D. C. Joy, J. Microsc. **147**, 51-64 (1987).
10. J. Llacer and E.L. Garwin, J. Appl. Phys. **40**, 2766-2775 (1969).
11. C. Geuzaine and J.-F. Remacle, Int. J. Numer. Meth. Eng. **79**, 1309-1331 (2009).
12. P. Dular, C. Geuzaine, F. Henrotte, W. Legros, IEEE Trans. Magn. **34**, 3395-3398 (1998).
13. A.J. Cepler, B. Bunday, B.L. Thiel, and J.S. Villarrubia, Proc. SPIE **8324**, 83241N (2012).

Keywords

Charging, contact hole, scanning electron microscopy (SEM), dimensional metrology, mathematical modeling, Monte Carlo simulation

TU–06

AUTOMATED STEM AND TEM METROLOGY OF ADVANCED SEMICONDUCTOR DEVICES

Mark J. Williamson, Michael Strauss, and David Horspool

FEI Company, 5350 NE Dawson Creek Drive, Hillsboro, Oregon, USA

INTRODUCTION

The increasing complexity of advanced semiconductor gate structures, including 3D transistors (e.g. FinFET or Tri-gate), shrinking line widths, thin films, and etch profiles, will require metrology techniques beyond those currently offered by conventional CD-SEM or scatterometry. These established metrology solutions offer excellent repeatability and throughput, but they each have limitations for investigating advanced three-dimensional integration schemes, such as those defined in the 2011 metrology roadmap presented at the ITRS Winter 2011 meeting [1]. For example, scatterometry does not offer the capability for line edge roughness analysis, and it is not possible to undertake sub-surface analysis using CD-SEM.

Scanning and transmission electron microscope based dimensional metrology (CD-STEM and CD-TEM) are possible candidates to overcome these limitations and extend metrology capabilities into the most advanced technology nodes. Recently, we have shown STEM and TEM based dimensional metrology provides good repeatability and robustness [2.3]. This paper summarizes the progress to date on such S/TEM based metrology and offers an outlook on possibilities for fully automating the whole process from sample navigation and alignment, through image acquisition, to the metrology itself.

CD-STEM METROLOGY

Automated metrology using the scanning transmission electron microscope has been widely adopted within the hard disk drive industry [4], [5], and has created a paradigm shift in the way STEM is viewed and used. This CD-STEM methodology has been employed for over six years in high volume production of thin film magnetic heads. It consistently provides 5-10 times greater throughput than conventional methods, and automated STEM metrology in this application has been demonstrated to provide CD measurement precision an order of magnitude better than comparable CD-SEM measurements [5].

For the semiconductor industry, there is currently a high-reliance on manual metrology measurements from data collected on conventional scanning and transmission electron microscopes (S/TEMs). This manual technique is generally throughput limited, has poor repeatability, and is prone to error.

The application of the CD-STEM process to semiconductor devices is relatively new, but a recent study has shown that fully automated STEM metrology on advanced gate structures is viable, with good throughput, repeatability and robustness [2]. Figure 1 shows examples of CD-STEM metrology on FinFET transistors.

TU–06

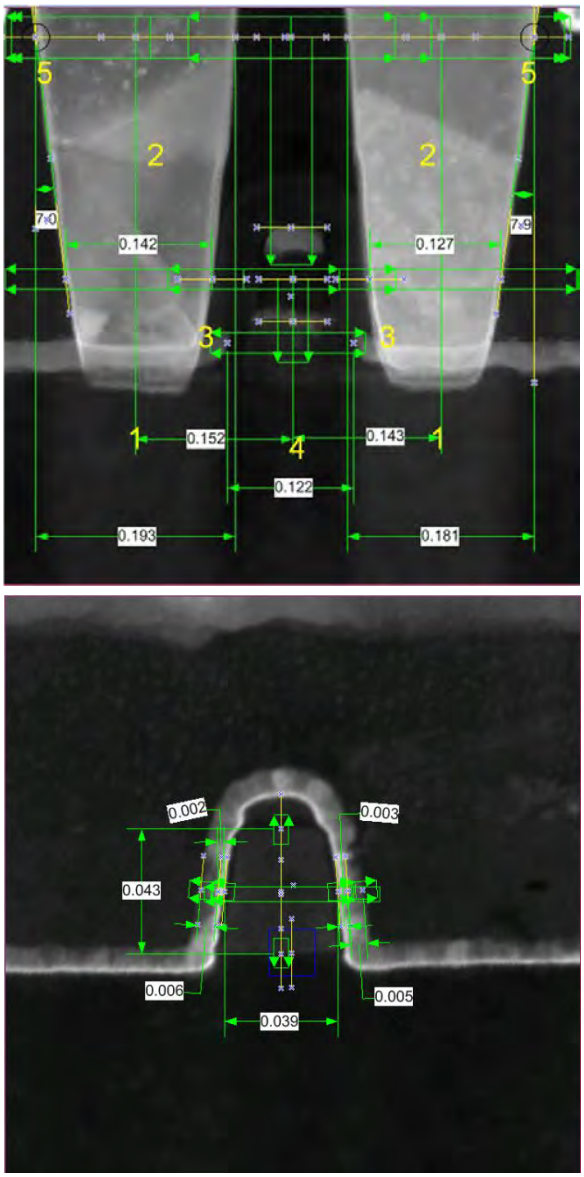


FIGURE 1. CD-STEM metrology data for FinFET 3D transistor device for (a) gate cross-section and (b) fin cross-section (units are microns). (Samples courtesy of SEMATECH).

CD-TEM Metrology

In parallel to the extension of CD-STEM into the semiconductor space, it's important that automated metrology in transmission electron microscopy (TEM) imaging mode is also developed in order to provide a complete, well-rounded metrology solution. The results of a preliminary investigation into automated metrology routines, performed on manually acquired TEM images of typical semiconductor samples has been presented [3]. A particular focus of this study was the understanding of the measurement repeatability of critical dimensions in a device, when obtained from automated metrology in the manner described above, Figs. 2, 3, Table 1.

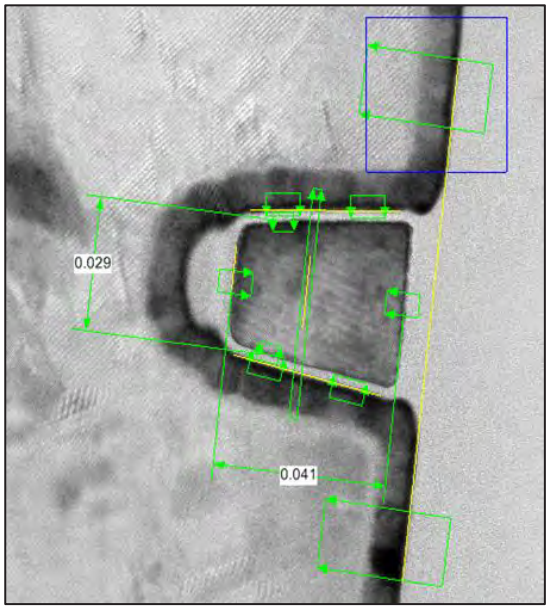


FIGURE 2. Bright field TEM image showing CD-TEM measurements on a FinFET (units are microns). (Sample courtesy of SEMATECH).

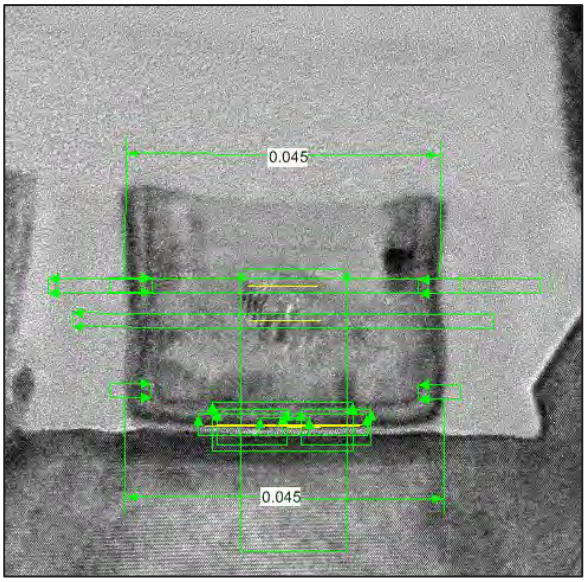


FIGURE 3. Bright field TEM image showing CD-TEM measurements on a metal gate of a commercial 32nm SRAM PMOS device (units are microns).

TU–06

TABLE 1. Summary of CD-TEM metrology data from 32nm SRAM.

Parameter	5nm above gate bottom	20nm above gate bottom
Average Gate Width (6 gates)	44.9 nm	44.4 nm
3σ static precision	1.4Å	1.1Å
3σ dynamic precision	3.7Å	4.2Å
Relative 3σ static precision	0.31%	0.25%
Relative 3σ dynamic precision	0.82%	0.95%

FEI is focusing on further automating the large portion of the data acquisition in addition to the metrology. To this end, the object oriented programming language historically used to control focused ion beam sample preparation systems has been extended to be used with S/TEM tools.

This programming language is being used to automate both certain microscope functions and repeatability testing of these automated functions. For example, the procedure of setting the sample to eucentric height has been automated and tested in an automated manner. The sample was set to randomized heights up to 100 microns above and below the correct eucentric height and the automated function was run; the resulting spread in eucentric heights, as determined by the automation, had a 3σ value of 1.6 microns.

CONCLUSIONS

TEM and STEM automation is being extended from the image acquisition and metrology described herein to the alignment of the sample, and will ultimately be extended to the alignment of the microscope. The introduction of automated routines for orienting the sample, setting the sample eucentric height, and focusing are expected to increase the ease of use of the microscope and make metrology more accessible.

Significant testing efforts are underway to characterize and validate the autofunctions for automated STEM and TEM application within the microscope. This poster will present this data along with the metrology sensitivity to autofunction repeatability.

ACKNOWLEDGEMENTS

The authors would like to thank SEMATECH for the provision of samples for this study. Part of this work has been funded by ENIAC JU project LENS. Significant contributions from FEI engineering and application personnel involved in the development of automated TEM operation, image collection and metrology are also gratefully acknowledged.

REFERENCES

1. C. Hacker, “ITRS Metrology Roadmap 2011”, ITRS Metrology Technical Working Group, 2011.
2. M. Strauss, J. Arjavac, D. N. Horspool, K. Nakahara, C. Deeb, C. Hobbs, “Automated S/TEM metrology on advanced semiconductor gate structures”, Proc. SPIE. 8324, Metrology, Inspection, and Process Control for Microlithography XXVI 83240Z (March 29, 2012) doi: 10.1117/12.916526
3. M. Strauss, A. Genc, G. Dutrow, D.N. Horspool, L.A. Dworkin, "Automated TEM metrology characterization of Si devices," Advanced Semiconductor Manufacturing Conference (ASMC), 2012 23rd Annual SEMI , vol., no., pp.88-90, 15-17 May 2012. doi: 10.1109/ASMC.2012.6212874
4. H. Wang, J. Fang, J. Arjavac, and R. Kellner, “Scanning transmission electron microscopy for critical dimension monitoring in wafer manufacturing”, Microscopy Today, vol 16(1), pp 24-27, 2008.
5. H. Wang, J. Fang, and M. Lederman, “Critical dimension monitoring with STEM in thin film magnetic head wafer production”, Microsc. Microanal, vol 14 (Suppl 2), pp 1026-1027, 2008.

KEYWORDS

CD-STEM, CD-TEM, STEM, TEM, metrology, automation

TU–07

CONTAMINATION-FREE SCANNING ELECTRON AND HELIUM ION MICROSCOPY

Purushotham K. P., András E. Vladár and Michael T. Postek.

National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899-8212, USA.

Instrument and specimen induced contamination has been a problem since the inception of the scanning electron microscope (SEM). Contamination frequently exhibits itself as a deposit of carbonaceous material on the surface of the specimen following examination. There are two basic sources of contamination, the instrument itself and surface adhering material transported by the sample into the instrument. Contamination is a serious problem when the fine surface structures of a specimen are observed or measured with the SEM. In the semiconductor community, this has been referred to as carry-over and can result in erroneous measurement data. Therefore, instrument manufacturers and critical users have attempted to eliminate this problem. Over time, improvements have been made; however, contamination has remained a nightmare for microscopists and microanalysts. Since the scanning helium ion microscope (HIM) is much more surface sensitive than the SEM, this presents an even bigger challenge (Figures 1-3).

It is well known that a specimen under observation can degrade with time. This can be a fast or slow process depending upon the level of hydrocarbons available. Typically, the image progressively darkens under observation as polymerized hydrocarbon layers, produced by the interaction of the electron beam and hydrocarbon molecules, build up (1-6). The deposited layer darkens because it changes the electron emission and intensity, and thereby decreases the contrast of the structural details to be observed or measured (7). More importantly for metrology, the layer changes the size of sample structures and greatly disturbs the dimensional measurement process and leads to misleading results.

If an unknown specimen is observed in a typical SEM and contamination is deposited, it is not clear if the contamination resulted from the specimen chamber, the specimen surface or from both. The sources must be separated. Instrument and sample cleaning procedures have been developed at NIST to separate these components. Using these procedures, the instrument can be cleaned sufficiently that no deposition of carbon contamination will result upon a “clean” sample. To achieve a “clean” sample, both wet and plasma cleaning sample cleaning procedures have been researched by NIST. Using a clean instrument and a clean sample no contamination will be deposited. To demonstrate this, a highly cleaned silicon chip with microfabricated amorphous Si features was used. The contamination test procedure consisted of acquiring images of a selected area before and after exposure to the beam. Exposure was carried out continuously for 10 minutes, at twice the magnification of the micrographs. The accelerating voltage was 1 kV and the beam current was 43 pA for the SEM, and 30 kV and 2 pA for the scanning helium ion microscope (HIM). Under these operating test conditions, specimen contamination would be expected in a “typical” instrument (Figures 1 and 2). Since this test sample has been

TU–07

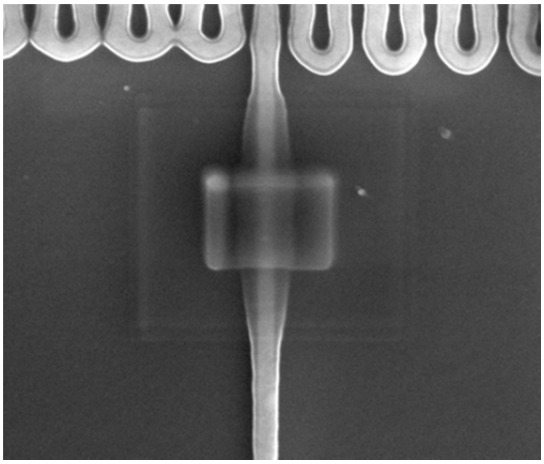


FIGURE 1. Contamination patterns due to sample, in SEM (Horizontal field width, HFW= 3 μm).

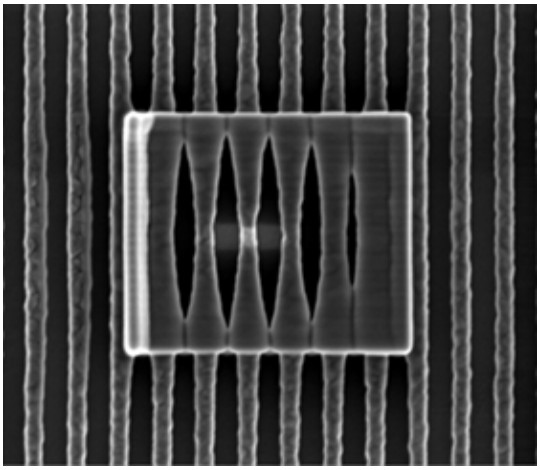


FIGURE 3. No perceptible contamination when a imaging a clean sample in a clean SEM. HFW= 2.5 μm

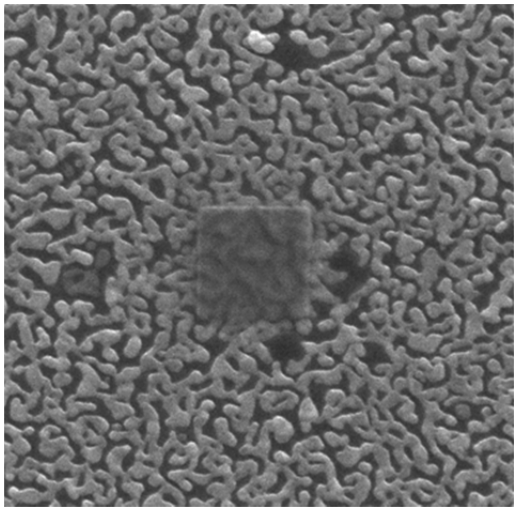


FIGURE 2. Contamination patterns due to sample, in HIM HFW= 1.9 μm

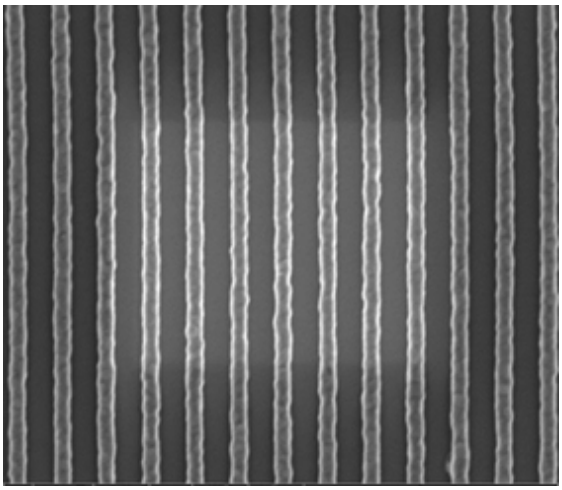


FIGURE 4. Contamination patterns due to instrument contamination (SEM). HFW= 2.5 μm

highly cleaned, no deposited hydrocarbon should be found, as confirmed in Figure 4. However, instrument cleanliness is a finite thing and if contamination is found, as shown in Figure 3, it can be concluded that the specimen chamber of the instrument has become contaminated and hence needs additional cleaning by using the NIST methods. A typical low-vacuum plasma cleaning process would involve the reaction between the plasma ion with the contaminants (hydrocarbons), and the evacuation of the reaction products from the system. Cleaning is typically carried out using oxygen or hydrogen or helium ion plasma at a vacuum of 40 Pa (3×10^{-1} Torr) and between 5 W and 50 W.

In conclusion, contamination can be effectively separated into instrument induced and specimen induced components. Once knowing this, each can be individually addressed with the appropriate cleaning methods. Sample contamination has become an artefact that should no longer exist.

TU–07

REFERENCES

1. Harada, Y., Tomita, T., Watabe, T., Watanabe, H. & Etoh, T.. Reduction of Contamination in Analytical Electron Microscopy, Scan. Elect. Microsc., 103 (1979)/II

2. Hren, J. J. Specimen Contamination in Analytical Electron Microscopy: Sources and Solutions, Ultramicroscopy, 3, 375 (1979).

3. Bruenger, W. H., Kleinschmidt, H., Hassler-Grohne, W. & Bosse, H. Contamination Reduction in Low Voltage Electron-Beam Microscopy for Dimensional Metrology, J. Sci. Technol. B 15(6), 2181 (Nov/Dec 1997).

4. Akishige Ono. Influence of Incident Electron Energy on Specimen Contamination in SEM Mode, Proc. XIth Int. Cong. On Electron Microscopy, Kyoto, 417 (1986).

5. Ura, K. Electron beam Interaction with Specimen, 175, Electron beam testing Technology, Ed. Thong J T, NY. (1993).

6. Hirsch, P., Kassens, M., Puttmann, M. & Reimer, L. Contamination in a Scanning Electron Microscope and the Influence of Specimen Cooling, Scanning Vol. 16, 101 (1994).

7. Black, J. T. The Scanning Electron Microscope: Operating Principles, Principles and Techniques of Scanning Electron Microscopy, Vol. 1, 1 (1974).

KEYWORDS

SEM, HIM, Plasma cleaner, Wafer, oxygen,

hydrogen, specimen contamination

TU–08

MEASUREMENT OF SILICA PARTICLES BY TRANSMISSION ELECTRON MICROSCOPE

F. Kole, Y. Guan, P. Konicek

VLSI Standards, Inc., Five Technology Drive,
Milpitas, California 95035 USA

INTRODUCTION

Particles of known sizes have been essential for calibrating the sensitivity of semiconductor wafer inspection systems. As more advanced inspection systems harness ultraviolet (UV) and deep ultraviolet (DUV) illumination to resolve smaller structures, there is a growing industry need for a new generation of particle standards that resist damage at these shorter wavelengths. This paper summarizes the techniques and results for the traceable measurement of a large array of silica particle sizes, using established methods in transmission electron microscopy (TEM), along with semi-automated digital image processing. We report the mean maximum diameters and expanded uncertainties for each of 14 particle sizes, ranging from nominal diameters of 32 nm to 1500 nm.

MEASUREMENT METHOD

As prior literature documents [1,2,3], size measurements using TEM images have to overcome the problem of variable magnification between images, even between successive images. This study applies the same technique reported in those papers – the "internal standard method" of measuring particles imaged by TEM. This method calibrates each image's magnification using standard reference particles present within the same field of view as the particles under measurement.

The sample preparation process individually dilutes 14 sizes of silica particles with deionized water and mixes each with a NIST Standard Reference Material – SRM 1963 [4] for nominal silica sizes up to 300 nm and SRM 1690 [5] for the remainder. Droplets of pre-mixed silica and SRM particles are applied to TEM grid discs, made of silicon nitride with embedded positive charge, rinsed with a drop of deionized water, and then dried, before imaging on an FEI Tecnai TF-20 FEG/TEM.

Fiji ("Fiji Is Just ImageJ") [6], an open source image analysis platform, provides image processing, indices for all particles, and measures maximum (Feret) diameter for each particle.

ANALYSIS

The internal standard method calculates a magnification correction for each image M_i by dividing the mean reference particle diameter in each image by the SRM's mean diameter [4,5].

$$M_i = \frac{\bar{d}_{r,i}}{D_r}$$

Within an image, i, the correction adjusts the measured diameter for each silica particle, j ,to produce a calibrated diameter.

$$D_m(i,j) = \frac{d_m(i,j)}{M_i}$$

The average value for each silica size calibrated diameter can then be expressed as:

TU–08

$$\bar{D}_m = \frac{1}{N_m}\sum_i \sum_j \frac{d_m(i,j)}{M_i} = \sum_i f_{m,i}\frac{\bar{d}_{m,i}}{\bar{d}_{r,i}} D_r$$

where N_m is the total number of silica particles measured, $f_{m,i}$ is the fraction of measured particles in the ith image, and $\bar{d}_{m,i}$ is the average measured diameter for silica particles in the ith image.

THRESHOLD EFFECTS

We estimate the relative standard uncertainty for edge-finding, ε, for each TEM magnification by selecting a range of likely thresholds in an image and calculating the standard deviation over mean of each particle's diameters. The relative standard uncertainty for one particle, j, is

$$\varepsilon_j = \frac{\sigma_j(T)}{\bar{d}_j(T)}$$

Averaging across all particles in an image's threshold series and dividing by the root of the particle count used in a threshold analysis give the standard uncertainty at one TEM magnification.

$$\frac{\bar{\varepsilon}_T \bar{d}}{\sqrt{\eta}}$$

ELECTRON BEAM EFFECTS

Prior work documents that electron beam effects on PSL-to-PSL measurements are not significant [1,2,3]. This study measures electron beam effect differences between NIST SRM 1963 PSLs and nominal 100 nm silica particles, using 5 different fields-of-view, acquired at time intervals of near-0, 10, 20, 30, and 60 seconds. The relative differences from each individual particle's starting diameter over time provide the basis for a quadratic fit for each of the two particle types. At the exposure interval of 20 seconds, typical of the primary sizing analysis, a t-test of the difference in the mean relative size changes between 64 PSL particles and 157 silica particles is 0.136%. This is similar in magnitude to the standard error on the difference, ∝= 0.133%. This analysis concludes that there is no significant difference in size change between the two particle types at 20 seconds and applies ∝= 0.133% to the uncertainty calculation.

UNCERTAINTIES

Starting from the calibrated diameter, the law of uncertainty propagation gives the following expression for the type A uncertainty for measured silica particles, $\bar{D}_m$.

$$u_A(\bar{D}_m)^2 = \sum_i \left[\left(f_{m,i}\frac{\bar{d}_{m,i}}{\bar{d}_{r,i}} D_r \right)^2 \left(\frac{u_A(\bar{d}_{m,i})^2}{\bar{d}_{m,i}^{\,2}} + \frac{u_A(\bar{d}_{r,i})^2}{\bar{d}_{r,i}^{\,2}} \right) \right]$$

The type A uncertainties are then

$$u_A(\bar{d}_m)^2 = \sum_i \left(f_{m,i}\frac{D_r}{\bar{d}_{r,i}}\frac{\sigma(d_{m,i})}{\sqrt{n_{m,i}}} \right)^2$$

$$u_A(\bar{d}_r)^2 = \sum_i \left(f_{m,i}\frac{\bar{d}_{m,i} D_r}{\bar{d}_{r,i}^{\,2}}\frac{\sigma(d_{r,i})}{\sqrt{n_{r,i}}} \right)^2$$

Each particle type also has several type B contributions. The first type B terms calculate pixilation effects on diameter measurements, using half of the image pixel size with a rectangular distribution [7]. The second type B terms quantify the uncertainty in finding edges for either particles.

$$u_{edge}(\bar{d})^2 = \sum_i f_{m,i}\left(\frac{\bar{\varepsilon}_T \bar{d}_i}{\sqrt{\eta}} \right)^2 = \frac{(\bar{\varepsilon}_T \bar{D})^2}{\eta}$$

The third type B terms represent the uncertainty in shrink rate differences in an electron beam.

$$u_{shrink}(\bar{d})^2 = \sum_i f_{m,i}(\propto \bar{d}_i)^2 = (\propto \bar{D})^2$$

The final type B term is the SRM uncertainty

$$u_B(D_r)^2 = \sum_i f_{m,i}\left(\frac{\bar{d}_{m,i}}{\bar{d}_{r,i}} u_{SRM} \right)^2 = \left(\frac{\bar{D}_m}{D_r} u_{SRM} \right)^2$$

Tables 1 and 2 summarize the sizing results and expanded uncertainties (k=2) for each of the 14 nominal particle sizes.

TABLE 1. Uncertainty contributions and sizing results by the nominal silica sizes 32 nm to 90 nm.

Parameter	Type	Term	32	40	50	60	70	80	90
Pixel size [nm]			0.39	0.39	0.39	0.58	0.58	0.58	0.58
Particle count, silica		N_m	2699	2676	1702	1042	798	962	512
Particle count, SRM		N_r	46	91	92	95	95	84	79
Finite sample, silica	A	$u_A(\bar{d}_m)$	0.11	0.14	0.19	0.31	0.42	0.48	0.53
Pixilation, silica	B	$u_{pixel}(\bar{d}_m)$	0.11	0.11	0.11	0.17	0.17	0.17	0.17
Edge finding, silica	B	$u_{edge}(\bar{d}_m)$	0.01	0.01	0.02	0.03	0.03	0.03	0.04
Shrink rate, silica	B	$u_{shrink}(\bar{d}_m)$	0.04	0.05	0.06	0.08	0.08	0.09	0.11
Finite sample, SRM	A	$u_A(\bar{d}_r)$	0.44	0.13	0.12	0.15	0.22	0.19	0.25
Pixilation, SRM	B	$u_{pixel}(\bar{d}_r)$	0.11	0.11	0.11	0.17	0.17	0.17	0.17
Edge finding, SRM	B	$u_{edge}(\bar{d}_r)$	0.13	0.12	0.12	0.14	0.14	0.14	0.14
Shrink rate, SRM	B	$u_{shrink}(\bar{d}_r)$	0.13	0.12	0.12	0.12	0.12	0.13	0.12
SRM uncertainty	B	$u(D_r)$	0.30	0.40	0.52	0.65	0.68	0.73	0.90
	Mean maximum diameter (nm)		30.4	40.0	51.9	65.1	68.3	73.8	90.2
	Expanded uncertainty, k=2 (nm)		1.2	1.0	1.2	1.6	1.8	1.9	2.2

TABLE 2. Uncertainty contributions and sizing results by the nominal silica sizes 100 nm to 1500 nm.

Parameter	Type	Term	100	150	200	300	600	800	1500
Pixel size [nm]			0.58	1.14	0.77	1.14	4.50	4.50	4.50
Particle count, silica		N_m	450	1374	170	126	487	195	141
Particle count, SRM		N_r	103	248	420	733	101	119	331
Finite sample, silica	A	$u_A(\bar{d}_m)$	0.98	0.44	1.68	2.36	1.93	3.16	4.29
Pixilation, silica	B	$u_{pixel}(\bar{d}_m)$	0.17	0.33	0.22	0.33	1.30	1.30	1.30
Edge finding, silica	B	$u_{edge}(\bar{d}_m)$	0.05	0.03	0.05	0.06	0.72	0.96	1.86
Shrink rate, silica	B	$u_{shrink}(\bar{d}_m)$	0.12	0.17	0.25	0.36	0.79	1.05	2.04
Finite sample, SRM	A	$u_A(\bar{d}_r)$	0.22	0.20	0.23	0.24	0.75	3.71	2.74
Pixilation, SRM	B	$u_{pixel}(\bar{d}_r)$	0.17	0.33	0.22	0.33	1.30	1.30	1.30
Edge finding, SRM	B	$u_{edge}(\bar{d}_r)$	0.14	0.10	0.08	0.10	1.51	1.51	1.49
Shrink rate, SRM	B	$u_{shrink}(\bar{d}_r)$	0.12	0.12	0.12	0.12	1.18	1.18	1.17
SRM uncertainty	B	$u(D_r)$	0.99	1.38	2.02	2.88	5.33	7.11	13.9
	Mean maximum diameter (nm)		99.4	139	204	290	596	796	1557
	Expanded uncertainty, k=2 (nm)		2.9	3.1	2.7	7.6	13	18	31

ACKNOWLEDGEMENTS

We thank Dr. George Mulholland of the University of Maryland and of the National Institute of Standards for guidance in quantifying the uncertainties and for review of this work.

REFERENCES

1. K. Y. Jung, B. C. Park, W. Y. Song, B.-H. O, and T. B. Eom, *Powder Technology* **126**, 255-265 (2002).
2. T. R. Lettieri, and G. G. Hembree, *Journal of Colloid and Interface Science* **127**, No. 2 (1989).
3. S. D. Duke, and E. B. Layendecker, *Duke Scientific Corporation,* TN-010.03 (2009).
4. G. W. Mulholland, B. P. Nelson, and C. Croarkin, *Aerosol Science and Technology* **31**, 39-55 (1999).
5. G. W. Mulholland, A. W. Hartman, G. G. Hembree, E. Marx, and T. R. Lettieri, *Journal of Research of the National Bureau of Standards* **90-1**, 3-26 (1985).
6. J. Schindelin, et al, *Nature Methods* **9**, 676-682 (2012).
7. B. N. Taylor and C. E. Kuyatt, *NIST Technical Note* **1297**, 3 (1994).

KEYWORDS

silica, particles, TEM, transmission electron microscopy, Internal Standard Method, Fiji

TU–09

APPLICATIONS OF ELECTRON TOMOGRAPHY TO ADVANCED CMOS PROCESS TECHNOLOGY

Hugh L. Porter*, Jeremy D. Russell**

*SEMATECH and GLOBALFOUNDRIES, 257 Fuller Road, Suite 2200, Albany, NY 12203
**GLOBALFOUNDRIES, 400 Stone Break Extension, Malta, NY 12020

INTRODUCTION

For years, electron tomography has been in common use for applications in the biological sciences [1,2]. Recently, it has been getting attention for semiconductor applications as well [2,3].

As semiconductor device dimensions continue to shrink, the transistors themselves are becoming smaller than the thickness of a transmission electron microscopy (TEM) lamella. If lamellae cannot be made smaller, electron tomography may soon be needed to resolve features that change within the thickness of the lamellae [2-5].

Semiconductor samples, however, have unique requirements that biological samples do not. For example, diffraction contrast must be minimized, which is not a problem for amorphous biological samples [2,6-9]. Also, semiconductor samples have many manmade (i.e. repeated, linear, non-randomly oriented) features that confuse the image recognition software [2].

Another barrier to widespread acceptance among the semiconductor industry is the nature of the investigations themselves. Most tomography research, not just biological, involves peering into complete unknowns. For example, biologists may wish to learn about the structure of a certain type of cell that has never been seen before. In this case, and any information they can get is more than what they already had. Semiconductor engineers, however, already know the structure of transistors. Tomography would add value only when comparing *specific* transistors. Thus, in semiconductor research, the need for data precision and integrity is vital for the widespread acceptance of tomography.

28 NM PROCESS TECHNOLOGY

The samples analyzed for this study were taken from the GLOBALFOUNDRIES 28 nm process technology, and were fabricated at GLOBALFOUNDRIES Fab 8 in Malta, NY.

A detailed description of the technology itself can be found online at: http://www.globalfoundries.com/technology/28nm.aspx.

EXPERIMENTAL

Details of the experimental procedure have been described elsewhere [10]. All samples for this study were cut into slabs with a dual-beam focused ion beam (FIB), and lifted out onto a TEM grid. Electron tomography experiments were performed on an FEI 80/300 Titan at SEMATECH in Albany, NY.

3D reconstruction and visualization were carried out by FEI Inspect 3D software and Amira software, respectively. All 3D rendering used

TU–09

procedures that preserved the raw data as much as possible.

Results and Discussion

PMOS e-SiGe

Modern process technology uses strained SiGe PMOS transistors. The e-SiGe approach involves etching Si out of the source and drain and growing SiGe in the remaining hole. Process engineers commonly want to see the shape of the epitaxially grown SiGe in every direction, so that the strain achieved can be predicted and controlled.

In this study, we created a three-dimensional image of strained SiGe. Figure 1 shows a scanning (S)TEM image of the devices. The wafer was removed from the production line before silicide formation, so that the SiGe would not need to compete for brightness with the much brighter NiSi. Because a finite amount of gray scale is available in each image, we wanted to be able to resolve the difference in the germanium concentrations between the two layers of SiGe that make up the source/drain island.

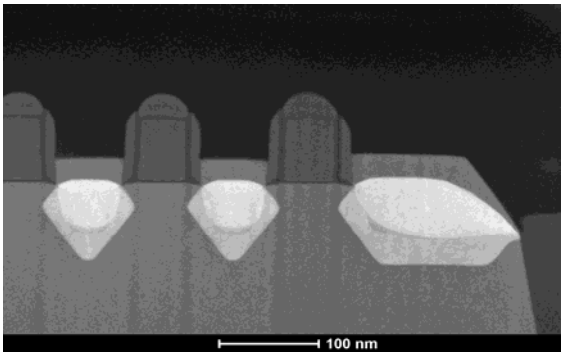


FIGURE 1. Partially processed PMOS devices showing two concentrations of SiGe in the source/drains.

Figure 2 shows the result of a tilt series and digital reconstruction. The "heat" color scheme is used with orange defined as brightest, and green as least bright. The first layer of SiGe is shown in yellow; the second layer is in orange. The shape of the SiGe crystals can be observed in any direction. Note also that most of the noise appears in the green area, and none of the noise in the original data has been removed. Noise has been left in the image to provide a way of estimating the amount of statistical confidence that can be placed on the data.

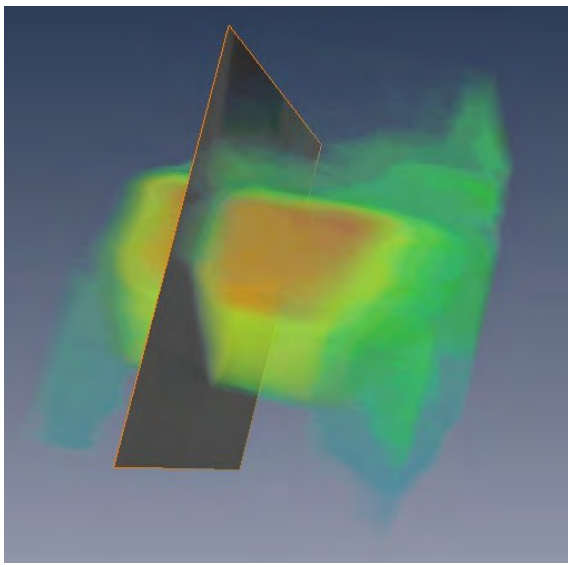


FIGURE 2. Three-dimensional reconstruction of a single PMOS source/drain. The gray scale image is included to show the direction of the original viewing plane.

NMOS NiSi

Spotty silicide is an important yield limiter for technologies that use nickel silicide. The NiSi grain structure does not always completely cover the source/drain/gate areas as needed. In transmission mode, it is not always obvious whether a device is sufficiently covered in silicide, because the grains project over each other. Thus, tomography has the potential to demonstrate the uniformity of NiSi coverage across a device.

We have performed a tomographic reconstruction on this type of sample. The data for this sample will be shown in the poster/presentation.

W Contact to NiSi

Another potential application of electron tomography to advanced CMOS technologies is analyzing the integrity of tungsten contacts on silicide. Since the contact etch can over-etch into the silicide, investigating whether the etch has removed too much silicide is useful. In standard

TU–09

transmission mode, it is not always clear if this has happened, since out-of-plane silicide is often projected over the area of interest.

The data for this sample will also be shown in the poster/presentation.

CONCLUSIONS

With three-dimensional FinFET transistors already commercially available and with the assumption that Moore's Law will continue beyond 14 nanometers, there is a push to either make lamellae thinner or make electron tomography work for semiconductor samples. If tomography is the answer, certain technical challenges need to be addressed. Sample throughput needs to improve, for example. But most importantly, the nature of tomography needs to be understood by both TEM engineers and internal requestors, and technical transparency should be maintained between the two groups. Leaving noise in the images so that all stakeholders have an equal chance to see the raw data and draw their own conclusions would be a good practice. The need to tune a semiconductor process requires speed of data and transparency and integrity of the technique. Based on our preliminary results showing tomographic images of advanced CMOS technology, it is our finding that tomography can add value to process development.

ACKNOWLEDGEMENTS

Sample preparation was carried out by Tower Adams and Lowell Hodgkins of GLOBALFOUNDRIES in Malta, NY.

COPYRIGHT

REFERENCES

1. P. A. Midgley, M. Weyland, T. J. V. Yates, I. Arslan, R. E. Dunin-Borkowski, and J. M. Thomas, "Nanoscale scanning transmission electron tomography," Journal of Microscopy, vol. 223, pp. 185-190, September 2006.
2. C. Kubel, A. Voigt, R. Schoenmakers, M. Otten, D. Su, T.-C. Lee, A. Carlsson, and J. Bradley, "Recent Advances in Electron Tomography: TEM and HAADF-STEM Tomography for Materials Science and Semiconductor Applications," Microscopy and Microanalysis, vol. 11, pp. 378-400, 2005.
3. P. A. Midgley, R. E. Dunin-Borkowski, "Electron tomography and holography in materials science," Nature Materials, vol. 8, pp. 271-280, April 2009.
4. A. J. Mardinly, "Electron Tomography and Three-Dimensional Aspects of Transmission Electron Microscopy," Electronic Device Failure Analysis, vol. 7, pp 6-12, 2005.
5. C. Kubel, J. Kubel, S. Kujawa, J.-S. Luo, H.-M. Lo, and J. D. Russell, "Application of Electron Tomography for Semiconductor Device Analysis," Microscopy and Microanalysis, vol. 12, pp. 1552-1553, August 2006.
6. M. Weyland, P. A. Midgley, "Electron Tomography," Materials Today, vol. 7, pp. 32-40, December, 2004.
7. J.-S. Luo, J. D. Russell, L.-Y. Huang, and T.-P. Chen, "Applications of Electron Tomography on Advanced DRAM," Proceedings of the 33rd International Symposium for Testing and Failure Analysis, pp. 115-120, November 2007.
8. J. Frank. Electron Tomography: Three-dimensional Imaging with the Transmission Electron Microscope. New York: Plenum Press, 1992, ch. 8, pp. 197-204.
9. J.-S. Luo, C.-C. Huang, and J. D. Russell, "Embedded Gold Markers for Improved TEM/STEM Tomography Reconstruction," ISTFA: Proceedings from the 34th International Symposium for Testing and Failure Analysis, pp. 172-179, 2008.
10. H. L. Porter, M.-G. Sung, E. Bersch, and A. Cordes. "Applications of Electron Tomography for Semiconductor Failure Analysis and Reference Metrology," International Symposium on Semiconductor Manufacturing, 2012.

KEYWORDS

TEM, electron tomography, advanced metrology, 28 nm, MOSFET, SiGe, NiSi

TU–10

QUANTITATIVE CHARACTERIZATION AND APPLICATIONS OF A 193 NM SCATTERFIELD MICROSCOPE

M. Y. Sohn [a, b], B. M. Barnes [a], and R. M. Silver [a]

National Institute of Standards and Technology (100 Bureau Drive, Gaithersburg, MD) [a]
Hyperion Biotechnology, Inc. (12002 Warfield, Suite 101, San Antonio, TX) [b]

INTRODUCTION

With decreasing feature sizes in semiconductor manufacturing, there is an acute demand for measurements of both critical dimensions (CD) and defects on the nanometer scale that must also be non-destructive measurement and provide high throughput[1]. Scatterfield optical microscopy is one method for meeting this demand as it provides high sensitivity for differentiating nanometer features[2]. The illumination angle at the sample in angle-resolved scatterfield microscopes is controlled through engineering at the conjugate back focal plane (CBFP), so that the scattered field from the sample yields unique information on the image plane as a function of illumination angle. We have developed a scatterfield microscope that uses a 193 nm ArF excimer laser and a 193 nm catadioptric objective lens, characterized it for semiconductor metrology, and obtained experimental data for defect detection and CD measurements.

MICROSCOPE STRUCTURE

To construct an effective optical tool for these purposes, the entirety of the microscope optics were designed in-house, specified for custom manufacturing, and optimized to coordinate with the catadioptric objective lens shown as Fig. 1. The illumination path was constructed to be telecentric across the CBFP with the best possible relationship between CBFP and the illumination beam on the sample. The scanning module at the CBFP consists of a rotating wheel of various apertures, and a piezo-controlled aperture was also installed on a separate stage. The collection path was constructed to provide both high magnification imaging and Fourier plane imaging. Both paths were equipped with polarizing elements to investigate the dependence of the scattered field on the incident polarization [3].

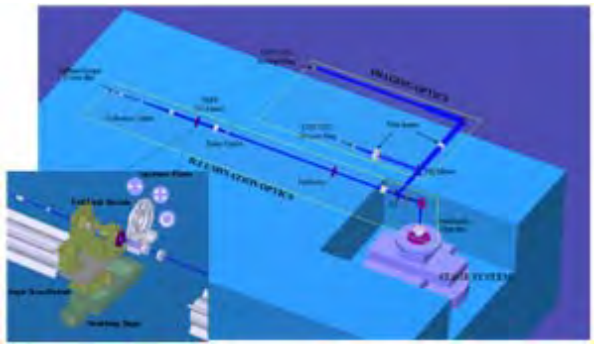


FIGURE 1. Schematic of 193 nm scatterfield microscope.

CHARACTERIZATION

Characterization is done by investigating separately the illumination and collection paths of the microscope as well as the overall imaging capability. Of critical importance are the laser energy fluency through the optical paths, the high

TU–10

resolution image quality, the image variation over time, and polarization characteristics through the optical paths. Evaluations are made using a $\lambda = 193$ nm capable CCD camera. For the illumination path specifically, the Köhler illumination homogeneity, the telecentricity across the CBFP, the through focus character along to the illumination angle and their dependence on polarization, and the relationship between CBFP and illumination angle on the sample were investigated. This characterization is used in defect detection and CD measurement. As an example, Fig. 2 shows the illumination angle broadness across the CBFP which directly affects the scattered field from the sample. Additional CBFP plane characteristics with respect to the illumination were investigated as the basis for quantitative measurement for applications such as the defect detection and CD measurement.

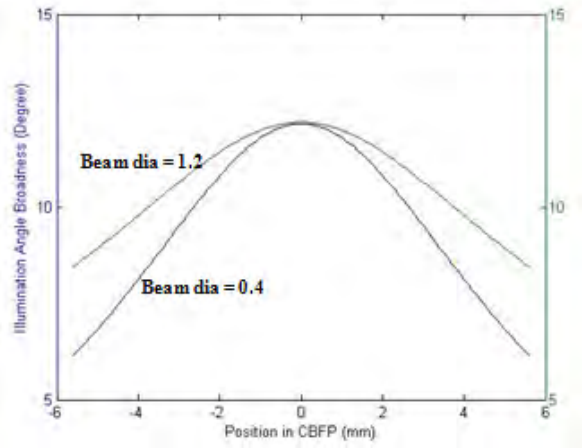
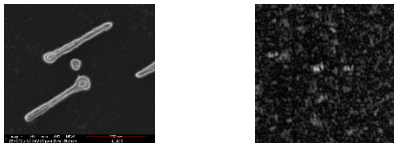


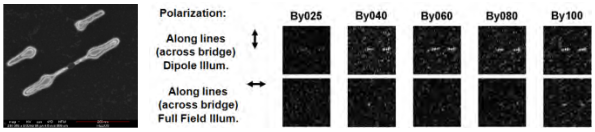
FIGURE 2. Illumination angle broadness over CBFP.

APPLICATIONS

Two important application areas in semiconductor metrology, defect detection and CD measurement were demonstrated using the developed 193 nm scatterfield microscope. Figure 3 shows the defect detection results of the island and bridge defects, respectively. The defect signal image was made by subtracting a defect image from a reference image that was generated by translating the stage by 2 μm, so that the signal image has two peaks in absolute value. The bridge defects, with CDs as small as 15 ± 2 nm (< λ/10) were detected by implementing an engineered illumination beam[4]. In this measurement the illumination angle and the polarization direction were dominant factors that effectively differentiated these defects. The effect of angular illumination on defect detection was analyzed by varying the polar and azimuthal angular ranges incident on the sample.



(a) Island defect (b) Island defect signal



(c) Bridge defect (d) Bridge defect signal

FIGURE 3. Defect detection: (a), (c) are SEM pictures and (b), (d) are their differentiated signal images by reference images shifted by 2 micrometers.

CD measurements are another area of application for 193 nm scatterfield microscope. The grating images of lines of 20 nm or less vary in the intensity though the images do not resolve the line, showing the differentiation according to the difference in linewidth. Parametric fitting against a simulated library is required for quantified measurements of these important critical dimensions.

REFERENCES

1. R. M. Silver, et al., *Proc. SPIE* **6152**, 61520Z (2006).
2. R. M. Silver, et al., *Appl. Optics* **46**, 4248-2257 (2004).
3. Y. J. Sohn, et al., *Proc. SPIE* **6158**, 61184Z (2007).
4. B.M. Barnes, et al., *Proc SPIE* **8324**, 83240F (2012).

KEYWORDS

193 nm, scatterfield microscopy, optical metrology, characterization, defect, critical dimension.

TU–11

3-D Optical Metrology of Finite sub-20nm Dense Arrays using Fourier Domain Normalization

J. Qin, H. Zhou, B. M. Barnes, R. Dixson, and R. M. Silver,

Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, 100 Bureau Dr. MS 8212, Gaithersburg, MD USA 20899-8212

Introduction

Reduced target dimensions requiring improved resolution and sensitivity have driven the need to use and analyze the phase and scattered frequency information available when using image-based scatterometry systems. One such system is scatterfield microscopy, which provides high magnification imaging, spatial selectivity, and a capability to capture all phase and frequency information within the collection numerical aperture. It has been shown that sensitivity to nanometer scale changes can be observed when measuring critical dimensions of sub-wavelength dense arrays that scatter only the 0^{th}-order specular diffraction component by engineering the microscope illumination to yield angle-resolved measurements [1]. Acceptable quantitative statistical analysis with rigorous agreement between experiment and theory has represented an important advance in image-based optical metrology to realize sub-nanometer scale uncertainty measurement for these 0^{th}-order targets [2]. However, many interesting features are either non-repetitive, irregular, or have pitches greater than the wavelength of light leading to scattering of multiple (or even a continuum of) frequency components. Of particular interest are the edges of a finite scatterometry target, whose optical response is a combination of its nearby substrate and the dense specular or high-order optical response from the linearly arrayed region. Here we present our new approach that enables rigorous analysis of 3-D through-focus and angle-resolved optical images that samples the three-dimensional electromagnetic field above and into finite targets of interest that scatter a continuum of scattered frequency components. This technique involves parametric fitting of the three-dimensional scattered field with rigorous electromagnetic simulation, experimental Fourier domain normalization procedures, and statistical methods to evaluate sensitivities and uncertainties.

Hardware platform and complex tool normalization

This new technique is based on optical images that were taken using scatterfield microscopy, which provides full access and control of the angular distribution of the incident light, has been described in detail elsewhere [3, 4]. Data are acquired as a function of angle or focus position. A kernel of each image is averaged into a profile and they are

TU–11

concatenated into a single data set for parametric fitting and statistical analysis. However, the success of this optical metrology for patterned targets is dependent upon the ability to fully characterize the complex imaging optics of the microscope, rigorously model measurements with an acceptable degree of accuracy, and quantitatively address uncertainties in measurements.

The scatterfield microscope consists of two groups of optical elements: illumination path optics that determine the light incident on the sample, and collection path optics that affect the scattered light transmissivity as a function of angle and polarization. They both introduce instrumentation errors to the image, that require proper experimental normalization procedures to allow accurate comparison of angle-resolved or focus-resolved measurements with theory. This is very complex when the scattered frequencies are continuous, and no simple method exists to isolate and measure the individual frequency components and normalize them separately. However, since electromagnetic scattering simulations inherently identify the scattering direction of each order, we apply the collection path tool function to the amplitudes of the simulated scattered orders before the image is constructed. Furthermore, the illumination path also needs to be characterized in order to correct the experimental data as the simulations assume unit incident light at each angle and polarization. Thus, both the illumination path tool function and the collection path tool function must be calculated and implemented separately for each individual illumination angle and the resulting vast spectrum of scattered light.

Regression Analysis and Simulation Studies

With this technique, a nonlinear regression model which can be expanded using a Bayesian approach to include a priori information for hybrid metrology is developed to analyze uncertainties [5, 6]. In this regression approach, we use concatenated data from each image profile that includes sensitive phase information which are usually smeared out in scatterometry and solve for the best parameter fit and parametric uncertainties. Here, simulation based studies were carried out to evaluate this technique for CD metrology for finite dense array targets with sub-20nm line width. We treat realistic noise-laden simulation sets, which include profiles from different focus positions or from different incident angles, as experimental data, followed by regression analysis and an uncertainty calculation This approach confidently predicts reduced uncertainties for finite dense array measurements.

Parametric Fitting and Uncertainty Analysis

Targets measured include a silicon step edge and the edge of finite sub-20 nm dense array. Libraries based on rigrous simulation are constructed followed by parametric fitting and regression analysis. Figure 1 shows one example of parametric fitting results of silicon step edge profiles at various focus positions.

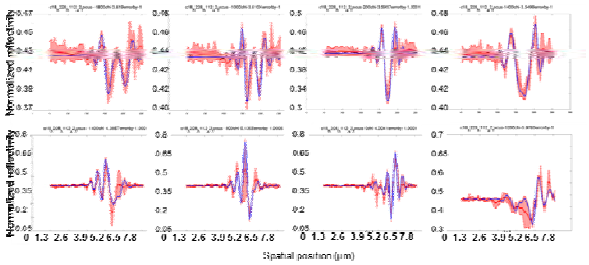


FIGURE 1. Selected focus-resolved theory-to-experiment fitting results of Si single edge target.

References

1. B. M. Barnes, etc. Proc. SPIE 6518, 65180F (2007)
2. R. M. Silver , J. Qin, etc. Proc. SPIE 83240N(2012).
3. Y. J. Sohn, B. M. Barnes, etc. Proc. SPIE 61523S (2006)
4. R. M. Silver, B. Barnes, etc. Applied Optics, Vol. 46, 20, pp. 4248-4257 (2007)
5. R. M. Silver, N. F. Zhang, etc. Proc. SPIE 797116 (2011)
6. N. F. Zhang, R. M. Silver, etc. Applied Optics, Vol. 51, Issue 25, pp. 6196-6206 (2012)

Keywords

OCD metrology, phase sensitive measurement, transmission tool function, Fourier domain normalization, parametric fitting and uncertainty analysis

TU–12

Multi-technique Approach for Determination of Crystalline Phase and Electronic Structure of Atomic Layer Deposited $HF_{1-x}Zr_xO_2$

Relja Vasić,* Steven Consiglio,** Robert Clark,** Kandabara Tapily, ** Manasa Medikonda,* Gangadhara Raja Muthinti,* Eric Bersch,*** Gert Leusink,** and Alain Diebold*

**College of Nanoscale Science and Engineering, University at Albany, 257 Fuller Rd., Albany, NY 12203*
***TEL Technology Center, America, LLC, 255 Fuller Rd., Albany, NY 12203*
****SEMATECH,* 257 *Fuller Rd., Albany, NY 12203*

Introduction

In order to continue the scaling of MOSFET devices it is necessary to decrease the equivalent oxide thickness of the gate dielectric and one method of achieving this is to increase its dielectric constant. As a replacement for SiO_2 based gate dielectrics Hf-based dielectrics have been chosen as viable materials.[1] Recent studies have shown that HfO_2 with an admixture of ZrO_2 has the potential to provide a higher dielectric constant by means of stabilization of the tetragonal phase as opposed to the thermodynamically preferred monoclinic phase which is typically obtained for HfO_2.[2,3]

We have previously reported on a multi-technique approach for the evaluation of the crystallinity of thin HfO_2 films using a combination of photoemission-based and spectroscopic ellipsometry (SE) measurements. X-ray and UV photoelectron spectroscopy (XPS and UPS) were used to show the presence of crystallinity and a specific absorption edge feature in spectroscopic ellipsometry was used to determine if the crystalline phase was monoclinic, and these results were corroborated with grazing incidence in-plane X-ray diffraction (GIIXRD).[4] In this study we extend this approach by utilizing near edge X-ray absorption fine structure spectroscopy (NEXAFS) to study $Hf_{1-x}Zr_xO_2$ films with x = 0, 0.6, and 1. These films were previously characterized using GIIXRD (Figure 1) and pole figure analysis using synchrotron radiation, [5] and in this study GIIXD and PF are complemented with NEXAFS.

Experimental

The films analyzed in this study were grown by atomic layer deposition (ALD) and a subset of these samples were grown using a cyclical deposition and annealing scheme, which is termed DADA (20 ALD cycles followed by inert anneal, repeated 5 times).[6] Grazing incidence in-plane X-ray diffraction (GIIXRD) measurements were performed at the beamline X20A of the National Synchrotron Light Source (NSLS) at Brookhaven National Laboratory using X-rays with wavelength of 1.5482 Å with angle of incidence set to 0.5° and the detector scanned in the plane of the film. NEXAFS was carried out at the National Synchrotron Light Source (NSLS) X1B undulator

TU–12

beamline at Brookhaven National Laboratory. For NEXAFS, in the energy range from 515 to 555 eV, the slit widths were set to give a resolution of 0.1 eV at 530 eV. XPS was performed in a laboratory based XPS system with a monochromatized Al K_α source. SE was measured over a wavelength range of 150 – 1000 nm using a Woollam vacuum ultraviolet-variable angle SE (VUV-VASE).

RESULTS AND DISCUSSION

Figure 2 shows the normal incidence NEXAFS spectra in the conduction band region of the O K-edge absorption above 531 eV with the metal d (Hf 5d and Zr 4d), s and p final states. For both as deposited and DADA processed films the lower energy peak at ~533 eV and the higher energy peak at ~538 eV are the crystal-field-split e_g and t_{2g} components of the unoccupied d states hybridized with O 2p orbitals.[7-8] The DADA films annealed at 800°C show sharper e_g and t_{2g} peaks and larger crystal field splitting consistent with higher ordered crystalline phases (monoclinic or tetragonal), in agreement with previous XRD measurements. [5] A series of well-defined s and p peaks in the higher energy range of 540-549 eV are indicative of ordered crystalline phases.[8,9] As deposited samples show only one broad peak in the energy range from 540-549 eV. The first peak at ~543 eV and second peak at ~545 eV are related to the metal s and p final states, respectively. The higher energy peaks beyond these are indicative of multiple scattering effects resulting in the fine structure oscillations; a unique signature of each crystalline phase. For the DADA $Hf_{0.4}Zr_{0.6}O_2$ sample, the spectra in the metal d, s and p regions indicate mixed monoclinic (m) and tetragonal (t) phases and structural m-t change with increase of Zr content.[5,8] Above 540 eV, the DADA ZrO_2 shows five peaks in agreement with predominantly tetragonal phase while DADA HfO_2 sample shows three peaks which is indicative of predominantly monoclinic structure.[9,10]

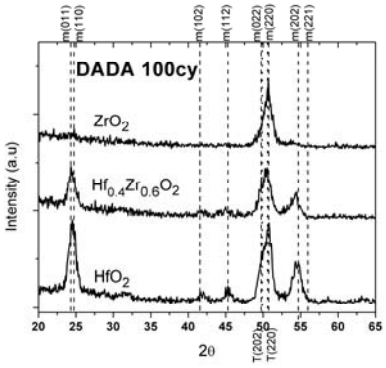


FIGURE 1. GIIXRD spectra of DADA processed films; m-HfO_2, $Hf_{0.4}Zr_{0.6}O_2$ and t-ZrO_2, vertical lines show table values for nearest monoclinic and tetragonal peaks.

Our previously reported GIIXRD measurements indicated higher ordering of in-plane lattice planes for DADA processed films.[5] The pole figure analysis also revealed a preferred orientation normal to the substrate (fiber texture); namely monoclinic M(-111) reflection for HfO_2 and tetragonal T(111) reflection for ZrO_2 films. NEXAFS spectra in normal beam incidence shows strong ordering of in-plane crystalline planes and texture in agreement with pole figure analysis.[5]

Conduction band minima (CBM) were derived from intercept of the first derivative of the inflection point of the lowest part of conduction band and the energy scale. (Table 1). The CBM, which is relevant in terms of device leakage, is observed to reduce with increasing ZrO_2 content.

TU–12

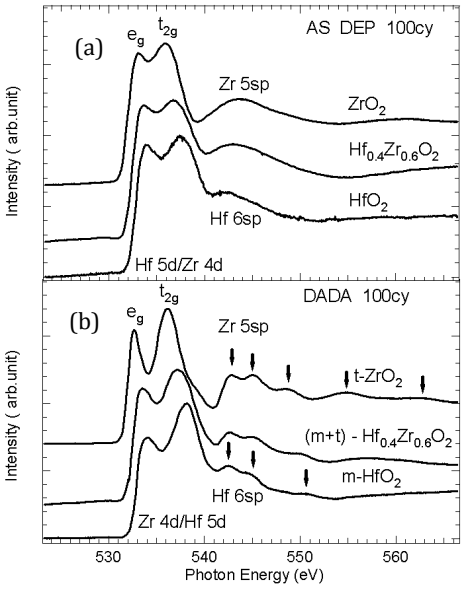


FIGURE 2. Normal incidence NEXAFS at O K edge for (a) as deposited and (b) DADA processed films. For DADA m-HfO_2 and t-ZrO_2, arrows show peaks in sp band and extended region.

TABLE 1. Conduction band minima (eV) for as deposited and DADA films at O K edge.

Sample	as deposited	DADA
HfO_2	532.0	532.4
$Hf_{0.4}Zr_{0.6}O_2$	531.6	531.9
ZrO_2	531.2	531.4

The XPS measurements of the valence band (Figure 3) show a clear double peak structure due to the valence band splitting of O 2p bonding and non-bonding states at high and low binding energy, respectively, for the crystalline films (denoted by black arrows).[9,10] In the case of amorphous films one broad peak is observed.

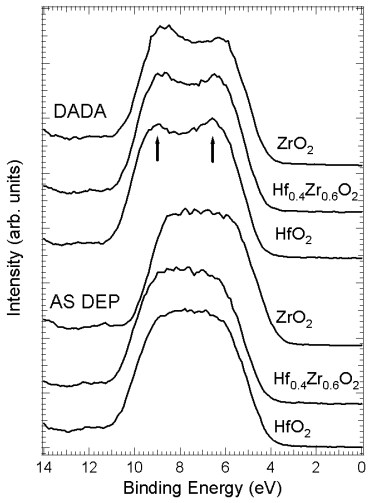


FIGURE 3. X-ray photoemission valence band spectra for HfO_2, $Hf_{0.4}Zr_{0.6}O_2$ and ZrO_2 as deposited and DADA.

The optical properties of $Hf_{1-x}Zr_xO_2$ films were studied by spectroscopic ellipsometry (Figure 4) by extracting the imaginary part of the dielectric function and observing the band edge absorption feature at about 6 eV.[4,11] The absorption feature at 6 eV is unique to monoclinic HfO_2 and it decreases with increasing ZrO_2 composition.

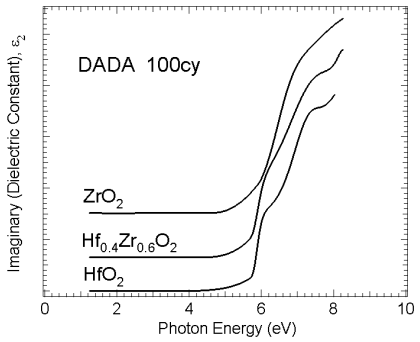


FIGURE 4. Imaginary dielectric constant (VUV-SE) of HfO_2, $Hf_{0.4}Zr_{0.6}O_2$, and ZrO_2 films from DADA process.

The systematic behavior of the absorption feature in transition from monoclinic to tetragonal structure is in agreement with GIIXD, pole figure, and NEXAFS data.

TU–12

CONCLUSIONS

The combination of XPS of the valence band and SE of the optical band edge can be used to identify crystallinity and the presence of monoclinic vs. tetragonal phase for $Hf_{1-x}Zr_xO_2$ high k materials. NEXAFS of the conduction band was used to unambiguously determine the electronic conduction band structure, crystalline phase, and the crystal phase transformation from monoclinic to non-monoclinic (mainly tetragonal) structure due to the addition of ZrO_2 in HfO_2. The combination of SE and XPS to determine crystalline phase may offer promise for an integrated in-line metrology and hybrid metrology approach for high-k dielectric development and monitoring.

ACKNOWLEDGEMENTS

Use of the National Synchrotron Light Source, Brookhaven National Laboratory, was supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DEAC02-98CH10886. We thank Shawn Sallis (Binghamton University) and Bo Chen (Boston University) for help in data collection.

REFERENCES

1. D. G. Schlom, et al., *MRS Bull.* **33**, 1017 (2008).
2. D. H. Triyoso, et al., *J. Vac. Sci. Technol. B* **25,** 845 (2007).
3. J. Müller, et al., *Microelectron. Eng*. **86**, 1818 (2009).
4. E. Bersch, et al., *AIP Conf. Proc*. **1395**, 154 (2011).
5. K. Tapily, et al., *ECS Trans*. **45**(3), 411 (2012).
6. S. Consiglio, et al., *J. Electrochem. Soc*. **159**, G80 (2012).
7. G. Lucovsky, et al., *Microelectron. Reliab.* **46**, 1623 (2006).
8. D.-Y. Cho, et al., *Phys. Rev. B* **82**, 094104 (2010).
9. M. Komatsu, et al., *Appl. Phys. Lett*. **89**, 172107 (2006).
10. S. Toyoda, et al., *J. Appl. Phys*. 97, 104507 (2005).
11. E. E. Hoppe, et al., *Appl. Phys. Lett*. **92**, 141912 (2008).

KEYWORDS

high k dielectrics, spectroscopy, NEXAFS, crystalline structure, electronic structure

TU–13

Quantification of Hafnium in Hafnium Oxide Film by Isotope Dilution Neutron Activation Analysis

Toshiko Takatsuka, Kouichi Hirata, Kenji Ito, Naoko Nonose, Tsutomu Miura

National Metrology Institute of Japan, National Institute of Advanced Industrial Science and Technology, Central 5, 1-1-1 Higashi, Tsukuba, Ibaraki 305-8565, Japan

Introduction

Hafnium oxide (high-k) dielectric films are utilized for silicon-based semiconductor devices in order to attain the higher performance. The front-end process on the device production requires a precise control of the thickness of the dielectric film for the device gate stacks. According to the international technology roadmap for semiconductors 2011, the thicknesses for the high-k films, typically having below several nm, are necessary to be adjusted within 4% process range[1]. However the accurate measurements of their thicknesses in length unit are laborious, possibly caused by the atomic fluctuation at interface layers. Due to the difficulty in the direct determination of the thickness, we aimed to quantity hafnium in hafnium oxide films in weight unit by means of the isotope dilution neutron activation analysis.

EXPERIMENTALS

Film Deposition

Hafnium oxide films were deposited on 4-inch Si wafers by magnetron sputtering. The target thickness was set to 4 nm. The homogeneity in thickness over the wafer was estimated less than 2% of standard deviation by using a 100-nm-thick film. The prepared wafers with the deposited 4-nm-thick hafnium oxide were cut into 10 mm × 10 mm pieces for the measurements.

Isotope Dilution Neutron Activation Analysis

The sample preparation procedure for the isotope dilution neutron activation analysis (ID- NAA) is summarized in Fig. 1. Two sequences of an isotope dilution (ID) and a reverse-ID are necessary to ensure traceability to the SI units; the latter sequence was performed to determine the hafnium concentration in a spike solution with a hafnium standard. The spike solution was prepared by dissolving ^{174}Hf-enriched hafnium oxide in a HNO_3 + HF aqueous solution at 100 °C for three hours, followed by diluting to a proper concentration. For calibrating the amounts of hafnium, a working standard solution was prepared by diluting NIST SRM 3122 gravimetrically.

Three samples were picked up from the cut wafer pieces. In order to calculate the surface areas of the samples, the lengths of four sides for each chip were measured from respective photo images taken using a commercial optical scanner with high resolution, calibrated by standard scales in length.

For the ID analysis, small amounts of the spike solution were dropped onto each hafnium oxide sample using a polyethylene pipette (ID-1 in Fig. 1), while those of the spike solution and standard solution were dropped separately onto different cleaned filter papers (ID-2 and ID-3 in Fig. 1). The hafnium contents of the droplets were determined by weighing the polyethylene pipettes before and

TU–13

after every dropping. Similar sample with the spike solution and standard solution was also prepared using cleaned filter paper for the reverse-ID analysis (R-ID in Fig. 1).

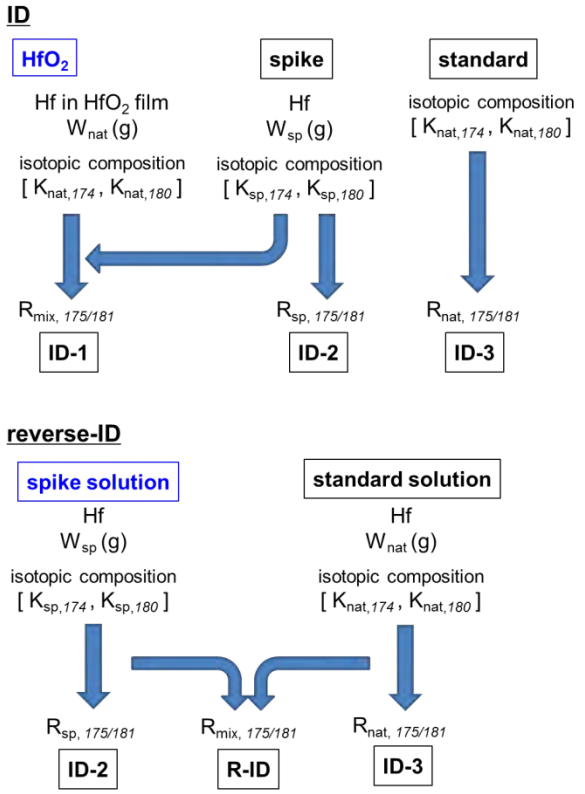


FIGURE 1. ID-NAA sample preparation procedure.

All the samples were sealed up separately in clean polyethylene bags. The sealed samples were stacked in a polyethylene container for the neutron irradiation. The irradiation was performed for 4 hours with a 5.5×10^{12} $cm^{-2} \cdot s^{-1}$ thermal neutron fluence rate at Pn-2 in the Kyoto university research reactor (KUR).

The gamma-ray activity of each sample was measured by a high-purity germanium detector (CANBERRA) with an energy resolution around 2.0 keV and a relative efficiency of 40% at 1333 keV. Every sample was set on a plastic plate placed at a distance of about 6 cm from the detector. The accumulation of the energy spectra for each sample was carried out twice and the counting times were varied so as to fix the integrated hafnium counts to be constant for all the measurements. More than 80000 counts were collected for the ^{175}Hf and ^{181}Hf peaks in each spectrum, so that the standard deviations due to the statistics were less than 0.35%.

RESULTS AND DISCUSSION

As shown in Fig. 2, several peaks due to the hafnium isotopes generated during the neutron irradiation are found in the gamma-ray spectrum. The peaks at 343 keV and 482 keV were selected to calculate the gamma-ray intensity ratio of ^{175}Hf to ^{181}Hf for the samples. The integrated peak areas were converted into the counting rates at the end of the irradiation, taking into account of the radioactive decay and the dead time of the measuring system. The amounts of hafnium in the hafnium oxide samples were calculated from the intensity ratios based on a formula reported in Ref. 2, and the results are summarized in Table 1. The obtained amounts are ranging between 3.504 μg and 3.518 μg. The varied values may be caused by several factors such as the measurement repeatability, thickness inhomogeneity of the hafnium oxide film, the size difference of the sample pieces. By dividing the hafnium amounts by the sample areas, the area densities were calculated to be in the range from 3.585 $\mu g/cm^2$ to 3.596 $\mu g/cm^2$. The resultant average for the three samples is 3.592 $\mu g/cm^2$ (equivalent to 4.4 nm in thickness with a density of 9.7 g/cm^3) and the relative standard deviation is 0.17%.

The major source of the uncertainty for the obtained hafnium contents includes the measurement repeatability, the counting statistics, and the difference between sample pieces, while another source is possible to originate from the area measurements. The surface area of each sample piece was calculated from the 4 side lengths of the rectangular piece determined by using their optical images. Thus the uncertainty in the area measurements is probably due to the difficulty in fixing the exact edge of each side. The other sources are the preparation of the standard solutions as

TU–13

well as the weighing hafnium amounts of the solutions. The estimation of the total uncertainty is still under evaluation.

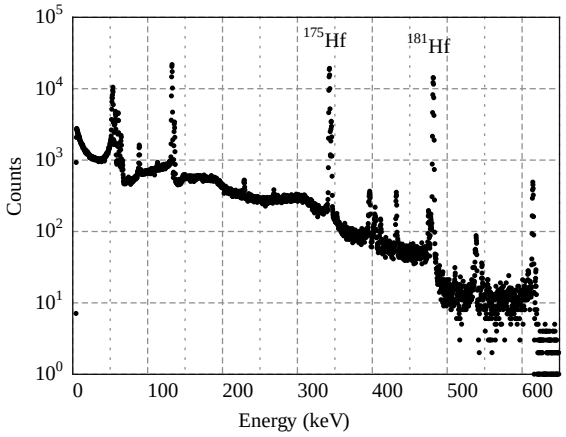


FIGURE 2. Gamma-ray spectrum of hafnium oxide film + spike solution.

TABLE 1. Hafnium contents in hafnium oxide samples.

	Hf content	**area**	**area density**
HfO_2-1	3.510 μg	0.9763 cm^2	3.595 μg/cm^2
HfO_2-2	3.504 μg	0.9742 cm^2	3.596 μg/cm^2
HfO_2-3	3.518 μg	0.9813 cm^2	3.585 μg/cm^2

SUMMARY

Hafnium amounts in hafnium oxide films were quantified as area densities through ID-NAA. The results demonstrated that ID-NAA is applicable for the precise methodology for semiconductor-device manufactures.

ACKNOWLEDGEMENTS

The NAA measurements were performed at the facilities of the Research Reactor Institute, Kyoto University.

REFERENCES

1. *The international technology roadmap for semiconductors 2011*.
2. C. Yonezawa and T. Komori, *Anal. Chem.* **55**, 2059-2062 (1983).

KEYWORDS

Hafnium oxide film, neutron activation analysis, isotope dilution

TU–14

COMPLEMENTARY METROLOGY – A PREREQUISITE FOR RELIABLE AND TRACEABLE CHARACTERIZATION OF SURFACES AND NANOLAYERS

Andreas Nutsch[1,2], Burkhard Beckhoff[1], Jaap Van Den Berg[3]

[1]*Physikalisch-Technische Bundesanstalt, Abbestr 2-12, 10587, Berlin, Germany*

[2]*previously Fraunhofer IISB, Schottkystrasse 10, 91058 Erlangen, Germany*

[3]*University of Huddersfield, Huddersfield, HD1 3DH United Kingdom*

INTRODUCTION

The continuous reduction of device dimensions for nano- and microelectronics drives the development of metrology, analysis and characterization. For solving challenging problems in the area of nanotechnologies the approach of complementary metrology is essential. This paper reviews the use of complementary metrology for carbon surface contamination and for nanolayer analysis.

CONCEPTS OF COMPLEMENTARY METROLOGY

Recently, complementary metrology was studied in a distributed joint laboratory for characterization of samples from nanoelectronics [1-3]. In a first step the analytical tasks or samples were defined with respect to possible measureands. Secondly, the analytical capabilities were determined. Based on these two criteria a matrix was set up which assigns each measurand analytical techniques. Complementarity of the metrology could be achieved by looking on a measurand and the possible analytical techniques. The methods benefit from each other by e.g. supporting the information on thicknesses or density not obtained but required by other methods.

CHARACTERIZATION OF CARBON ON SURFACES

A challenge for the characterization of organic compounds on semiconductor surfaces is their quantification and classification. For carbon surface contamination the analytical techniques Thermal Desorption Gas Chromatography Mass Spectrometry (TD GCMS), time of flight secondary ion mass spectrometry (TOFSIMS) and Total Reflection X-Ray Fluorescence (TXRF) in combination with Near Edge X-ray Absorption Fine Structure (NEXAFS) were bench-marked. The combination of all three methods was shown to give a holistic approach for characterization of both volatile and non volatile organics on surfaces.

TU–14

The volatile carbon contamination was found to be twice or even an order of magnitude higher compared to the non-volatile organic contamination. Typical carbon layers on the surfaces were found to be approx. 0.7 nm thick. It should be mentioned that the carbon amount on the surface was determined under ultra-high vacuum conditions, and therefore the volatile organics are expected to have mostly desorbed. Furthermore, only the carbon was quantified without taking into account OH and chlorine, sulphur, metals, etc. compounds of the organics. Therefore, carbon quantification showed only 70-80% of the non-volatile organic surface contamination.

Currently, for quantification of volatile organic compounds (VOC) with boiling points below 300°C TD GCMS is suitable. Analytical techniques operating in ultra high vacuum are not able to deal with organic compounds having both low boiling points and low vapor pressure. For the quantification of the total carbon surface contamination, reference-free TXRF and NEXAFS operated at excitation energies below 1.8 keV is ideal. For the benchmarking of methods see Table 1. As a result one should keep in mind that only the use of at least two techniques e.g. NEXAFS and GCMS are able to describe the organic surface contamination.

TABLE 1. Comparison of Analytical techniques TOFSIMS, TDGCMS and TXRF-NEXAFS for characterization of organic contamination on semiconductor surfaces.

Method	TOFSIMS	TD-GCMS	TXRF NEXAFS
probing conditions	vacuum; beam raster of 200 x 200 μm^2	atmosphere whole wafer	Vacuum spot of 70x140 μm^2
detection of volatile organics	limited	strength: detection of VOC	limited
detection of non-volatile Compounds	strength: detection of non-volatile organics	not possible	strength: determination of total carbon amount on surfaces
identification of organic compounds	limited due to method and database	strength: identification using a database	limited to specific lines e.g. Br etc.
quantification	difficult	semi quantitative to n-hexadecane	reference-free

CHARACTERIZATION OF NANO LAYERS

Accurate structural and compositional characterization of high-k hafnium silicate (HfSiOx) layers enables an understanding of their properties and the ability to control these. Those high-k layers were used to compare medium energy ion scattering (MEIS) with spectroscopic ellipsometry (SE), x-ray photoelectron spectroscopy (XPS), and high resolution transmission electron microscopy (XTEM) and reference-free synchrotron radiation based X-ray fluorescence (XRF). For MEIS especially modeling and the knowledge of material parameters is crucial for the reliability of results as well as for the other techniques. MEIS was shown to perform elemental profiling at nanostructures having at nanometer depth resolutions. The techniques presented are able to show highly precise results for dimensional, compositional and contamination analysis focusing on both inorganic and organic components.

The material system and layer thickness of nominally 2 nm were chosen. Those state-of-the-art samples were prepared by IMEC in Leuven (B). Sample D07 remained as deposited sample D 08 obtained after post-growth decoupled plasma

nitridation (DPN) at 800°C. Results obtained with the various techniques are summarized in Table 2 for the two different densities including the error bounds for each technique.

The strength of MEIS is to determine both layer thickness and composition of nanolayers independently. XRF is a reference-free method and XPS is able to give bond specific or compound information but in common with XRF its ability in determining the layer thickness relies on the measurement of the total amount of material of a particular species in the layer. For all these methods knowledge of the film density is vital. HRTEM is able to determine the layer thickness with good accuracy, but complications can affect the result. SE was found to be sensitive to organic surfaces contamination. For these reasons the results were different from the other methods.

TABLE 2. Comparison of the layer thickness measurements for samples D07 and D08 using the different analytical techniques. Results are given for two different densities of the sili-cate layers.

Sample	Layer / density [g cm^{-3}]		$d_{nominal}$ [nm]	MEIS d [nm]	SE d [nm]	XPS d [nm]	XRF d [nm]	HREM d [nm]
D07	SiO_2	2.2	1	~0.8 ± 0.2	(.5) + 0.73	1.0 ±0.2		1.6 ±0.4
	$HfSiO_x$	6.1	2	1.5 ±0.1	2.1-2.5	1.9 ±0.1	1.5±0.2	1.3 ±0.3
	$HfSiO_x$	6.7		1.4 ±0.1		1.8 ±0.1	1.4±0.2	
D08	SiO_2	2.2	1	~1.3 ±0.2	(.5) + 0.94	1.2 ±0.1		2.7 ±0.3
	$HfSiO_x$	6.1	2	1.75 ±0.1	2.2-2.3	1.9 ±0.1	1.6±0.2	1.4 ±0.4
	$HfSiO_x$	6.7		1.6 ±0.1		1.8 ±0.1	1.5±0.2	

CONCLUSION

The use of complementary metrology but also of reference samples is crucial for the advancement of analytical methodologies.

The combination of TD-GCMS, TOF-SIMS, and TXRF-NEXAFS allows the characterization of surfaces with respect to all organic compounds. The combination of methods compensates the limitations due to measurement conditions, e.g. localized measurement or vapor pressure and boiling point of organic compounds.

The use of various analytical techniques for analysis of nanolayers was found to improve the reliability and validation of the achieved results. This was demonstrated using approx. 2 nm thick high k layers. Such a well characterized sample is ideal as reference sample.

ACKNOWLEDGMENTS

This work was partially supported by the European Commission under the FP6 Program through the Integrated Infrastructure Initiative "ANNA" contract no. 026134-RII3.

REFERENCES

1. A. Nutsch, B. Beckhoff, R. Altmann, J. A. Van Den Berg, D. Giubertoni, P. Hoenicke, M. Bersani, A. Leibold, F. Meirer, M. Mueller, G. Pepponi, M. Otto, P. Petrik, M. Reading, L. Pfitzner, H. Ryssel, Sol. State Phenom. **145-146**, 97 (2009)
2. B.Beckhoff, A.Nutsch, R.Altmann, G.Borionetti, C.Pello, M.L.Polignano, D.Codegoni, S.Grasso, E.Cazzini, M.Bersani, S.Gennaro, M.Kolbe, M.Müller, P.Kregsamer, F.Posch, ECS Trans. **25** (3), 311 (2009)
3. M. Müller, A. Nutsch, R. Altmann, G. Borionetti, T. Holz, C. Mantler, P. Hönicke, M. Kolbe and B. Beckhoff, Proceedings of the UCPSS 2010

KEYWORDS

thin layer analysis, organic contamination, semiconductor manufacturing, nanotechnologies, NEXAFS, TXRF, GCMS, MEIS

TU–15

SIMS Correction And Depth Profiling Of Ion Implantations Using Grazing Incidence XRF

Philipp Hönicke[1], Burkhard Beckhoff[1], Yves Kayser[2] and Sven Kayser[3]

1: Physikalisch-Technische Bundesanstalt, Abbestr. 2-12, 10587 Berlin, Germany
2: Paul Scherrer Institut, 5232 Villigen PSI, Switzerland
3: ION-TOF GmbH, Heisenbergstr. 15, 48149 Münster, Germany

Introduction

The continuing shrinking of the component dimensions in ULSI technology requires ultra shallow junctions (USJ) with depths in the 20-nm regime and below. These ultra shallow dopant distributions can be formed by ultra-low energy (ULE) ion implantation. However, accurate measurement techniques for ultra-shallow dopant profiles are required in order to characterize ULE implantation and the necessary rapid thermal annealing (RTA) processes.

Numerous efforts have been made to apply Secondary ion mass spectrometry (SIMS) as a well-established depth profiling technique to USJ characterization. Various effects, especially in the first few nanometers below the sample surface, lead to increased uncertainties in the SIMS determined profile shape and the determined doses [1].

Grazing Incidence X-Ray Fluorescence (GIXRF) analysis has already demonstrated the potential to be used as an alternative depth profiling technique [2-4]. In this work, the capabilities of GIXRF for the characterization of higher energy ion implants and for depth profiling in other than silicon semiconductors is shown. Furthermore, the method was applied to the correction of various SIMS depth profiles of USJ ion implantations.

Experimental

The GIXRF depth profiling is based on the induced in-depth changes of the X-ray Standing Wave (XSW) field intensity. The XSW field arises between the primary and the reflected beam and is dependent on the incident angle [3] between the sample surface and the X-ray beam. It can either be calculated using software packages, e.g. IMD [5], own software or it is calculated from X-ray reflectivity and the optical constants of the sample [6].

The implanted depth profile is convolved with this intensity distribution and other parameters, resulting in a distribution specific angular fluorescence curve during a GIXRF measurement. If the relevant experimental (e.g. the solid angle of detection [7]) and fundamental parameters of the X-ray fluorescence process are known, this GIXRF curve can be modeled by assuming a depth profile and modifying its shape [3].

The GIXRF measurements have been carried out in the laboratory of the Physikalisch-Technische Bundesanstalt (PTB) at BESSY using monochromatized synchrotron radiation of well-known radiant power and spectral purity. The plane grating monochromator (PGM) [8] and the four crystal monochromator (FCM) [9] beamlines provide photons in the energy range from 78 eV to

TU–15

10.5 keV. PTB's radiometrically calibrated instrumentation [7] was used to allow for reference-free quantification.

Comparative measurements using grazing exit X-ray fluorescence (GEXRF) [10] were performed at the ID21 beamline of the ESRF in Grenoble. SIMS measurements have been performed using the dual beam depth profiling technique with a Time of Flight mass analysis at ION-TOF GmbH unless otherwise noted.

RESULTS

The GIXRF method has been applied to the depth profiling of ion implantations into other substrate materials, e.g. GaAs, InP or other III-V semiconductors. In Figure 1, the result of a 300 keV Zn implant into InP is shown in comparison to a SIMS depth profile, measured at RTG Mikroanalyse GmbH as well as a TRIM profile [11]. The agreement between the different profiles is very good. For a Cd implant into GaAs, the agreement between SIMS and GIXRF is of comparable quality. These examples show, that GIXRF is easily adoptable to more complex matrix materials. They also demonstrate, that high energy implants with depth distributions up to the micrometer range can be characterized using GIXRF. The limiting factor determining the probable depth is the absorption behavior of the implants fluorescence line.

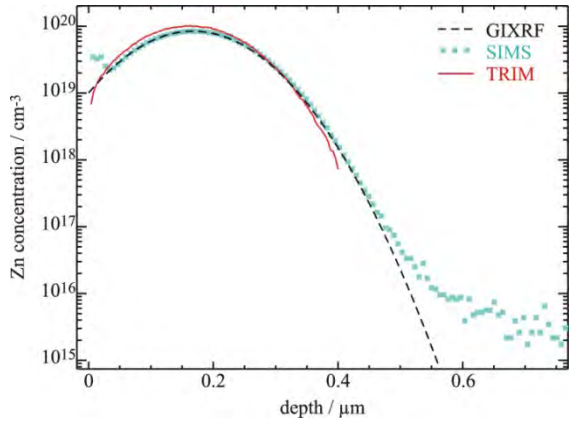


FIGURE 1. Comparison of the GIXRF determined depth profile for a 300 keV Zn implant into InP in comparison to SIMS, measured by RTG Mikroanalyse GmbH and a TRIM calculation [11].

The knowledge of the X-ray Standing Wave (XSW) field intensity is of great importance for these analyses. In general, the XSW can be calculated for an unimplanted matrix with software tools, e.g. IMD [5]. If the implanted dose is very high or if the ratio between the implants – and the matrix elements absorption coefficients is very high, the XSW calculation is more complex. Shifted depth profiles are determined with GIXRF if this is not considered (see the uncorrected GIXRF profile in Fig. 2). By introducing an XRR based iterative approach, with a recalculation of the XSW using both the XRR and the implantation depth profile the agreement to SIMS and GEXRF could be drastically improved [6]. The SIMS profile was measured at RTG Mikroanalyse GmbH.

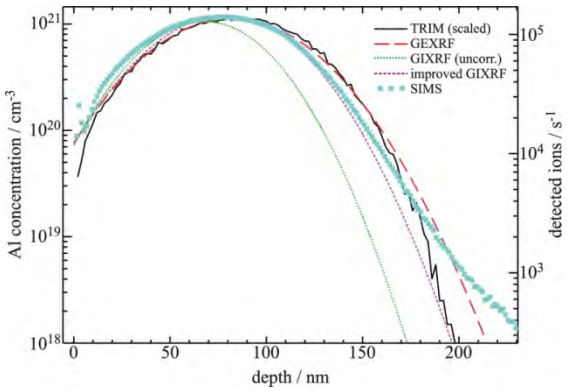


FIGURE 2. Comparison of different analytical results for a 50 keV Al implant into silicon with a dos of 10^{16} cm^{-2} [6]. Due to the high dose, the ion implant had to be considered for the XSW calculation (see text for details).

By replacing the mathematical function for the elemental depth profile of the implant with a SIMS measurement, the GIXRF technique can be used to either qualify different SIMS approaches on an identical sample, calibrate a SIMS measurement when no appropriate standard is available or even correct for the profile shape manipulating effects in the surface near parts. As an example, two SIMS results of a 0.75 keV B implant into silicon with a dose of 10^{15} cm^{-2} were corrected and compared. The corrected SIMS profiles are shown in Fig. 3 together with the measured profiles. A depth scale correction [12] was applied to take into account the sputter rate variations close to the surface. To

TU–15

further improve the agreement between GIXRF measurement and SIMS based calculation, a correction function for the shape of the depth profile close to the surface was introduced here. Both correction functions were fitted for the two SIMS results leading to very similar depth profiles.

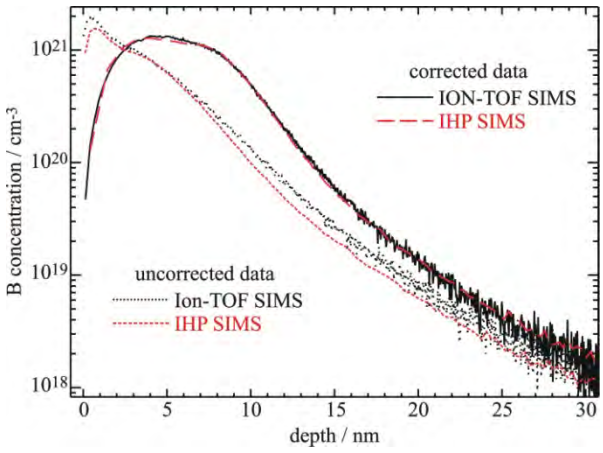


FIGURE 3. Results of the GIXRF based SIMS correction for two different SIMS results of an identical sample. A 10^{15} cm^{-2}, 0.75 keV B implant into silicon was used.

This approach was also applied to SIMS measurements of annealed implant samples, where the GIXRF fitting with a TRIM derived mathematical model function is not reasonable.

Conclusion

The GIXRF based elemental depth profiling of ion implantations is capable of achieving comparable results to SIMS and other techniques. It is a very flexible method with regard to both the implant element and the implanted matrix. Due to the very high surface sensitivity of the method, it is very suitable for USJ characterization. Depending on the absorption behavior of the fluorescence radiation, also high energy implants can be characterized with a good accuracy.

The method is very well suited for correcting SIMS measurements, where the surface near parts of the depth profile can be manipulated by different effects. Since these effects falsify the profile in depth ranges where GIXRF is most sensitive, such a combination of both methods is very fruitful.

Additionally, GIXRF can be used for the calibration of other depth profiling techniques taking advantage of the reference-free quantification capabilities of the technique.

References

1. W. Vandervoorst, T. Janssens, R. Loo, M. Caymax, I. Peytier, R. Lindsay, J. Frühauf, A. Bergmaier and G. Dollinger, *Appl. Surf. Sci.* **203-204**, 371-376 (2003).
2. A. Iida, K. Sakurai, A. Yoshinaga, Y. Gohshi, *Nucl. Instrum. Meth. A* **246**, 736-738 (1986).
3. P. Hönicke, B. Beckhoff, M. Kolbe, D. Giubertoni, J.A. van den Berg, G. Pepponi, *Anal. Bioanal. Chem*. **396(8)**, 2825-2832 (2010).
4. B. Beckhoff, P. Hoenicke, D. Giubertoni, G. Pepponi, M. Bersani, *AIP Conf. Proc.* **1173**, 29-33 (2009).
5. D. Windt, *Comput. Phys*. **12**, 360-370 (1998).
6. P. Hönicke, Y. Kayser, B. Beckhoff, M. Müller, J.Cl. Dousse, J. Hoszowska, S.H. Nowak, *J. Anal. At. Spectrom.* **27**, 1432-1438 (2012).
7. B. Beckhoff, R. Fliegauf, M. Kolbe, M. Müller, J. Weser, G. Ulm, *Anal. Chem.* **79**, 7873-7882 (2007).
8. F. Senf, U. Flechsig, F. Eggenstein, W. Gudat, R. Klein, H. Rabus and G. Ulm, *J. Synchrotron Radiat.* **5**, 780-782 (1998).
9. M. Krumrey, *J. Synchrotron Rad*. **5**, 6-9 (1998).
10. Y. Kayser, D. Banás, W. Cao, J.-Cl. Dousse, J. Hoszowska, P. Jagodziński, M. Kavčič, A. Kubala-Kukuś, S. Nowak, M. Pajek, J. Szlachetko, *Spectrochim. Acta B* **65**, 445-449 (2010)
11. J.F. Ziegler, M.D. Ziegler and J.P. Biersack, *Nucl. Inst. Meth. B* **268(11-12)**, 1818 (2010).
12. G. Pepponi, D. Giubertoni, M. Bersani, F. Meirer, D. Ingerle, G. Steinhauser, C. Streli, P. Hönicke, B. Beckhoff, *J. Vac. Sci. Technol. B* **28**, C1C59-64 (2010).

Keywords

Ultra-Shallow Junctions, Synchrotron and Neutron Techniques, Novel Measurement Methods

TU–16

TOWARDS NANOELECTRONICS METROLOGY WITH A LABORATORY SET-UP IN THE SOFT X-RAY RANGE

D. Grötzsch[1], B. Kanngießer[1], I. Mantouvalou[1], C. Herzog[1], K. Witte[1], M. Spanier[1], J. Lubeck[2], P. Hönicke[2] and B. Beckhoff[2]

[1] *Technische Universität Berlin, Institut für Optik und Atomare Physik, Hardenbergstr. 36, 10623 Berlin*
[2] *Physikalisch Technische Bundesanstalt, Abbestr. 2-12, 10587 Berlin, Germany*

INTRODUCTION

Grazing Incidence and Grazing Exit X-ray Fluorescence (GI- and GE-XRF) analyses in the soft X-ray range are excellent non-destructive method to analyze layers located at or near the surface. They are for example used for the characterization of atomic layer deposition processes (ALD) [1] or to characterize depth profiles of dopants for ultra shallow junction (USJ) applications [2,3]. At the Physikalisch-Technische Bundesanstalt (PTB), German's national metrology institute, these investigations are carried out using synchrotron radiation and calibrateted instrumentation at BESSY II. Here, we like to show the possibility to perform such kind of angle-resolved measurements with a laboratory set-up. A new laser-produced plasma-source for the soft X-ray range was developed by the Berlin Laboratory for innovative X-Ray Technologies (BLiX) at the Technical University of Berlin (TUB) and is be used for various applications [4]. Calculations for the laboratory set-up relying on depth-profile measurements by the PTB are carried out in order to demonstrate the analytical possibilities for USJ applications. In contrast to the use of synchrotron radiation, the main advantages of enabling such measurements with a laboratory set-up are higher flexibility and higher cost efficiency.

EXPERIMENTAL

The GIXRF measurements as performed at the PTB employ monochromatized synchrotron radiation provided by the plane grating monochromator (PGM) beamline for undulator radiation at BESSY II [5]. This beamline provides radiation in the energy range of 78 eV to 1860 eV. The measurements are conducted in a UHV chamber, which allows for very flexible and precise sample manipulation. The fluorescence radiation is detected with a calibrated windowless SDD. GIXRF measurements were performed on boron implanted silicon wafers, implanted at different energies [6]. This example is used to demonstrate the possibilities to transfer these measurements to the laboratory set-up.

LABORATORY SET-UP

This set-up is relying on a laser-produced plasma-source (LPS) [4] as the excitation source, a multi-purpose X-ray fluorescence (XRF) UHV experimental chamber, developed in cooperation with PTB and a compact reflection grating spectrometer [7] or a window-less SDD detector.

TU–16

A Excitation With A Laser-Produced Plasma-Source

The laser system used for the LPS is a modified Thin Disk Technology Laser by TRUMPF Inc. It delivers output pulses at 1030 nm, with a length of 1,1 ns, energies up to 250 mJ (±2%) and a repetition rate of 100 Hz to 200 Hz. The laser is focused (30 µm FWHM) on a metal target. Currently a copper target is used, but other materials are also possible. The LPS with a copper (Cu) target delivers radiation from 1 nm to 20 nm or 62 eV to 1248 eV respectively (see figure 1).

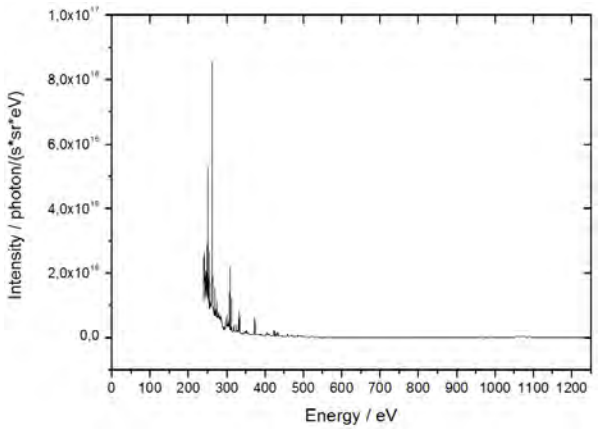


FIGURE 1. output spectrum of the LPP with a Cu target measured with a transmission grating spectrograph

B Sample Handling With A Multi-Purpose X-Ray Fluorescence (XRF) UHV Experimental Chamber

A UHV chamber with flexible in-vacuum sample handling during measurement was built in cooperation with PTB. The flange geometry is designed to realize variable measuring geometries and principles: conventional 45°/45° XRF, transmission XRF, GEXRF and GIXRF. The main part of the chamber is an UHV qualified seven axis goniometer, for flexible sample handling, accurate positioning and geometry variations. Two axes are available for monitoring diodes. The goniometer is shown in figure 3. The chamber is mounted on a base frame designed as an external four axis goniometer (X,Y,Z and rotation). The sample can be changed quickly and without venting by a load lock. Figure 2 shows the chamber with the goniometer inside on the base frame.

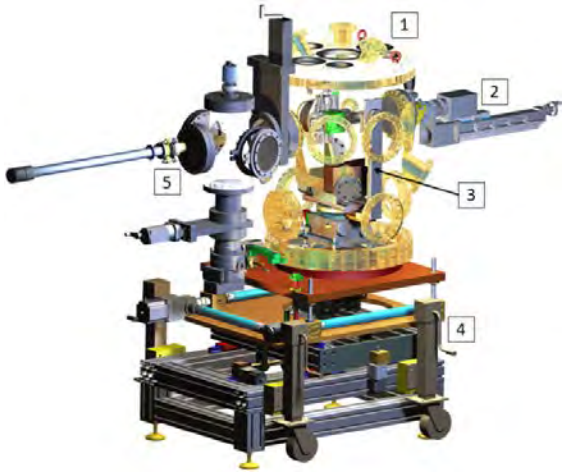


FIGURE 2. CAD model of the multi-purpose XRF UHV experimental chamber (1: vacuum chamber, 2: detector (spectrograph or SDD), 3: seven axis UHV goniometer, 4: base frame, 5: load lock)

The goniometer was qualified in collaboration with the PTB by autocollimator measurements. Precise axes are crucial for angle resolved experiments, e.g. GI- or GE-XRF measurements, as every inaccuracy of the angle leads directly to uncertainties in the depth information.

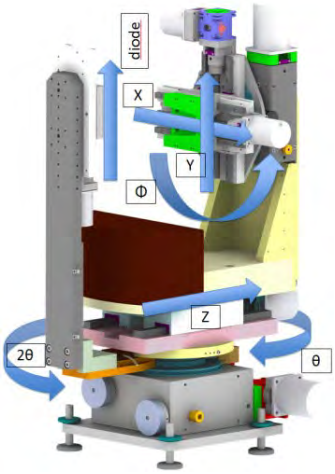


FIGURE 3. CAD model of the UHV goniometer with axis labeling

TU–16

C Detection With A Compact Reflection Grating Spectrometer

A compact reflection grating spectrometer was designed with respect to the UHV experimental chamber as well as the plasma excitation chamber. The spectrometer is necessary to characterize the excitation radiation of the LPS and as detector for different XRF measurements in soft X-ray regime. It can be used with two different reflection gratings: The gratings are designed for a spectral range of 1 nm to 5 nm (250 eV to 1240 eV) and 5 nm to 20 nm (62 eV to 250 eV) respectively. With the used CCD-detector (pixel size of 13,4 µm × 13,4 µm) the energy resolution is less than 10 eV. The size of the spectrograph could be minimized by using spherical varied-line-space (VLS)gratings [7].

Calculations

In order to assess the capabilities of the laboratory set-up for characterizing USJ dopant profiles theoretical fluorescence intensities where calculated in grazing-exit (GE) geometry. By altering the exit angle (α) the absorption path of the fluorescence radiation inside the sample is varied by factor 1/sin(α). Due to the exponential Lambert-Beer law of absorption, the relative contribution to the fluorescence signal by atoms closer to the surface is enhanced in comparison to those deeper in the sample at shallow angles. Additionally, for angles close to the critical angle of total reflection, fresnel diffraction has to be taken into account, which leads to an enhancement of contributions from surface-near regions at shallow angles [8]. Together, this allows for depth-sensitive measurements. It is, however, no direct method, as the obtained signal is always an integral one with contributions from all depths. For back-calculation, a parameterization of the profiles or regularization approaches like in [9] are therefore needed.

A Varying The Implant Energy

Fluorescence intensities were calculated using a fundamental-parameter approach based on the Sherman equation. The determined spectral source flux of the LPS was taken into account, the profiles determined by the PTB [6] were approximated by Gaussian functions and then divided into homogeneous layers, see figure 4. For solid-angle calculations, the beam profile was projected onto the sample and shadowing effects by the detector collimation were taken into account.

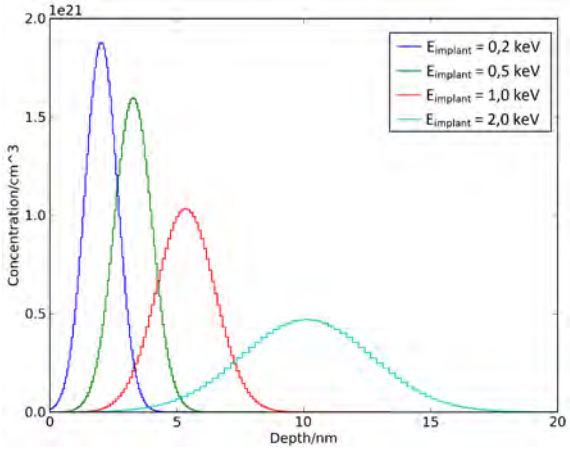


FIGURE 4. B implant profiles with varying implant energy according to the samples measured at the PTB [5] (blue - 0,2 keV, green - 0,5 keV, red - 1,0 keV, light blue - 2,0 keV)

The angular resolution of the detector is mainly determined by the size of the beam footprint on the sample and is smaller than 1.5° at 5° exit angle and smaller than 11° at 45° for the assumed 2 x 4 cm footprint. The calculated fluorescence intensities per sterad as a function of the exit angle are shown in figure 5. They show that it is possible to differentiate the shapes of the profiles from each other.

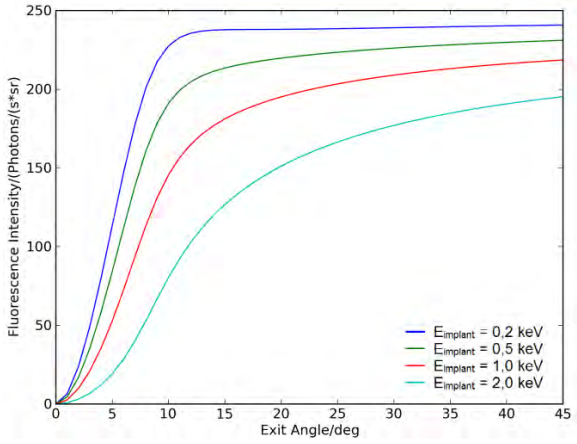


FIGURE 5. Calculated GE-XRF measurements

TU–16

Boron is a very challenging element for fluorescence analysis because of its low fluorescence yield (ω~7E-4 for the K-shell) and soft fluorescence radiation (183eV for Boron-K_α). Hence, the analysis of Boron profiles with the laboratory LPS is certainly pushing the limits. Compromises regarding angular resolution have to be made. Nevertheless the calculations are encouraging with respect to the differentiability of Boron profiles. The use of focusing optics in the respective wavelength region would be a possible way to shorten measuring times and enhance angular resolution.

OUTLOOK

Initial calculations demonstrate the high potential of the laboratory set-up to differentiate dopant profiles of Boron with varying depth. The principal suitability of this method for the analysis of an element as challenging as Boron rise expectations for other material systems. The laboratory set-up will establish new opportunities of analyzing dopant profiles or nanolayers such as ALD on novel substrate types. Therefore it will be possible to use this measurement method flexible and cost effective in the laboratory. Furthermore the set-up is expected to substantially contribute to measurements of materials for photovoltaic applications such as CIGSe.

REFERENCES

1. A. Delabie, S. Sioncke, J. Rip, S. Van Elshocht, M. Müller, B. Beckhoff and K. Pierloot, J. Vac. Sci. Technol. A**30**, 01A127 (2012)
2. P. Hönicke, Y. Kayser, B. Beckhoff, M.Müller, J. Cl. Dousse, J. Hoszowska, S. H. Nowka, *J. Anal. At. Spectrom.* **27**, 1432 (2012)
3. P. Hönicke, B. Beckhoff, M. Kolbe, D. Giubertoni, J. van den Berg, G. Pepponi, *Anal Bioanal Chem* **396**, 2825-2832 (2010)
4. I. Mantouvalou, R. Jung, J. Tuemmler, H. Legal, T. Bidu, H. Stiel, W. Malzer, B. Kanngießer and W. Sandner, *Rev. of Sc. Inst,* **82**, 066103 (2011)
5. F. Senf, U. Flechsig, F. Eggenstein, W. Gudat, R. Klein, H. Rabus, G. Ulm, *J. Synchrotron Rad.* **5**, No.3, 780-782 (1998)
6. B. Beckhoff, P. Hönicke, D. Giubertoni, G. Pepponi and M. Bersani, *AIP Conf. Proc.,* **1173**, 29-33 (2009)
7. T. Harada, K. Takahashi, H. Sakuma and A. Osyczka, *Applied Optics* **Vol. 38, No 13** (1999)
8. H.P. Urbach, P.K. De Bokx, *Phy.Rev. B,* **Vol. 53, No 7** (1996)
9. P.K. de Bokx, Chr. Kok, A. Bailleul, G. Wiener, H.P. Urbach, *Spectrocim. Acta B,* **52,** 829-840 (1997)

KEYWORDS

grazing incidence X-ray fluorescence analysis, grazing exit X-ray fluorescence analysis, laser- produced plasma-source

TU–17

LOCAL TUNNELING MEASUREMENTS OF *IN-SITU* GATED TOPOLOGICAL INSULATORS

Jeonghoon Ha[1,2,3], Niv Levy[1,2], Tong Zhang[1,2],
Young Kuk[3] and Joseph A. Stroscio[1]

[1]*Center for Nanoscale Science and Technology, NIST, Gaithersburg, MD 20899, USA*
[2]*Maryland NanoCenter, University of Maryland, College Park, MD 20742, USA*
[3]*Department of Physics and Astronomy, Seoul National University, Seoul, 151-747, Korea*

INTRODUCTION

Topological insulators (TIs) are a quantum phase of matter where the bulk interior is insulating and the surface states are metallic and are protected by time-reversal symmetry, meaning these highly conducting states cannot be removed by surface passivation if it does not break time-reversal symmetry. These protected surface states are helical Dirac fermions which are predicted to host many interesting quantum phenomena [1]. Angle resolved photoemission spectroscopy (ARPES) and scanning tunneling microscopy (STM) measurements confirmed the existence of these surface states and their helical spin structure [1]. However, in order to fully utilize the unique properties of these surface states, the Fermi level (E_F) needs to be close to the Dirac Point and tunable across it.

IN-SITU GATE TUNABLE TOPOLOGICAL INSULATOR THIN FILMS

Three-dimensional TIs (like Bi_2Se_3 and Sb_2Te_3) are usually heavily doped narrow gap semiconductors, with the Fermi level away from Dirac point. While bulk and surface chemical doping has been used to tune E_F , it is preferable to tune the carrier density using a gate induced electric field. The combination of local probe studies of the density of states using STM and a gate tunable TI device remains challenging, mostly due to the sensitivity of the TI materials to exposure to atmosphere. Unlike graphene, *ex-situ* fabrication and processing will significantly degrade the surfaces of TI materials, making them inaccessible to STM. To resolve this issue, we demonstrate the fabrication of gate-tunable 3D TI devices that are suitable for STM studies. In this presentation, we report results on atomically flat Bi_2Se_3 and Sb_2Te_3 films grown on $SrTiO_3$ substrates using Molecular Beam Epitaxy (MBE). $SrTiO_3$ has a very large dielectric constant of $\approx 10^4$ at 4 K, allowing tuning of the TI Dirac point and carrier density even with a relatively thick dielectric of 100 μm. The $SrTiO_3$ substrates were pre-patterned with platinum electrodes and mounted in specially designed sample holders as shown in figure 1, allowing us to *in-situ* control the carrier density with a back gate on *in-situ* grown TI films, avoiding any *ex-situ* post processing of the samples. As a result, we are able to continuously change the carrier density and observe the local electronic structure of pristine grown TI films using scanning tunneling spectroscopy (STS) techniques.

TU–17

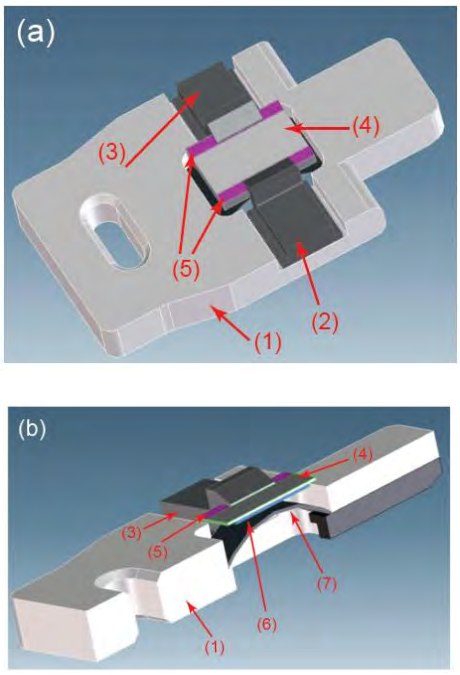


FIGURE 1. 3D computer-automated drawings of the high temperature sample holder with in situ back gating capability. (a) Top view. (b) Cross-sectional view. Part list: (1) alumina sample holder, (2) W source/drain electrode, (3) W source/drain electrode, (4) STO substrate, (5) Pt electrodes on $SrTiO_3$ for source/drain electrodes, (6) Pt back gate electrode on $SrTiO_3$, (7) W spring clip to hold $SrTiO_3$ which is also the back gate contact.

STM/STS OF GATE TUNABLE TI FILMS

Initial STM/STS measurements at a sample temperature of 5 K are focused on very thin films of 2 to 10 quintuple layers of TI films (figure 2). STS of the thin film's surface electronic structure allow us to study the gate's efficiency vs. local film thickness in a single sample. We find that the efficiency of gating the top surface state's electronic structure depends on the film thickness, with a decreasing efficiency for thicker films. In addition to simply shifting E_F, the electric field is capable of altering the surface band structure of TI ultrathin films, where the top and bottom surface states are coupled, and open a hybridized gap at the Dirac point [2]. We observe substantial differences in gating between Bi_2Se_3 and Sb_2Te_3 which will be discussed with models of the gating of carriers in the bottom and top surface states through the bulk films at different bulk carrier densities. In addition, standing wave scattering patterns of the TI surface state at terrace step edges are investigated as a function of gate voltage and step edge direction. We find that the wavelength of the standing waves varies with gate voltage due to the shift of the Dirac point with carrier density. The scattering intensity and the Fermi velocity vary with the gate voltage due to the change of carrier density and Dirac point. We will present these results and further measurements planned at ultra-low temperatures and high magnetic fields.

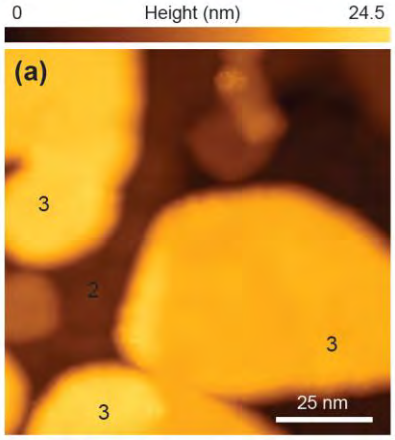


FIGURE 2. STM topographic image, 100 nm x 100 nm, of 3 QL Bi_2Se_3 film grown by MBE on the gated sample holder in Fig. 1. The layer numbers are indicated. Tunnel parameters: I=30 pA, V_B=1.5 V.

REFERENCES

[1] M. Z. Hasan and C. L. Kane, Rev. Mod. Phys. **82**, 3045 (2010).
[2] M. Kim, C. H. Kim, H.-S. Kim, and J. Ihm, PNAS **109**, 671 (2012).

KEYWORDS

Scanning Tunneling Microscopy, Scanning Tunneling Spectroscopy, Topological Insulator, Molecular Beam Epitaxy, Gate Effect, *in-situ* Gating

TU–18

COMPREHENSIVE CHARACTERIZATION AND UNDERSTANDING OF MICRO-POROUS LOW-K INTERCONNECTS USING PALS, EP AND XRR

D. Yang[1], R.L. Opila[1], G. Jiang[2], V. Pallem[2], D.W. Gidley[3] and N. Bhargava[4]

1. Department of Materials Science and Engineering, University of Delaware, Newark, DE 19716

2. Delaware Research & Technology Center, Air Liquide America, Newark, DE 19702

3. Department of Physics, University of Michigan, Ann Arbor, MI48109

4. Department of Electrical Engineering, University of Delaware, Newark, DE 19716

INTRODUCTION

As transistor density on integrated circuits doubles every 18 months as driven by Moore's Law[1], propagation delays from interconnections at the back-end-of-line (BEOL) have begun to dominate the overall delay. Low dielectric constant (k) materials, e.g. organosilicate glasses (SiCOH)[2], have been introduced to replace silicon oxide and decrease RC delay. In order to further decrease k, porosity is being introduced by deposition of hybrid films composed of a backbone skeleton matrix and a labile phase which will be removed to create pores[3].

However, while low k is realized by lowering density in terms of porosity incorporation, not only mechanical properties degrade[4], but pore interconnection resulting from high porosity also lead to serious problems in subsequent manufacturing processes, e.g. degrading adhesion, copper diffusion and photoresist poisoning[5]. Therefore, pore architecture characterization and understanding have become essential for high porosity low-k materials. However, due to the complexity of nano-scale pore architecture, each pore characterization technique has its advantages and limitations. In order to acquire complete understanding of porous low-k material structure, three different techniques are used; Ellipsometric porosimetry (EP), which provides information on open meso-pores accessible to organic solvents but may underestimate porosity without probing closed pores and pores smaller than the probing organic molecule[6]; Positron Annihilation Lifetime Spectroscopy (PALS), which probes the amount of free surface and is able to detect micropores but with some limitation on analyzing necking structure and therefore quasi-closed pores[7]; X-ray Reflectivity gives absolute overall porosity in terms of film density but few details on pore size distribution[8].

In this work, all three techniques will be used to characterize porous low-k films of various porosity and pore size distribution, results will be compared to each other and packed for a comprehensive understanding of pore structure. This study will provide valuable guidance for future porosity characterization, data comprehension, porosity understanding and further structural optimization of porous low-k materials.

TU–18

RESULTS AND DISCUSSION

Porous low dielectric thin film deposited on silicon wafers with dielectric constant k=2.0 and 2.2 are used to for characterization techniques comparison purpose and named sample A and B accordingly. Both samples A and B have been characterized by Ellipsometric Porosimetry (EP), Positron Annihilation Lifetime Spectroscopy (PALS) and will be measured by X-ray Reflectivity (XRR) for future work.

In EP, refractive index and thickness are recorded in-situ when stepwise increasing partial pressure of absorbent, toluene in this case as shown in Figure1. Sample A has 44% porosity compared to 25% of sample B. Higher porosity of sample A explains its lower dielectric constant at 2.0 compared to sample B at 2.2. In the desorption curve of sample A, a hysteresis which shows lower partial pressure is required for desorption respect to absorption indicates possible existence of necking structure in sample A. Pore size distribution derived from EP absorption and desorption isotherm are shown in Figure2. Sample A demonstrates a pore size of 1.9nm while smaller pores of 1.1nm shown in sample B. Overall, according to EP measurements, sample A of lower dielectric constant demonstrates higher porosity therefore larger pore size and possible necking structure compared to sample B which has lower porosity and therefore lower dielectric constant.

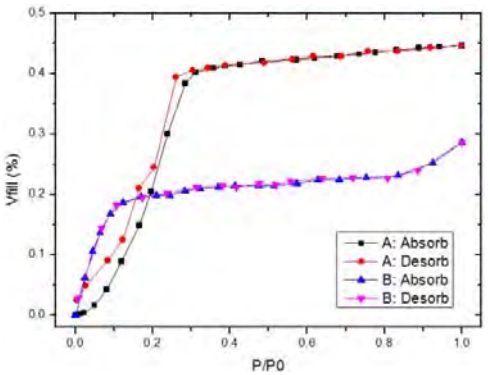


FIGURE 1. Absorption and desorption isotherms of porous dielectrics of sample A and B measured by EP

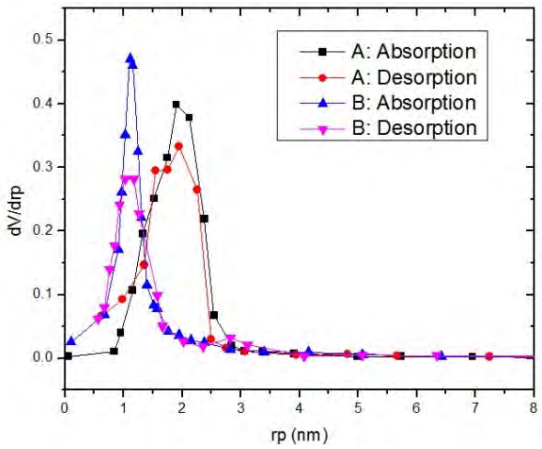


FIGURE 2. Absorption and Desorption Pore size distribution(PSD) of porous dielectrics of k=2.2 and 2.0 measured by EP

In PALS, sample A presents high Ps formation intensity with high porosity and the pores are fully percolated and mean free path length is 2.4nm while sample B presents a low intensity of positronium distributed in two distinct pore sizes (one micropore and one mesopore) and with no interconnection between the pores. PSD fitting of sample B is shown in Figure3 with bimodal distribution centered at 0.7nm and 2.3nm. Moreover, Sample B is also higher in density and the low Ps intensity and no pore interconnection indicate a rather low film porosity respect to sample A which has high Ps intensity annihilating in pores indicating high porosity.

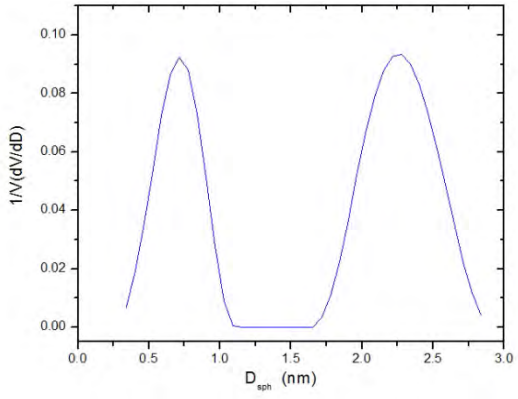


FIGURE 3. sample B: PALS bimodal PSD fitting

TU–18

Table 1 compares pore size derived from EP and PALS respectively. For sample A, pore size derived from these two techniques are in approximate agreement with slightly larger pore size from PALS than EP. In sample B, PALS probes two discrete pore distribution locates at 0.7nm and 2.3nm while EP only demonstrates one pore size at 1.1nm. The smaller pore is likely come from free space generated by dangling group from matrix and the large one may be generated by removing labile organic phase in post treatment. Since EP is a continuous in-situ measurement, e.g. pores of different sizes are filled simultaneously, the pore sized distribution is not able to resolve pores of similar sizes. Therefore the single PSD of samples B may contains contributions from both small and large pores, in other words, pore size measured by EP can be "effective" pore size which explains the discrepancy between PAL and EP in sample B. From the perspective of porosity, comparison of Ps annihilation intensity indicates a higher porosity from sample B than A which is consistent with EP results.

TABLE 1. Pore size of sample A and B measured by EP and PALS

Pore size/nm / k	EP: Absorption and Desorption	PALS
A:k=2.0	1.9/1.9	2.4
B: k=2.2	1.1/1.1	0.7 and 2.3

REFERENCES

1. Moore, B. G. E. Cramming more components onto integrated circuits. **38**, (1975).
2. Latrasse, L. *et al.* High deposition rates of uniform films in tetramethylsilane-based plasmas generated by elementary microwave sources in matrix configuration. *Surface and Coatings Technology* **203**, 2343–2349 (2009).
3. Grill, a. & Patel, V. Ultralow-k dielectrics prepared by plasma-enhanced chemical vapor deposition. *Applied Physics Letters* **79**, 803 (2001).
4. Hasaka, T. & Tnoue, M. First-Principle Molecular Model of PECVD SiQCH Film for the Mechanical and Dielectric Property Investigation. 66–68
5. Hoofman, R. *et al.* Challenges in the implementation of low-k dielectrics in the back-end of line. *Microelectronic Engineering* **80**, 337–344 (2005).
6. Leuven, B.- Ellipsometric Porosimetry of Porous Low-k Films with Quazi-Closed Cavities. *Materials Research* **812**, 5–10 (2004).
7. Gidley, D. W., Frieze, W. E., Dull, T. L., Sun, J. & Yee, A. F. Determination of pore-size distribution in low-dielectric thin films. **1282**, 4–7 (2012).
8. Plantier, L. *et al.* Ultra Low-κ Metrology Using X-Ray Reflectivity And Small-Angle X-Ray Scattering Techniques. *AIP Conference Proceedings* **931**, 347–351 (2007).

KEYWORDS

Micro-porous; Low-k Characterization; Positron Annihilation Lifetime Spectroscopy (PALS); Ellipsometric porosimetry (EP); X-Ray Reflectivity (XRR)

TU–19

Direct Analysis of Undiluted Photoresist with Inline Autodilution Inductively Coupled Plasma Mass Spectrometry

Hyun-Kee Hong[1], J. S. Lee[2], Austin Schultz[2], Paul Field[2] and Daniel Wiederin[2]

[*]Samsung Electronics Co. Ltd., San #5, Banwol-Dong, Hwasung City, Gyeonggi-Do, Korea 445-701
[2]Elemental Scientific, 1500 North 24th Street Omaha, NE 68110, U.S.A.

Abstract

Metal contaminants in photoresists used in semiconductor manufacturing processes can lead to defects and poor quality of final devices. Therefore, it is very important to adequately monitor levels of metal contaminants in photoresist in order to maintain product quality. Generally, these metal contaminants must be controlled at sub-ppb levels. The main elements of interest include Li, Na, Mg, Al, K, Ca, Ti, Cr, Mn, Fe, Ni, Cu, Zn, Sn and Pb [1]. However, as device dimensions shrink, it is expected that the permissible impurity levels will become correspondingly lower.

It can be said that most photoresist is currently analyzed by inductively coupled plasma mass spectrometry (ICPMS). The photoresist is usually diluted about 10 times by solvents before introduction to ICPMS, which is a time-consuming step due to the difficulty of accurately diluting viscous samples.

Solvents used for dilution include N-methyl-2-pyrrolidone (NMP), propylene glycol methyl ether acetate (PGMEA) and ethyl lactate. The diluted photoresist still contains high polymeric matrix and therefore, it can be difficult to maintain long-term stability of the ICPMS signal. Additionally, for prolonged analysis, clogging or polymer buildup in the sample introduction system is commonly found, requiring relatively frequent ICPMS maintenance.

This presentation discusses a fully automated method to analyze metal contaminants in undiluted photoresists using ICPMS and a new inline dilution system called prep*FAST*.

prep*FAST* is a fully-automated inline sample and standard autodilution system consisting of a syringe pump unit (S400V), an 8-port inline mixing valve and an autosampler. The sample is loaded from the autosampler into a loop on the valve. After the valve moves to the inject position, a syringe-driven solvent carrier stream pushes the sample out of the loop where it is mixed inline and in-valve with syringe-driven diluent and internal standard streams before introduction to the ICPMS nebulizer. The flow rates are precisely and variably controlled at rates between 1 and 500 µL min^{-1}. With prep*FAST* ICPMS, it is possible to introduce and analyze undiluted photoresist samples.

Because the samples are automatically diluted inline by the prescribed dilution factor, the difficult and contamination-prone off-line dilution step is avoided. The valve system also minimizes the amount of sample introduced to the ICPMS, improving long-term instrument stability. This real time dilution feature of prep*FAST* ICPMS reduces reagent consumption, lowers contamination risks, minimizes ICPMS maintenance and minimizes human exposure to hazardous chemicals. This

TU–19

presentation evaluates and discusses inline dilution and analysis of four photoresist-related chemicals in terms of linearity, precision, accuracy and stability.

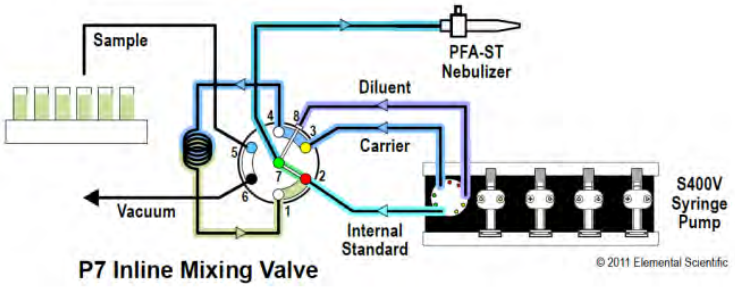


FIGURE 1. Schematic diagram of prep*FAST*, fully automated inline autodilution system.

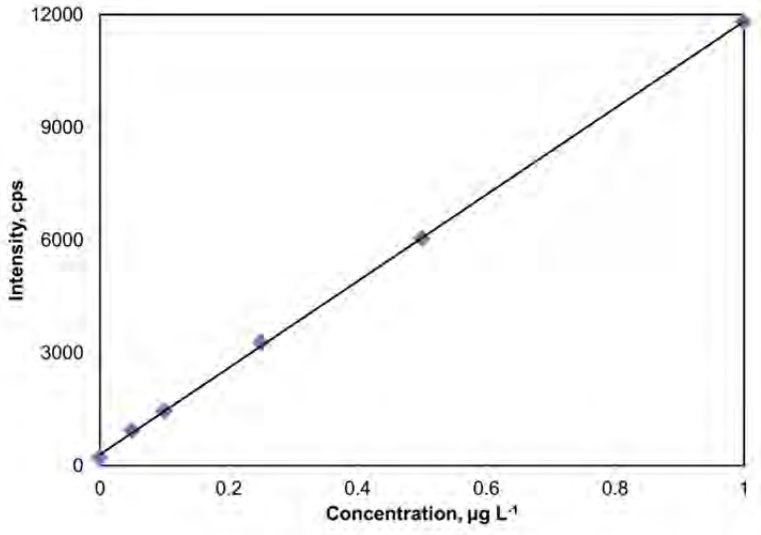


FIGURE 2. Six point addition calibration curve of Sn is automatically prepared in N-methyl-2-pyrrolidone (NMP) from a single 1 µg L^{-1} standard solution with ICPMS. The correlation coefficient of the curve is 0.99993.

References

1. D. Capitanio, Y. Mizuno and J. Leeca, *Proc. SPIE 3678, Advances in Resist Technology and Processing XVI,* 684 (June 11, 1999)

Keywords

photoresist, contaminants, inline, autodilution, prep*FAST*, ICPMS

TU–20

EXTRACTION OF INTERFACIAL DOPING DENSITY IN METAL/SILICON CONTACTS

Khaled Ahmed

Intermolecular, Inc.
3011 North First Street, San Jose, California 95134, USA

INTRODUCTION

The specific contact resistivity (ρ_C) has become very critical for scaling high performance/low power CMOS to 14nm node and beyond. An important parameter that is necessary to interpret the observed ρ_C reductions as function of process technology is the active doping density at the metal/silicon interface (N_D) after contact formation. In this work, we demonstrate a method for accurate determination of N_D using electrical measurements of: (1) Specific contact resistivity on heavily-doped silicon and (2) The Schottky barrier height (SBH) on lightly-doped silicon (ϕ_{B0}). The accuracy of the method is demonstrated on Silicide/*n*-Silicon contact systems.

HIGH DOPING EFFECTS

At a Schottky contact between a metal and a heavily-doped silicon the SBH, ϕ_B, is different from the intrinsic SBH, ϕ_{B0}, that is typically measured on lightly-doped silicon, due to two high doping effects: (1) image force barrier lowering (IFBL) [1,2], and (2) band-edge-tailing and impurity-band effects [3]. Prior models for current transport in metal/n^+-Si contacts have not or only partially included high doping effects. Padovani and Stratton [4] did not include any high doping effects. Guðmundsson included image force barrier lowering but ignored band-edge tailing and impurity-band effects [1]. Lou and Wu [3] included band-edge tailing and impurity-band effects, but ignored image force barrier lowering.

EXTRACTION METHOD

Once an accurate model for the ρ_C versus N_D at a given ϕ_{B0} is calculated, one can then use the measured ρ_C to accurately estimate the active doping density at the metal/silicon interface, with ϕ_{B0} measured independently using lightly-doped silicon [5]. The key then for accurate estimation of N_D is the accuracy of the $\rho_C(\phi_{B0}, N_D)$ model. In this work, an improved analytical model that includes both image force barrier lowering and band-edge tailing and impurity-band barrier enhancement is presented. This model is the basis of the extraction method presented in this work.

THE MODEL

IMAGE FORCE BARRIER LOWERING

At a Schottky contact between a metal and a heavily-doped silicon, an important phenomenon that will significantly affect the calculated ρ_C at given ϕ_{B0} and N_D is the image force barrier lowering (IFBL). IFBL dependence on bias was used by Sze *et al*. to extract the dielectric constant of silicon when N_D and ϕ_{B0} are known [2]. IFBL is given by [2]:

$$\delta\phi_{B1} \approx -\left[\frac{q^3 N_D(\phi_{B0} - \xi - V - kT/q)}{8\pi^2\varepsilon^3}\right]^{\frac{1}{4}} \qquad (1)$$

TU–20

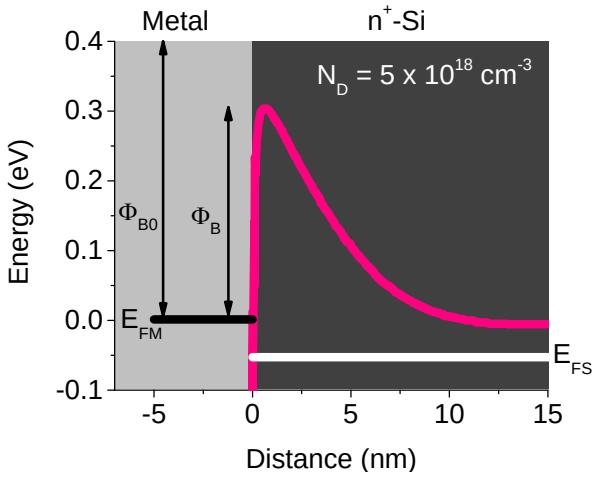


FIGURE. 1. Modeled energy band diagram for a metal/n⁺-Si contact with $\phi_{B0} = 0.4$ eV and $N_D = 5 \times 10^{18}$cm^{-3} at an applied reverse bias of $V = 0.05$ V. Image force barrier lowering is shown [1]. In this case, the barrier height is lowered by ~100mV compared to the intrinsic value of 0.4 eV.

BAND EDGE TAILING & IMPURITY BAND

As N_D increases, the electron population considering only the "parabolic band" accumulates in an energy regime that is higher than that considering the band-edge-tailing and impurity-band. The electrons located in the higher energy regime will have higher transmission probability during the tunneling process, and hence a higher tunneling current (i.e. lower ρ_C). In other words, models that do not include band-edge-tailing and impurity-band effects will underestimate ρ_C for a given ϕ_{B0} and N_D. This was shown numerically by Lou and Wu [3]. For the purpose of compact modeling, it is proposed here that the effects of band-edge tailing and impurity-band may be incorporated through a positive "shift" in the barrier height:

$$\delta\phi_{B2} \approx +c_0 \times e^{c_1 N_D} \tag{2}$$

Where $c_0 \approx 4 \times 10^{-3}$eV and $c_1 \approx 0.1303$ cm^3 for $N_D \geq 3 \times 10^{19}$cm^{-3}. These values were empirically derived from the numerical calculations performed by Lou and Wu [3]. This simple semi-empirical equation both captures the physics of band-edge tailing and impurity-band effects and enables compact modeling of ρ_C as function of ϕ_{B0} and N_D.

We base our model on the metal/n⁺-Si compact current transport model by Padovani and Stratton [4].

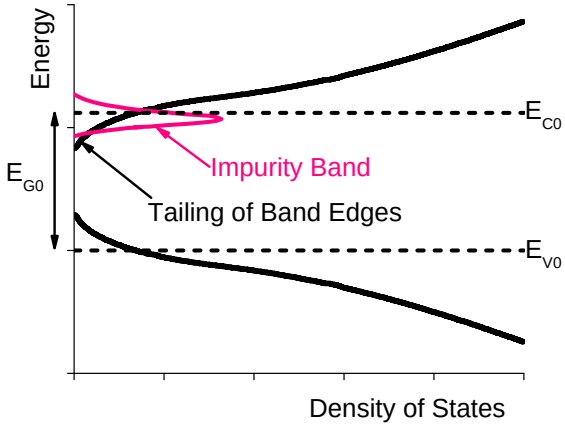


FIGURE. 2. A schematic diagram of the density of states for n⁺-Si at N_D. Impurity bands and tailing of band edges are formed. Electrons located in the lower energy regime (introduced by band-edge tailing and impurity band) will have lower transmission probability during the tunneling process (compared to parabolic band case), and hence a lower tunneling current (i.e. higher ρ_C).

In this work, it is proposed that the barrier height is adjusted using two terms: $\delta\phi_{B1}$ and $\delta\phi_{B2}$ so that

$$\phi_B \approx \phi_{B0} + \delta\phi_{B1} + \delta\phi_{B2} \tag{3}$$

The specific contact resistivity is given by the following compact model equations:

$300 < T_0$

$$J = \frac{A\, e^{-b_1}}{(c_1 kT)^2} \frac{\pi c_1 kT}{sin(\pi c_1 kT)} [1 - e^{-c_1 V}] \tag{4.a}$$

$300 \geq T_0$

$$J = \frac{A\sqrt{\pi E_{00}(\phi_B - V - \xi)}}{kT\, cosh\left(\frac{E_{00}}{kT}\right)} e^{\left(\frac{\xi}{kT} - \frac{\phi_B + \xi}{E_0}\right)} e^{\frac{V}{E_0}} \tag{4.b}$$

$$A \equiv 4 \times 4\pi m_{\parallel} q \frac{(kT)^2}{h^3} \quad \begin{matrix} T_0 \\ \equiv \left(k(c_1 + \sqrt{2f_1})\right)^{-1} \end{matrix} \tag{5}$$

$$E_{00} = \frac{qh\sqrt{\frac{N_D}{2\varepsilon}}}{\pi\sqrt{2m^*}} \qquad E_0 = E_{00} coth\left(\frac{E_{00}}{kT}\right) \tag{6}$$

$$b_1 = \frac{\Phi_B - V}{E_{00}} \qquad c_1 = \frac{ln\left(\frac{4(\phi_B - V)}{\xi}\right)}{2E_{00}} \tag{7}$$

$$f_1 = \frac{1}{4} E_{00} \xi \qquad \xi = E_F - E_C \tag{8}$$

$$\rho_C \equiv \frac{V}{J} \qquad 0 \leq V \leq 0.05 \tag{9}$$

TU–20

MODEL RESULTS

The system of equations (1) to (9) is used to model ρ_C at a given N_D and ϕ_{B0}. Figure 3 shows modeled ρ_C versus N_D for $\phi_{B0} = 0.6$ eV(as a way of example) using different levels of approximations. The modeled specific contact resistivity including both high doping effects is shown in Curve (b). When ρ_C and ϕ_{B0} are measured using heavily-doped and lightly-doped silicon substrates, respectively, one can estimate the active doping density at the metal/silicon interface.

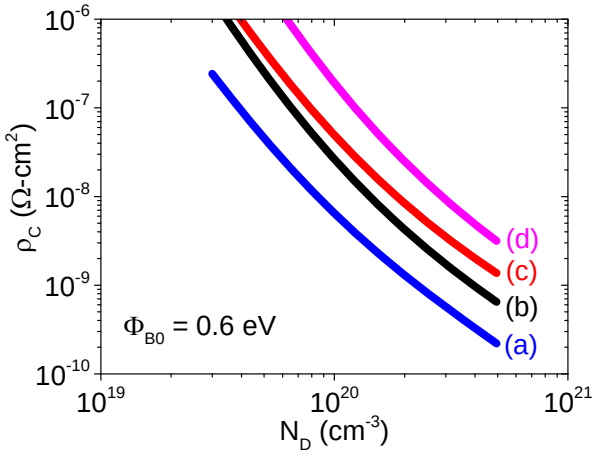


FIGURE 3. Modeled ρ_C vs. N_D with different model approximations: (d) only band-edge tailing and impurity band effects, (c) no high doping effects, (b) both high doping effects, and (a) only image-force barrier lowering effect. $m^* = 0.19\, m_o$. When ϕ_{B0} is measured using Richardson's plot on lightly-doped n⁻-Si, and ρ_C is measured using CBKR structure on n⁺-Si [7,8], one can estimate the doping density at the metal/silicon interface using curve (b).

APPLICATION

The method presented above is applied to the data published recently by Kenny *et al.* [6] for various Sb implant doses in Silicide/n⁺-Si contacts. The results are shown in Figure 4. Clearly, the extracted interfacial active doping density tracks the implanted Sb dose, as expected.

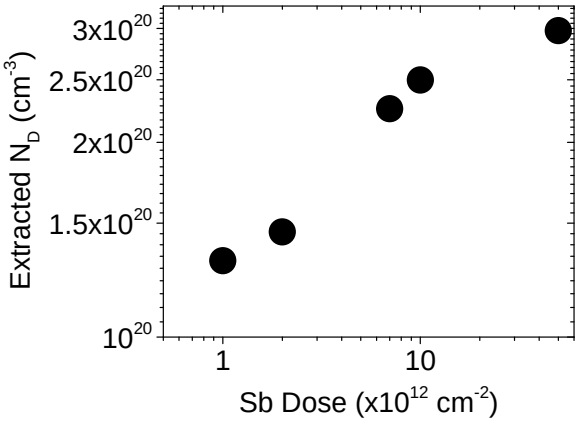


FIGURE 4. Extracted a active doping density from silicide/n⁺-Si contacts experimental data published by Kenny *et al.* [6]. The extracted N_D tracks the Sb implanted dose as expected.

REFERENCES

1. V. Guðmundsson, PhD Thesis, KTH Royal Institute of Technology, Sweden, 2011.
2. S. M. Sze *et al.*, JAP, vol. 35, no. 8, p. 2534, 1964.
3. Y-S. Lou and C-Y. Wu, SSE, p. 163, 1995.
4. F. Padovani and R. Stratton, SSE, p. 695, 1966.
5. C. Kenney *et al.*, IEEE Transactions on Electron Devices, vol. 58, no. 8, p. 2423, 2011.
6. C. R. Kenny et al., p. 17, VLSI Technology Symposium Technical Digest 2012.
7. K. Ohuchi *et al.*, Jap. Journal of Applied Physics, vol. 50, p. 04DA03, 2011.
8. H-N. Lin et al., p. 102, VLSI Technology Symposium Technical Digest, 2009.

KEYWORDS

Schottky contact, Specific contact resistivity, contact resistance, CBKR, active doping, extraction.

TU–21

SUB-SURFACE METROLOGY USING X-RAY EMITTING AFM PROBES

Faisal K. Chowdhury, H. Pourzand and M. Tabib-Azar

Dept. of Electrical and Computer Engineering, University of Utah
Salt Lake City, UT, USA, 84112

INTRODUCTION

Atomic Force Microscopy (AFM) is extensively used to study material surfaces with very high spatial resolution. In its simplest form, AFM produces topography maps but it can also be used to provide a wide range of information and images regarding surface conductivity, electrochemical activity, magnetic domains, ferroelectric activity, thermal conductivity, etc. Although AFM can produce sub-surface information by using microwave or spreading current/potential imaging, its resolution in these techniques is usually around 10 nm. The main purpose of this work is to add X-ray imaging capabilities to AFM to enable very high spatial resolution imaging of materials with better than 0.1 nm resolution.

There are various ways to add X-ray imaging capabilities to the AFM system. In its simplest form, the X-ray source can be integrated with the AFM probe and the X-ray detector can be situated under the sample. The detector converts the transmitted X-rays through the sample to electrical signals that can be input to the AFM control system to produce X-ray images concurrently with the AFM topography images. This was the first approach we selected and used irradiation of AFM probes in a nuclear reactor to convert them into an X-ray source.

One can also use the AFM probe to scatter X-rays toward the sample instead of using the AFM probe as the X-ray source. In this approach, a separate X-ray source is used to controllably (intensity and photon-energy) produce X-rays. We also explored this approach but the first approach was simpler and readily produced good X-ray images. The second approach is still being developed.

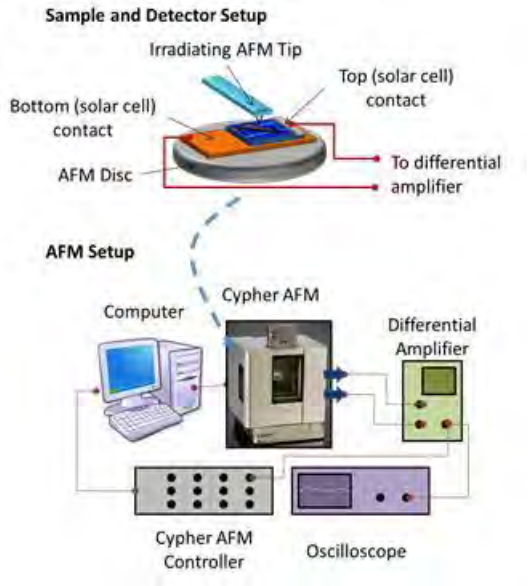


FIGURE 1: Experimental setup for X-ray AFM probe and Cypher AFM system coupled to differential amplifier and computer.

X-Ray Emitting-Tip Experiment

We present a unique local probe microscopy technique using an X-ray source on an AFM probe to study the interface between dentin and epoxy filler. X-rays have been used in medicine (absorption by heavy Ca atoms), material inspection (to detect cracks and non-uniformities), crystallography using x-ray diffraction (XRD) and chemical identification through X-ray fluorescence (XRF) [1,2]. In all these applications either diffraction patterns generated by the interaction between X-rays and crystal structure or X-ray

TU–21

absorption or fluorescence are used. The ability to scan a low intensity X-ray source very close to a sample to directly map its internal structures with nanometer spatial resolution constitutes the motivation for the present work.

Although it is possible to directly integrate cathode-ray X-ray generation sources on an AFM probe, the first method uses nuclear irradiation to convert regular silicon AFM probes with chromium coating in to a localized X-ray source. The AFM tips were mounted carefully in a holder and transferred into the nuclear reactor facility (TRIGA) at the University of Utah. The tips were exposed to ionizing radiation and nuclear species for approximately 30mins at 90kW. Typical neutron flux was ~$3x10^{12}$ neutrons/cm^2-sec at the core. The energy range of the neutrons varied from 0.025 eV to 10 MeV, but most of them had neutron energies less than 1 MeV. In general, alpha particles do not exist in the reactor core except for inside the fuel element which has an average energy of 6 MeV. It is known that Gamma rays exist ubiquitously in the reactor core. Approximate gamma flux at the AFM probes was on order of 10^{13} gamma/cm^2-sec (or higher). Gamma particles' energy ranged from approximately several keV to 3 MeV. Beta particles' flux at 90 kW was approximately 10^{13} beta/cm^2-sec and typical energy of a beta particle was between 100 keV ~1500 keV.

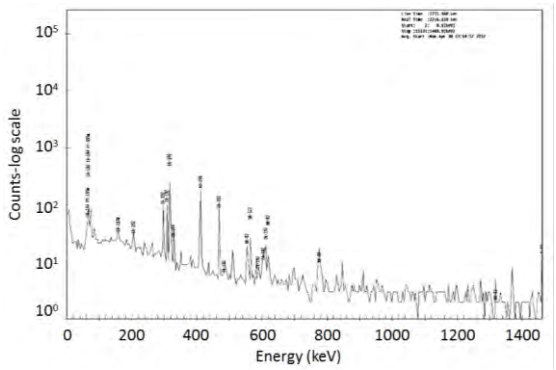


Figure 2: X-ray emission spectrum of the irradiated AFM probe.

Next, we converted a silicon solar cell to an X-ray detector by completely covering it with an opaque non-conducing tape and mounted the detector in a Cypher AFM system (figure 1). The output of the X-ray detector was coupled to a differential amplifier that was AC coupled and amplified voltage changes in the 0.1Hz to 0.1MHz frequency range. The output of the differential amplifier was coupled to the input of the Cypher AFM system via its Analog I/O such that real time voltage fluctuations could be plotted while the X-ray AFM tip scanned across the topology of the sample that was mounted over the X-ray detector on the AFM's sample holder.

Figures 3 and 4, respectively, show the contact-mode image along with the X-ray signal map of the dentin-epoxy sample that was simultaneously obtained. The AFM image is used to register the X-ray map with topographical features on the sample. It appears that the X-rays were diffracted along the interfacial plane that are nearly perpendicular to the sample's surface and produced a relative large signal at the detector. These glazing X-rays reveal detailed map of the dentin-epoxy interface and can be used to quantitatively map the density variations in the transition region of importance in developing strong epoxy filling in dentistry.

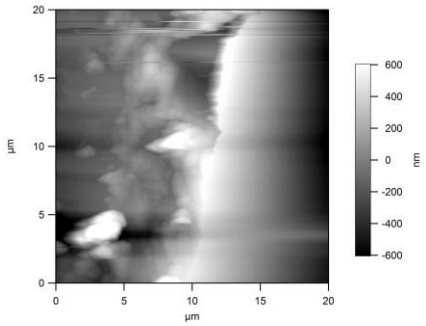


FIGURE 3: Contact AFM topography image of the dentin epoxy sample.

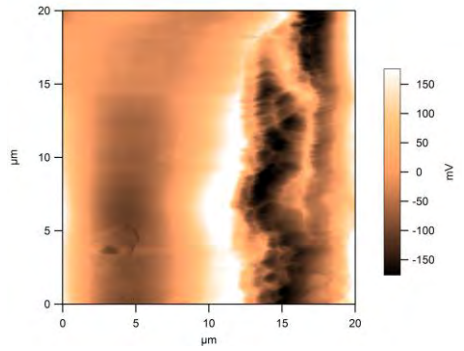


FIGURE 4: Voltage map generated by X-ray detector (solar-cell) output after AFM scan over dentine-epoxy region exposing sub-surface details

Figure 4 contains SEM images of the dentine surface on the location that was interrogated with this system. We are currently in the process of integrating a variable intensity/energy X-ray source

TU–21

on the AFM probe to enable multi-spectral X-ray scanning of materials.

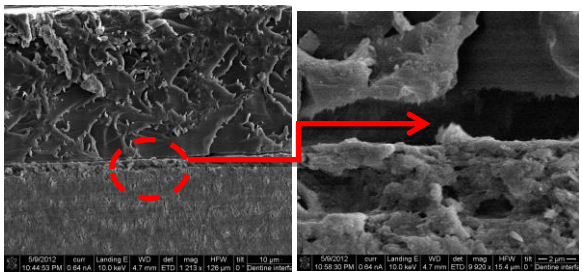


FIGURE 5*:* SEM Image of region that was interrogated by the AFM-Xray system.

External X-ray Source

In order to incorporate X-ray in the AFM setup an AFM tip can be made to radiate or reflect the X-ray and detect the transmission through a sample using a detector underneath it. Another method would be to radiate the sample with X-ray from below and sense the transmitted X-radiation using a small detector on the AFM cantilever. The detector or the X-ray source should be small so that it can reach high resolution subsurface metrology and link the change in transmitted X-ray signal to subsurface density characteristic of each point. However, the latter, is a challenging task and will be considered in future publications. The former method uses X-ray cathode ray tubes that are generally used in spectroscopy because of its simplicity. In this method the X-ray is generated by an external source and is modulated by the AFM tip. The modulated & reflected X-ray is passed through the sample and recorded by an x-ray detector. The output is passed through a pass band filter, an amplifier and lock-in amplifier to detect the signal.

The band-pass filter should be set so that it passes the cantilever resonance frequency. Reference of the lock-In amplifier should also be the driving frequency of cantilever Piezoelectric transducer. A result typical of such a setup is shown in figure 6 where a macro-scale equivalent of AFM tip coupled to external x-ray source was setup. The plot indicates a clear change in detectable voltage when x-rays are blocked by the Copper substrate. Similar sub-surface density versus location plots can be obtained using the technique presented here.

CONCLUSIONS

Two methods are investigated to incorporate x-ray based sub-surface metrology using AFM. In the first method AFM probes were put into a nuclear reactor to study the interface between dentin and epoxy filler. In the second method an external source of x-ray was used and the reflected and modulated signal was detected by the sensor. Both methods will be studied further to increase the AFM device capabilities substantially in sub surface analysis of the samples.

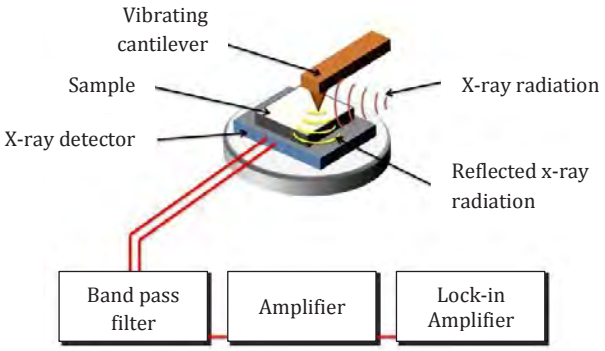


FIGURE 6*:* Schematic of the X-ray-AFM setup

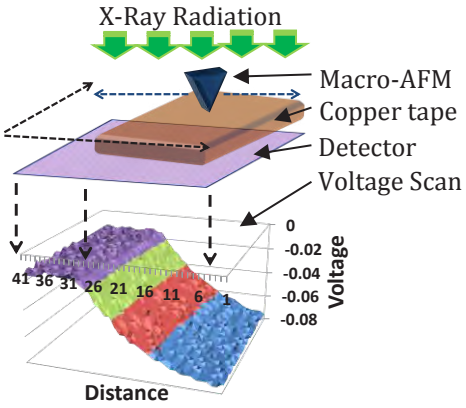


FIGURE 7*:* Results of macro-scale AFM-X-ray surface scan over Cu tape.

References

1. H. Roehrig, et al., "Photoelectronic Imaging for Radiology", *IEEE Transactions on Nuclear Science*, vol. 28, 1981, pp. 189-204
2. R. Kovacs, "X-ray inspection systems and applications", *International Spring Seminar on Challenges of Electronics Technology Progress*, 2004.27th, 2004, vol.1. pp. 14-19.

Keywords

Sub-surface metrology, X-ray atomic force microscopy X-ray AFM, near-field X-ray

TU–22

WORK FUNCTION CHARACTERIZATION OF $Si_{1-x}Ge_x$ HETEROSTRUCTURE USING KELVIN FORCE MICROSCOPY AND ELECTRON SPECTROSCOPY

Sylvain Pouch, Nicolas Chevalier, Denis Mariolle, Eugenie Martinez, Pradeep Kumar, Olivier Renault, Julien Morin, Jean-Michel Hartmann, Łukasz Borowik

CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France.

INTRODUCTION

SiGe/Si heterostructures are intensively used in order to boost the performances of ultra-short gate length complementary metal-oxide semiconductor (CMOS) devices [1-4]. For instance, intrinsic SiGe channels can be used to tune the threshold voltage and significantly increase holes mobility in p-type metal-oxide- semiconductor field-effect transistors (MOSFETs).

Kelvin force microscopy (KFM) and electronic microscopy like photo emission electron microscopy (PEEM) or scanning Auger microscopy (SAM), provide coupled information on local work function together with surface topography or chemical composition.

In this paper, we evaluate the work function variation of $Si_{1-x}Ge_x$ sample in function of the germanium concentration.

EXPERIMENTAL SECTION

We first describe the characteristics of the sample studied in this paper, and then we define measurement conditions and settings of two principal techniques: KFM and electron spectroscopy. The following study will highlight their ability to provide an accurate measurement of the local work function.

$Si_{1-x}Ge_x$ HETEROSTRUCTURE

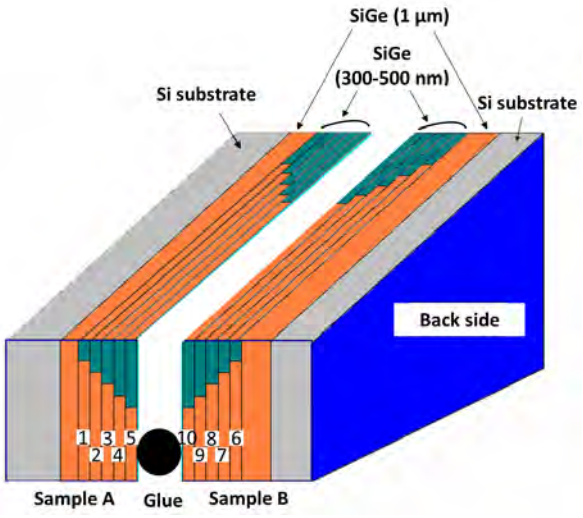


FIGURE 1. Theoretical disposition of the SiGe sample. The ten indicated layers have a gradual Ge percentage increasing of about 6% between each layer.

Epitaxial heterostructures consisting in stacks of 300-500 nm thick SiGe layers with increasing Ge concentration from 6% to 49% were used as reference samples. An Epi Centura Reduced

TU–22

Pressure – Chemical Vapor Deposition industrial cluster tool from Applied Materials was used to grow at high temperatures the SiGe multilayers on a p-type boron doped [~7-10 Ω·cm] (001) oriented Si substrates. The fabrication process has been described elsewhere [5]. The Ge concentrations were quantified by X-ray diffraction (XRD) measurements with the protocol described in Ref. [6].

Figure 1 shows a diagram of the SiGe/Si heterostructures. In order to prevent eventual edge artifacts on the measurement, two samples are glued in front of each other. In this experiment we use two samples with different Ge concentration (Sample A: from 6% to 29%, Sample B: from 34% to 49%). The sample is then polished using a Gatan Centar mechanical polishing machine. Finally, the surface is cleaned with diluted (1%) hydrofluoric acid to remove native Si and Ge oxides.

Kelvin Force Microscopy

The KFM Measurements have been performed with Bruker Dimension 3100 AFM using a NanoSensors PPP EFM tip (k~2N/m). KFM is one of the techniques used to detect the contact potential difference (CPD). In KFM, an electrostatic excitation (dc+ac voltage) is applied to the tip at the cantilever resonance frequency. The electrostatic excitation generates a cantilever oscillation (or resonance frequency shift) if the cantilever DC bias does not match the sample CPD. To measure CPD, a DC bias feedback is introduced so as to nullify the cantilever oscillation amplitude (or frequency shift) at the electrostatic excitation angular frequency. This generates a map of CPD. During the experiments, both amplitude modulation mode (AM) and frequency modulation mode (FM) are used [7]. Moreover, the single–pass and double-pass methods are employed. The CPD is directly related to work function (see [7] for further information).

Electron Spectroscopy

Electron spectroscopy analysis has been performed using a PHI-700 Xi Auger nanoprobe system equipped with a co-axial cylindrical mirror analyzer (CMA) with energy resolution varying from 0.1 to 0.5%. The measurements were carried out with an electron beam voltage from 10 to 20 keV and current from 5 to 10 nA [~(8-22) nm spot size]. This technique is based on the acquisition of the emission threshold of secondary electrons which is directly related to the work function [8]. The difference of threshold energy can be extracted for different localizations on sample surface. Then, energy difference is used to obtain a relative work function between the localizations. Measurements of characteristic Auger lines (C KLL, Si KLL and Ge LMM) is done at the same time. Consequently, this method gives information about work function and elementary chemical composition.

Results And Discussion

Here we compare results of KFM and electron spectroscopy, and discuss about the capabilities of each technique. The relevant value is the work function step between two layers of SiGe material with different Ge ratio. Thanks to the work of R. Ferguson [9], we can theoretically estimate that a 6% [Ge] step will induce about 25 meV of work function difference in the bulk. We will demonstrate that our instruments are able to detect such a tiny move.

KPFM Measurements

Here we present KFM results obtained under ambient conditions (Figure 2). The several layers with different Ge percentages can be distinguished.

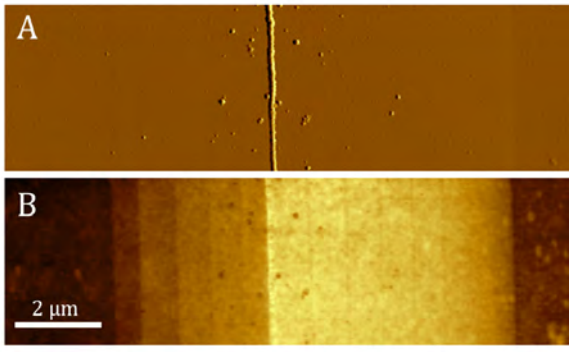


FIGURE 2. (A) Derivative height signal showing flatness of SiGe sample, except for the glue used to paste samples; (B) CPD image with of the SiGe layers (z scale 200 mV).

TU–22

A step of ~35 meV is measured between each layer. The difference between theoretical value and measured value can be induced by the surface states. To avoid surface contamination, coupled KFM and PEEM characterizations are scheduled in ultra-high vacuum (UHV) (10^{-10} mbar). A UHV suitcase is used to transfer the sample between both microscopes and prevent oxidation and contamination under air exposure.

Electron Spectroscopy Measurements

In this part we present an improved protocol of the former SAM work function measurement [8]. A stack of emission curves is obtained (see Figure 3) by analyzing each SiGe layer successively. Then, the difference of threshold energy is extracted for each step to obtain a measurement of work function difference between these layers.

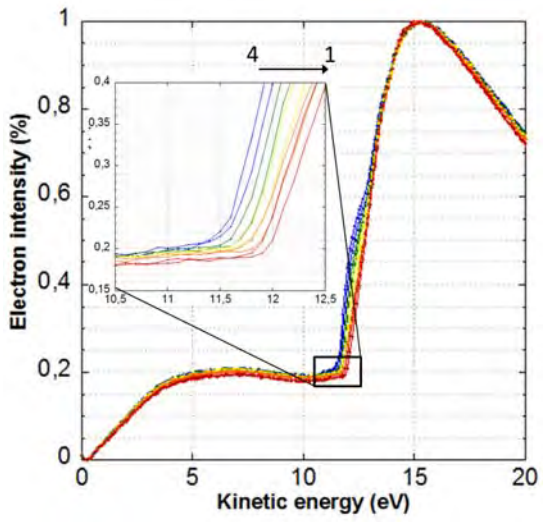


FIGURE 3. Characterization of emission thresholds made from layer four to one. Zoom is showing a constant energy shift between each SeGe layer.

Here we found about 40 meV of work function difference between two SiGe layers. This value is quite similar to KFM. The advantage of this technique is the fact that we can also determine the chemical composition by Auger measurements, which brings complementary information to the work function.

Conclusion

This work presents a comparative study of SiGe heterostructures using two characterization techniques. The work function can be measured by very different ways with advantages and disadvantages specific to each method. The KPFM provide important information on topography, but is also very dependent on this topography, which can bring artifacts. PEEM and SAM measurements can also analyze the chemical composition, but are sensible to charging effects on some materials.

As perspective, additional KFM and PEEM measurement are scheduled. By crossing information of three instruments we might be able to establish a model of the physical properties of SiGe, as a function of its Ge ratio.

This work was supported by the French "Recherche Technologique de Base" Program. The measurements were performed on the CEA Minatec Nanocharacterization Platform (PFNC).

References

1. Mizuno T. et al., 2003 *IEEE Trans. Electron Devices* **50** 988.
2. Packan P. et al., Proceedings of the 2009 IEDM Conference, p. 659.
3. Le Royer C. et al., 2011 *Solid State Electronics* **65-66** 9.
4. Le Royer C. et al., Proceedings of the 2011 IEDM Conference, p. 391.
5. Hartmann J M. et al., 2006 *ECS Transactions* **3** 219.
6. Destefanis V. et al., 2009 *J. Cryst. Growth* **311** 1070.
7. Sadewasser S. et al., 2011 Kelvin Probe Force Microscopy: Measuring and Compensating Electrostatic Forces, *Springer*, Heidelberg, Dordrecht, London, New York.
8. Baschmann G. et al. *1987 Fresenius J. Analytical Chemistry* **329** 195-200.
9. Ferguson R. 2002 *J. Vac. Sci. Technol. B,* **20**, 2133.

Keywords

SiGe, KFM, PEEM, SEM, Auger, Work Function

TU–23

MEASUREMENT UNCERTAINTIES IN MEMS KINEMATICS BY SUPER-RESOLUTION FLUORESCENCE MICROSCOPY [1]

Craig D. McGray, Samuel M. Stavis, and Jon Geist

The authors are with the National Institute of Standards and Technology in Gaithersburg, MD 20899.

INTRODUCTION

Microelectromechanical systems (MEMS) have characteristic structural dimensions best measured in micrometers, but often exhibit nanoscale motions that are critical to system performance. Super-resolution fluorescence microscopy [2, 3] has been used to characterize the nanoscale kinematics of a standard MEMS actuator [4, 5]. Fluorescent nanoparticles are deposited onto the MEMS device, providing a constellation of near-ideal point sources of light, as shown in Figure 1. The constellation is imaged with a widefield epifluorescence microscope. If the size of a fluorescent nanoparticle is beneath the Rayleigh resolution of the microscope, then the image of the nanoparticle will appear as the point spread function of the microscope. In the case of ideal optics this image would be an Airy pattern. The Airy function is well-approximated by a Gaussian function, and so the center position of the point spread function is calculated by nonlinear regression to a Gaussian. Translations and rotations of the MEMS device are measured by computing the rigid transform that best maps the calculated positions of the point sources in the constellation between each pair of consecutive images.

The standard uncertainties of such measurements can be determined empirically by experimental tests. Estimates of the uncertainty achievable under ideal circumstances, known as the *localization precision* [6], can also be predicted theoretically. The difference between the experimentally tested measurement uncertainty and the theoretically predicted localization precision provides an assessment of the errors due to non-idealities in the experimental setup and indicates the improvement achievable from refinement of the measurement technique.

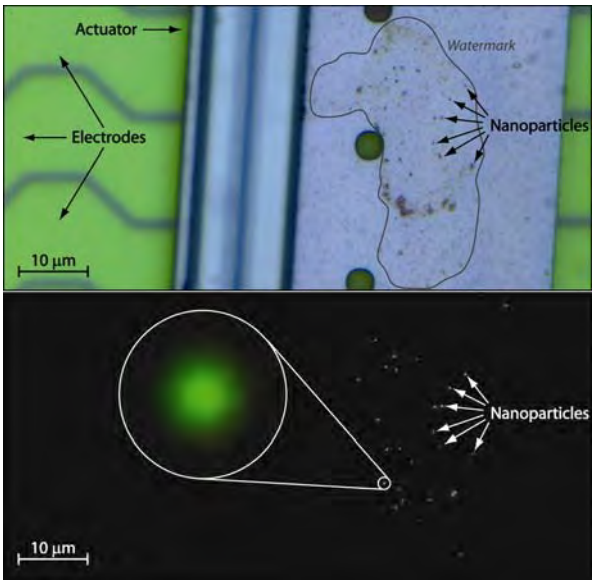


FIGURE 1. A constellation of fluorescent nanoparticles deposited on a canonical MEMS actuator. **Top:** A brightfield micrograph shows the structure of the actuator. The nanoparticles are barely visible. **Bottom:** A fluorescence micrograph shows the nanoparticles with high contrast. The image of each nanoparticle closely resembles a two-dimensional Gaussian function.

TU–23

EXPERIMENTAL TESTS

Experimental tests were conducted on a MEMS scratch drive actuator [7, 8] labeled with a constellation of 10 fluorescent polystyrene nanoparticles, each having a diameter of approximately 200 nm [4]. The actuator was operated for a single duty cycle and then stopped. While the actuator was immobile, two sequential fluorescence micrographs were captured on a charge-coupled device (CCD) digital camera and were stored for subsequent analysis. This procedure of a single actuator step followed by two images was repeated 150 times for a total of 300 images. The position of each nanoparticle within the orthogonal (x, y) coordinate frame of the image was determined by Gaussian estimation, and the centroid of the nanoparticle constellation in each image was calculated. Each pair of sequential images that were separated in time by an actuator step provided a measurement of the actuator step size. Each pair of sequential images that were not separated in time by a step of the actuator provided a sample of the measurement noise. Time series data on the actuator step size and the empirical measurement noise are plotted in Figure 2.

The pair of images following each actuator step provides two independent samples from the population of possible observed positions for each coordinate of the centroid of the nanoparticle constellation. The mean and standard deviation can be extracted from the sample pair. From the set of 150 collected sample pairs, a pooled standard deviation of the measurement [9] can be extracted for the x coordinate and another for the y coordinate. These pooled standard deviations describe statistical x-axis and y-axis uncertainties of the centroid position measurement. The standard uncertainty of the centroid displacement measurement is therefore the sum in quadrature of uncertainties from four independent measurements: two x-axis position measurements and two y-axis position measurements. The standard uncertainty of the x-axis position was found to be 0.91 nm, while the standard uncertainty of the y-axis position was 0.94 nm. The *combined standard uncertainty* [9] of the displacement measurement was therefore 1.85 nm. Similarly, a pooled standard deviation of the orientation of the constellation can be used to calculate the standard uncertainty of the stepwise rotation. The standard uncertainty of orientation was found to be 70.7 μrad, and the combined standard uncertainty of the stepwise rotation measurement was 100 μrad.

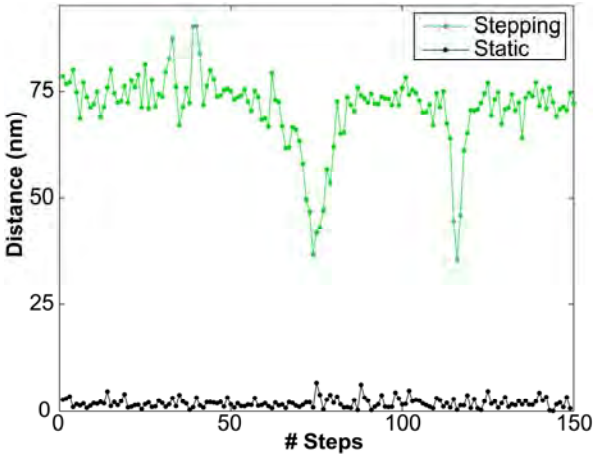


FIGURE 2. Time-series data for the position of a scratch drive actuator. Green data points represent the distance traveled in a single step of the actuator, while black data points represent the motion of the actuator measured between two frames when it was not stepping. The latter measurements are used to calculate empirical uncertainties.

THEORETICAL PREDICTIONS

In contrast to the empirically-determined uncertainties described above, the calculated localization precision reflects the displacement measurement uncertainty that is theoretically achievable with super-resolution fluorescence microscopy, given certain assumptions about the instrumentation. In this idealized model, the measurement uncertainty is limited by the total number of detected photons that form the image of a fluorescent nanoparticle, the number of detected background photons per pixel, the point spread function of the microscope, and the magnified sampling pitch of the CCD detector.

The localization precision of the position of a fluorescent nanoparticle is expressed as follows [6]:

TU–23

$$L_P = \sqrt{\frac{16\left(\sigma^2 + a^2/12\right)}{9N} + \frac{8\pi b^2\left(\sigma^2 + a^2/12\right)}{a^2 N^2}}$$

Where σ is the standard deviation of the gaussian approximation of the point spread function, a is the sampling pitch of the CCD detector, b^2 is the expected number of background photons per pixel, and *N* is the total number of detected photons.

The optical system described in this paper had a fitted gaussian standard deviation of $\sigma = 160$ nm and a green channel sampling pitch of $a = 46.82$ nm after accounting for the Bayer filter pattern of the color CCD camera. The total number of detected photons *N* can be calculated from the detected signal intensity by the following expression:

$$N = \left(I_S - I_B\right)\left(\frac{C}{G_A \cdot G_{EM} \cdot E_Q}\right) = \left(I_S - I_B\right)P$$

where I_S is the intensity of the detected signal, I_B is the background (*i.e.* dark) signal of the CCD sensor, G_A is the analog gain, G_{EM} is the electron multiplier gain, E_Q is the quantum efficiency, C is a constant conversion factor of the camera, and P is a constant that combines the various optoelectronic properties of the camera.

The color CCD camera used in [4] was calibrated against a monochrome CCD camera having a gain of 1, a quantum efficiency of 0.92 over the range of emission wavelengths measured, and a conversion factor of 5.8, as specified by the manufacturer, yielding an optoelectronic constant of 6.3043. To perform this calibration, fluorescent nanoparticles were imaged with both cameras under nearly identical radiometric conditions such as photon collection geometry and optics, excitation intensities, and exposure times. The total measured intensity of each nanoparticle was calculated by summing the intensity of each pixel within the image of the nanoparticle as determined by thresholding. The effective optoelectronic constant of the color CCD camera across the distribution of wavelengths emitted from the fluorescent nanoparticles was thereby determined to be 0.0374.

Calibrating the optoelectronic constant of the color CCD camera allowed calculation of the number of photons detected in each pixel of the color camera. An average of $N = 257{,}000$ photons were detected from each nanoparticle over a 400 ms exposure time, with an average background intensity of $b^2 = 15$ detected photons per pixel. The localization precision of the position of a single nanoparticle was therefore determined to be $L_c = 0.42$ nm.

The use of multiple fluorescent nanoparticles deposited on a rigid MEMS device further improves the localization precision. When the position of the device is defined as the centroid of the positions of the nanoparticles, then the central limit theorem applies and the centroid localization precision under an optics-limited model is:

$$L_c = \sqrt{\frac{16\left(\sigma^2 + a^2/12\right)}{9N\eta} + \frac{8\pi b^2\left(\sigma^2 + a^2/12\right)}{a^2 N^2 \eta}}$$

Where L_c is the localization precision of the centroid and η is the number of nanoparticles. A constellation of 10 nanoparticles was used for the experiment described in [4], yielding an achievable centroid localization precision of $L_c = 0.13$ nm. Since displacement measurements are simply two centroid position measurements in the same coordinate frame, the uncertainties of the two position measurements add in quadrature, yielding a localization precision of 0.18 nm.

CONCLUSIONS

The experimental uncertainty of the displacement measurements presented here was found to exceed the theoretical value by an order of magnitude. This indicates that the limiting factors in the uncertainty of the measurements described here are not accounted for in the idealized localization precision that is commonly used to express the minimum

TU–23

achievable uncertainty of super-resolution fluorescence microscopy measurements. Reductions in microscope stage drift and the addition of stationary reference nanoparticles in the field of view of the microscope together provide a clear path towards an improved experimental measurement uncertainty of MEMS kinematics. For quasi-static kinematic measurements, such as those described here, the spatial resolution may approach a value that is less than the diameter of a single silicon atom.

ACKNOWLEDGEMENT

This research was performed in the Physical Measurement Laboratory and the Center for Nanoscale Science and Technology at the National Institute of Standards and Technology.

REFERENCES

1. OFFICIAL CONTRIBUTIONS BY THE NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY ARE NOT SUBJECT TO COPYRIGHT.
2. N. BOBROFF, *REVIEW OF SCIENTIFIC INSTRUMENTS,* **57***(6)*, 1152-1157, (1986).
3. J. W. LICHTMAN AND J. A. CONCHELLO, *NATURE METHODS,* **2***(12)*, 910-919, (2005).
4. C. D. MCGRAY, S. M. STAVIS, J. GILTINAN, E. EASTMAN, S. FIREBAUGH, J. PIEPMEIER, J. GEIST AND M. GAITAN, *MICROELECTROMECHANICAL SYSTEMS, JOURNAL OF,* **PP***(99)*, 1-9, (2012).
5. G. T. A. KOVACS. NEW YORK: MCGRAW-HILL, (1998).
6. K. I. MORTENSEN, L. S. CHURCHMAN, J. A. SPUDICH AND H. FLYVBJERG, *NATURE METHODS,* **7***(5)*, 377-U59, (2010).
7. T. AKIYAMA, D. COLLARD AND H. FUJITA, *JOURNAL OF MICROELECTROMECHANICAL SYSTEMS,* **6***(1)*, 10-17, (1997).
8. B. R. DONALD, C. G. LEVEY, C. D. MCGRAY, I. PAPROTNY AND D. RUS, *JOURNAL OF MICROELECTROMECHANICAL SYSTEMS,* **15***(1)*, 1-15, (2006).
9. W. G. ISO TECHNICAL ADVISORY GROUP 4, ED: INTERNATIONAL STANDARDS ORGANIZATION, (1995).

KEYWORDS

Uncertainty, Super-Resolution, Fluorescence Microscopy, Localization Precision, MEMS, Kinematics, Nanoscale, Nanometer

TU–24

SAMPLE ALIGNMENT OF X-RAY REFLECTOMETRY USING THICKNESS AND DENSITY FROM CERTIFIED REFERENCE MATERIALS

Donald Windover[1], David L Gil[1], Yasushi Azuma[2], and Toshiyuki Fujimoto[2]

[1]National Institute of Standards and Technology, Gaithersburg, MD 20899, USA
[2]National Metrology Institute of Japan,
National Institute of Advanced Industrial Science and Technology, Tsukuba 305-8568, Japan

INTRODUCTION

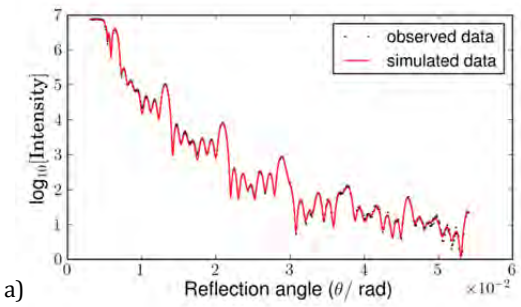
XRR modeling is a first principle's solution of Maxwell's equations for the reflected intensity of parallel X-rays incident at a glancing angle upon a film and is typically modeled using a structure of stacked layers of uniform electron density. Interfaces of differing electron density exhibit Fresnel refraction. This refraction, in turn, leads to a modulation of reflected intensity, which provides layer thickness information. Also, information relating to the electron density of individual stack layers (with correlates with mass density) and surface and interface roughness can be extracted with more complex data analysis (see Dalliant [1]).

In the last decade, an international collaboration under the Versailles Project on Advanced Materials and Standards (VAMAS) performed round-robin study on several candidate materials to be used as thickness standards for XRR [2]. One structure, a three-repeat bi-layer of GaAs/AlAs (total of six layers) deposited on a GaAs wafer, was developed by NMIJ as a pre-standard for a NMIJ Certified Reference Material (CRM). Data taken in 2004 by researchers at NMIJ on a similarly deposited structure (Pre-CRM) using the NMIJ/AIST Traceable X-Ray Reflectometer (T-XRR) is the focus of this study. NIST has been developing Bayesian approaches to estimate uncertainty in modeling XRR parameters [3, 4]. In this study, we apply a more direct and commercially available method, Differential Evolution [also known as genetic algorithm (GA) fitting] to fit the high quality reflectivity data (see Wormington [5]).

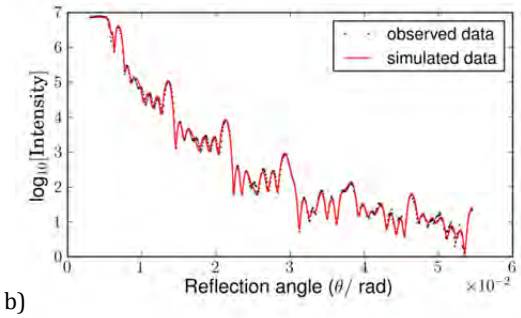
EXPERIMENTAL DETAILS

Due to the nested nature of equations which model XRR phenomena, the inter-relation between instrument alignment and parameter estimation accuracy is somewhat opaque. In this study, we intentionally apply an offset to the measured incident angle information contained in a high-quality XRR data set [over six orders of magnitude reflectometry information over 7.0° of reflected angular range] to create a set of 11 new data sets. Each data set was offset emulating an incremental range of sample misalignments between ±0.025° ω. An identical structural model was refined to each data set using both a NIST developed and a commercial GA refinement to assess the effect of misalignment has on parameter estimation. For examples of refinement, see Figure 1.

TU–24



a)



b)

Figure 1: XRR measurement data and GA model refinement result for data: a) aligned and b) +0.025 degrees in ⍰ incident angle shift. Data represented by points with a line representing GA refinement. Note that misaligned data refinement fails to capture some oscillations in the data.

The structure used in the GA refinement is comprised of seven layers, of assumed composition and thickness defined in Table 2. In each of the 11 refinements, the GA was allowed to vary in density and thickness around bulk density and nominal certified thickness values. Surface layer parameters and roughness refinement did not follow predictable trends, however, the density and thickness information from buried layers did follow observable trends.

Table1. Refinement model and thickness for Pre-CRM

Layer #	Material	Thickness (nm)
1	Al2O3-surface oxide	*1.23*
2	GaAs	*9.05*
3	AlAs	9.44
4	GaAs	9.27
5	AlAs	9.43
6	GaAs	9.26
7	AlAs	9.44
Substrate	GaAs	Inf.

As Figure 2 demonstrates, the thickness variation for the refinement of thickness for layers 4 and 6 (see Table 1) follows a downward sloping linear trend moving from 9.34 nm to 9.17 nm. Although this only represents a 2% difference in thickness, the effect is fairly robust over multiple refinements and may provide us with a method for sample misalignment determination, if sufficient uncertainties in parameter thickness can be determined for a reference sample.

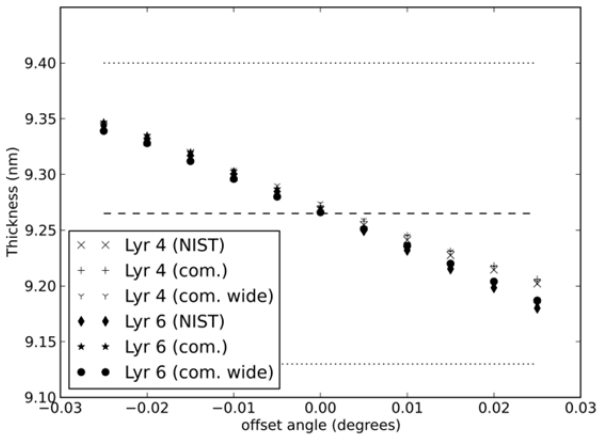


Figure 2. Thickness determination of GaAs layers in multilayer stack, as a function of sample misalignment, ⍰. Note a decrease in slope for thickness as a function of sample misalignment. Dashed line represents the bulk value of GaAs. Dotted lines represent the expanded uncertainty in thickness for this layer structure from a prior NIST Monte Carlo study.

Figure 3 also shows a pronounced shift in density, over ± 20% deviation from bulk density for layer 4 in the model. If one presumes a high quality film of nearly perfect bulk density, this deviation could provide us with a robust calibration for sample alignment using this structure.

TU–24

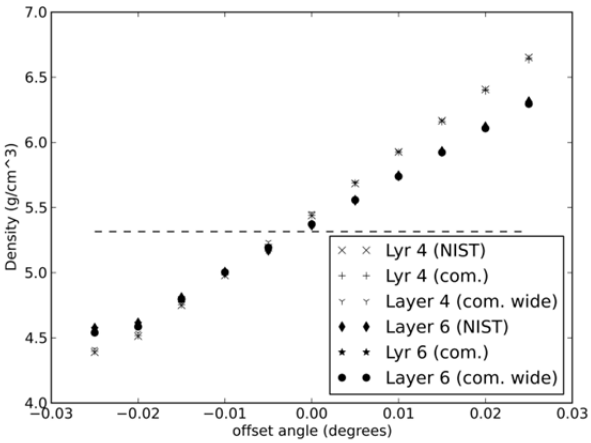


Figure 3: Density determination via genetic algorithm of GaAs layers in multilayer stack, as a function of sample misalignment, w. Note the robust refinement between results from commercial GA code and NIST developed code. Also, note the variation in the slope of density variance between layers in the stack. Layer 4 is clearly more sensitive to misalignment than layer 6.

Figure 3 also shows a pronounced shift in density, over ± 20% deviation from bulk density for layer 4 in the model. If one presumes a high quality film of nearly perfect bulk density, this deviation could provide us with a robust calibration for sample alignment using this structure.

Conclusions

Both film thickness and density determination via X-ray reflectometry analysis are highly correlated with sample alignment. By repeated re-mountings and measurements of a certified reference material, sample alignment protocol and stability can be validated by using certified thickness and density values along with a NIST/NMIJ derived calibration curve.

Further studies are needed in repeatability on either a NIST or NMIJ instrument, to test the validity of this new alignment method. And this study will be a focus of future collaborative research.

References

[1] J. Daillant, A. Gibaud (Eds.), X-ray and Neutron Reflectivity: Principles and Applications, 1st Edition, Springer, 2010.

[2] P. Colombi, D. Agnihotri, V. Asadchikov, E. Bontempi, D. Bowen, C. Chang, L. Depero, M. Farnworth, T. Fujimoto, A. Gibaud, et al., Reproducibility in x-ray reflectometry: results from the first worldwide round-robin experiment, Journal of Applied Crystallography 41 (1) (2008) pp. 143-152.

[3] D. Windover, D. L. Gil, J. P. Cline, A. Henins, N. Armstrong, P. Y. Hung, S. C. Song, R. Jammy, A. Diebold, NIST method for determining model-independent structural information by x-ray reflectometry, AIP Conference Proceedings 931 (1) (2007) pp. 287-291

[4] D. Windover, N. Armstrong, J. Cline, P. Hung, A. Diebold, Characterization of atomic layer deposition using x-ray reflectometry, in: D. Seiler, A. Diebold, R. McDonald, C. Ayre, R. Khosla, E. Secula (Eds.), Characterization and Metrology for ULSI Technology 2005, Vol. 788, Amer. Inst Physics, Melville, 2005, pp. 161-165

[5] M. Wormington, C. Panaccione, K. M. Matney, D. K. Bowen, Characterization of structures from x-ray scattering data using genetic algorithms, Philosophical Transactions of the Royal Society of London Series A - Mathematical Physical and Engineering Sciences 357 (1761) (1999) pp. 2827-2848.

Keywords

X-Ray Reflectivity, thickness, density, accuracy uncertainty, reference material

Wednesday, March 27

Registration

8:00 AM – 8:30 AM

Nanoscale Thermo and Mechanical Characterization

Session Chair: Bob Havemann, SRC

8:30 AM
Adhesion and Thermo-Mechanical Reliability in Emerging Thin Film Device and Energy Technologies 133
Reinhold Dauskardt, Stanford University

9:00 AM
Nano-Scale Characterization of ULK and BEoL Structures: Modulus Mapping and Wedge Indentation Adhesion Measurements 134
Kong Boon Yeap and Ehrenfried Zschech, Fraunhofer

3D

Session Chair: Bob Havemann, SRC

9:30 AM
Metrology Requirements for Manufacturing 3D Integrated Circuits 137
Martin Schrems, AMS

10:00 AM
Coffee Break and Poster Viewing

10:30 AM
Multi-Scale Resolution 3D X-ray Imaging for 3D IC Process Development and Failure Analysis . . . 140
Wenbin Yun, Xradia

Novel Characterization Methods

Session Chair: Usha Varshney, NSF

11:00 AM
Nanoscale Acoustics, Energy Flow, and Imaging Using Tabletop Coherent EUV High Harmonic Light Sources 141
Margaret M. Murnane, Univ. of Colorado/Boulder

11:30 AM
The Uniqueness and Impact of Using Neutrons to Characterize Semiconductor Materials 144
Greg Downing, NIST Neutron Center

12:00 PM
Positron Annihilation Spectroscopy for Porosimetry Determination of Micro- and Meso-Porous Systems 147
Reinhard Krause-Rehberg, Martin Luther University Halle

12:30 PM
Lunch and Poster Viewing

2:00 PM
Nanoscale Electrical Microscopy 149
Wilfried Vandervorst, IMEC

Next Generation Defect Metrology

Session Chair: Shifeng Lu, Micron

2:30 PM
Scatterfield Microscopy, Review of Techniques that Push the Fundamental Limits of Optical Defect Metrology 150
Rick Silver, NIST

3:00 PM
Coffee Break and Poster Viewing

3:30 PM
Frontiers in Defect Detection 153
Lothar Pfitzner, Fraunhofer

4:00 PM
Mirror Electron Microscopy for High-Speed and Highly Sensitive Defect Inspection 158
Masaki Hasegawa, Hitachi

Extreme CMOS Manufacturing

Session Chair: Amal Chabli, CEA-Leti

4:30 PM
Critical Metrology for Advanced CMOS Manufacturing. 161
Zhiyong Ma and Markus Kuhn, Intel

5:00 – 6:00 PM
Poster Session (with Wine and Cheese)

6:05 PM
Depart for Barbecue at Smokey Glen Farm

Poster Presentation

WE-01, A Versatile Variable Field Module for Asylum Cypher Scanning Probe System. 164
Hongxue Liu[1], Ryan Comes[1], Jiwei Lu[1], Stuart Wolf[1], Jim Hodgson[2], and Maarten Rutgers[2]
[1]Department of Materials Science and Engineering, University of Virginia, Charlottesville, VA 22904
[2]Asylum Research, Santa Barbara, CA 93117

WE-02, Metrology for Organic Monolayers on Cobalt Surfaces 167
S. Pookpanratana[1], L. K. Lydecker[1,2], H.-J. Jang[1], C. A. Richter[1], and C. A. Hacker[1]
[1]Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology
[2]College of Nanoscale Science and Engineering, University at Albany

WE-03, Evaluation of Possible Standards for X-Ray Reflectometry 170
P. DeHaven[1], E. Nolot[2], A. Madan[1], A. Michallet[3], S. Favier[3], D. Le Cunff[3], and R. Duru[3]
[1]IBM Corporation, 2070 Route 1 52, Hopewell Junction, NY USA
2CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France.
[3]ST Microelectronics - 850, Rue Jean Monnet, 38926 Crolles Cedex, France.

WE-04, Metrology Studies with NEMO, a Multimillion Atom Simulation Tool 173
G. Klimeck[1], J. E. Fonseca[1], R. Rahman[1], N. Kharche[2,3], G. P. Lansbergen[4], and S. Rogge[5]
[1]Network for Computational Nanotechnology, Purdue University, West Lafayette, IN USA
[2]Department of Physics, Rensselaer Polytechnic Institute, Troy, NY, USA
[3]Brookhaven National Laboratory, Upton, NY, USA
[4]Kavli Institute of Nanoscience, Delft University of Technology, The Netherlands
[5]Centre for Quantum Computation & Communication Technology, School of Physics, The University of New South Wales Sydney, Australia

WE-05, Impact of X-Ray Synchrotron Studies on Nanoelectronics 176
Jonathan Lang, David Keavney, Volker Rose, Ross Harder, Yuxin Wang, Jon Tischler, Wenjun Liu, Jin Wang, Tao Sun, Steve Heald, Albert Macrander, Lahsen Assoufid, and Jyotsana Lal
X-Ray Science Division, Advanced Photon Source, Argonne National Laboratory, Argonne, IL-60439, USA

WE-06, The MEMS 5-in-1 Test Chips (Reference Materials 8096 and 8097) 179
Janet Cassard[1], Jon Geist[1], Craig McGray[2], Richard A. Allen[1], Muhammad Afridi[3], Brian Nablo[1], Michael Gaitan[1], and David G. Seiler[1]
[1]Semiconductor and Dimensional Metrology Division, Physical Measurement Laboratory, National Institute of Standards and Technology, Gaithersburg, MD 20899-8120
[2]Modern Microsystems, Inc., 11522 Soward Dr., Silver Spring, MD 20902
[3]Potomac Networks, 1301 Delaware Avenue SW #N716, Washington DC 20024

WE-07, Contact Resonance AFM on TiN-Low-κ Dielectric Films and Patterns 183
Gheorghe Stan[1,2], Lawrence Friedman[1], Robert Cook[1], Sean King[3], Alan Myers[4], Marc van Veenhuizen[4], and Chris Jezewski[4]
[1]Material Measurement Laboratory, NIST, Gaithersburg, MD
[2]Department of Mechanical Engineering, University of Maryland, College Park, MD
[3]Logic Technology Development, Intel Corporation, Hillsboro, OR
[4]Components Research, Intel Coporation, Hillsboro

WE-08, Adhesion Characterization of $SiCN/SiO_2$ in BEOL and Thin Si/Passivation For TSV Integration Using Nanoscratch Technique 186
Guohua Wei, Sam Ireland, Junting Liu-Norrod, Jaspreet Gandhi, Irina Vasilyeva, Anurag Jindal, Rita Klein, Tom Mendiola, Harold Krasinski, David Fillmore, and Shifeng Lu
Micron Technology, Inc., 8000 S. Federal Way, Boise, ID, USA

WE-09, Analysis of Local Stress Distribution in a Metal Gate MOSFET with a New Raman Simulation Method 189
Tetsuya Tada[1], Vladimir Poborchii[1], Hiroshi Arimoto[1], Akira Satoh[1], Koichi Fukuda[1], Kazuhisa Fujita[2], and Toshihiko Kanayama[1]
[1]National Institute of Advanced Industrial Science and Technology (AIST), 1-1-1 Higashi, Tsukuba, Ibaraki 305-8562, Japan
[2]ASTOM R&D, 2-3-13 Minami, Wako-shi, Saitama 351-0104 Japan

WE-10, Automated Strain Measurement Using Nanobeam Diffraction Coupled with Precession . . 192
A. Darbal[1], R. Narayan[1], C. Vartuli[2], G. Lian[2], S. Nicolopoulos[3], and J. K. Weiss[1]
[1]AppFive, LLC, 1095 W. Rio Salado Pkwy, Suite 110, Tempe, AZ 85281, USA
[2]Texas Instruments, 13121 TI Boulevard, Dallas, TX 75243, USA
[3]NanoMEGAS SPRL, Blvd Edmond Machtens 79, B-1080 Brussels, Belgium

WE-11, Optical Dynamic Picocalorimeter for Fast Thermodynamic Measurements. 195
Brian G. Burke and David A. LaVan
Materials Measurement Science Division, National Institute of Standards and Technology, Gaithersburg, Maryland, USA

WE-12, Accuracy and Resolution of Nanoscale Strain Measurement Techniques 197
Will Osborn[1], Lawrence Freidman[1], Mark Vaudin[1], Steve Stranick[1], Michael Gaither[1], Justin M. Gorham[1], Victor Vartanian[2], and Robert Cook[1]
[1]Materials Measurement Science Division, National Institute of Standards and Technology, Gaithersburg, MD
[2]3D enablement Center Metrology, Sematech, Albany, NY

WE-13, Full Wafer Spatially Resolved Adhesion Testing of ULK-Films Without Sample Preparation . . 200
Ude D. Hangen, Andy Romano, and David Vodnick
Hysitron, Inc., 9625 West 76th Street, Minneapolis, MN 55344

WE-14, Design of Test Structure for 3D-Stacked Integrated Circuits (3D-SiCs) Metrology 203
Lin You, Jung-Joon Ahn, and Joseph J. Kopanski
Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD 20899, USA

WE-15, A New Prognostic Tool for TSV Reliability Assessment Using RF Signals 206
Chukwudi Okoro[1], Pavel Kabos[1], June W. Lau[1], Jan Obrzut[1], Klaus Hummler[2], and Yaw S. Obeng[1]
[1]National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899
[2]SEMATECH, 257 Fuller Road, Albany, NY 12203

WE-16, TSV Reveal Height and Bump Dimension Metrology by the TSOM Method: from Nanometer to Micrometer Scale 209
Victor Vartanian[1], Ravikiran Attota[2], Steve Olson[3], Robert Edgeworth[4], Iqbal Ali[1], Craig Huffman[1], Pete Moschak[3], Harry Lazier[3], and Elizabeth Lorenzini[3]
[1]SEMATECH, Albany, NY, USA
[2]Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD, USA
[3]College of Nanoscale Science and Engineering (CNSE), SUNY Albany, assignee to SEMATECH
[4]Intel assignee to SEMATECH

WE-17, Defect Metrology of Epitaxial Ge on Patterned Si Wafers Using an Inline HRXRD Tool . . . 212
M. Wormington[1], P.Y. Hung[2], M.-H. Wong[2], C.T. Schamp[3], A. Giladi[4], M. Klinov[4], , W.-E Wang[2], G. Bersuker[2], P. D. Kirsch[2], and R. Jammy[2]
[1]Jordan Valley Semiconductors, Austin, TX 78744, USA
[2]SEMATECH, Albany, NY 12203, USA
[3]Novati Technologies, Austin, TX 78741
[4]Jordan Valley Semiconductors, Migdal Ha'Emek 23100, Israel

WE-18, XPS Tool Matching and Optimization for EUV Optics Contamination Studies 216
Yudhishthir Kandel[1], Mihir Upadhyaya[1], Gregory Denbeaux[1], and Cecilia Montgomery[2]
[1]College of Nanoscale Science and Engineering, University at Albany, SUNY, 257 Fuller Rd, Albany, NY 12203
[2]SEMATECH, 255 FullerRd, Albany, NY 12203

WE-19, Cross Spectrum Noise Spectroscopy for Deep Level Trap Detection in Nano-Scale Semiconductor Devices 219
Deepak Sharma[1,2], Sergiy Krylyuk[1,3], Abhishek Motayed[1,3], Qiliang Li[1,2], and Albert V. Davydov[1]
[1]National Institute of Standards and Technology, Gaithersburg, MD 20899 USA
[2]Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030 USA
[3]IREAP, University of Maryland, College Park, MD 20742 USA

WE-20, Development of High Resolution Topographic Characterization at Die Scale by Interferometry. 221
F. Dettoni[1], C. Beitia[2], S. Gaillard[1], O. Hinsinger[1], F. Bertin[2], and M. Rivoire[1]
[1]STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France
[2]CEA, Leti, campus MINATEC, 17, rue des Martyrs, 38054 Grenoble Cedex 9, France

WE-21, Development of Three-Dimensional Raman Spectra Analysis System for TCAD Stress Simulation in FinFET Structures 224
Hiroshi Arimoto[1], Akira Satoh[1], Vladimir Poborchii[1], Tetsuya Tada[1], Koichi Fukuda[1], Koji Usuda[2], Kazuhisa Fujita[3], and Toshihiko Kanayama[1]
[1]National Institute of Advanced Industrial Science and Technology (AIST), 1-1-1 Higashi, Tsukuba, Ibaraki, Japan
[2]Green Nanoelectronics Center (GNC), AIST West, 16-1 Onogawa, Tsukuba, Ibaraki, Japan
[3]ASTOM R&D, 2-3-13 Minami, Wako-shi, Saitama, Japan

WE-22, Characterization of SiO_2/Si Interface Quality by Photoluminescence. 227
Shiu-Ko Jang Jian[1], Chih-Cherng Jeng[1], Ting-Chun Wang[1], Chih-Mu Huang[1], Ying-Lang Wang[1], and Woo Sik Yoo[2]
[1]Taiwan Semiconductor Manufacturing Company, Ltd., No. 1-1, Nan-Ke Rd., Science-Based Industrial Park, Tainan, 741-44, Taiwan
[2]WaferMasters, Inc., 254 East Gish Road, San Jose, CA 95112, USA

4–1

Adhesion and Thermo-Mechanical Reliability in Emerging Thin Film Device and Energy Technologies

Reinhold H. Dauskardt

Dept. of Materials Science and Engineering
496 Lomita Mall, Durand Bldg., Rm. 121
Stanford University
Stanford, CA 94305 – 4034

Introduction

Materials and interfaces in emerging device technologies operate near the envelope of their mechanical and adhesive properties with remarkably high levels of film stress. Adhesion and cohesive fracture are major challenges for materials and device reliability at all levels of processing, packaging and service.

Device Technologies

In the area of emerging microelectronic and energy technologies, the impact of high-volume and cost-effective depends critically on their reliability and durability over extended operating lifetimes. Commercialization requires accurate lifetime predictions and product warranties over extended time periods. In the case of photovoltaic technologies, this often exceeds other device technologies. Despite optimistic forecasts for cost-effective solar, uncertain degradation mechanisms, the lack of testing metrologies, poor accelerated testing protocols and science-based kinetic degradation models, and uncertain lifetimes currently present significant barriers for success.

Research

We describe research aimed at characterizing thin-film thermomechanical properties including adhesion and cohesion that are critical for emerging device technologies. Particular challenges of integrating new thin film adhesive layers as well as ultra thin barriers are considered. Applications include solar energy devices and modules, display technologies, and microelectronic devices and packages.

Quantitative in-situ characterization techniques to measure the synergistic effect of mechanical stresses, temperature, environmental species and the presence of in-situ simulated solar UV light on inherent thermo-mechanical properties including interface decohesion kinetics and cohesive failure of layers are described. Research techniques and results are described for a number of material and interface systems relevant to emerging technologies, including solar, encapsulation and ultra-barriers, transparent electrodes, optical elements, and flexible and multi-junction solar cells. Implications to optimize materials, develop accelerated test methods and provide the fundamental basis for realistic lifetime predictions are described.

Keywords

Reliability, thin-films, devices, adhesion

NANO-SCALE CHARACTERIZATION OF ULK AND BEOL STRUCTURES: MODULUS MAPPING AND WEDGE INDENTATION ADHESION MEASUREMENTS

Kong Boon Yeap[1], Malgorzata Kopycinska-Mueller[1,2], Lei Chen[3], Martin Gall[1], Ehrenfried Zschech[1,2]

[1] *Fraunhofer Institute for Nondestructive Testing, Dresden, Germany*
[2] *Technical University Dresden, Dresden, Germany*
[3] *Institute of High Performance Computing, Singapore*

INTRODUCTION

For high-performance microelectronic products, porous organosilicate glasses with low dielectric permittivity are used as insulating material between metal on-chip interconnects. However, the mechanical weakness of these thin films, particularly their low Young's modulus which is decreasing with increased porosity, is a reliability concern. We have shown for the first time, that pore topology has a significant effect on the Young's modulus of these materials. Particularly, organosilicate glasses with translation-symmetric pores with constant pore size show a significantly higher elastic modulus compared to films with randomly distributed pores [1,2]. The understanding of the role of the pore topology on small-scale deformations of these thin films is essential for the integration of novel materials into microelectronic products. Nanoindentation and atom force acoustic microscopy (AFAM) are complementary techniques which provide the needed information.

NANOINDENTATION AND AFAM ELASTIC MODULUS STUDIES

The deformation of organosilicate glass at sub-20nm indentations provides information about deformation mechanism and pore-topology, which cannot be deduced from the conventional elastic modulus and hardness measurements. Ultra-sensitive instruments coupled with precise tip calibration have allowed us to study the deformation of a material at sub-3nm precisely. An organosilicate glass with broad pore size distribution is deformed exactly as described by the Hertzian model. For an organosilicate glass with narrow pore size distribution and ordered arrangement, unexpected deformation mechanisms: elastic stiffening and elastic hysteresis, corresponding to pores densification and pore-wall buckling can be deduced from the load-penetration (*P*-*h*) curves (Fig.1A-1C). This observation can be explained by availability of the deformation mechanism with the lowest energy consumption, e.g. the bending of siloxane bonds [3] and the stress distribution in the porous material. Coupled with finite-element simulations of the deformation of porous glass with different pore

4–2

topology models, small-scale indentation at sub-3nm becomes a powerful approach to deduce the pore topology of a given glassy material (Fig.2A). The CVD deposited organosilicate glass (CVD-OSG) with broad pore size distribution follows the random overlapping solid sphere model. On the other hand, a threshold pore-coalescence porosity, $p > 0.3$, at which the pores begin to overlap for an ordered porous structure, is determined for a new type of self-assembled organosilicate glass (SA-OSG [2,4]) (Fig.2B). The SA-OSG material with defined pore topology and properties approaching the Hashin-Shtrikman (HS) upper bound is a potential low-k dielectric material to be integrated into the on-.chip interconnect stack of future microelectronic devices.

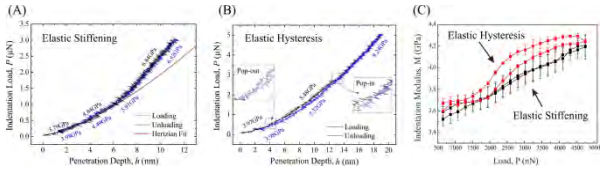


FIGURE 1. (A-B) Nanoindentation load-penetration (P-h) curves for SA-OSG (p=0.4). Indentation modulus values at different depth and load are included at the corresponding position. (A) Complete match between loading and unloading curves. A Hertzian curve with E=4GPa is added for better visualization of the elastic stiffening effect. (B) Elastic hysteresis, i.e. pop-in at 13nm, pop-out at 4nm. Insets are added to enlarge the pop-in and the pop-up parts, so that separation and overlap of loading and unloading curves can be clearly seen. (C) High resolution measurement of indentation modulus by atomic-force-acoustic-microscopy (AFAM) for SA-OSG (p=0.4).

.

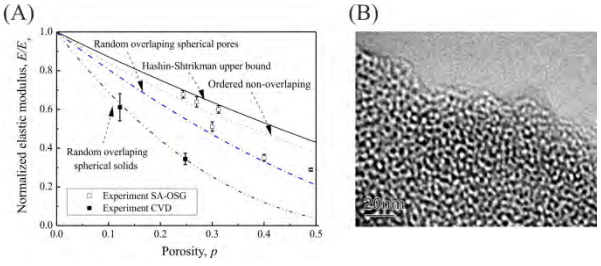


FIGURE 2. (A) Plot of normalized elastic modulus against porosity (E/E_s vs. p) for different models. (B) TEM image of a calcined SA-OSG film with p>0.3 [2].

WEDGE INDENTATION ADHESION MEASUREMENTS

The adhesion of low-k materials is widely determined by four-point-bending (FPB) and double-cantilever-beam (DCB) techniques on blanket films. However, application of these techniques on a manufactured die will not provide the adhesion value of ULK interfaces, but an average value characterizing the entire on-chip interconnect stack. Therefore, local adhesion measurements applying the indentation technique are a potential option for process control and quality control of ULK materials [6,7].

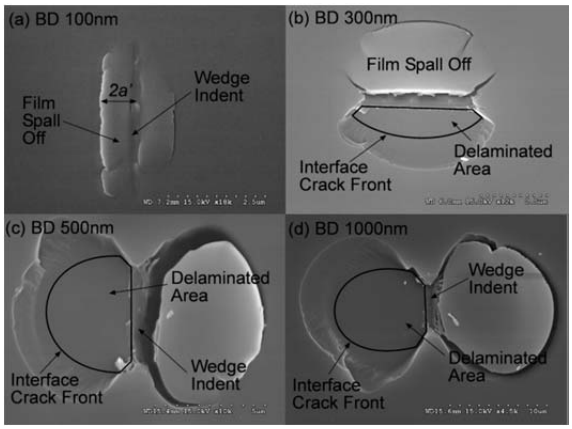


FIGURE 3: Interfacial crack geometry for OSG films (BlackDiamond™, Applied Materials Inc., USA) with 100nm, 300nm, 500nm, and 1000nm thickness [7].

Fig. 3 shows the evolution of the geometry of interfacial cracks induced by wedge indentation with increasing film thickness. The procedure to determine the geometry of the interfacial crack area is reported in [7]. The curvature of the crack front decreases exponentially with the increase of the ratio of wedge length and film thickness (l/t). Based on a 3D simulation of the stress-strain field beneath the wedge indentation with different l/t ratio, it has been found that the geometry of the interfacial crack is dependent on the distribution of the stress induced by indentation [8]. The difference in the stress-strain condition will affect the buckling condition of the film above the interfacial crack. However, further consideration of the buckling condition for OSG films shows that the critical buckling stress is higher than the indentation

induced stress, thus the effects of buckling of the film can be neglected.

Despite the difference in the stress-strain condition, consistent interfacial adhesion results are obtained for different *l/t* ratios using the general equation for the average indentation stress. The consistency of the interfacial adhesion results is expected since the empirical equation for indentation induced stress is a general solution for both plane strain and plane stress conditions.

Further comparisons with the FPB results on OSG films interfacial adhesion reported in literature show good agreement with the results from wedge indentation experiments. The estimated phase angle of steady-state crack propagation during wedge indentation is about 56°. In addition to the experimental studies, a forward-reverse analysis of the interfacial adhesion energy and adhesion strength of the OSG films, based on simulations of the wedge indentation induced delamination, provides similar results too [9].

Since the calculation of the interfacial adhesion as mentioned above only requires two simple experimental inputs: (a) interfacial crack area and (b) critical indentation depth, and the test does not require any prior sample preparation, the interfacial adhesion determination can be automated. Coupling with a quick non-destructive test (NDT) technique to determine the interfacial crack area, the wedge indentation test can evaluate the interfacial adhesion of ULK films in an extremely short time frame of 3 to 5mins/data. High measurement throughput required for process control in volume manufacturing seems to be possible to achieve. One potential NDT technique for the determination of the interfacial crack area is the modulus mapping option provided in the Hysitron TI 950 system. Examples will demonstrate the application of the approach described.

Summarizing, this paper presents a new approach to characterize adhesion of ULK materials at test structures of product or test wafers, applying the wedge indentation method without excessive particles generation. Together with modulus mapping of the indented area, the interfacial crack area can be precisely determined non-destructively.

Since the interfacial crack can be induced applying wedge indentation long before the complete material delamination and spall-off, there are not many particles generated in the indented region after the adhesion measurement. This result provides promising visions for the use of this technique not only in out-of-fab labs. Further studies are needed considering the high requirements in semiconductor manufacturing.

REFERENCES

1. E. Zschech, K. B. Yeap, R. Huebner, Int. Conf. AMC, San Diego (2011).
2. K.B. Yeap, M. Kopycinska-Mueller, L. Chen, S. Mahajan, M. Phillips, W. R. Bottoms, Y. Chen, J. Vlassak, M. Gall, E. Zschech, in preparation.
3. U. Rabe, Applied scanning probe methods II, (Springer, Berlin, 2006), p.37.
4. J.M. Knaup, H. Li, J.J. Vlassak, E. Kaxiras, Phys. Rev. B **83**, 054204 (2011).
5. K. Landskron, B.D. Hatton, D.D. Perovic, G.A. Ozin, Science **302**, 226 (2003).
6. A.A. Volinsky, J.B. Vella, W.W. Gerberich, Thin Solid Films 429, 201 (2003).
7. K.B. Yeap, K.Y. Zeng, H.Y. Jiang, L. Shen, D. Z. Chi, J. Appl. Phys. 101, 123531 (2007).
8. L. Chen, K.B. Yeap, K.Y. Zeng, and G.R. Liu, unpublished.
9. L. Chen, K.B. Yeap, K.Y. Zeng and G.R. Liu, *Phil. Mag.*, 89, 1395-1413, (2009).

Keywords: Mechanical characterization, Modulus mapping, Nanoindentation, AFAM, Adhesion

5–1

METROLOGY REQUIREMENTS FOR MANUFACTURING 3D INTEGRATED CIRCUITS

Martin Schrems, Franz Schrank, Joerg Siegert, Jochen Kraft, Jordi Teva, Siegfried Selberherr*

ams AG,
Tobelbaderstrasse 30, A-8141, Unterpremstaetten, Austria
** Institute for Microelectronics, TU Wien,*
Gusshausstrasse 27-29, A-1040, Vienna, Austria

ABSTRACT

Three-dimensional integrated circuits (3D ICs) introduce wafer bonding and Through Silicon Vias (TSVs) as new modules, thus extending manufacturing requirements beyond CMOS. A 3D IC with a photosensor is taken as an example to further analyze the resulting new metrology requirements for mass production. For the wafer bond module, data on defects before and after bonding, bond interface adhesion strength, and the module, thickness control for deposited layers and defect metrology including the trench sidewall and bottom are identified as key requirements. Mass production requires non-destructive inline metrology in all cases. This has been achieved for electrical parameters, bond void (Scanning Acoustic Microscopy), and TSV depth monitoring (optical methods). Other parameters such as bond strength, as well as layer thickness or defect metrology inside TSVs, demand further R&D.

INTRODUCTION

Recently there has been a strong trend from classical packaging using bond-wires towards Wafer Level Packaging (WLP) using bumps. This is mainly driven by form factor and cost reduction. Additional Through Silicon Via (TSV) technology has enabled a conductive path connecting wafer front side and back side. This allows the placement of electrically functional structures on both sides of a chip as well as the stacking of chips to form 3D ICs. Open TSVs with Cu or W liner and Cu or W filled TSVs have emerged as the two main concepts [1], [2]. Likewise high density "TSV middle" [3] for memory or processor stacking and lower density "TSV last" [4] e.g. for sensor integration have emerged as the two main process integration schemes. The general metrology requirements are, however, very similar for all of these concepts because of the identical TSV and bond interface topography.

3D INTEGRATED CIRCUIT

BASIC STRUCTURE AND PROCESS FLOW

As an example for manufacturing requirements, a 3D integrated photosensor connected to an IC via an open TSV (Fig.1, [5]) has been chosen.

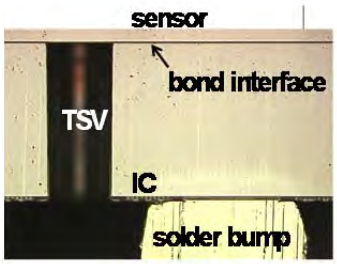


FIGURE 1. Cross-section of a 3D IC and a photosensor connected by an open TSV.

Key non-CMOS process modules are wafer to wafer (W2W) bonding and TSV formation (Figure 2, [5]).

5–1

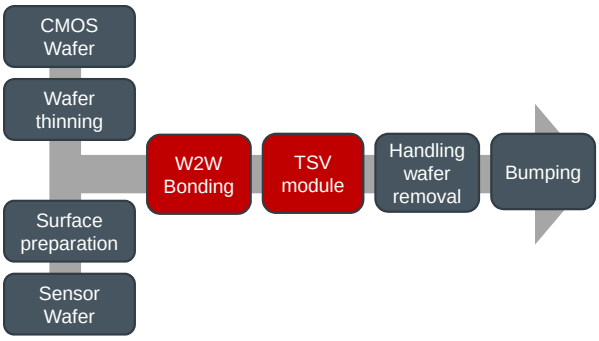


FIGURE 2. Schematic process flow for the 3D IC with photosensor and TSV from Figure 1.

ELECTRICAL CHARACTERIZATION

Important parameters are the TSV resistance, the leakage current to the Si bulk, and the TSV breakdown voltage [6]. The TSV resistance is routinely measured in a production environment.

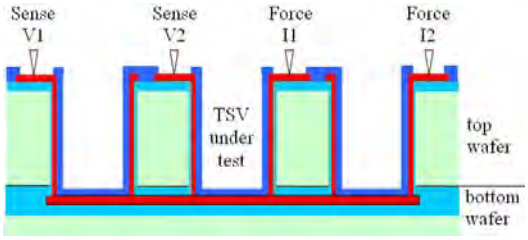


FIGURE 3. 4-point measurement enables precise contact resistance measurement on TSVs [6].

Two additional TSVs are used for forcing a current on the one hand and measuring the potential on the other hand (Fig. 3). Thus a high precision resistance measurement can be established. Figure 4 shows the TSV resistance distribution of 11.000 TSVs.

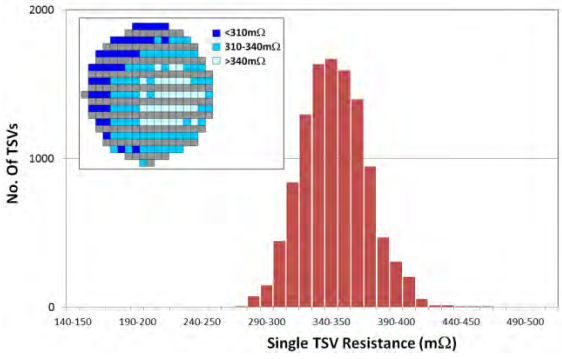


FIGURE 4. TSV resistance distribution [6].

The measured TSV resistance of 350mOhm aligns well with theoretical calculations for the materials used. Reliability investigations comprising thermal cycling, environmental stress, and thermal aging did not show any degradation.

IN-LINE METROLOGY

WAFER BONDING

Different bonding methods for CMOS compatible processing have recently been developed [7]. Temporary handling wafers, for example, may be attached to a CMOS wafer via adhesive wafer bonding. Due to the relatively thick polymer layer the requirements relating to surface topography and particle density are not very high. The demand on bond quality is considerably higher, if the bond interface remains part of the final product, such as in the case of direct wafer to wafer bonding (Fig.1) or metal bonding (e.g. Cu-Cu bonding). Control of bond quality is mandatory in such cases. Non-bonded areas (bond voids) must be minimized and the bond strength must be maximized close to the level of monolithic material. Bond defects smaller than 100x100µm^2 can be detected by C-mode Scanning Acoustic Microscopy (C-SAM, Fig. 5).

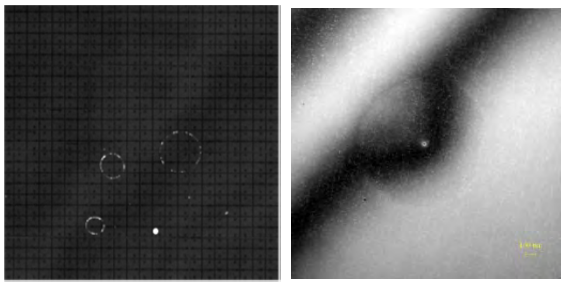


FIGURE 5. C-SAM image of bond defects: drying residues (left), particle in the bond interface (right).

While bond voids can be measured in-line, no non-destructive technique exists for determining the bond strength. Instead the tests rely on mechanically separating the bonded parts. While several methods exist, the only one satisfying the demand for robust measurements is the micro chevron test [8], [9]. Chevron structures are formed by patterning the bond oxide (Fig. 6 (left)). After bonding, external forces are applied. The maximum load needed to break the micro chevron structure is then recorded as a measure for the bond strength.

5–1

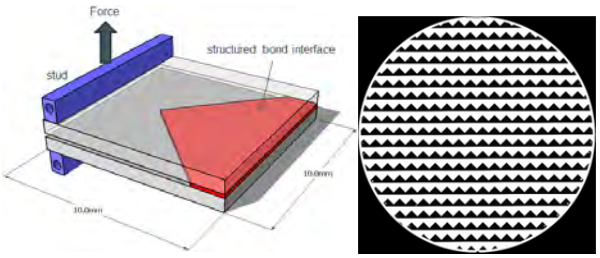


FIGURE 6. Chevron test structure (left) and C-SAM measurement at wafer level (right).

Chevron structures can be measured for test wafers to characterize a bond process (Fig.6, right). For product wafers a non-destructive method would be needed. Therefore some further work to provide a non-destructive bond strength analysis, e.g., by C-SAM was proposed [10].

THROUGH SILICON VIA (TSV) MODULE

TSV processing comprises the key process steps of Si Deep Reactive Ion Etching (DRIE) forming a trench, isolation layer deposition and etch, barrier layer deposition (TiN, Ta, ...), metal deposition (W, Cu, ...) , and passivation layer formation. The only structural difference is that metal is either deposited as a liner (open TSV, Fig.1) or used to fill the TSV explaining similar metrology requirements. An inherent issue of DRIE is the formation of scallops due to the switching between etching and sidewall passivation cycles. Defects include side wall damage during DRIE due to insufficient passivation, and residuals.

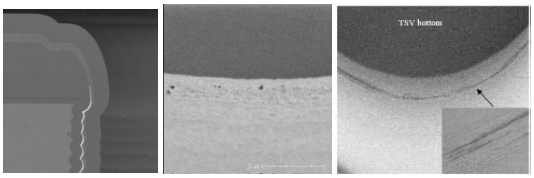


FIGURE 7. Scallops (left), particles and damage (center) and residuals inside the TSV (right).

Therefore, inspection after TSV etching and cleaning is required. For deposited layers, film thickness measurements and defect inspection is also mandatory. Side wall inspection can be performed by methods such as tilted SEM. The trench depth and the TSV bottom can be inspected using optical tools such as spectrophotometers and interferometers [11].

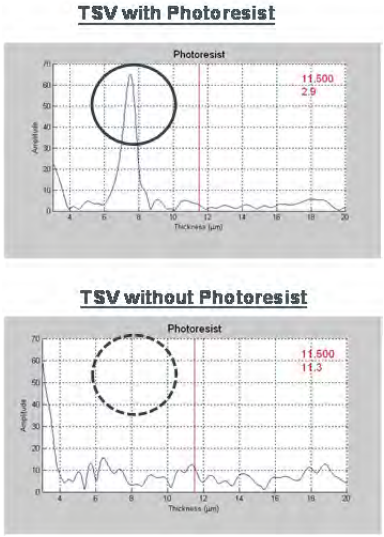


FIGURE 8. Resist thickness measurements at the TSV bottom using a commercial white light spectrophoto-meter [11].

Results for non-destructive in-line resist thickness measurements inside the TSV are shown in Fig. 8.

CONCLUSIONS

Various 3D IC metrology methods already exist. Cost reduction in manufacturing 3D ICs will benefit from further metrology R&D especially for non-destructive bond strength as well as defect- and film thickness measurements inside TSVs.

REFERENCES

1. J. Kraft, et. al, Proc. ECTC (2011)pp.560-566.
2. J.Wolf et al., ECTC(2008)pp.563-570.
3. M.G.Farooq et al., IEDM (2011)pp.143-146.
4. D.H.Triyoso, ICICDT (2010)pp.118-121.
5. F. Schrank et al., Semicon Europe 3D IC session (2012).
6. C.Cassidy et al.,, IEEE Transactions on Device and Materials Reliability, Vol.12, Issue 1, (2012).
7. V. Dragoi *et al*., *Microsyst. Techn.* 18,(2012)1065-1075.
8. J. Siegert *et al*., *ECS Transactions*, 50(7)(2012)253-262.
9. SEMI MS5-0310, published Feb 2010.
10. O.Vallin et al., Materials Science and Eng. R50 (2005).
11. D.Marx et al., Proceedings of the IEEE International Conference on 3D System Integration (2009).

KEYWORDS

metrology, 3D, Integrated Circuit, manufacturing, Through Silicon Via, wafer bonding

5–2

MULTI-SCALE RESOLUTION 3D X-RAY IMAGING FOR 3D IC PROCESS DEVELOPMENT AND FAILURE ANALYSIS

Wenbing Yun, Michael Feser, Jeff Gelb, Luke Hunter

Xradia, Inc. 5052 Commercial Circle, Concord, CA 94520

ABSTRACT

Multi-scale resolution 3D x-ray imaging with 50 nm resolution offers unique capability to new process development, failure analysis, and production monitoring of 3D IC devices. Its nondestructive nature allows parts to be imaged without sample preparation induced artifacts or time lapse imaging (4D imaging) to study failure mechanism such as current or stress induced failures. It images a large number of features simultaneously and allows quick feedback on manufacturing processes to speedup process development. The spatial resolution of 3D x-ray imaging is been continuously improved and 30nm and 50nm resolution has been developed using synchrotron and laboratory x-ray sources, respectively. The performance and application examples of two major 3D x-ray imaging systems will be presented and discussed

6–1

NANOSCALE ACOUSTICS, ENERGY FLOW, AND IMAGING USING TABLETOP COHERENT EUV HIGH HARMONIC LIGHT SOURCES

Damiano Nardi[1], Kathleen M. Hoogeboom-Pot[1], Matt Seaberg[1], Daniel Adams[1], Emrah Turgut[1], Patrick Grychtol[1], Bosheng Zhang[1], Dennis Gardener[1], Jorge N. Hernandez-Charpak[1], Marie Tripp[2], Sean W. King[2], Erik H. Anderson[3], Ronggui Yang[1], Justin Shaw[4], Thomas J. Silva[4], Margaret M. Murnane[1], and Henry C. Kapteyn[1]

1) JILA, Department of Physics and NSF Engineering Research Center in Extreme Ultraviolet Science and Technology, University of Colorado and NIST, Boulder, CO 80309-0440

2) Intel Corp. 2501 NW 229th Ave, Hillsboro, OR, 97124

3) Center for X-Ray Optics, Lawrence Berkeley National Laboratory, Berkeley, CA 94720

4) Electromagnetics Division, National Institute of Standards and Technology, Boulder, CO 80305

INTRODUCTION

Advances in extreme nonlinear optics make it possible to efficiently upshift tabletop femtosecond lasers into the ultraviolet (EUV) and soft X-ray regions of the spectrum, to wavelengths as short as 8 Å [1, 2]. In an optimized phase-matched geometry, the resultant high-order harmonics naturally emerge as fully spatially coherent beams, with ultra broad bandwidths spanning tens to hundreds of eV, corresponding to pulse durations in the few-femtosecond range. This unique light source is ideally suited for range of nano-imaging and element-specific nano-metrologies of materials, thin film and magnetic samples.

APPLICATIONS OF EUV HIGH HARMONICS

High harmonic generation (HHG) is a universal response of atoms and molecules in strong femtosecond laser fields. In this process, an intense fs laser pulse is focused into an atomic gas. Due to the extreme distortion and acceleration of the electron wave function by the strong laser field, the atom acts like a nanoscale radiating antenna, emitting high harmonics of the driving laser. In the EUV region of the spectrum (<100 eV), where bright (phase matched) HHG beams have been demonstrated and optimized, conversion efficiencies > 10^{-5}/harmonic can be obtained, corresponding to μW of power per harmonic when driven by few watt femtosecond lasers with wavelengths around 0.8μm.

A host of applications in nanoscience and nanotechnology have now been demonstrated using EUV HHG, including probing the elastic properties of thin films of thicknesses < 50 nm, implementing full-field 2D microscopes with record 22 nm spatial resolution (≈1.6λ), quantifying how nanoscale energy flow differs from bulk, and measuring how fast a material can change its electronic or magnetic state, or how spin currents can control and enhance magnetization in ultra thin films [3 - 8].

6–1

In the following, we describe two applications of HHG: EUV acoustic nano-metrology and coherent diffractive imaging. We also present a brief outlook for future applications of soft X-ray HHG beams.

Acoustic Nano-Metrology using EUV Beams

In EUV acoustic nano-metrology, simply by replacing the conventional laser sources currently used by shorter wavelength HHG beams, it is possible to directly characterize nanoscale thermal, mechanical and interfacial properties of thin films and nanostructures in the 1 – 100 nm range.

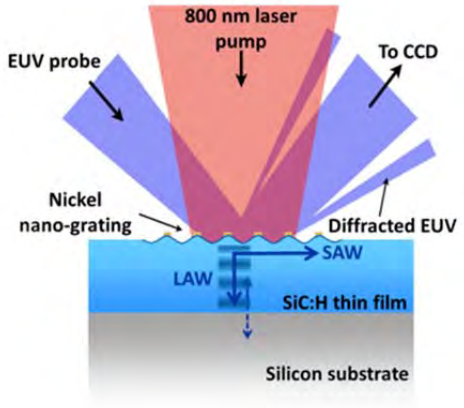


FIGURE 1. Setup for EUV acoustic nano-metrology. A femtosecond laser pump pulse heats a metal nano-grating and launches SAWs and LAWs, which are then probed using a time-delayed EUV probe beam.

As shown in Fig. 1, to launch very short wavelength surface acoustic waves (SAWs), we impulsively excite a nano-patterned metallic grating with a femtosecond infrared laser pulse to simultaneously launch both longitudinal and short-wavelength transverse acoustic waves (LAWs and SAWs) in the material. Since SAWs propagate with a penetration depth proportional to a fraction of their acoustic wavelength, the SAW wavelength set by the grating selects the thickness of the layer to which the measurement sensitivity to the material's mechanical properties is confined. At the same time, LAWs travel into the material, reflecting from any interface present. When both waves are fully confined within a thin film, the 3D mechanical properties of the film (Young's modulus and Poisson's ratio) can be precisely characterized.

Photoacoustic metrology has long been used as an excellent non-contact tool to characterize the elastic properties of thin films, as a nondestructive and noncontact optical metrology [9]. However, its utility for studying nanoscale systems has been limited by the visible wavelengths used to probe the acoustic waves. Nano-indentation using an AFM provides a local but destructive measurement technique. Though well established, it has major drawbacks in speed and often leads to results that are difficult to interpret and influenced by the substrate. Brillouin Light Scattering can characterize 100 nm films, but because it requires a complicated interpretation and is very sensitive to

In exciting work using EUV nano-metrology shown in Figs. 1 and 2, we have already demonstrated the ability to extract the elastic properties of 50 nm a-SiC:H films deposited on silicon substrates. The same measurements can also probe heat dissipation from 30 – 65 nm hotspots. Most recently, we demonstrated that EUV photoacoustics can reliably detect and characterize metallic films of only a few-nm thickness by very sensitively detecting the longitudinal waves reflected from layered nano-grating pillars.

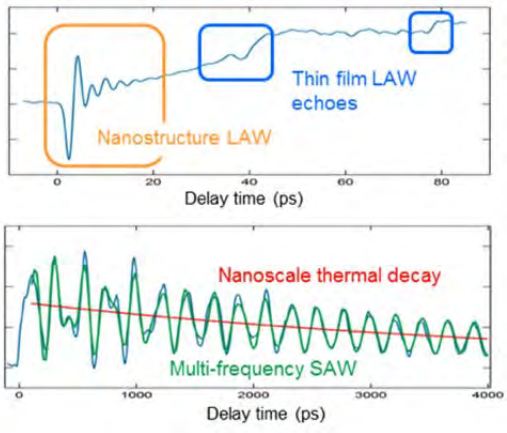


FIGURE 2. The acoustic dynamics in the thin-film/substrate system separates into two timescales. On ps timescales (top), LAWs in the metal nanostructures (orange box) and thin film (blue boxes) can be seen. On ns timescales (bottom), heat dissipates from the nanostructures to the substrate (red).

6–1

Coherent Nano-Imaging using HHG

In coherent diffraction imaging (CDI), an object is illuminated with a coherent beam of light. Rather than using a conventional imaging lens system to form an image, the light scattered from the object is captured on a CCD. Although only the intensity, and not the phase, of the coherent light is recorded, provided that constraints can be placed on the object or the illuminating beam, a computer algorithm can be used to iteratively extract the optical phase, and therefore an image of the object.

A great attraction of CDI is that it obviates the need for one of the most-difficult part of a soft X-ray microscope—the imaging lens. Conventional soft X-ray microscopy uses zone plate imaging lenses, which have a resolution limited by their smallest feature size. As a result, the record zone plate X-ray image resolution is ~15 nm – much greater than X-ray wavelengths. In contrast, the highest CDI resolution using synchrotrons or XFELs is ~2 nm for materials, and 11 nm for biological specimens. Using EUV HHG sources, record tabletop full field microscope resolution of 22 nm (Fig. 3) was achieved using 13 nm HHG beams (resolution < ⍰λ⍰.

Looking to the future, high harmonic sources at wavelengths down to 1 nm will enable both imaging and characterization of sub-10 nm structures. Moreover, by using high pulse energy EUV beams, SAWs could be launched by interfering two EUV pump pulses, making it possible to characterize the elastic properties of very thin films without the need for depositing a nano grating. Finally, a great advantage of HHG sources is the possibility for a wide variety of separate measurements using the same setup. EUV high harmonics are sensitive to magnetic and thermal dynamics and can also be used to directly image a sample via coherent diffractive imaging. Therefore this technique offers the possibility of a unique flexible nanometrology tool capable of a wide variety of imaging and characterization modalities.

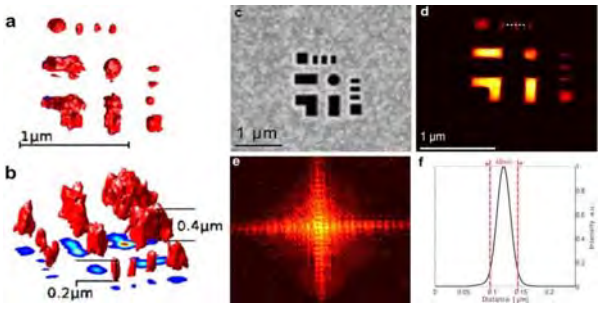


FIGURE 3. a, b. 3D diffractive imaging of the sample shown in c. c Scanning electron microscope image of the sample. d Retrieved 2D image. e 2D scatter pattern. f Lineout with resolution of 22 nm.

References

1. A. Rundquist, C. Durfee, Z. Chang, C. Herne, C., H. Kapteyn, M. Murnane, Science **280**, 1412 (1998).
2. T. Popmintchev et al., Science **336**, 1287 (2012).
3. M Siemens, Q. Li, R. Yang, K. Nelson, E. Anderson, M. Murnane H. Kapteyn, Nature Materials **9**, 26 (2010).
4. D. Nardi, M. Travagliati, M. Siemens, Q. Li, M. Murnane, H. Kapteyn, G. Ferrini, P. Parmigiani, F. Banfi, Nano Letters **11**, 4126 (2011).
5. M. Seaberg, D. Adams, E. Townsend, D. Raymondson, W. F. Schlotter, Y. Liu, C. Menoni, H. C. Kapteyn, and M. M. Murnane, Optics Express **19**, 22470 (2011).
6. Q. Li, K. Hoogeboom-Pot, D. Nardi, M. Murnane, H. Kapteyn, M. Siemens, E. Anderson, O. Hellwig, B. Gurney, R. Yang, K. Nelson, Physical Review B **85**, 195431 (2012).
7. S. Mathias, C. La-O-Vorakiat, P. Grychtol, J. Shaw, R. Adam, H. Nembach, M. Siemens, S. Eich, C. Schneider, T. Silva, M. Aeschlimann, H. Kapteyn, M. Murnane, PNAS **109**, 4792 (2012).
8. D. Rudolf, C. La-O-Vorakiat, M. Battiato, R. Adam, J.M. Shaw, E. Turgut, P. Maldonado, S. Mathias, P. Grychtol, H.T. Nembach, T.J. Silva, M. Aeschlimann, H.C. Kapteyn, M.M. Murnane, C.M. Schneider, P.M. Oppeneer, Nature Communications **3**, 1037 (2012).
9. C. Thomsen, H. Grahn, J. Maris, J. Tauc, Opt. Comm. **60**, 55 (1986).

Keywords

EUV, acoustics, metrology, imaging

6–2

THE UNIQUENESS AND IMPACT OF USING NEUTRONS TO CHARACTERIZE SEMICONDUCTOR MATERIALS

R. Gregory Downing

National Institute of Standards and Technology, Chemical Science Division,
100 Bureau Drive, Gaithersburg, MD 20899

INTRODUCTION

Semiconductor technology requires a host of complimentary metrological tools to support device development, product yield, and quality control. Mechanical and radiation probes extract information on the smallest domains and defects in the materials that define the devices, while supporting research and sustaining production. One of the lesser known and therefore lesser used metrological probes in the study of semiconductor materials is the neutron. This particle has metrological properties that complement those of the electron and photon and often give unique insight into material structure and composition. Although applications of the neutron to semiconductor studies extends back many decades, described here are a few recent applications of neutron beams and neutron fields to inform and stimulate thinking on how this radiation probe might benefit future development of semiconductors.

THE NEUTRON

The neutron has no measureable charge, a mass slightly greater than the proton, and a weak magnetic moment. Neutrons interact with the atomic nucleus and are insensitive to the electron density in the material. Consequently the interactions of a neutron with matter are primarily confined to short-range nuclear and magnetic properties. Since the interaction probability is typically small, neutrons penetrate bulk materials rather well. Low energy neutrons are used much like photons for their wave properties. A thermal neutron corresponds to ≈25 meV in energy or 0.18 nm wavelength. Moderating the neutrons to lower energies can extend the wavelength to greater than 2 nm in wavelength. This wavelength regime is conveniently suited for the study of atomic and molecular structures over relatively long distances. Furthermore, the neutron can be reflected by surfaces at low glancing angles enabling the study of the near surface structure of matter. The neutrons scatter from specific nuclei in samples or by the magnetic moments associated with unpaired electron spins in magnetic samples and corresponding strength. Of particular value to the study of polymer coatings, neutrons interact in marked contrast with hydrogen versus deuterium even though chemically they are essentially equivalent. Moreover, since neutron beams are low in energy compared to x-ray or electron beams, neutron probes do not typically increase sample temperatures under investigation whether solid, liquid, or otherwise. These advantageous properties enable researchers to use neutrons for uniquely exploring bulk matter, surface structures, and dynamics.

6–2

APPLICATIONS

Neutron applications for the treatment and characterization of semiconductors have continued since the 1940's. The electrical character of bulk semiconductor materials is precisely controlled by neutron transmutation doping. Likewise, neuron activation analysis (NAA), prompt gamma activation analysis (PGAA), and neutron depth profiling (NDP) have long been used worldwide to characterize the presence of trace contaminates or to establish the total analyte mass in reference materials. NIST sells a number of SRMs of importance to semiconductor industry that are certified using these nuclear techniques including; SRM 2133 Phosphorous implant in Silicon Depth Profile, SRM 2134 Arsenic in Silicon, and SRM 2137 Boron implant in Silicon Depth Profile.

Low-level nuclear radiation is nearly unavoidable in the environment, especially near the Earth's surface. Neutron radiation dominates at inducing soft error upsets (SEU) in semiconductor devices (1) and the effect is exacerbated as device sizes continue to decrease. This discovery has lead to use of custom isotopic compositions in critical semiconductor materials to minimize neutron induced faults. On the other hand, artificial radioactivity introduced as radiotracers (2) in metrological studies monitors atomic migration in devices due to thermal and electrical forces.

Some neutron probe applications are perhaps not so well known to the semiconductor community but are making substantial contributions to the understanding of semiconductor materials. One such technique used with a number of variations includes the neutron scattering technique neutron reflectometry (NR).

Prabhu, et al. (3) applied neutron reflectivity for the first time to understand how photoresist swelling during development correlates to resolution and line edge roughness (LER). The reflected waves in a neutron measurement display subnanometer profile resolution as a result of the wavelengths used e. g., 0.475 nm for one of cold neutron reflectometer at the NIST Center for Neutron Research (NCNR). The challenges in photoresist characterization are of the order of nanometers scale, so neutron reflectivity is capable of resolving the area-average density of the roughness or composition depth profile in the latent and developed phases. The neutron atomic scattering length varies randomly from element to element. However the coherent scattering contrast from hydrogen can be substantially enhanced if hydrogen in known portions of the resist is substituted by the use of deuterium. Neutron reflectivity is used to observe the chemical gradient, the in-plane roughness, and the interfacial structure during photoresist development. The structures are analyzed leading to better photoresist chemistry to achieve better control of device features.

Taking advantage of the magnetic moment character of the neutron, Klose, et al., used spin-polarized neutron reflectometry to probe magnetic recording media. (4) They observed long-range spin-triplet supercurrents in Josephson junctions containing ferromagnetic materials. Specifically they showed that the supercurrent was enhanced by 20 times after subjecting their sample to large in-plane magnetic fields. This occurs because the of "spin-flop" transition in the sample of Co/Ru/Co synthetic antiferromagnetic with two outer thin ferromagnetic layers composed of either pure Ni or a PdNi alloy. Polarized neutron reflectometry revealed the two Co layer magnetizations end up nearly perpendicular to the magnetization of the two thin ferromagnetic layers. Furthermore, the nuclear profiles agree well with the data obtained from scanning electron microscopy with polarization analysis.

Kirby, et al., (5) also applied polarized neutron reflectometry to the study of field dependent magnetization of Co/Pt multilayers patterned onto nanoporous alumina substrates. The technique distinguishes the character of magnetization in the surface multilayer from the magnetic state of the material deposited into the nanopores. Moreover, they were able to determine variations in the nuclear and magnetic profiles as a function of the aspect ratio and depth into the nanopores. Using polarized neutron reflectometry this work exposed

6–2

the complexities of magnetic order in nanoporous heterostructures.

Beyond the few examples discussed above the range of semiconductor materials being studied using neutron techniques is ever expanding. Neutron diffraction techniques applied to II-VI semiconductor compounds doped with magnetically active ions (6) have uncovered near-spherical (<10 nm) local nanodistortions of the crystal lattice. Other fields benefiting from the use of neutron probes include optoelectronics, photovoltaics, semiconducting organic films, sensors, packaging, and so forth, limited only by the knowledge of the researcher in the neutron tools available.

There is a present day shortage of neutron beam time available for researchers at the limited number of neutron facilities. This shortage is recognized worldwide and is leading to the construction of new fission and spallation neutron facilities so that the unique abilities neutron probes offer to material scientists can be leveraged into new knowledge of semiconductor materials. The last decade has seen marked development of existing neutron instruments and new instruments are appearing as improved neutron optics and detectors are brought online. Researchers into semiconductor materials and properties will benefit greatly from these tools.

References

1. J.D. Dirk, M.E. Nelson, J.F. Ziegler, A. Thompson, and T.H. Zabel, IEEE Trans. Nucl. Sci. **50**(6) 2060-2064 (2003)
2. H. Wolf, J. Kronenberg, F. Wagner, M. Deicher, Th. Wichert, and ISOLDE Collaboration, *Appl. Phys. Lett.* **100**, 171915 (2012)
3. V.M. Prabhu, S. Kang, D.L. VanderHart, S.K. Satija, E.K. Lin, and W-l. Wu, Adv. *Matls*. **XX**, 1-21 [2010]
4. C. Klose, T.S. Khaire, Y. Wang, W.P. Pratt, Jr., N.O. Birge, B.J. McMorran, T.P. Ginley, J.A. Borchers, B.J. Kirby, B.B. Maranville, and J. Unguris, *Phys. Rev. Lett.* **108**, 127002 (2012)
5. B.J. Kirby, M.T. Rahman, R.K. Dumas, J.E. Davies, C.H. Lai, and K. Liu, *J. Appl. Lett*. **113** (2013) *In Press*
6. T.P. Surkova, S.F. Dubinin, V.I. Maximov and S.A. Lopez-Rivera, *Phys. Status Solidi*, **C9** 1830-1832 (2012)

Keywords

neutron, metrology, photoresists, magnetic structure, standards, depth profile

6–3

POSITRON ANNIHILATION SPECTROSCOPY FOR POROSIMETRY OF MICRO- AND MESO-POROUS SYSTEMS

R. Krause-Rehberg, M. Jungmann and S. Thraenert

Martin-Luther University Halle-Wittenberg, Inst. of Physics, 06099 Halle, Germany

INTRODUCTION

Positron annihilation has been used for decades to study the real and electronic structure of solids. Information on vacancy-type defects can be obtained. However, in dielectric media positrons can combine with an electron and form positronium (Ps) [1].

POSITRONIUM

Positronium as the lightest atom is formed in its singlet state as para-Ps (25%) and in the triplet state as ortho-Ps (75%). p-Ps has antiparallel spins and exhibit a very short lifetime of 125 ps which is not influenced by the host medium. It annihilates with two antiparallel gamma quanta of 511 keV each (m_0c^2). o-Ps has parallel spins and the lifetime in vacuum is 142 ns. It annihilates with three quanta summing up also to 1022 keV. In a medium, e.g. in a porous system o-Ps interacts with the pore walls and can exchange the electron to one with the opposite spin, i.e. forming p-Ps. This reduces the o-Ps lifetime distinctly. This process is called pick-off annihilation. In small pores the pick-off happens faster, i.e. the o-Ps lifetime becomes a unique function of the pore size.

This process can be described using quantum-mechanical models. The Tao-Eldrup model [2,3] takes into account only the ground state of Ps in a three-dimensional quantum well. It is valid to a pore size of 2 nm diameter. For larger pores, more sophisticated models include exited states of o-Ps and describe the whole size dependence up to a diameter of 100 nm where the vacuum lifetime of 142 ns is reached, e.g. [4].

POROSIMETRY USING O-PS

Fig. 1 shows the result of a calibration experiment were we studied controlled pore glass of a wide pore size range by positron annihilation [5]. The o-Ps lifetime τ_4 and the lifetime distribution σ_4 can be used to determine the pore size and the pore size distribution.

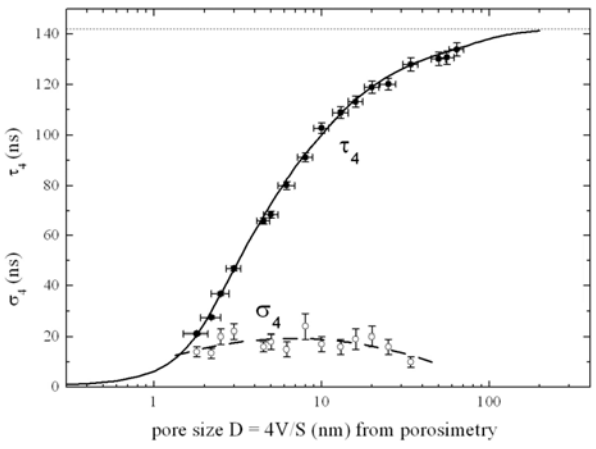


FIGURE 1. The o-Ps lifetime τ_4 and the lifetime distribution σ_4 obtained for controlled pore glass. The pores size was independently obtained by nitrogen absorption at 77K [5].

6–3

The pore size in Fig. 1 was obtained in parallel experiments using nitrogen adsorption at 77K. The sensitivity limit of positron annihilation ranges from micro- to mesopores, from about 0.3 nm to 40 nm pore diameter. In the talk, further examples of porosimetry in the field of low-k dielectric layers will be shown.

The Intense Slow Positron Source MePS at HZDR

Positrons can be obtained from radioactive isotopes such as 22-Na. However, the source strength is limited and the β^+ spectrum exhibits a broad energy distribution up to the maximum energy of 540 keV. This leads to a deep penetration into porous samples up to 1 mm. Thus, thin layers cannot be studied. However, positrons can be moderated e.g. at W surfaces to obtain a slow, monoenergetic positron beam [6]. To obtain a high intensity source, positrons are better obtained by pair production in a reactor or using bremsstrahlung in a target of a high-energy electron beam. The MePS system (Mono-energetic Positron System) at the ELBE accelerator center at the Helmholtz-Center Dresden-Rossendorf (HZDR) utilizes a pulsed 40-MeV electron beam to obtain slow positron by pair production which can be re-accelerated to get depth profiles of porous layers [7].

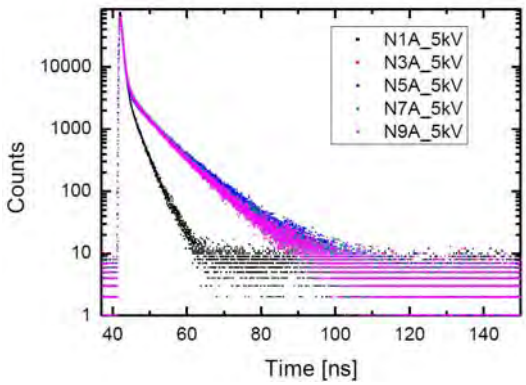


FIGURE 2. Positron lifetime spectra obtained using the MePS system at low-k layers at a depth of 450 nm.

Fig. 2 shows examples of positron lifetime spectra obtained for differently treated low-k dielectric layers of about 500 nm thickness at a positron energy of 5 keV corresponding to a mean penetration depth of 450 nm. From such data, the pore size distribution can be obtained as shown in Fig. 3.

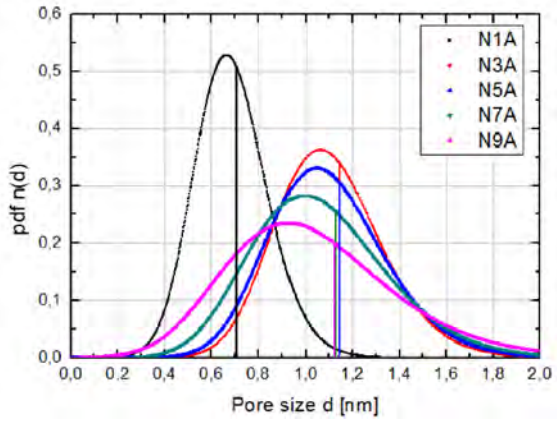


FIGURE 3. Pore size distribution obtained from positron lifetime spectra of Fig. 2.

References

1. Y. C. Jean, D. M. Schrader and P. E. Mallon, *Principles and applications of positron & positronium chemistry*, New Jersey, London; World Scientific, 2003.
2. S. J. Tao. *J. Chem. Phys.*, **56**, 5499 (1972).
3. M. Eldrup, D. Lightbody, J. N. Sherwood. *Chem. Phys.*, **63**, 51 (1981).
4. T. Goworek, K. Ciesielski, B. Jasinska and J. Wawryszczuk. Chem., *Phys. Lett.*, **272**, 91 (1997).
5. S. Thraenert, E. M. Hassan, D. Enke, D. Fuerst and R. Krause-Rehberg, *phys. stat. sol. (c)* **4**, 3819 (2007)
6. P. J. Schultz and K. G. Lynn. *Rev. Mod. Phys.*, **60**, 701 (1988).
7. R. Krause-Rehberg, G. Brauer, M. Jungmann, A. Krille, A. Rogov and K. Noack, *Applied Surface Science* **255**, 22 (2008) .

Keywords

porosimetry, micropores, mesopores, positron annihilation

6–4

NANOSCALE ELECTRICAL MICROSCOPY

Wilfried Vandervorst

IMEC

Abstract not available at time of press.

7–1

SCATTERFIELD MICROSCOPY, REVIEW OF TECHNIQUES THAT PUSH THE FUNDAMENTAL LIMITS OF OPTICAL DEFECT METROLOGY

Richard Silver, Bryan Barnes, Francois Goasmat, Hui Zhou, and Martin Sohn

National Institute of Standards and Technology, Gaithersburg MD

INTRODUCTION

The semiconductor manufacturing industry is now facing serious challenges in achieving defect detection rates with acceptable throughput and accuracy. With conventional bright-field and dark-field inspection methods now at their limits, it has become essential to explore alternative optical methods such as angle-resolved scatterfield microscopy, 193 nm short wavelength solutions, and coherent illumination. In this presentation we evaluate new optical technologies capable of extending high throughput defect inspection beyond the 22 nm node. We investigate source optimization for angle and polarization resolved illumination, measurement wavelengths down to 193 nm and a new approach for three-dimensional optical defect inspection validated with electromagnetic simulations and in the laboratory.

EXTENDING OPTICAL INSPECTION METHODS

A key to extending optical technologies is to engineer the illumination fields using only specific angles and polarization states that best enhance edge-based image analysis when combined with high numerical aperture (NA) imaging optics [1,2]. This approach can be applied to dense features that normally show only a "zero order" optical response. Multiple fixed-angle illumination configurations are evaluated to investigate performance gains from using specific spatial frequency components defined by dipole or more complex illumination.

ANGLE AND POLARIZATION RESOLVED-IMAGING

In the application of scatterfield microscopy to defect detection, the data are generally presented as a function of illumination angle and polarization [3]. As an aperture is scanned in the conjugate back focal plane, the illumination angle at the sample changes and an image is acquired for each illumination angle. This allows isolation of particular angles of illumination that best highlight the defects and give improved sensitivity.

The data in Fig 1 show an example of angle resolved illumination for a 22 nm node intentional defect array. The data show differential image simulations for different polarizations. Finite-difference time-domain (FDTD) simulations of both line-to-line and end-to-end defects with 15 nm critical dimensions were performed for λ = 193 nm using both transverse-electric (TE) and transverse-magnetic (TM) polarizations. Both the the polar (q) and azimuthal (f) angles were varied to assess all possible illuminations using our 193 nm tool. Defect detectability varied with polarization and angle at λ = 193 nm. The "Bx" and "By" defect orientations are orthogonal to each other, and the best polarization for each is TE and TM,

7–1

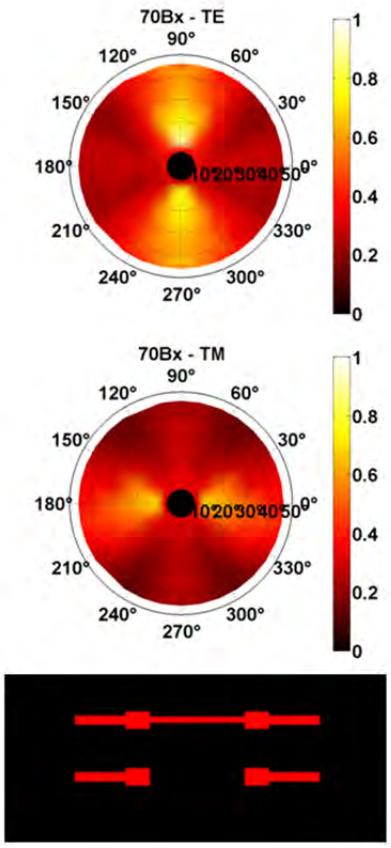


FIGURE 1. 15 nm nominal pitch bridge defect simulations at λ =193 nm. Detectability is plotted as a function of polarization s (TE), p (TM), and incident angle. The mean absolute intensity is the metric of the difference images. High azimuthal angles with s polarization show best detection.

Wavelength and Focus Sensitivity

We have completed comprehensive simulations for several defect types at wavelengths from 193 nm to 546 nm. An important result is that the optimum measurement wavelength depends on the materials stack. This is due to the different optical properties for each of the stacks. The absorption edges in the optical properties can change the optimum wavelength sensitivity. During the wavelength optimization specific attention was paid to evaluating 325 nm, 266nm and 193 nm wavelengths. The results summary is that 266 nm and 193 nm almost always outperform the longer wavelengths. However, there is not a clear winner between 193 nm and 266 nm since specific stack info affected the resolution limits and detectability.

In addition to wavelength optimization, there has been much recent work to utilize focus position [4]. In much of our previous published material, it was shown that best defect detectability is often found offset from the conventional best focus position. Another consistent trend is that defects nearly always exhibit a range of focus depth where the differential image defectivity grows in strength, forms a maximum at "best defect" focus, followed by a reduction in defect signal. The focus position optimization has recently led to a full 3-D analytical capability described in the next section.

3-D Defect Detection

We have implemented a powerful new method to fully utilize 3-D defect information [5]. A set of images are acquired in 100 nm focus increments to form a 4-D data set that is interpolated to form a dense volume of optical information. A differential "image" volume is then formed by aligning and subtracting a set of 4-D volumes. An example of a resulting 4-D differential volume plot showing X, Y, Z, and ΔI. is shown in Fig 2. A key advantage is we can now use 3-D filtering algorithms and include 3-D defect continuity.

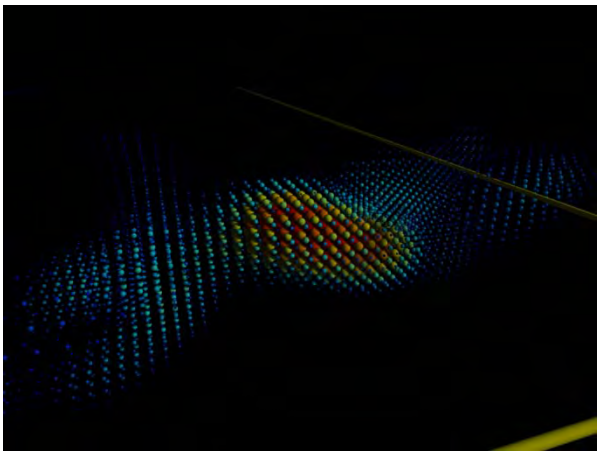


FIGURE 2. 4-D graphical representation of the simulated differential image from a defect.

7–1

DATA ACQUISITION: EXPERIMENTAL VALIDATION

NIST has developed a 193 nm excimer laser scatterfield microscope. The purged optical instrument sits on a custom air table that floats on a concrete slab suspension system. The main features include an angular scan mode and a full-field flexible illumination mode configurable with a variety of apertures such as a dipole. The fully custom 193 nm instrument has been described elsewhere in detail [6,7].

A set of experimental data acquired at 193 nm with a dipole illuminator is shown in Fig 3.

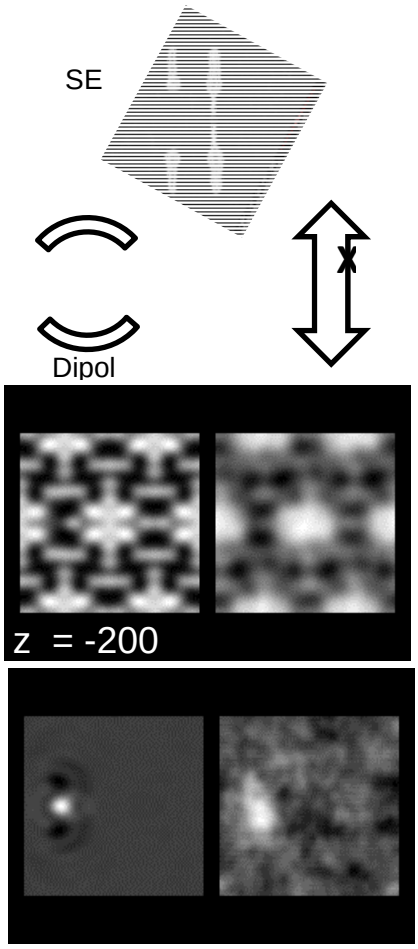


FIGURE 3. This figure shows simulation (left) to experiment (right) comparisons.

The data in Fig 3 are arranged with the actual images shown at -200 nm focus position and the differential intensity image was acquired with the polarization shown. The target imaged was a line-to-line defect nominally 70 % of the 22 nm node IDA design rule [3]. SEM analysis of smaller IDA design rule targets confirmed that actual defects as small as 15 nm were observed optically.

This paper evaluated a variety of new optical microscopy methods for defect inspection using simulation and experimental methods for the visible-to-DUV range. An important result of this paper is the evaluation and optimization of the key roles of wavelength, angle, polarization, and numerical aperture to extend optical methods. A key recent advance is a methodology that enables the full utilization of 3-D optical data. This new approach allows one to use full 3-D filtering and defect extraction techniques in addition to the significant gain in optical information in going from 2-D to full 3-D data acquisition and analysis.

ACKNOWLEDGEMENTS

The authors are indebted to Abraham Arceo and SEMATECH for wafer design and fabrication.

REFERENCES

1. T. Crimmins, *Proc. SPIE* **7638**, 76380H (2010).
2. R. M. Silver, B. Barnes, R. Attota, J. Jun, M. Stocker, E. Marx, and H. Patrick, *Appl. Optics*, **46**, 4248-4257 (2007).
3. B. Barnes, R. Quinthanilha, Y.-J. Sohn, H. Zhou, and R.M. Silver, Proc. SPIE **7971**, 79710D (2011).
4. R. Silver R. Attota, B. Barnes, and H. Zhou, "A Theoretical and Experimental Evaluation of Scatterfield Microscopy for use in Patterned Defect Inspection", Sematech Tech Transfer Doc (2007).
5. B.M. Barnes, Adv Litho San Jose, Proc SPIE 2013.
6. Y. J. Sohn, R. Quintanilha, L. Howard and R. M. Silver, *Proc. SPIE* **7272**, 72723T (2009).
7. Y. J. Sohn and R. Silver, *Proc. SPIE* **6518**, 65184V (2007).

KEYWORDS

Defect detection, illumination engineering, full 3-D reconstruction, electromagnetic modeling

7–2

FRONTIERS IN DEFECT DETECTION

Lothar Pfitzner, Sabrina Anger, Matthias Koitzsch, Markus Pfeffer, Georg Roeder, Martin Schellenberger

Fraunhofer Institute for Integrated Systems and Device Technology (IISB)
Schottkystrasse 10, 91058 Erlangen, Germany

INTRODUCTION

Micro- and nanoelectronics is still following the same lines and pace already recognized by Gordon Moore back in 1965 [1] . Strong increase in processing complexity requires growing efforts in tackling of the challenges in yield control. This also addresses the authors understanding of defects and defect detection. All of the defects shown below need to be identified and controlled to achieve and to increase the manufacturing yields.

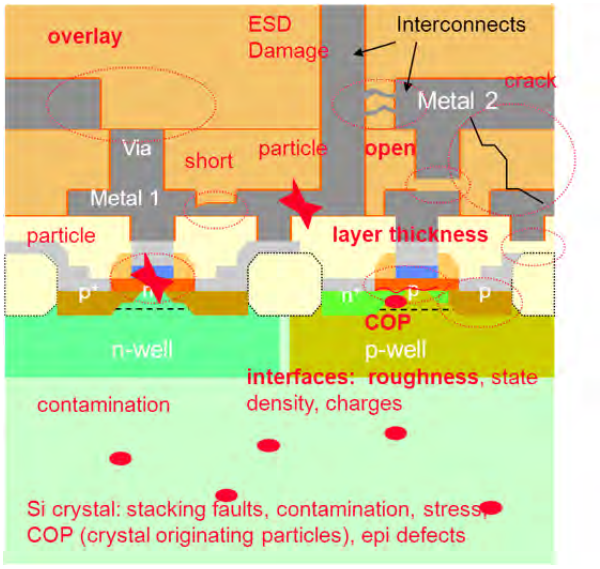


FIGURE 1. Examples of yield distracting defects possible during microelectronics production processes (source: ITRS YE chapter)

In addition, such challenges in defect detection are prevalent in every phase of the implementation of any new technology – in the process research and development phase, in pilot production and in the final high volume manufacturing. Certainly there are different levels of defect detection at such different levels of technology implementation, always kept to the minimum of indispensable control of physical, chemical caused and electrical defects.

YIELD ENHANCEMENT & ITRS

Defect detection has been one major scope within the context of ITRS yield enhancement activities in the last years. However, the focus of respective activities changed during the last five to ten years. Starting from initially concentrating on defect detection for leading edge technologies, the scope recently was extended in order to face the demands of broad applications. However, the challenge of keeping the in-line inspection costs low ever remains irrespective of the approached application. Since 2005 defect detection and classification mainly focused on the ability to detect and classify defects of sizes that scale as quickly or faster than the device features. A demand for increased sensitivity of

7–2

measurement with simultaneously enhanced differentiation between nuisance defects and killer defects was closely related to this objective. Moreover wafer edge inspection and development of respective inspection techniques became crucial in respect of yield loss. Whilst improvement of optical detection systems seemed to fulfill the demands of size shrinking, requirements for new generations of inspection tools were identified due to the introduction of 450 mm wafers in 2009. The need for improving quality and reducing the amount of measured data in order to maintain throughput and cost-effectiveness was closely linked to this progress. Continuous technology development furthermore necessitated improvement of 3D inspection. The challenges for defect characterization, inspection and analysis became even broader by facing the demands of broad applications, e.g. in the areas of "More Moore" and "More than Moore" technologies as well as power electronics, mechatronics and MEMS applications and appropriate packaging and assembly. Requirements arising from continuous shrinking of device dimensions and corresponding defect dimensions persist further on, thus frequently posing new challenges to defect detection and tolerable contaminations, but also to automated and intelligent data analysis. They are moreover supplemented with demands of inspections of patterns for assembly and packaging and 3D interconnects. In order to face these huge challenges despite of a lack of accordant measurement capacity, recent considerations regarding defect characterization, inspection and analysis within ITRS are heading for acquisitions of electrical characteristics of devices and determination of pass or fail characteristics of chips in addition to straightforward defect and contamination detection. Together with inclusion of statistical and systematical approaches for data analysis, this approach probably involves advantages in time and measuring possibility with relation to the broad range of requirements of recent technologies and applications.

Latest Equipment Developments

DEFECT INSPECTION TOOLS

State-of-the-art defect inspection tools which have been incorporated at the most advance fabs are able to review defects both in patterned and unpatterned wafers. Major defect inspection technologies comprise utilization of scanning electron microscopes (SEM), providing a pixel resolution below 3nm. But the variety of defect types makes defect root-cause analysis more and more difficult, so that image based defect analysis is limited, and defect material information gains importance.

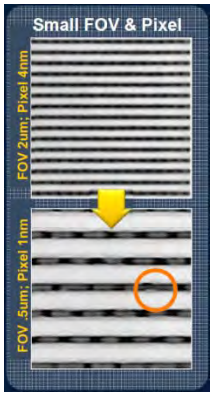


FIGURE 2. Improvement in defect detection by increase of pixel resolution (source: Applied Materials)

Therefore, the integration of additional material analysis detectors like EDX enables improved analysis of defect origin. For improved throughput and therefore reduction

7–2

of costs for defect inspection, solutions like the integration of multiple e-beam columns for parallel inspection of large wafer areas are introduced. Especially for the future introduction of 450mm wafer processing, this ability will gain more and more importance.

GI-SAXS

Additionally, the utilization of novel functional layers like porous low-k materials and complex layer stacks requires new inspection techniques like GI-SAXS (Gracing-incident small-angle X-ray scattering), e.g. for monitoring of pore size distribution. In combination with traditional techniques like XRD and XRR, this will provide full characterization of thin layers and layer stacks in terms of film thickness, film density, and crystallographic properties, and therefore also allows drawbacks regarding defects. For improved throughput, those techniques are integrated into combined metrology platforms.

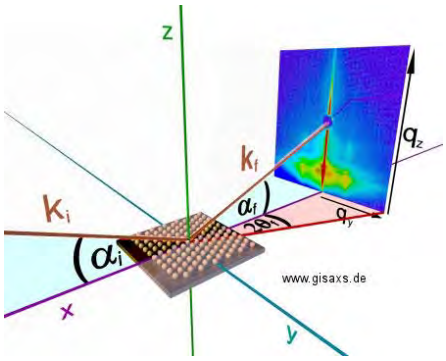


FIGURE 3. Principle of GI-SAXS inspection technique (source: Institute of Physical Chemistry - University of Hamburg)

VACUUM ULTRA-VIOLET (VUV)

Vacuum ultra-violet (VUV) spectroscopic reflectometry is a new measurement method, which extends the measurement wavelength region to the region below 200 nm down to 120 nm in commercially available systems. These wavelengths correspond to an excitation energy of 6.2 eV and 10.3 eV respectively, such that in typical high-k dielectric materials as well as SiO2, absorption processes play a significant role in the measurement whereas at conventional wavelength ranges (e.g. 250 nm and above) these materials are transparent. The inclusion of the information on the absorption (or extinction coefficient respectively) significantly enhances the sensitivity of the measurement and analysis to variations in multiple sample parameters i.e., film thickness, optical properties, and film composition at ultra-low film thicknesses (< 5 nm). A main application of the VUV reflectometry measurement is control of thickness and composition of nitraded SiO2 (SiON) layers and high-k materials which often comprise two components, e.g. HfO2/ZnO2. In contrast to alternative x-ray based methods, e.g. angle-resolved X-ray Photoelectron Spectroscopy reliable mapping inline measurements are possible at high throughput.

Due to its inherent sensitivity, VUV reflectometry is also sensitive to the presence of surface and environmental contamination. In the VUV reflectometer, these effects are controlled by specific instrument calibration procedures and measurement under vacuum and dry nitrogen atmosphere to enable stable measurements. Hence, thin contamination films, e.g. by adsorbed water films can be detected, monitored, and cleaned from the wafer surface such that measurement and analysis of films without surface contamination is possible.

At Fraunhofer IISB, a production worthy 200mm/300mm VUV reflectometer was thoroughly assessed. Optimized procedures and measurement strategies were developed for different dielectric materials, e.g. SiO2, Si3N4 and Al2O3 to further improve

7–2

measurement stability, detect, monitor and clean surface contamination films to reduce their influence on the measurement, and avoid potential layer modification by the VUV radiation. The applicability of the VUV method to quantify film composition was studied at the example of nitraded SiON layers using XPS measurements as reference method.

Makyoh Metrology Tool

One example for tool development dedicated to topography measurements is the "Makyoh"-sensor. The original "Makyoh" (magic mirror) method is qualitative and has been used for the detection of topography defects on semiconductor wafers for a long time. The method has been developed further to make quantitative topography measurements possible. The principle of structured illumination is used therefor. The evaluation of the distortion of a reflected projection pattern allows calculating the surface gradients. A prototype sensor was designed and built. Different means of illumination structuring like intensity coding or wavelength coding were introduced to gain an efficient tool for topography measurements with high resolution. With these new approaches it is possible to achieve a large measuring area. Thus a wafer can be measured with one single shot and high throughput. The focus is on the determination of nanotopography e.g. for the inspection of CMP wafers.

Virtual Metrology (VM)

Virtual Metrology (VM) is a powerful new method within other Advanced Process Control (APC) techniques to predict post process variables using process and wafer state information that could include upstream metrology and sensor data. In typical application scenarios, VM aims at the prediction of so called quality parameters, e.g. film thickness after deposition processes or trench depth in etch-process. VM is typically based on statistical or machine learning methods, and process or equipment models are trained from available data and then applied for prediction of quality parameters from new input. VM models may be adapted during application depending on the requirements induced by process changes, e.g. by drifts or maintenance actions. VM enables quality parameter predictions for every available data set and hence virtual metrology results are available for every wafer which significantly supports other APC applications such as run-to-run control or predictive maintenance of upcoming equipment failures or events, their root causes and corresponding maintenance tasks. A major strength of VM is that this technique may be also applied for the prediction of failures in processes which are not readily detectable from inline measurements, e.g. due to defect generation in the process, and the prediction of yield.

In several large European projects, Fraunhofer IISB developed VM concepts and algorithms, and significantly contributed to framework architectures for the application of VM. Within an ENIAC [a public private partnership program in nanoelectronics, see www.eniac.eu] project with the acronym IMPOVE, VM algorithms for the prediction of etch depth in a trench etch process were developed which enable etch depth prediction with an accuracy of better than 1%. Additionally, a framework architecture together with a software implementation were developed which enables the integration of VM in fabrication environments with different automation infrastructure. In the completed ENIAC project EEMI450 and the ongoing European Union FP7 [Framework programme

7–2

VII] project with the acronym SEAL, work aims at the closer application of VM on equipment level rather than on fab level. In EEMI450, concepts for the application of VM to control an RTP spike anneal process were developed. In SEAL, VM methods are studied at the example of a microwave plasma oxidation process to improve process models derived from individual DOEs and to include additional experimental results obtained during process development and equipment assessment.

Zero defect resizing of large crystalline silicon wafers with Thermal Laser Separation

Within the advent of "More than Moore" (MtM) devices, a novel separation technique will become important: zero defect resizing of large Si wafers. MtM devices are produced, e.g., by combining MEMS and CMOS devices [2] on wafer level. For that purpose, state-of-the-art 300 mm CMOS wafers have to be resized to a diameter of, e.g., 200 mm MEMS devices are currently produced on. This resizing process has to be clean, i.e., zero particles, and must not leave any damage like Haze or residual mechanical stress on the thus produced smaller wafers. The only possibility of resizing with zero defects is to use ablation free separation techniques. One promising technique – Thermal Laser Separation (TLS) – is currently being developed to meet requirements for zero defect resizing. TLS uses thermally induced mechanical stress to cleave crystalline wafers along a predefined line, e.g., a circular line. By doing so, small circular demo wafers could be produced out of large Si wafers [3]. Currently, TLS is being developed for producing alignment marks such as notches and flats on the cut-out wafer.

Summary

With this paper, the authors would like to give an overview and examples of innovative aspects of future metrology in all areas of defect detection and yield control strategies. Further details will be given in the paper presentation.

References

[1] Gordon E. Moore: "Cramming More Components onto Integrated Circuits", Proc. Of the IEEE, Voln 86, No. 1, Jan 1998/ Electronics Magazine Vol 38, No. 8, April 19, 1965

[2] H. Baltes, O. Brand, A. Hierlemann, D. Lange, C. Hagleitner: „CMOS MEMS – Present and Future", Sensors and Actuators 82, pp. 2-23, 2000

[3] M. Koitzsch, D. Lewke, M. Schellenberger, L. Pfitzner, H. Ryssel, H.-U. Zühlke:„Enhancements in Resizing Single Crystalline Silicon Wafers up to 450 mm by using Thermal Laser Separation", Proceedings of ASMC 2012, Saratoga Springs, NY, USA, pp. 336-341, 2012

Keywords

yield enhancement, ITRS, defects, inspection, x-ray, metrology, zero defect resizing

7–3

MIRROR ELECTRON MICROSCOPY FOR HIGH-SPEED AND HIGHLY SENSITIVE DEFECT INSPECTION

Masaki Hasegawa

Hitachi, Ltd., Central Research Laboratory

1-280, Higashi-koigakubo Kokubunji-shi, Tokyo, 185-8601 Japan

INTRODUCTION

Recent progress in electronic devices industry, such as continuous reduction of the critical dimensions of semiconductor electronic nano-circuits and the introduction of wide bandgap materials to the substrates of power devices, has required a breakthrough in the defect inspection technology. The capability of conventional inspection techniques using DUV light to provide sufficient detection sensitivity in the coming 10-nm era is being questioned. In the field of power devices, some crystal defects of wide bandgap materials that degrade the device reliability are not detected by using optical scattering and optical microscope techniques.

Although the scanning electron microscope (SEM) has been a candidate to overcome the resolution issue in the inspection techniques and to detect electric defects in LSI patterns, its low inspection speed and introduction of surface contamination and damage due to electron bombardment prevent the electron beam inspection technique from being widely used. A mirror electron microscope (MEM) was recently found to be a promising candidate to deal with these issues.[1-4] In this paper, we will explain the principle of MEM imaging and its properties for providing damage-less, highly sensitive, and high-speed image acquisition, and we will report on the MEM applications of defect detection for a modeled semiconductor pattern and an SiC epitaxial wafer.

MIRROR ELECTRON MICROSCOPE

Figure 1 is a schematic illustration of an electron optical system of a proof-of-concept MEM apparatus developed in our laboratory. Electrons from a Schottky-type electron source in the obliquely mounted electron gun are accelerated to 3 keV and focused by using the condenser lens. The electron beam after the lens is deflected onto the sample surface by the separator consisting of eight electro-magnetic poles. The focal point of the condenser lens is on a back focal plane of the electrostatic objective lens so that the electrons are directed normally onto a sample surface as a parallel electron bundle with a diameter of around 100 μm. The sample bias is adjusted to nearly equal to the accelerate voltage of the electrons so that the irradiated electrons are reflected in the opposite direction before reaching the sample surface. The objective lens forms an image of the reflected electrons on the center of the separator, and magnetic projection lenses magnify this image onto the fluorescent plate. The fluorescent image is captured by a CCD camera.

7–3

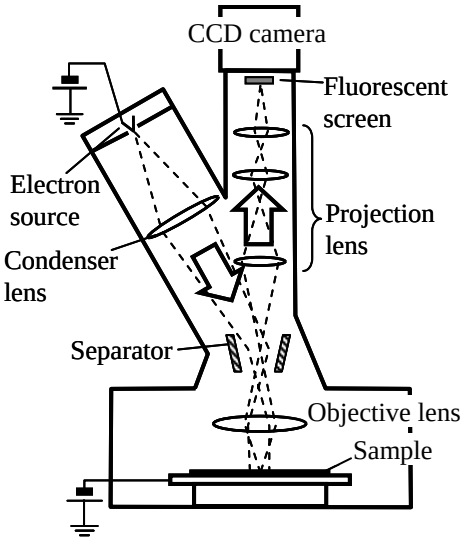


FIGURE 1. Schematic illustration of MEM developed at Hitachi Central Research Laboratory.

The contrast in a MEM image describes the topographical unevenness of an equipotential surface on which the incoming electrons are reflected. Figure 2 schematically shows the electron reflection trajectories near an uneven sample surface. If there is a pit on the surface (left in Fig. 2), the equipotential surface is concavely distorted along the pit. When there is a protrusion, the equipotential is convexly distorted (right in Fig. 2). When the incoming electrons with parallel trajectories are reflected onto the distorted equipotential surface, the reflected trajectories converge (left) or diverge (right) depending on the surface figure. When an object plane for the objective lens is above the sample surface (over-focus condition), a MEM image shows a bright point at the position of the pit (left) or a large darker spot at the protrusion (right), that is, these MEM images describe the topographical unevenness of the equipotential surface as a dark and bright contrast. When the object plane is under the sample surface (under-focus condition), the relations between the surface figure and the MEM contrast are reversed.

When electric charges are localized in a flat sample, the equipotential surfaces over the sample distort in the same way as the surface figure unevenness. As shown in Fig. 3., when there is a positive (left in Fig. 3.) or a negative charge concentration (right in Fig. 3.), the equipotential surfaces are concavely (left) or convexly (right), respectively distorted. A bright point appears at the positive charge concentration (left) and a dark spot at the negative charge concentration (right) in a MEM image when the objective lens is operated in the over-focus condition.

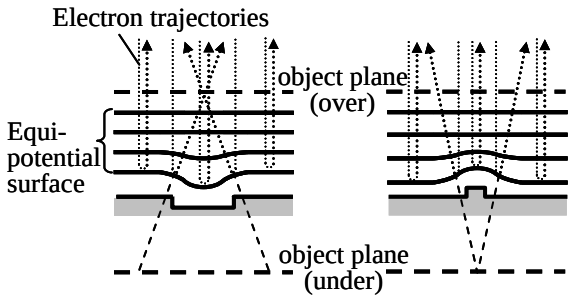


FIGURE 2. Electron trajectories near sample surface with topographic unevenness in MEM.

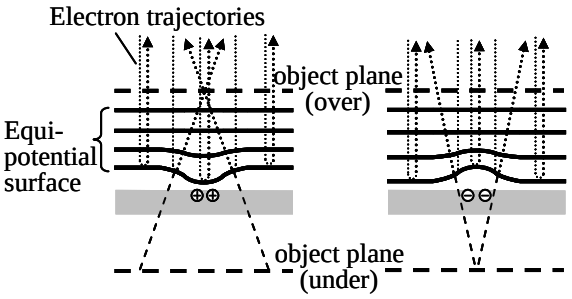


FIGURE 3. Electron trajectories near sample surface with local concentration of electric charges in MEM.

The image generation principle in the MEM explained above leads to advantages in terms of its application to defect inspection. At first, the MEM can acquire images for inspection without damaging of a sample because the electrons do not impinge the surface. Second, because a particle on a wafer distorts the equipotential in wider area than the size of the particle itself, MEM can detect it with a lower resolution for observing the particle, i.e. it can achieve higher inspection speed than a conventional SEM inspection apparatus preserving high sensitivity. Third, the MEM can detect a defect due to electrical imperfection in a semiconductor wafer or a nano-circuit on the wafer.

7–3

APPLICATIONS OF MEM

In the following paragraphs, we discuss some examples of MEM images acquired with our apparatus. These examples show promising MEM properties for next-generation inspection techniques.

PATTERN CD ERROR

Figure 4 shows a MEM image of an 80-nm line and space (L/S) patterned on Si that includes 16-nm built-in CD errors in their spaces. The inlet image is a SEM image of the CD error in the L/S. The pixel size of the image is 50 nm. MEM dose not resolve the L/S itself, but clearly shows CD errors with larger pixels than the space difference. This property emphasizing figure differences in the MEM imaging allows improving sensitivity and speed simultaneously in the pattern inspection.

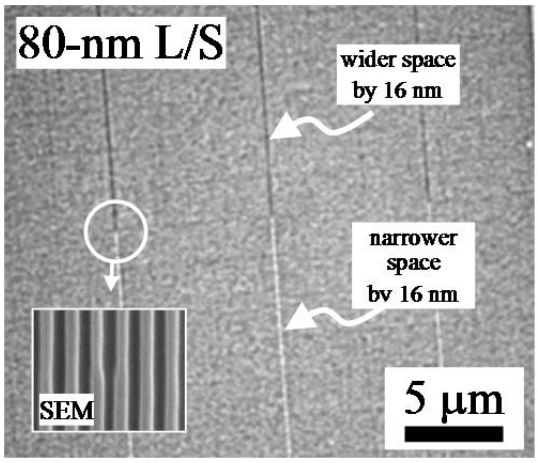


FIGURE 4. MEM image of Si 80-nm line and space pattern. The inlet is a SEM image of a built-in CD error. Pixel size of the MEM image is 50 nm.

CRYSTAL DEFECTS IN 4H-SIC WAFER

Figure 5 describes an example of MEM application in 4H-SiC crystal defect detection. An in-grown stacking fault (IGSF) in an epitaxial layer on 4H-SiC substrate appears in Fig. 5(a). The IGSF is buried in the layer as shown in Fig. 5(b). Since the MEM image was obtained under ultraviolet light irradiation, UV excited careers (electrons) are trapped on the IGSF. The dark triangle in Fig. 5(a) is formed by a convexly distorted surface equipotential although the sample surface above the IGSF is flat. This result shows that MEM can be used in crystal defect inspection without any damage on the surface.

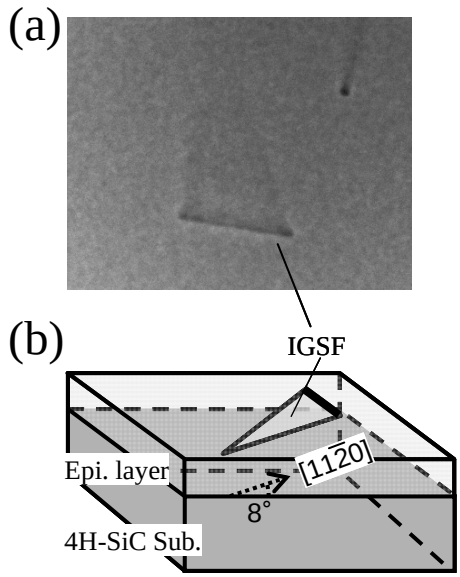


FIGURE 5. MEM image (a) of in-grown stacking fault (IGSF) in 4H-SiC epitaxitial wafer as schematically described in (b). The image was obtained under ultraviolet light irradiation.

REFERENCES

1. M. Hasegawa and T. Shimakura, *Mater. Res. Soc. Symp. Proc.* **1088**, 1008-W04-02 (2008).

2. T. Shimakura, Y. Takahashi, M. Sugaya, T. Ohnishi, M. Hasegawa, and H. Ohta, *Microelectron. Eng.* **85**, 1811-1814 (2008).

3. T. Shimakura, M. Hasegawa, H. Suzuki, and H. Ohta, *Proc. of SPIE* **7823**, 78230Q-1 (2010).

4. M. Hasegawa and T. Ohno, *J. Appl. Phys.* **110**, 073507 (2011).

KEYWORDS

mirror electron microscope, defect inspection, non-destructive, surface electric potential, cd error, SiC, crystal defect

8–1

CRITICAL METROLOGY FOR ADVANCED CMOS MANUFACTURING

Markus Kuhn, Ying Zhou and Zhiyong Ma

Corporate Quality Network, Intel Corporation
2501 NW 229th Ave, Hillsboro, Oregon 97124

INTRODUCTION

Advanced CMOS technology development has evolved from the use of geometric scaling to the introduction of novel devices, new materials and non-planar architectures. These inclusions have added significant complexity to all aspects of process development and also to the fab and lab metrologies that support the development and manufacturing of those processes.

TECHNOLOGY TRENDS

Recent technology enhancements such as strained Si, metal gate/high k, 3D transistors, immersion lithography, etc. [1-4] have introduced a new set of critical process and material parameters that require increasingly precise measurement and control. Examples of such measurements include imaging and quantification of 3D transistor dimensional parameters (Figure 1), nano-scale channel strain (Figure 2), ultrathin film properties (including composition, structure, defects and contamination), and overall patterning/etch morphology.

Transistor and thin film scaling has also resulted in an increased sensitivity to more subtle process variations which need to be evaluated at the transistor, die and wafer levels (Figure 3).

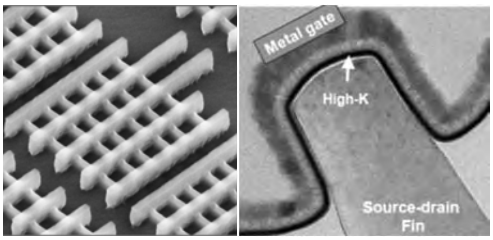


FIGURE 1. 22nm 3D transistors. Added dimension results in significantly higher amount of imaging required to elucidate critical device parameters.

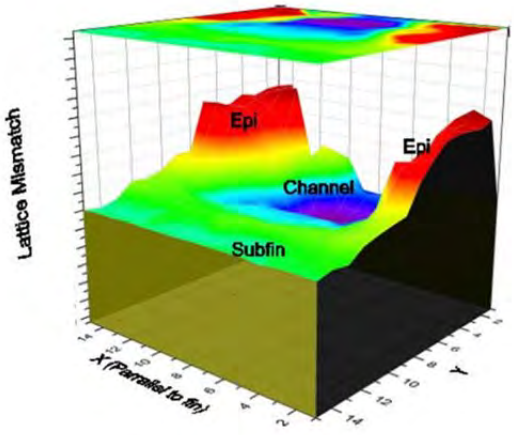


FIGURE 2. 2D strain map of 22nm 3D transistor.

8–1

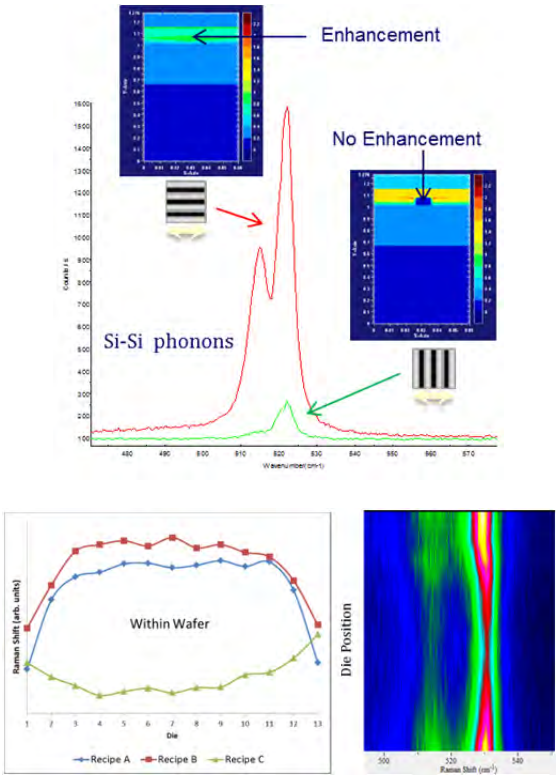


FIGURE 3. Due to field enhancement effects, UV Raman has the potential capability to perform rapid wafer level strain measurements on 3D device arrays.

Future technology nodes will include further scaling of the transistor architecture, continued introduction of novel and atomically-scaled films, and a shift to 450mm processing which will all contribute to increased process variation and the need to understand and control much more subtle process interactions.

There is a distinct and growing gap between existing metrology capabilities and those required for advanced CMOS process manufacturing.

LAB-BASED METROLOGY

Labs are traditionally expected to provide fundamental understanding through the development and application of state of the art scientific metrology capabilities. However, when process control is not feasible with inline fab metrology tools, the labs are increasingly tasked to also provide dedicated metrology support in a manufacturing environment even though these tools are not designed for that. Figure 4 shows lab demand has increased tremendously over the past 10 years as technology continued to scale from 90nm to <22nm nodes.

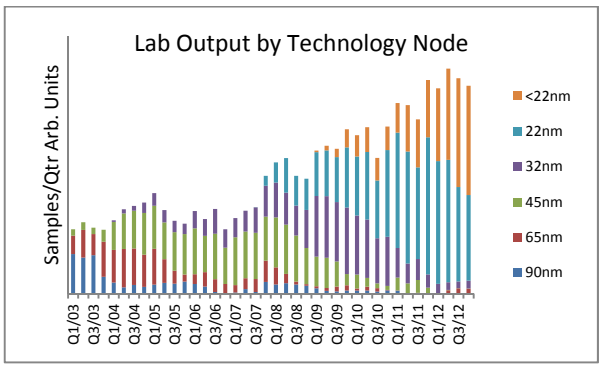


FIGURE 4. Output for one of the Intel Labs over past 10 years showing significant increase in imaging and materials characterization demand with recent technology nodes.

Closer examination of these trends shows that the increased metrology demand is driven by four main factors:

1) Dimensional metrology. Imaging needs are significantly higher with the introduction of non-planar transistors and an increased number of critical transistor parameters (see Figure 1);

2) Ultrathin film characterization. Driven by the introduction of novel ultrathin films, coupled with the increased complexity associated with non-planar device structures;

3) Lab-based fab process control. Limitations in inline fab metrology, particularly in the aforementioned areas, has required dedicated process control support from lab systems;

4) Multiple Analyses. Increased complexity requires more extensive and diverse analytical support, i.e. more integrated problem solving.

8–1

Typically lab-based metrology measurements can provide the needed technical capabilities but do not meet the operational requirements, without significant infrastructure investment.

EMERGING METROLOGY NEEDS

The difference between traditional fab and lab metrology has become increasingly blurred as there is an increased dependence on lab data for direct process control due to the fact that inline metrology tool capability is lagging behind what's needed in today's CMOS manufacturing. Therefore no distinction should be made between the requirements for lab and fab-based metrology tools and they should be treated holistically.

The advanced CMOS manufacturing environment is changing rapidly and new measurement requirements are constantly emerging, driven by an increasing array of technology enhancement options. Continued physical scaling is also driving an increased need to better control existing process/material parameters. Rapid understanding of the process variation and its subtle interactions is crucial, info turn and precision are key.

Of particular concern is the growing need for nano- and atomic-scale dimensional measurements to provide morphological, structural and chemical measurements all on a "real time basis". 3D architectures and film scaling result in complex systems with many overlapping features, driving the need for near-atomic tomographic imaging solutions. Similarly, measuring composition of these complex 3D structures requires continued advancement in emerging analytical fields such as atom probe tomography and hyper spectral imaging.

Also of concern is a general lack of measurement capability suitable for manufacturing monitoring to ascertain ultrathin and atomically-scaled film properties including their structure, composition, strain, and mechanical properties, etc. The diversity of these films is increasing dramatically as they are being introduced to replace traditional transistor building blocks, including the gate electrode, the method of introducing dopants and the channel material itself.

Lastly, the emergence of non-CMOS options, with a new set of exotic materials and device architectures also needs to be considered and will require their own unique metrology needs.

Analytical capability such as resolution and sensitivity may be the foremost priority for academic research pursuit but is not necessarily the only selection criterion for a manufacturing metrology choice. In addition to the fundamental capability requirement for a given measurement, the chosen metrology platform ideally must be highly parallel and automated, offers high precision, high quality and timely data meeting factory info turn needs.

SUMMARY

The insatiable need for more transistors and functionality at low power will drive continued pursuit for innovations in nanoelectronics. These innovations are increasingly about new device or interconnect architectures, novel materials and integration schemes. Metrology will continue to play a pivotal role in enabling these technology discoveries and breakthroughs and sustaining high yielding and high volume manufacturing.

REFERENCES

1. T. Ghani, *Electron Devices Meeting, IEDM '03 Technical Digest. IEEE International*, 11.6.1 - 11.6.3 (2003).
2. K. Mistry, *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 247-250 (2003).
3. C-H Jan, *Electron Devices Meeting, 2012. IEDM 2012. IEEE International*, 44-47 (2012).
4. S. Natarjan, *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 1-3 (2008).

KEYWORDS

Materials, characterization, CMOS, manufacturing

A VERSATILE VARIABLE FIELD MODULE FOR ASYLUM CYPHER SCANNING PROBE SYSTEM

Hongxue Liu, Ryan Comes, Jiwei Lu and Stuart Wolf

Department of Materials Science and Engineering, University of Virginia, Charlottesville, VA 22904

Jim Hodgson and Maarten Rutgers

Asylum Research, Santa Barbara, CA 93117

INTRODUCTION

With the rapid progress of nanotechnologies, atomic force microscopy (AFM) has become one of the most widely used techniques for imaging, measuring and manipulating various characteristics of materials at the nanoscale. However, there are very limited options for the characterization of multiferroic samples with simultaneous electric and magnetic stimuli. In this work, we demonstrate a versatile variable field module (VFM) with magnetic field up to 1800 Oe built for the Asylum Research Cypher system. The capability of the VFM system is demonstrated by degaussing a floppy disk media with increasing magnetic field. The written bits are erased at about 850 Oe. Angular dependent measurements clearly show the evolution of the magnetic domain structures. A completely reversible magnetic force microscopy (MFM) phase contrast image appears when the magnetic field is rotated by 180°. A further demonstration of magnetic switching of $CoFe_2O_4$ pillars in $CoFe_2O_4$-$BiFeO_3$ nanocomposites will be presented and field dependent MFM and piezoresponse force microscopy (PFM) will be discussed.

SYSTEM DESIGN

Figure 1 shows the actual picture of the VFM mounted on Cypher AFM (Asylum Research). The module consists of several integral parts including a rotating shaft to which a strong rare earth magnet is attached, a micrometer with both X and Y adjustments, and a mounting stage to attach the rotating shaft to the micrometer. The basic principle of the design is to change the magnetic field strength of the scanning area under the probe tip by adjusting the distance between the probe tip and a permanent magnet. The magnetic field vector can be readily changed by rotating the magnet. In order to quantitatively determine the magnetic field, a sample post with a built-in hall sensor right under the probe tip is fabricated. The hall sensor is calibrated with known magnetic fields.

In order to reach high magnetic fields, the magnet needs be placed near the probe tip, as close as possible. This leads to some limitations and design compromise due to the way that AFM works which relies on laser reflection from the top surface of the cantilever to measure the deflection of the cantilever. The magnet, when placed too close to the tip, will readily block the laser reflection and thus interfere with the operation. In this case, the smaller the size of the magnet, the closer the magnet can be placed to the probe tip. On the other hand, too short a distance between tip and magnet limits the scan region to the edge of a sample which is probably not the best place for characterizing the sample. In this case, a larger size magnet is preferred since it can extend the field to a higher value and also has better field resolution along the

WE–01

length. For these reasons, a 1/4" cubic neodymium magnet (Grade N52, K&J Magnetics) is chosen which gives magnetic fields up to 1800 Oe without affecting the operation of the Cypher AFM. Due to the limited adjustment range of the micrometer, there are several soft lock positions of the rotating shaft relative to the mounting stage along the X-direction to extend the range of distance of the magnet from the probe tip. This produces magnetic fields from less than 100 Oe to 1800 Oe.

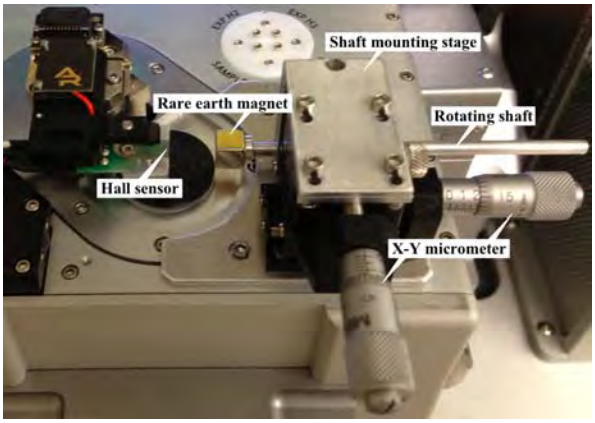


FIGURE 1. VFM module installed in Cypher system.

TEST RESULTS

The capability of the VFM system is tested by degaussing a floppy disk media. The field dependent magnetic properties of the floppy disk media measured at 300 K show it has a strong in-plane magnetic anisotropy. Figure 2 (a-d) show the MFM images taken under different magnetic fields. The distinct blue and red stripe contrast in the MFM image taken without magnetic field clearly represents the magnetic bit profile. After applying increasing in-plane magnetic fields, the stripe contrast starts to disappear, indicating that the magnetic bit profile is progressively destroyed. The written bits are erased at around 850 Oe, close to the coercivity of 830 Oe determined from the M-H curve in Fig. 2. With further increasing fields up to 1750 Oe, no significant changes of phase contrast and roughness were observed, indicating the magnetization was quickly uniformly aligned. Figure 2 (e-h) show the angular dependent MFM images taken under 1750 Oe, clearly demonstrating the evolution of magnetic domain structures under fields with different rotation angles relative to the original in-plane fields used for degaussing. A completely reversible MFM phase contrast is observed when the field is rotated by 180°.

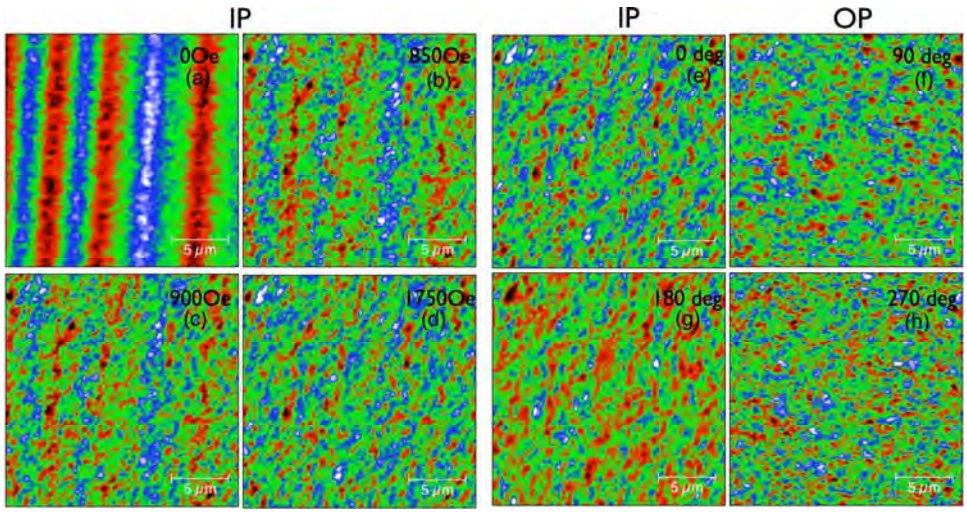


FIGURE 2. MFM phase images of a floppy disk media taken (a) before applying magnetic field, after applying in-plane fields of (b)850 Oe, (c) 900 Oe, (d) 1750 Oe, and (e - h) angular dependent MFM images taken at 1750 Oe.

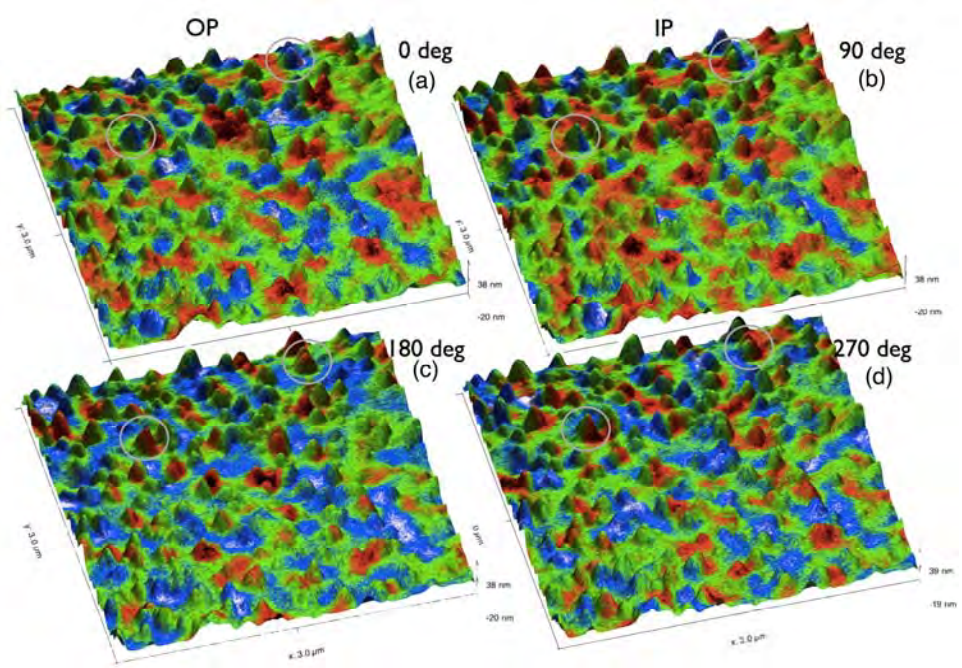


FIGURE 3. MFM phase images of a CFO/BFO composite film taken at (a, c) out-of-plane magnetic field, (b, d) in-plane magnetic field. The applied magnetic field is 1750 Oe.

Fig. 3 (a, c) and (b, d) show the MFM images of a CFO/BFO composite film grown on STO (001) substrate co-deposited by pulsed electron deposition (PED), after applying magnetic fields in the out-of-plane and in-plane directions, respectively. While a uniform out-of-plane or in-plane magnetization can not be explicitly determined and perfectly matched to the height profile of CFO pillars, the magnetization of some CFO pillars is clearly switched to either out-of-plane or in-plane dependent on the applied field vector directions, as shown in the reversible blue and red contract marked in several circle areas. The difference of MFM images under out-of-plane and in-plane magnetic fields is also clearly observed. The absence of uniform magnetization along the applied field is not clear but can be ascribed to the following reasons. First the pillar density (pillar distance), size, and aspect ratio in a co-deposited sample do not have a perfect uniformity, which means microscopically not all the CFO pillars have the same magnetic characteristics (coercivity, anisotropy) measured macroscopically by a vibrating sample magnetometer. Some of the pillars with larger coercivities need higher magnetic fields to switch. Second the magnetic exchange interaction between very close CFO pillars can be strong and complicate things further. We are currently working with the team at University of Alabama whose expertise in micromagnetic simulation will help us understand the magnetic switching process and properties.

In summary, we demonstrated a versatile variable field module (VFM) with magnetic field up to 1800 Oe for the Asylum Research Cypher system. The magnetic field is changed by adjusting the distance between the probe tip and a rare earth magnet, and the magnetic field vector is changed by rotating the magnet. The field dependence and angular dependence measurement capabilities of the VFM system are successfully demonstrated by degaussing a floppy disk media with increasing magnetic field. VFM can be used in combination with MFM and PFM to investigate the in-situ electric assisted magnetization reversal process in multiferrioc nanocomposites.

KEYWORDS

Atomic Force Microscopy, Multiferroics, Magnetic Force Microscopy.

WE–02

METROLOGY FOR ORGANIC MONOLAYERS ON COBALT SURFACES[1]

S. Pookpanratana[a], L. K. Lydecker[a,b], H.-J. Jang[a], C. A. Richter[a], and C. A. Hacker[a]

[a] *Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, 100 Bureau Drive Stop 8120, Gaithersburg, MD 20899-8120*

[b] *College of Nanoscale Science and Engineering, University at Albany, 257 Fuller Road, Albany, NY 12203*

INTRODUCTION

The organic electronics field has grown exponentially in the last 10 years due to applications for light emitting diodes and solar cells [2]. The incorporation of organic materials for spintronic devices is a research thrust for next generation electronic devices.

The molecule-metal electrode interface is crucial for the realization of organic spintronics. It has been suggested that this interface governs the tunneling of electron spin across a ferromagnetic metal into an organic semiconductor [3]. A challenge to control this interface lies with the lack of control of the interface composition (i. e., oxide formation) between the molecular layer and metal. Previously, electrochemically prepared oxide-free ferromagnetic surfaces have been used for molecular self-assembly [4] [5]. Recently, phosphonic acid-based molecules were self-assembled onto (La,Sr)MnO_2 (LSMO) without an electrochemical step, to create a LSMO/molecule/LSMO junction where the molecules served as a tunneling barrier [6]. Critical metrology questions involve characterization and control of the interface formation between organic materials and the ferromagnetic electrode for the advancement of organic spintronics.

Template-stripped Co surfaces and self-assembled monolayers (SAMs) are used to engineer the molecule-cobalt interface, and the surfaces are physically characterized to determine parameters that influence the interface formation. Microscopy was used to confirm the Co surface topography and its suitability for SAM formation. Chemically-sensitive X-ray and infrared spectroscopies are used to identify the Co chemical structure (i. e., extent of oxidation) and the molecular structure of the SAMs, respectively. Materials characterization tools are used to identify the challenges and assess the progress of preparing the organic-cobalt interface.

EXPERIMENTAL

Template-stripped cobalt layers were initially prepared on fluorine-treated (F1) silicon wafers by physical vapor deposition (PVD) and referred to as treated-Si (tSi) [7]. Co (50 nm) was evaporated onto tSi by electron-beam deposition (P = 2.66E-4 Pa or or lower). For some samples, Au (100 nm) was sequentially evaporated afterwards within the same chamber (i. e., without breaking vacuum). Finally, the polyethylene terephthalate (PET) substrate was laminated to the (Au)/Co/tSi surface using a commercial imprinting tool.

Self-assembly of octadecanethiol (ODT) and mercaptohexadecanethiol MHA (1 mmol/L concentration in ethanol) was performed in a N_2-purged glovebox. ODT serves as the "fruit fly" molecule since it has been studied extensively on Au surfaces. MHA is chosen because the thiol and carboxylic acid ends provide a test for selective attachment on Co surfaces. The PET/(Au)/Co/tSi substrates were transferred to the glovebox, where

the Co/(Au)/PET was stripped off from the tSi, and the Co/(Au)/PET was immediately placed in the prepared solutions. Atomic force microscopy (AFM) was used to characterize the surface topography of the template-stripped cobalt. Molecular self-assembly was directly confirmed using reflection absorption infrared (RAIRS) and X-ray photoelectron (XPS) spectroscopies.

Results And Discussion

An AFM image of the template-stripped cobalt surface is shown in fig. 1. The surface exhibits regions of gaps (dark spots in fig. 1). The root-mean-square roughness of the Co surface is 1.3 nm. We speculate that the gaps are likely due to the uneven stripping of the Co layer from the tSi surface, and are discussed again with our XPS findings below. Uneven stripping occurs when the Co adhesion to the tSi is too large and is evidenced by some F1 molecules on the Co surface and Co on the tSi surface. The increased Co adhesion is likely due to impurities in the F1 molecular layer; either defects or regions of multilayer formation. The slight variation of the Si surface could affect the final topography of the Co surface.

Infrared spectroscopy confirmed the molecular presence of ODT and MHA on freshly stripped Co/Au/PET. In fig. 2, RAIRS was used to identify the C-H bonds in ODT and MHA, and confirm molecular assembly on the Co surfaces. Also, spectra of ODT and MHA self-assembled onto Au are shown in fig. 2 as a reference. The C-H stretches (υ_{asym} and υ_{sym}, dashed lines in fig. 2) of the alkyl backbone are observed in the molecular layers assembled on the Co/Au/PET samples. The absorbance intensities of υ_{asym} and υ_{sym} of ODT and MHA on Co are comparable to those on Au, which indicates similar packing density on both surfaces. The C-H stretches representative of the terminal methyl group (marked as asterisks in fig. 2) is not apparent in the spectrum of ODT on Co when compared to on Au. The methyl υ_{asym} C-H stretch is likely the small feature in the ODT/Co spectrum at 2957 cm^{-1} (shifted from 2964 cm^{-1} in the ODT/Au spectrum). It's possible that the tilt of the ODT molecules on Co differs from Au, tilting the -CH_3 group away from the surface normal and thus difficult to identify in reflection IR due to the IR surface selection rules. The C=O stretch (not shown) from the carboxylic acid group is not present for MHA/Co. The absence of the C=O feature indicates that the MHA assembly on Co can be by either the thiol or carboxylic acid group. The lack of bonding selectivity adds complexity for incorporating bifunctional molecules onto Co surfaces.

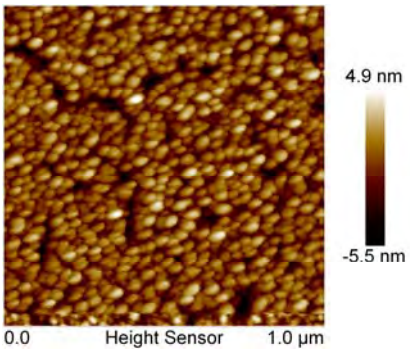


FIGURE 1. AFM image of the template stripped PET/Au/Co surface.

We use XPS to directly assess the chemical composition of the template-stripped Co surfaces before and after self-assembly. In fig. 3, the stripped Co surface (bottom spectrum) has undergone some oxidation as indicated by the O 1s signal and Co 2p mutliplet peaks (detail not shown). The oxidation could have occurred during the evaporation process or after the stripping process. The surface also has photoemission signals arising from F and C which

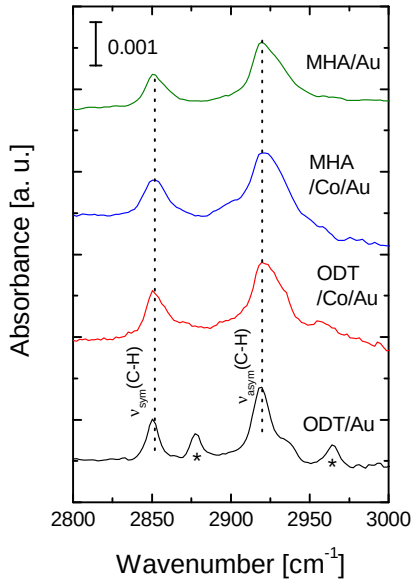


FIGURE 2. RAIRS spectra of molecular monolayers assembled on Co/Au/PET and Au. The dashed lines and asterisks indicate the C-H stretches of the alkyl backbone and methyl group, respectively.

we attribute to the F1 molecule. During the template stripping process, some of the F1 molecule was transferred from the tSi to the Co substrate, giving rise to the voids in the AFM image in fig. 1.

Monolayer formation was directly confirmed by the detection of S atoms on the ODT- and MHA-treated Co surfaces (in fig. 3, top two spectra). The C 1s signal increases and the F 1s signal decreases for MHA/Co (top spectrum), and confirming the attachment of MHA and displacement of F1 molecules on the stripped Co surface. The attachment of ODT on Co is confirmed, but the C 1s and F 1s relative intensities vary from run to run. The MHA coverage does not vary as much and could be due to its ability to dock via the thiol or carboxylic acid end. Using the Co 3s signal attenuation, we estimate that the molecular density of ODT and MHA on Co surfaces is about 2 and 4 molecules per nm^2, respectively. Typical values of molecular density on Au are 5-6 molecules per nm^2. The Co 2p signal of ODT/Co and MHA/Co also show multiplet peaks, and is likely that the Co surface undergoes some oxidation before the self-assembly process. Although the stripped Co surface is oxidized, the Co surface can still be functionalized with molecules by self-assembly. Preliminary results suggest that template stripped Co surfaces

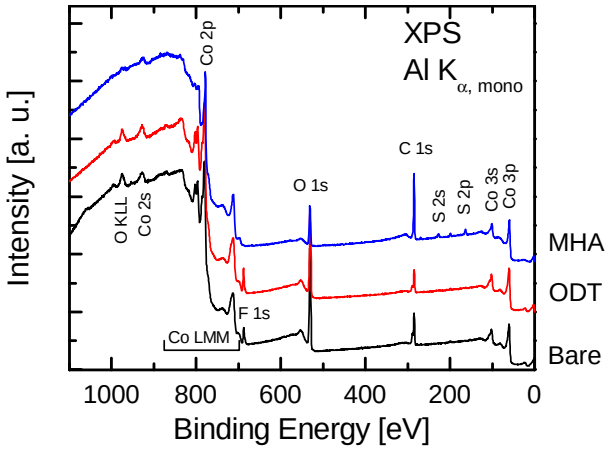


FIGURE 3. XPS spectra of bare template-stripped Co (bottom), and ODT (middle) and MHA (top) self-assembled on the same surface.

are a promising route for controlling the organic-cobalt interface for fabricating organic-ferromagnetic devices.

CONCLUSION

Surface-sensitive material characterization tools identify the challenges of preparing the molecule-Co interface and were used to assess the method we developed of template stripping and SAM formation on Co surfaces for organic spintronic applications. AFM show that these surfaces are relatively smooth and contain some gaps from the template-stripping process. IR and X-ray spectroscopies directly confirm the molecular attachment of two different molecules on these oxidized Co surfaces, and their molecular packing density is comparable to that on Au. With improvements, this route may provide a way to engineer and modify the interface between a ferromagnetic electrode and organic material for spin injection into organic semiconductors or spin tunneling devices.

Acknowledgement

S. P. acknowledges the NRC-NIST ARRA program. L. K. L. was supported through a NIST Summer Undergraduate Research Fellowship, partly by the NSF under Agreement No. ECC-0754355.

REFERENCES

1. Official contributions by the National Institute of Standards and Technology are not subject to copyright.
2. Y. –L. Loo and I. McCulloch, *MRS Bulletin* **33**, 653 – 658 (2008).
3. C. Barraud et al., *Nat. Phys.* **6**, 615 – 620 (2010).
4. S. Devillers et al., *Langmuir* **27**, 14849 – 14860 (2011).
5. P. G. Hoertz et al., *J. Am. Chem. Soc.* **130**, 9763 – 9772 (2008).
6. S. Tatay et al., *ACS Nano* **6**, 8753 – 8757 (2012).
7. S. Pookpanratana et al., submitted (2012).

KEYWORDS

Molecular layer, self-assembly, ferromagnetic materials

WE–03

EVALUATION OF POSSIBLE STANDARDS FOR X-RAY REFLECTOMETRY

P. DeHaven[1], E. Nolot[2], A. Madan[1], A. Michallet[3], S. Favier[3], , D. Le Cunff[3], R. Duru[3]

(1) IBM Corporation, 2070 Route 52, Hopewell Junction, NY USA
(2)CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France.
(3) STMicroelectronics - 850, Rue Jean Monnet, 38926 Crolles Cedex, France.

INTRODUCTION

X-Ray Reflectivity (XRR) is becoming increasingly important as a metrology tool in the semiconductor industry, not only for in-depth investigation of complex samples in characterization labs but also for inline process monitoring and for reliable Lab to Fab metrology strategies [1]. Despite the worldwide recognition of the advantages of XRR as a reliable metrology technique, the further utilization of XRR for quality control and in the optimization of industrial process still suffers from the lack of reference samples. In the absence of a NIST traceable XRR Standard Reference Material, there is a need to obtain a practical material that can serve as a calibration standard. Based on an evaluation of variety of samples, either made of single layer films grown on silicon or consisting in multi layers structures grown by epitaxy on silicon, we have found that silicon nitride and (SiGe/Si) superlattice are potential candidates as thickness standards. The use of single crystal silicon as a calibration standard for XRR density measurements will also be discussed.

EVALUATION OF EXISTING STANDARDS

We have first evaluated VLSI (NIST-traceable) thickness standards that are extensively used in semiconductor fabs for the calibration of optical metrology tools such as ellipsometers (SE). These standards are made of thermally grown SiO_2 films or silicon nitride films grown by low pressure chemical vapor deposition technique (LPCVD) on silicon wafers. Though SE-deduced and XRR-deduced thicknesses show excellent agreement, the density profile in SiO_2/Si systems is too smooth for SiO_2 thin films to be materials of choice for XRR using frequently employed sealed copper tubes [Fig.1].

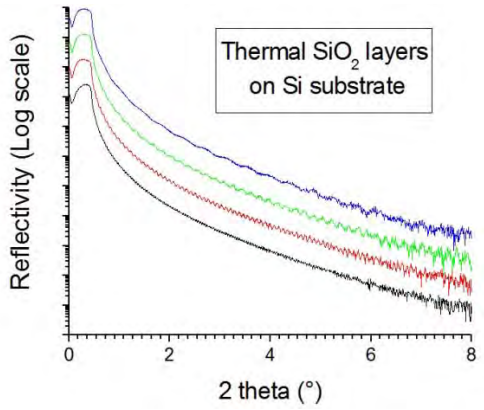


FIGURE 1. XRR scans of 20 to 200n- thick silicon oxide layers thermally grown on silicon substrate.

LPCVD silicon nitride samples are more likely to meet the requirements of specular reflectivity experiments. Nevertheless the evaluation of two

WE–03

distinct VLSI nitride samples highlighted unexpected in-depth density gradient [Fig.2] which induces a significant discrepancy between standardized thickness information and XRR-deduced values and limits their use as XRR standards.

Other possible standards such as AlAs/GaAs multilayer and thin TaN/Ta bilayer, which have been investigated in the frame of the VAMAS project [2,3], will be discussed in this paper.

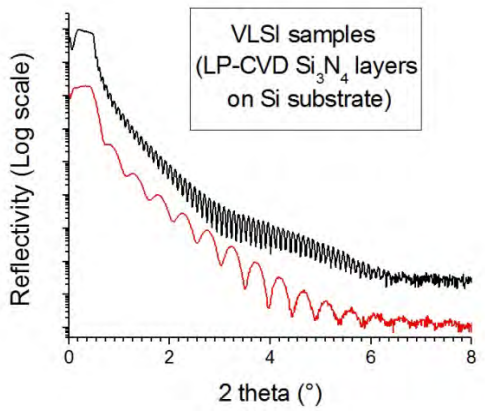


FIGURE 2. In-depth density profile in nitride layers revealed by multiple frequencies in the Fourier space.

EXPERIMENTAL

We have designed a sample set consisting in three types of samples:

- Single crystal silicon has been found extremely effective, for routine monitoring of Lab and Fab tools and for tool check after any modification in the optical path. In addition, this sample allows for control of the instrumental function around the total external reflection region, and thus determination of appropriate angle shift correction, either in the case of tools based on focused-beam geometry or for chuck-induced deviation [Fig. 3].

- Silicon nitride thin films grown by LPCVD with careful control of deposition conditions to avoid the formation of density gradients.

- (SiGe/Si) superlattice grown by epitaxy on Silicon 001 substrate, with varied germanium content (26% or 31%) and number of pairs (3 or 5). The presence of marked thickness interference fringes on the high-resolution diffraction scans [Fig. 4] are characteristic of pseudomorphic stacks, *i.e.* without significant misfit dislocations or stacking faults and with abrupt interfaces between Si and SiGe.

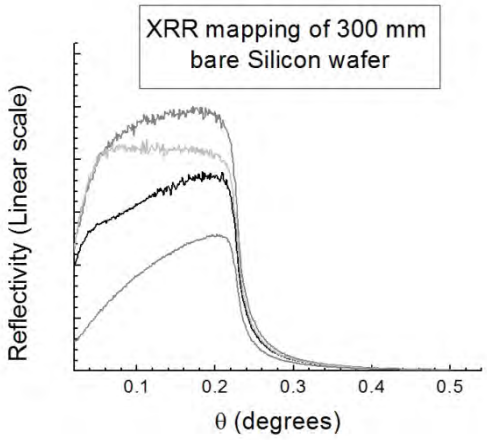


FIGURE 3. Chuck-induced variability of the critical angle region as revealed by mapping of a bare silicon wafer.

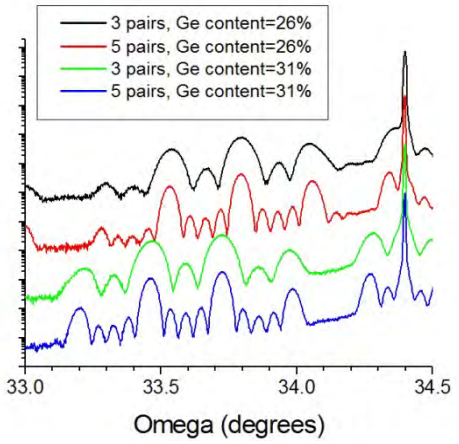


FIGURE 4. Omega-2Theta scans around the (004) X-Ray Diffraction order for SiGe/Si superlattice samples

The samples have been evaluated on five different platforms with varying features such as collimated or focused beam geometry, theta-theta or four-circle setup, Lab tools or inline tools, etc.

WE–03

Stability, correlation across different platforms, and comparison with other techniques such as ellipsometry [Fig. 5] will be discussed.

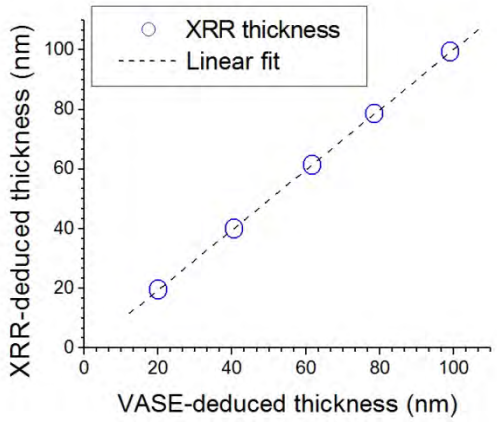


FIGURE 5. Excellent agreement between silicon nitride thickness deduced from XRR and variable-angle SE.

CONCLUSION

Three types of samples made of crystalline silicon substrate, silicon nitride films and SiGe/Si superlattice have been evaluated as XRR standards through stability tests and inter-laboratory tests and comparison with other techniques.

REFERENCES

1. E. Nolot et al, *Proc. SPIE* 8466, 846605 (Oct. 11, 2012); doi:10.1117/12.928368
2. P. Colombi, et al, J. Appl. Crystallogr. 41 (2008) 143
3. R.J. Matyi et al. / Thin Solid Films 516 (2008) 7962–7966.

KEYWORDS

X-ray reflectometry, standards, thin films

WE–04

METROLOGY STUDIES WITH NEMO, A MULTIMILLION ATOM SIMULATION TOOL

G. Klimeck[1], J. E. Fonseca[1], R. Rahman[1], N. Kharche[2,3], G. P. Lansbergen[4], S. Rogge[5],

[1]*Network for Computational Nanotechnology, Purdue University, West Lafayette, IN USA*
[2]*Department of Physics, Rensselaer Polytechnic Institute, Troy, NY, USA*
[3]*Brookhaven National Laboratory, Upton, NY, USA*
[4]*Kavli Institute of Nanoscience, Delft University of Technology, The Netherlands*
[5]*Centre for Quantum Computation & Communication Technology, School of Physics, The University of New South Wales Sydney, Australia*

INTRODUCTION

The NEMO NanoElectronic MOdelling tool suite has been developed to characterize electronic properties of multimillion atom semiconductor devices [1]. Here, we summarize previously published data under the aspect of metrological studies. The summarized work has used NEMO 3-D which incorporates modeling and simulation strategies refined over the years for investigating such experimental results as resonant tunneling diodes [2], polysilicon-gated MOS devices [3], and SiGe/Si quantum wells [4]. This versatile, open source software package allows calculating single-particle electronic states and optical response of various semiconductor structures including bulk materials, quantum dots, impurities, quantum wires, quantum wells and nanocrystals. NEMO 3-D uses the valence force field method to compute strain and the electronic structure is based on the tight-binding $sp^3d^5s^*$ electronic band structure model. Successful applications of NEMO 3-D are demonstrated in the atomistic calculation of single-particle electronic states of the following realistically-sized nanostructures each consisting of multimillion atoms: (1) self-assembled quantum dots including long-range strain and piezoelectricity; (2) stacked quantum dots as used in quantum cascade lasers; (3) Phosphorus (P) impurities in Silicon used in quantum computation; (4) Si on SiGe quantum wells (QWs); and (5) SiGe nanowires. These examples demonstrate the broad NEMO 3-D capabilities and indicate the necessity of multimillion atomistic electronic structure modeling. The quantitative simulation agreement with experiment, without any material or geometry parameter adjustment in a general atomistic tool, leads us to believe that the era of nanotechnology computer-aided design is approaching.

METROLOGY STUDIES WITH NEMO 3-D

NEMO 3-D was used to simulate valley splitting in strained silicon quantum wells grown on (001) and modeled with 2 degree miscuts, step disorder and alloy disorder [4]. Atomistic disorder was identified to be the critical physics. This work showed that the analysis of valley splitting in strained Si quantum wells grown on strained SiGe required atomistic analysis of 10 million atoms to match experimental data (Fig. 1). Valley splitting was enhanced due to the steps as well as alloy disorder and was on the same order of magnitude as reported in experiments.

WE–04

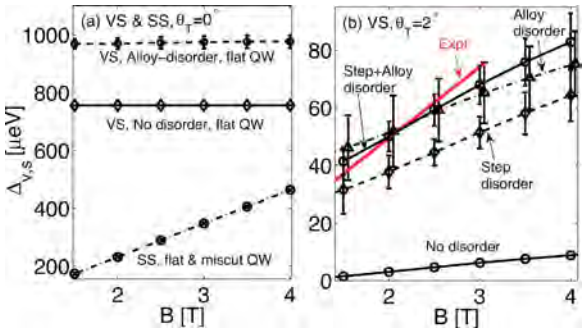


FIGURE 1. Valley splitting (VS) in a flat QW and SS in flat and miscut QWs. VS increases due to the SiGe alloy disorder. SS remains unchanged by disorders or miscut surfaces. (b) VS in 2° miscut Si QWs in the presence of realistic disorders. Error bars represent standard deviation in VS. Data from reference [4].

NEMO 3-D can simulate devices with incidental and deterministically placed impurities and can reproduce experimental results [5]. Atomistic NEMO 3-D simulations of the D^0 to D^- charging energies of a gated donor in silicon as a function of applied fields and donor depths were found to provide good agreement with experimental measurements [6]. A self-consistent field large-scale tight-binding method is used to compute the D^- binding energies with a domain of over 1.4 million atoms, taking into account the full band structure of the host, applied fields, and interfaces. A detailed quantitative comparison of the charging energies with transport spectroscopy measurements with multiple samples of arsenic donors in ultrascaled metal-oxide-semiconductor transistors validates the model results and provides physical insights. The experimental device is shown in Fig. 2 and a comparison of experimental and simulation results is shown in Table 1.

Experiments show that InGaAs quantum dots have their wavelengths tuned by adjusting the In fraction. NEMO 3-D simulations of multimillion-atom electronic structure calculations closely match and explain nonlinear experimental results both qualitatively and quantitatively [7]. Insight garnered from these simulation studies show that the quantum dot changes its shape.

Other metrology work in ultra-scaled FinFETs investigated device differences attributed to random single impurities. NEMO 3-D was used to identify the impurity's chemical species and determine their concentration, local electric field and depth below the Si/SiO2 interface. [8]. NEMO 3-D has the ability to model excited states as well as ground states, a key feature to metrological studies of atomistic impurities. NEMO 3-D has been used to investigate spin blockade. In a coupled pair of donor-based quantum dots, the experimental binding energies of the first few electrons matched well with NEMO 3-D's atomistic tight-binding. [9]. Metrology studies using NEMO 3-D have also allowed for precise determination of ion location in single-atom (phosphorus in silicon) spin qubit devices [10] and calculation of negative differential resistances of current-voltage characteristics in weakly-coupled double quantum dots [11].

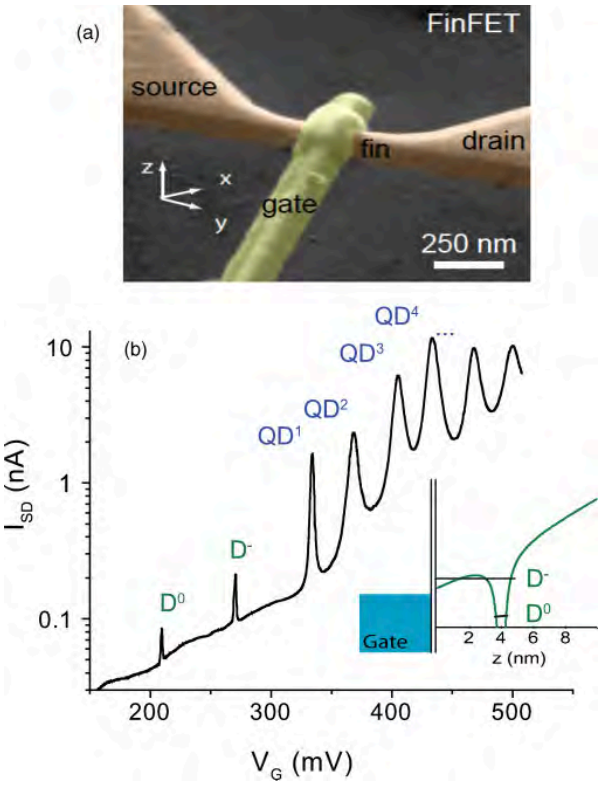


FIGURE 2. Geometry and electrical characteristics of a single donor located in the channel of a FinFET device. (a) Scanning Electron Micrograph of typical FinFET device. (b) Band diagram along the x-direction with the D^0-state in resonance combined with the measured source/drain current versus gate voltage for a typical sample. Data from reference [8].

TABLE 1. First three measured excited states of each sample versus the best fit to the NEMO 3-D model. Simulation data given in parentheses. The fit yields a unique combination of (F, d) for each single donor device. The measurement error for each level is estimated to be around 0.5 meV.

Device sample	E1(meV)	E2(meV)	E3(meV)	d(nm)	F(MV/m)	S(meV)
10G16 – EXP (N3)	2 (2.2)	15 (15.6)	23 (23.0)	(3.3)	(37.3)	(0.59)
11G14 – EXP (N3)	4.5(4.5)	13.5(13.5)	25(25.0)	(3.5)	(31.6)	(0.04)
13G14 – EXP (N3)	3.5 (3.6)	15.5 (15.7)	26.3 (21.5)	(3.2)	(35.4)	(0.17)
HSJ18 – EXP (N3)	5 (4.5)	10 (9.9)	21.5 (21.8)	(4.1)	(26.1)	(0.63)
GLG14 – EXP (N3)	1.3(1.3)	10 (10)	13.2(12.4)	(5.2)	(23.1)	(0.28)
GLJ17 – EXP (N3)	2(1.3)	7.7(7.7)	15.5(15.8)	(4.9)	(21.9)	(0.77)

NANOHUB.ORG

A web-based online interactive version of NEMO 3-D for educational purposes is freely available on the NCN portal http://www.nanoHUB.org. The nanoHUB is a cyberinfrastructure for scientific computing with over 240,000 users. Tools such as the "Quantum Dot Lab", which runs on the NEMO toolkit engine, allow researchers, students, and students to run simulations in a web browser, while transparently harnessing the computational power provided by a high performance computing grid [12].

REFERENCES

1. Gerhard Klimeck et al, IEEE Transactions on Electron Devices, **54**, 2079 - 2089 (2007).
2. R. Bowen, G. Klimeck, R. Lake, W. Frensley, T. Moise, *J. Appl. Phys.* **81**, 3207 (1997).
3. E. M. Vogel, C. A. Richter, B. G. Rennex, Solid State Elec. **47**, 1589-96, (2003).
4. N. Kharche, M. Prada, T. B Boykin, G. Klimeck, *Appl. Phys. Letters* **90**, 092109-1-092109-3 (2007).
5. G. Lansbergen, et al. , IEEE IEDM, San Francisco, USA, , (2008).
6. R. Rahman, et al. *Phys. Rev. B* **84**, 115428 (2011).
7. M. Usman, H. Ryu, I. Woo, D. S. Ebert, G. Klimeck, *IEEE Transactions on Nanotechnology* **8**, 330-344, (2009).
8. G.P. Lansbergen, et al., **arXiv:1111.4238**, (2011).
9. B. Weber, et al., in preparation.
10. F. A. Mohiyaddin, et al., in preparation.
11. B. Muralidharan, H. Ryu, Z. Huang, G. Klimeck, J. Comput. Electron., **7,** 403–406, (2008).
12. G. Klimeck, M. McLennan, S. Brophy, G. Adams III, M. Lundstrom, IEEE Computers in Engineering and Science (CISE)**10**, 17-23 (2008).

KEYWORDS

Quantum computing, quantum dots, P donors in Si, single impurities

WE–05

Impact of X-ray Synchrotron Studies on Nanoelectronics

Jonathan Lang, David Keavney, Volker Rose, Ross Harder, Yuxin Wang, Jon Tischler, Wenjun Liu, Jin Wang, Tao Sun, Steve Heald, Albert Macrander, Lahsen Assoufid and Jyotsana Lal

X-ray Science Division, Advanced Photon Source, Argonne National Laboratory, Argonne, IL-60439, USA.

INTRODUCTION

The future trends in nanoelectronics products are to be 'smaller', 'faster' and 'more complex'. This requires the characterization of materials on the nano length scales and at fast time scales. One of the tools for investigation is the X-rays produced at synchrotron at the Advanced Photon Source (APS). A wide range of X-ray techniques for characterization of materials at the nanoscale are available at the APS.

X-ray micro/nano beams are an emerging characterization tool with broad implications for nanoelectronics (1). These submicrometer hard x-ray beams with the ability to penetrate tens to hundreds of micrometers into most materials and with the ability to determine local composition, chemistry, and (crystal) structure can characterize buried sample volumes in small samples. Besides directly imaging nanostructures, the high brilliance and continuous tunability of synchrotron radiation also allows high-resolution images to be acquired at close energy intervals to produce an "energy scan." Such spectral imaging techniques provide a unique means of mapping the elemental composition of samples as well as certain chemical bonding states (XAFS Spectroscopy) (2).

Spectroscopic x-ray techniques, for example, can be applied to extract element specific information about the magnetic, charge, and orbital character of a device. By varying the detection scheme such information can obtained from a particular structural layer within a device or isolate the contributions arising solely at the interface between layers. The high x-ray flux provided by such facilities enables such measurements from sample volumes substantially less than one atomic layer. Further, the pulsed nature of synchrotron radiation enables pump-probe studies to observe the dynamics of such phenomena using optical or magnetic excitation on times scales down to ~100ps. X-ray diffraction measurements, on the other hand, can be used to understand the atomic structure at interfaces in complex heterostructured materials. Not only can these measurements be performed on static devices, but can also be applied in-situ during growth of a material to optimize these processes. As such synchrotron techniques can be used to provide valuable information on such disparate systems such as magnetic heterostructures and recording media, ferroelectric and/or multiferroic devices, and interfaces in semiconductors. Here, a few selective examples

WE–05

from diffraction, spectroscopy and imaging are highlighted.

EXAMPLES

Figure 1 is an example of high-resolution 3D imaging and material analysis with transmission X-ray microscopy (2). Another example, is material changes in tantalum oxide-based memristive devices, investigated using x-ray based spectromicroscopy and nanospectroscopy (3). A synchrotron-based microscopy and spectroscopy study was performed after the electrical cycling of a tantalum oxide resistance switching device without using any destructive sample preparation. The Ta-rich channel was surrounded by a modified phase of the oxide, which had a spectral signature distinct from the as-grown layer. Generally speaking, the chemical and structural characterization of resistive switching centers is challenging, because of the extremely small volume of material involved and the desire to perform analyses nondestructively.

The micro-diffraction instrument at the APS sector 34ID-E contains a dedicated instrument for making micro-diffraction measurements on crystalline materials. It has two main features: first the main strength of this instrument is that you not only measure the orientation of one crystal (this was first done by Laue over 100 years ago), but you can measure the spatial distribution of orientations in a volume. Second, it is still quite challenging to precisely assess strain and its influence on device characteristics. 34-ID-E is the most important strain-sensitive scanning instrument and is the white-beam Laue scanning microprobe beamline, which can measure the full strain tensor at every measurement point (4,5).

The sample-averaging limitations of the above method described so far have been overcome by the development of Coherent Diffractive Imaging (CDI) as a 3D structural analysis method for individual small crystals. These recent introduction of coherence-based methods at the newer synchrotron radiation sources has enabled diffraction patterns to be phased and inverted to form 'lensless' images, for individual small crystals. It is easy to demonstrate that the presence of strain breaks the local symmetry of a diffraction pattern about the Bragg point and results in complex phase. The complex phase is the projection of the local deformations of the crystal lattice on to the reciprocal lattice vector Q of the Bragg peak about which the diffraction is measured (6,7) (Figure 2).

Recently, at the APS, a surface/interface imaging technique, coherent surface scattering imaging (CSSI) was developed (9), which works in grazing-incidence geometry (9). CSSI is capable of reconstructing not only planar images of surface structures but also 3-D architectures with nanometer resolution along the surface normal direction. The CSSI technique demonstrated here promises applications in elucidating structures in substrate-supported and buried nano-electronics/photonics. In particular, it can be an effective means to perform nondestructive structural analysis of emerging 3-dimensional integrated circuits.

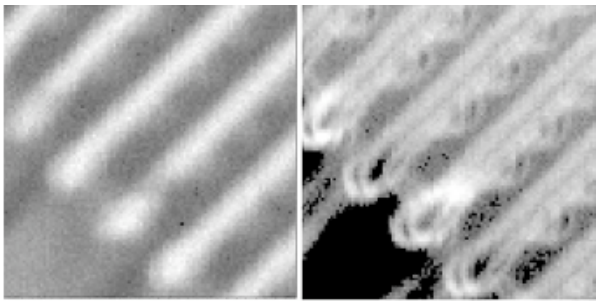


FIGURE 1. An integrated circuit imaged at 2-ID-B beamline at Advanced Photon Source, Argonne National Laboratory from reference 2 (present resolution 17nm).

One of the principal questions yet to be understood is how and on what time scale magnetization reverses in patterned structures. Therefore, time-resolved X-PEEM is accomplished in a pump-probe mode. In such experiments, shown in Figure 3, an excitation pulse is synchronized with the incoming X-ray pulses and applied to the sample with a variable delay. Then, by varying the delay and integrating over many repeats of this cycle, the average response of the sample to the excitation pulses can be mapped out in time (10).

WE–05

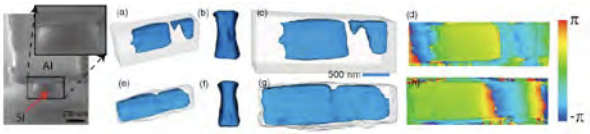


FIGURE 2. The SEM image of a 1200 nm silicon-on-insulator (SOI) wire shows a wedged cross section due to undercutting in the etching process. SOI wire offers the opportunity for strain engineering to enhance electron mobility. Visualization of strain inside a SOI wire using two different algorithms a-d and e-h. The first algorithm a-d could not retrieve the entire structure, it gave well-defined boundaries for those sections with relatively small lattice deformations. With the second improved algorithm (e-h) the resulting CDI images had smooth boundaries, and continuous density at the locations with greater deformation of the lattice. The phase (in radians) or deformations are shown as colours (8).

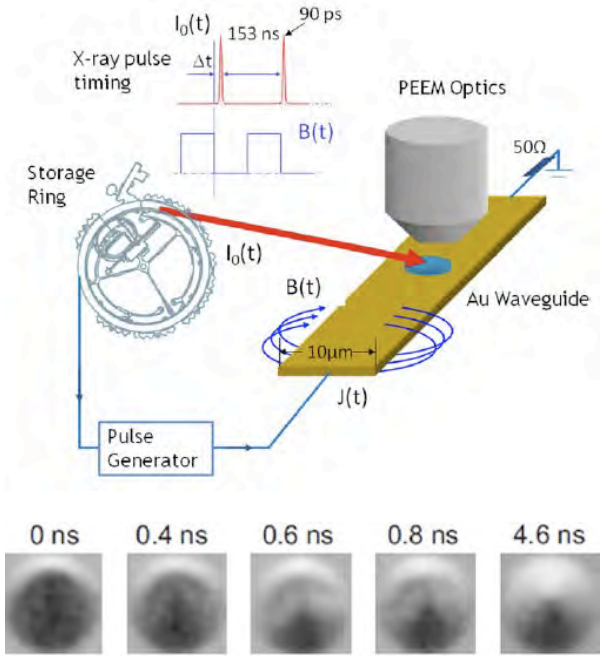


FIGURE 3. (a) Schematic diagram of a pump-probe time-resolved magnetic imaging experiment (b) Transient domain states observed in nanostructures at the APS (11)

X-ray spectroscopic signatures from XAFS contain a wealth of element-specific information about valence, bonding configuration and local structure which has been used to study thin film growth of metal overlayers on Si and GaAs at sector 20. A number of systems for potential spintronics applications such as transition metal doped TiO_2, ZnO, and In_2O_3 have been investigated. UHV chambers for in-situ preparation of thin films are provided (12).

White beam crystal X-ray topography reveal non destructively the irregularities in a non-ideal crystal lattice is available as an additional capability on 1-BM-B.

These Synchrotron based techniques are operated as public research facilities for both academic and industrial users free of charge for nonproprietary work and at a modest fee for proprietary use. To better accommodate the timescales that industrial users may require, a small amount of beam time is set aside for "rapid-access measurements."

REFERENCES

1. G. E. Ice, J. D. Budai, J. W. L. Pang, *Science*, **334** 1234-1239 (2011).
2. Y. Wang, Characterization of Materials, edited by Elton N. Kaufmann. Copyright John Wiley & Sons, Inc., 2012, pp.1-10.
3. J.P. Strachan, G. Medeiros-Ribeiro, J. J. Yang, M.-X. Zhang, F. Miao, I. Goldfarb, M. Holt, V. Rose, and R. S. Williams *App. Phys. Letters* **98**, 242114, (2011)
4. Lyle Levine *et.al.*, *Nat. Mater.* **5**, 619 (2006)
5. G.E. Ice, *et.al.* J. of Synch. Radiation, **12**,155 (2005).
6. I. K. Robinson, R. Harder, *Nat. Mater.* **8**, 291–298 (2009).
7. M. A. Pfeifer, G. J. Williams, I. A. Vartanyants, R. Harder & I. K. Robinson, *Nature*, **442** 63 (2006).
8. X. Huang, R. Harder, G. Xiong, X. Shi, and I.K. Robinson, *Phys. Rev. B* **83**, 224109 (2011).
9. T. Sun, Z. Jiang, J. Strzalka, L. Ocola and J. Wang, *Nat. Photonics*, **6**, 586-590 (2012).
10. X. M. Cheng and D. J. Keavney, *Rep. Prog. Phys.* **75** 026501 (2012)
11. K. Yu Guslienko, X. F. Han, D. J. Keavney, R. Divan and S. D. Bader *Phys. Rev. Lett.* **96** 067205 (2006).
12. S. M. Heald, A. Mokhtari, A. J. Behan, H. J. Blythe, J. R. Neal, A. M. Fox, and G. A. Gehring, *Phys. Rev. B* **79**, 075202 (2009).

KEYWORDS

X-rays, Synchrotron, Imaging, Devices

Acknowledgments

This work was performed at Argonne National Laboratory, a U.S. Department of Energy Office of Science laboratory, supported under Contract No. DE-AC02-06CH11357.

WE–06

THE MEMS 5-IN-1 TEST CHIPS (REFERENCE MATERIALS 8096 AND 8097)[1]

Janet Cassard, Jon Geist, Craig McGray,* Richard A. Allen, Muhammad Afridi,**
Brian Nablo, Michael Gaitan, and David G. Seiler

Semiconductor and Dimensional Metrology Division, Physical Measurement Laboratory
National Institute of Standards and Technology, 100 Bureau Drive, Stop 8120, Gaithersburg, MD 20899-8120
**Modern Microsystems, Inc., 11522 Soward Dr., Silver Spring, MD 20902*
***Potomac Networks, 1301 Delaware Avenue SW #N716, Washington DC 20024*

INTRODUCTION

This paper presents an overview of the Microelectromechanical Systems (MEMS) [1] 5-in-1 Reference Material (RM), which is a single test chip with test structures from which material and dimensional properties are obtained using five documentary standard test methods (from which its name is derived). Companies can validate their use of the documentary standard test methods by comparing their in-house measurements taken on the RM with the National Institute of Standards and Technology (NIST) measurements taken on the same test structures. In addition, the MEMS 5-in-1 can be used to:

- Characterize or validate a process,
- Take local measurements of customer-designed structures,
- Compare measurements meaningfully between laboratories on similarly (or differently) processed test structures (e.g., to facilitate communications between suppliers and customers),
- Trouble-shoot a process, and
- Calibrate an instrument.

Reference values are given for an RM 8096 chip used at NIST for stability studies.

It takes a considerable amount of time to develop an RM and NIST would be willing to help customers develop their own. Alternatively, they are available for purchase from the NIST SRM Program Office [1].

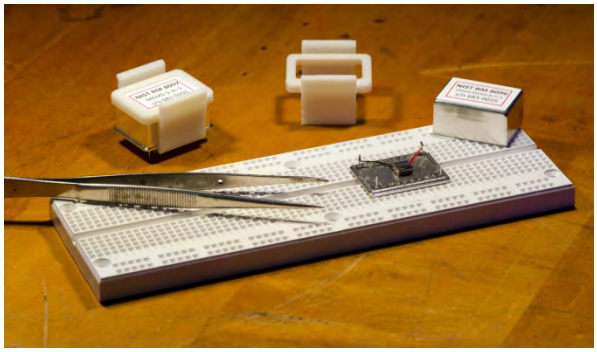


FIGURE 1. A MEMS 5-in-1 Reference Material (RM 8096).

THE MEMS 5-IN-1

The MEMS 5-in-1 is a reference device sold as a NIST Reference Material (RM) that is used to measure dimensional and material properties. There are two RM chips (8096 and 8097). RM 8096, as seen in Figures 1 and 2, was fabricated on a multi-user 1.5 µm complementary metal oxide semiconductor (CMOS)

[1] Official contributions by the National Institute of Standards and Technology (NIST) are not subject to copyright.

[1] MEMS are also referred to as microsystems technology (MST) and micromachines.

WE–06

process [2][2] followed by a bulk-micromachining etch. For this RM, the material properties of the composite oxide layer are reported on the Report of Investigation, which accompanies each unit of the RM. RM 8097, as seen in Figure 2, was fabricated using a polysilicon multi-user surface-micromachining MEMS process with a backside etch [3]. For this RM, the material properties of the first or second polysilicon layer are reported on the Report of Investigation.

The Five Standard Test Methods

Five standard test methods are used to obtain the properties of the MEMS 5-in-1 test chip. These test methods are for measuring Young's modulus [4], step height [5], residual strain [6], strain gradient [7], and in-plane length [8]. The Young's modulus and step height test methods were published by the Semiconductor Equipment and Materials International (SEMI) and the residual strain, strain gradient, and in-plane length test methods were published by the American Society for Testing and Materials (ASTM) International. Each of the five standard test methods includes round robin precision and bias data.

Eight Properties Reported

Eight properties are typically reported on the Report of Investigation. The five properties mentioned in the previous section are reported plus three more properties: residual stress, stress gradient, and beam thickness. Residual stress and stress gradient are found from calculations in the Young's modulus test method, and the beam thickness is obtained using the step height test method in an electro-physical technique [9] for RM 8096 and in an opto-mechanical technique [10] for RM 8097, as described in the NIST Special Publication SP 260-177 [11]. Therefore, five standard test methods are used to obtain eight properties.

[2] Commercial equipment, instruments, or processes may be identified. This does not imply recommendation or endorsement by the National Institute of Standards and Technology (NIST), nor does it imply that the equipment, instruments, or processes are the best available for the purpose.

Instrumentation

As specified in the respective measurement methods [4-8,11-12], the Young's modulus measurements are taken with an optical vibrometer, stroboscopic interferometer, or comparable instrument. The measurements using the other four test methods are taken with an optical interferometer and stylus profilometer, or comparable instruments.

The MEMS Calculator

The MEMS Calculator website (Standard Reference Database 166) [13] contains data analysis sheets for calculating the MEMS properties. This website is accessible via the NIST Data Gateway (http://srdata.nist.gov/gateway/) with the keyword "MEMS Calculator." Initially, the measurements are input on the pertinent data analysis sheet; then the "Calculate and Verify" button is clicked to obtain the results. A verification section is at the bottom of each data analysis sheet. If all the pertinent boxes in this section say "ok," then the data are verified. Otherwise, the specific issue is addressed by modifying the inputs and recalculating.

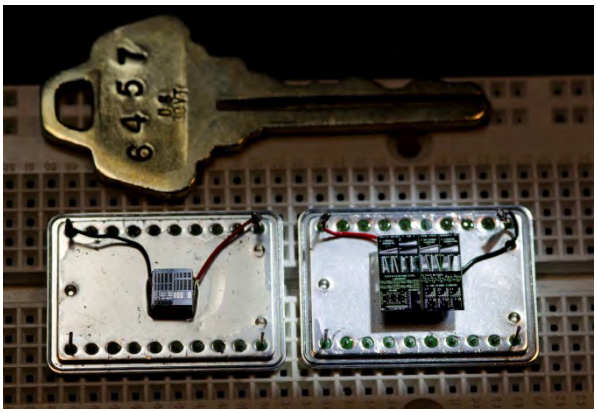


FIGURE 2. RM 8096 (left) and RM 8097 (right).

Accompanying Material

Each MEMS 5-in-1 is accompanied by a Report of Investigation, the pertinent data analysis sheets [13], the five standard test methods [4-8], and the NIST SP 260-177 [11]. The data analysis sheets that accompany the MEMS 5-in-1 identify the specific test structures for measurement and include the raw data

WE–06

used at NIST to obtain the measurements on the Report of Investigation. The SP 260 is a comprehensive user's guide for the MEMS 5-in-1. It specifies that the applicable SEMI or ASTM standard test methods be used to take the measurements on the same test structures that the NIST measurements were taken. It also recommends a method by which the user's measurements can be compared with the NIST-measured values on the Report of Investigation in order to validate their use of the documentary standard test methods.

THE REPORT OF INVESTIGATION

The RM Report of Investigation provides a NIST reference value for each property. A NIST reference value is a best estimate of the true value provided on a NIST Certificate/Certificate of Analysis/Report of Investigation where all known or suspected sources of bias have not been fully investigated by NIST [14]. Table 1 includes example NIST reference values for an RM 8096 monitor chip used at NIST for stability studies. An effective value is reported when there are deviations from the ideal geometry or composition of the measured test structure(s) [11].

TABLE 1. Example NIST Reference Values for RM 8096.

Measurement[a]	**NIST Reference Value ± Expanded Uncertainty (for k=2 for ≈95 % confidence)**
1. Effective Young's modulus, E	56.6 GPa ± 17.8 GPa
2. Effective residual strain, ε_r	$-2.83\times10^{-3} \pm 0.71\times10^{-3}$
3. Effective strain gradient, s_g	1101 m^{-1} ± 167 m^{-1}
4. Step height,[b] $step1_{AB}$	0.499 µm ± 0.108 µm
5. In-plane length,[c] L (at 25×)	202.2 µm ± 3.0 µm
6. Effective residual stress, σ_r	−160 MPa ± 67 MPa
7. Effective stress gradient, σ_g	62.3 TPa/m ± 18.9 TPa/m
8. Thickness, t_{SiO2}	2.65 µm ± 0.20 µm

[a] These measurements, except where noted, are for a composite oxide layer.

[b] This is a metal2-over-poly1 step from active area to field oxide. Other physical step height standards are available with lower uncertainty values and are recommended for calibrating instruments.

[c] The in-plane length measurement is taken between two metal2 lines.

ACKNOWLEDGEMENT

The authors would like to acknowledge Robert L. Watters, Jr. (Chief, Measurement Services Division) and those in the Measurement Services Division for their work in releasing the RMs to the public. Also, the following people at NIST are thanked for reviewing this paper: Theodore V. Vorburger, David T. Read, W. Robert Thurber, and Erik M. Secula.

REFERENCES

1. Contact the NIST SRM Program Office to obtain a MEMS 5-in-1 (which comes with its Report of Investigation, the pertinent data analysis sheets, the five standard test methods, and the SP 260-177) by visiting http://ts.nist.gov/measurementservices/referencematerials/index.cfm.
2. The RM 8096 chips were fabricated through MOSIS on the 1.5 µm On Semiconductor (formerly AMIS) CMOS process. The URL for the MOSIS website is http://www.mosis.com.

3. The RM 8097 chips were fabricated at MEMSCAP using MUMPs-Plus! (PolyMUMPs with a backside etch). The URL for the MEMSCAP website is http://www.memscap.com.
4. SEMI MS4-0212, "Test Method for Young's Modulus Measurements of Thin, Reflecting Films Based on the Frequency of Beams in Resonance," February 2012, (visit http://www.semi.org for ordering information).
5. SEMI MS2-0212, "Test Method for Step Height Measurements of Thin Films," February 2012, (visit http://www.semi.org for ordering information).
6. ASTM E08, "E 2245 Standard Test Method for Residual Strain Measurements of Thin, Reflecting Films Using an Optical Interferometer," ASTM E 2245-11, December 2011, (visit http://www.astm.org for ordering information).
7. ASTM E08, "E 2246 Standard Test Method for Strain Gradient Measurements of Thin, Reflecting Films Using an Optical Interferometer," ASTM E 2246-11, January 2012, (visit http://www.astm.org for ordering information).
8. ASTM E08, "E 2244 Standard Test Method for In-Plane Length Measurements of Thin, Reflecting Films Using an Optical Interferometer," ASTM E 2244-11, December 2011, (visit http://www.astm.org for ordering information).
9. J. C. Marshall and P. T. Vernier, "Electro-physical technique for post-fabrication measurements of CMOS process layer thicknesses," *NIST J. Res.*, Vol. 112, No. 5, pp. 223-256, 2007.
10. J. C. Marshall, "New Optomechanical Technique for Measuring Layer Thickness in MEMS Processes," *Journal of Microelectromechanical Systems*, Vol. 10, No. 1, pp. 153-157, March 2001.
11. J. M. Cassard, J. Geist, T. V. Vorburger, D. T. Read, M. Gaitan, and D. G. Seiler, "Standard Reference Materials: User's Guide for RM 8096 and 8097: The MEMS 5-in-1, 2013 Edition," NIST SP 260-177, February 2013.
12. J. Cassard, J. Geist, M. Gaitan, and D. G. Seiler, "The MEMS 5-in-1 Reference Materials (RM 8096 and 8097)," *Proceedings of the 2012 International Conference on Microelectronic Test Structures*, ICMTS 2012, San Diego, CA, pp. 211-216, March 21, 2012.
13. The data analysis sheets, SP 260-177, and MEMS 5-in-1 details can be found at the MEMS Calculator website (Standard Reference Database 166) accessible via the NIST Data Gateway (http://srdta.nist.gov/gateway/) with the keyword "MEMS Calculator."
14. W. E. May, R. M. Parris, C. M. Beck, J. D. Fassett, R. R. Greenberg, F. R. Guenther, G. W. Kramer, S. A. Wise, T. E. Gills, J. C. Colbert, R. J. Gettings, and B. R. MacDonald, "Definitions of Terms and Modes Used at NIST for Value-Assignment of Reference Materials for Chemical Measurements," NIST SP 260-136 (2000) http://ts.nist.gov/MeasurementServices/ReferenceMaterials/PUBLICATIONS.cfm.

KEYWORDS

MEMS 5-in-1, MEMS Calculator, Reference Material, RM 8096, RM 8097, test chip

WE–07

CONTACT RESONANCE AFM ON TIN-LOW-*K* DIELECTRIC FILMS AND PATTERNS

Gheorghe Stan[1,2], Lawrence Friedman[1], Robert Cook[1], Sean King[3], Alan Myers[4], Marc van Veenhuizen[4], Chris Jezewski[4]

[1]*Material Measurement Laboratory, National Institute of Standards and Technology, Gaithersburg, MD 20899*
[2]*Department of Mechanical Engineering, University of Maryland, College Park, MD 20742*
[3]*Logic Technology Development, Intel Corporation, Hillsboro, OR 97124*
[4]*Components Research, Intel Corporation, Hillsboro, OR 97124*

INTRODUCTION

In the last few years, various scanning probe microscopy based techniques have been developed to accurately interrogate the mechanical response of materials at the nanoscale. Such measurements are critical for mechanical characterization of discrete and integrated nanoscale building blocks of high-performance electronics. In this work, by using contact-resonance atomic force microscopy (CR-AFM), nanoscale contact stiffness measurements were performed on TiN films and TiN/interlayer dielectric (ILD) structures. From these measurements, the elastic moduli of thick TiN films were determined by using the Hertz contact model. In the case of TiN/ILD structures, a significant reduction in the elastic modulus of TiN was found.

TIN FILMS AND PATTERNS

In semiconductor interconnect structures, narrow trenches are defined in low-*k* dielectric films by patterning TiN hard masks deposited on top of the dielectric films. When the dimensions of the patterned structures are well under 100 nm, the mechanical properties of both dielectric films and TiN could change during processing. The stack structure of films characterized in this work was as following: Sample 1: 300 nm TiN on 100 nm SiO_2 on Si; Sample 2: 25 nm TiN on 100 nm SiO_2 on Si; Sample 3: 25 nm TiN on 200 nm ILD on 100 nm SiO_2 on Si; Sample 4: 300 nm wide strips of 40 nm TiN on 200 nm ILD on 100 nm SiO_2 on Si; Sample 5: 300 nm wide strips of 18 nm TiN on 320 nm ILD on 100 nm SiO_2 on Si. The grain morphology of the TiN films of Samples 2 and 3 was obtained by AFM and is shown in Figure 1. From the side-by-side comparison of these AFM scans and their height distributions, subtle morphological

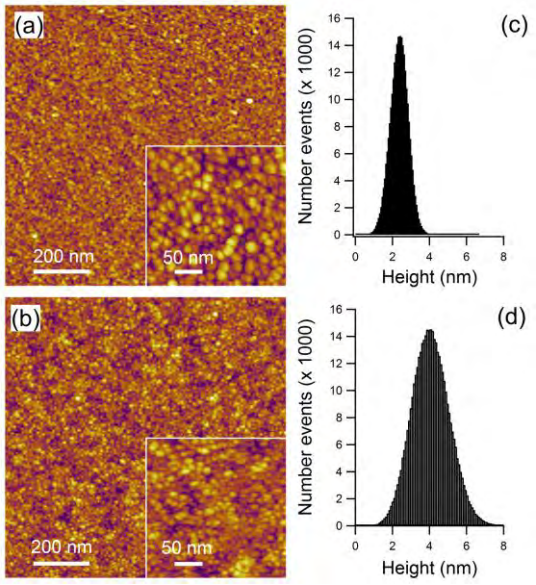


FIGURE 1. (a) and (b) Topographical grain distribution of Sample 2 and Sample 3; in the insets the TiN grains are shown at a scale factor 4 times larger than in (a) and (b). The height distributions of (a) and (b) scans are shown in (c) and (d).

WE–07

differences are observed between TiN films deposited on ILD and SiO_2/Si substrates: Sample 3 (TiN on ILD) has smaller grain size and bigger roughness than Sample 2 (TiN on SiO_2/Si).

CONTACT-RESONANCE AFM

Among AFM-based techniques, CR-AFM is remarkably distinguished in terms of elastic modulus measurements at the nanoscale, its applicability being tested in the last years on various compliant and stiff materials, thin films, integrated circuits, and nanostructures.[1, 2, 3] With controlled applied forces in the range of nanonewtons and contact radii in the range of nanometers, CR-AFM dynamically interrogates the local stiffness response of a material probed. Thus, when the probe of an AFM is brought into contact with a material, its resonance frequency changes accordingly with the stiffness of the material. The measured contact stiffness is then converted into the elastic modulus by means of a contact model that best describes the tip-sample contact. An improved accuracy in determining elastic modulus from CR-AFM is obtained when relative measurements are performed on the tested material and materials with known elastic moduli (referred to as reference materials). In the case of a Hertzian contact geometry, the reduced elastic moduli of the tested, E_S^*, and reference, E_R^*, materials are related with the contact stiffnesses measured on these materials at the same applied force by

$$E_S^* = E_R^* \left(k_S^* / k_R^* \right)^{3/2}.$$

The reduced elastic modulus includes the indentation moduli of the tip and the sample, $1/E_S^* = 1/M_T + 1/M_S$, with the indentation modulus given by the Young's modulus and Poisson's ratio of the material, $M = E/(1-\nu^2)$.

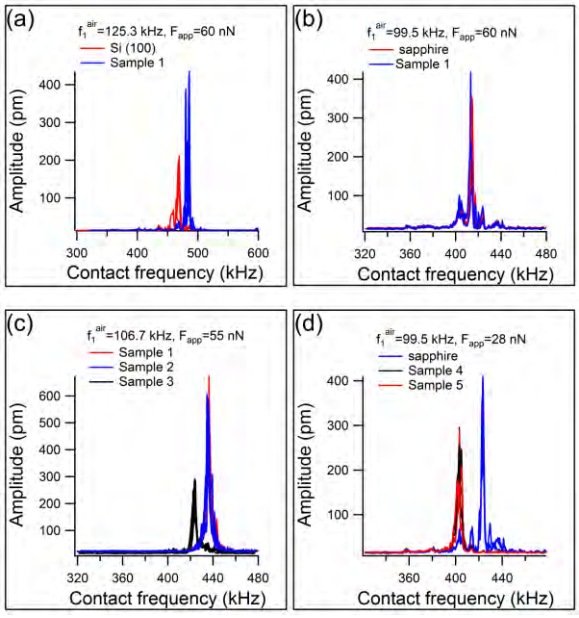


FIGURE 2. Measured contact resonance frequencies on various TiN films and patterns (300 nm wide strips) as compared with those measured on single crystal materials like Si(100) and sapphire.

In Figure 2 CR-AFM measurements are shown in terms of contact resonance peaks for the materials probed in this work. Different AFM probes were used during measurements, with the first free resonance frequency specified in each panel of Figure 2. The sets of first contact resonance peaks shown in each panel of Figure 2 corresponds to the CR-AFM measurements made alternatively on the tested materials and a reference material. For an increased measurement accuracy, two different reference materials were considered for calibrating the CR-AFM measurements on Sample 1: Si(100) with an indentation modulus of 165 GPa (see panel (a) of Figure 2) and sapphire with an indentation modulus of 467 GPa (see panel (b) of Figure 2). As can be seen, the resonance frequencies measured on Sample 1 are higher than those on Si(100), which means that Sample 1 is stiffer than Si(100), and are coincidentally close to the resonance frequencies from indenting the much stiffer sapphire. However, from the CR-AFM frequencies shown in panels (c) and (d) of Figure 2, both the TiN blanket film (Sample 3) and TiN strips (Sample 4 and Sample 5) deposited on ILD substrates appear to be more compliant than either sapphire or TiN on SiO_2/Si substrates. Thus, a direct test for the substrate contribution to the stiffness of the overlaid TiN films can be concluded from CR-AFM

TABLE 1. Contact stiffnesses and elastic moduli from CR-AFM measurements

Sample tested	Reference	$M_{Reference}$ (GPa)	$k^{*test}/k^{*reference}$	M (GPa) (from Hertz model)
Sample 1	Si	164.8	1.265 ± 0.010	408 ± 17
Sample 1, Sample 2	sapphire	466.5	0.990 ± 0.009	440 ± 20
Sample 3	Sample 1, Sample 2	440 ± 20	0.685 ± 0.033	116 ± 16
Sample 4	sapphire	466.5	0.662 ± 0.013	108 ± 5
Sample 5	sapphire	466.5	0.660 ± 0.013	109 ± 5

measurements made on Sample 2 and Sample 3 (refer to panel (c) of Figure 2), each of them having a 25 nm thick TiN film but with a measured CR-AFM frequency about 20 kHz higher on Sample 2 (SiO_2/Si substrate) than on Sample 3 (ILD substrate). Similarly, about 20 kHz difference is observed in panel (d) of Figure 2 between the contact resonance frequencies measured on TiN strips on ILD (Samples 4 and 5) and sapphire.

The elastic moduli calculated from the CR-AFM measurements discussed above are summarized in Table 1. Very good agreement for the indentation modulus of Sample 1 was obtained with the Hertz contact model between the two sets of measurements, with either Si(100) or sapphire as reference: 410 GPa vs 420 GPa (first two rows of Table 1). In the case of TiN films on ILD substrates (Sample 3, 4, an 5), the Hertz contact model, without any consideration of the substrate contribution, indicates an indentation modulus for the TiN films of about 110 GPa (refer to the last three rows of Table 1). Additionally, the finite element method was used to simulate indentations with parameters from measurements on Sample 4: an applied force of 28 nN, tip radius of 27 nm (from CR-AFM made on reference materials), layer thicknesses (from transmission electron microscopy measurements), and elastic moduli for ILD as small as few GPa. Simulations confirm that the elastic modulus of etched TiN is significantly lower, but also that it is important to augment the Hertz model with substrate effects.

CONCLUSIONS

CR-AFM measurements on TiN films and strips deposited on SiO_2/Si and ILD substrates indicated a substantial increase in the compliance of TiN films on ILD substrates. From Hertz approximation and finite element modeling a significant reduction in the elastic moduli of TiN films on ILD was found.

REFERENCES

1. G. Stan and R. F. Cook, *Nanotechnology*, **19**, 235701 (2008).
2. G. Stan, S. Krylyuk, A. V. Davydov, and R. F. Cook, *Nano Letters* **12**, 2031-2037 (2010).
3. G. Stan, S. W. King and R. F. Cook, *Nanotechnology*, **23**, 215703 (2012).

DISCLAIMER

ACKNOWLEDGMENT

This work was performed under the sponsorship of the U. S. Department of Commerce, National Institute of Standards and Technology

KEYWORDS

contact-resonance, atomic force microscopy, nanoscale mechanics

WE–08

ADHESION CHARACTERIZATION OF SiCN/SiO_2 IN BEOL AND THIN SI/PASSIVATION FOR TSV INTEGRATION USING NANOSCRATCH TECHNIQUE

Guohua Wei, Sam Ireland, Junting Liu-Norrod, Jaspreet Gandhi, Irina Vasilyeva, Anurag Jindal, Rita Klein, Tom Mendiola, Harold Krasinski, David Fillmore and Shifeng Lu

Micron Technology, Inc., 8000 S. Federal Way, Boise, ID, 80707, USA

INTRODUCTION

Interfacial adhesion is critical to the reliability of microelectronic/nanoelectronic devices, which extensively use multilayer thin films. The metrology for adhesion characterization plays an important role in enabling process development and optimization to produce interfaces possessing reliable adhesion. Since the 4 point bend (4PB) technique was developed, it has been widely accepted by the semiconductor industry as the standard method for measuring interface adhesion [1], because it is capable of quantitatively measuring the interfacial fracture energy for a variety of material systems, even for interface with ultra-thin (3-4 nm) adjacent films [2]. Although it is a powerful technique, there exist interfaces and sample geometries that are challenging for 4PB to measure.

In Back End of Line (BEOL), a dielectric barrier film such as SiCN is adjacent to both Cu and SiO_2 layers (see Fig. 1 (a)). The adhesion of SiCN/Cu interface has been successfully measured by 4PB. The SiCN/SiO_2 interface adhesion is believed to be strong, but it can still delaminate under certain thermal and residual stress levels, causing reliability issues (see Fig. 1 (b)). During the 4PB test, however, the sample containing the SiCN/SiO_2 interface broke vertically instead of being delaminated. Therefore, an alternative method is needed to characterize the SiCN/SiO_2 adhesion.

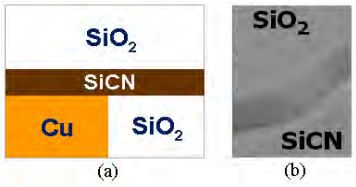


FIGURE 1. (a) Schematic of the SiO_2/SiCN/Cu multilayer structures seen in BEOL; (b) SEM image showing the SiO_2/SiCN delamination (part of SiO_2 films are gone).

Through-Silicon Via (TSV) integration involves thinning the Si wafer that contains TSVs and then depositing a passivation layer on the back side of the Si. Depending on the thinning and cleaning methods, the adhesion of thinned Si/passivation interface could be weak, affecting the subsequent process steps. From the process development point of view, it is desired to measure the adhesion between the thinned Si (<100 μm) and the passivation layer directly, which is challenging for 4PB.

WE–08

The ramping-load nanoscratch technique is a qualitative method for adhesion measurement [3-5], and has been identified as a feasible metrology to deal with the above adhesion characterization challenges. This paper presents a systematic study of applying the nanoscratch technique to measure the adhesion of SiCN to SiO_2 and thinned back side Si to the respective passivation layer. Six Si/SiCN/SiO_2 wafers deposited with different SiCN processes, and four Si/passivation wafers prepared with various thinning and cleaning methods were measured by nanoscratch test, and distinct adhesion differences were detected. The nanoscratch-induced delamination mechanism is also discussed.

RESULTS AND DISCUSSION

Fig. 2 shows the schematic crack propagation path (indicated by arrows) and the typical load-displacement curve obtained during the 4PB test for the Si/SiCN/SiO_2 sample. It can be seen that regardless of the notching side, the crack always penetrates the SiCN/SiO_2 interface vertically at a high load instead of propagating along it. It has been reported that the crack penetration across an interface into the adjacent material can occur when the interface fracture toughness exceeds about one quarter of that of the material across the interface [6]. Both SiCN and SiO_2 are brittle materials, and it is possible that the SiCN/SiO_2 interface fracture toughness exceeds ¼ of that of SiCN and SiO_2. Therefore, it is challenging for 4PB to measure such "brittle/brittle" interface with strong adhesion.

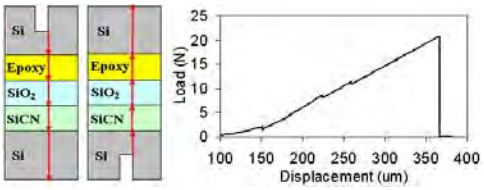


FIGURE 2. Schematic crack propagation path (indicated by arrows) and the typical load-displacement curve.

Fig. 3 shows the SEM image and the corresponding displacement curves obtained during the 75 mN nanoscratch test made on one SiCN/SiO_2 sample. In this figure, point "d" of the "during-scratch profile" shows that the maximum displacement (~670 nm) at the end of scratching was less than the SiO_2 thickness. It means that the scratch tip did not penetrate into the SiCN/SiO_2 interface during the entire nanoscratch test, preventing the tip from cracking the underlying SiCN layer. However, the plateau between point "a" and "b" of the "after-scratch profile" shows a residual depth that was close to the SiO_2 thickness. It can be deduced that starting from point "c", the SiO_2 films were delaminated due to the nanoscratch-induced stress. The normal load corresponding to point "c" is defined as "critical load", which can be used to compare the adhesion.

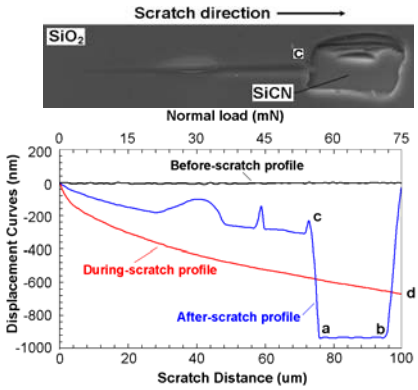


FIGURE 3. Representative SEM image and displacement curves obtained during the 75 mN nanoscratch test.

To verify that the nanoscratch-induced delamination interface was SiCN/SiO_2, not Si/SiCN, AES analysis was performed (see Fig. 4). The AES detected Si, C and N signal at the delaminated area, confirming the SiCN/SiO_2 delamination. Fig. 5 shows the optical images of the scratches and the bar chart of the critical load of six SiCN/SiO_2 wafers. The shining regions in the optical images indicate the exposed SiCN. By changing the SiCN deposition process, the SiCN/SiO_2 adhesion was significantly improved from sample A to F.

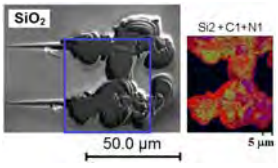


FIGURE 4. SEM image of two 150 mN scratches and the AES data obtained at the delaminated area.

WE–08

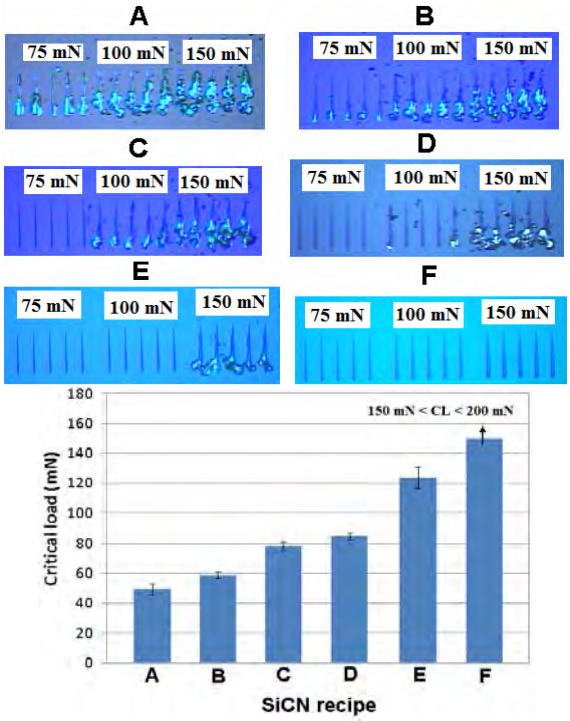


FIGURE 5. Optical images of the scratches made on six $SiCN/SiO_2$ wafers, and the bar chart of the critical load.

Fig. 6 shows the wafer stack seen during the TSV integration process. During the 4PB test, the Fig. 6 (a) sample was delaminated at the Si/adhesive interface due to its weak adhesion, and the Fig. 6 (b) sample broke either at very low load or relatively high load depending on the notching side.

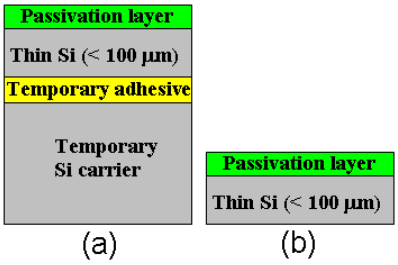


FIGURE 6. Schematic of the wafer stack for TSV integration. (a) With adhesive; (b) Adhesive removed.

Fig. 7 shows the optical images of the 200 mN scratches made on four wafers with the stack of Fig. 6 (a). It can be seen that nanoscratch test was able to induce Si/passivation delamination and clearly detect the adhesion difference among four wafers. More results will be discussed in the full length paper.

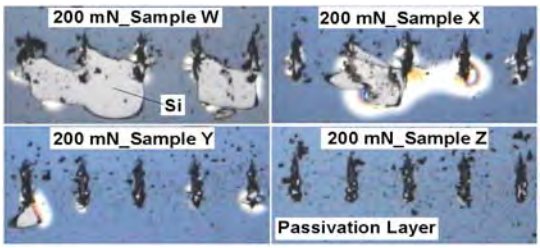


FIGURE 7. Optical images of the 200 mN scratches made on four samples with the stack of Fig. 6 (a).

CONCLUSIONS

The nanoscratch technique is able to characterize the adhesion of $SiCN/SiO_2$ interface used in BEOL, a "brittle/brittle" interface with strong adhesion, which is challenging for 4PB to measure. By controlling the normal load, thus the penetration depth, the nanoscratch-induced stress was controlled to be high enough to delaminate the $SiCN/SiO_2$ interface, but not sufficient to initiate crack in the underlying SiCN layer. The capability of nanoscratch technique as a member of the adhesion characterization metrology family is further demonstrated by its successful characterization of the thin Si/passivation adhesion for TSV integration.

REFERENCES

1. R. H. Dauskardt, M. Lane, Q. Ma and N. Krishna, *Eng. Fract. Mech*. **61**, 141-162 (1998).

2. R. P. Birringer, P. J. Chidester and R. H. Dauskardt, *Eng. Fract. Mech*. **78**. 2390-2398 (2011).

3. W. J. Liu, J. N. Zhou, A. Rar and J. A. Barnard, *Appl. Phys. Lett.* **78**, 1427-1429 (2001).

4. G. Wei and J. A. Barnard, *J. Appl. Phys.* **91**, 7565-7567 (2002).

5. G. Wei, J. Liu, D. Fillmore, M. Violette and S. Lu, *Mater. Res. Soc. Symp. Proc*. **997**, I10-09 (2007).

6. A. R. Akisanya, N. A. Fleck, *Int. J. Fract.* **55**, 29 (1992).

KEYWORDS

Adhesion, nanoscratch, four point bend, BEOL, TSV

WE–09

ANALYSIS OF LOCAL STRESS DISTRIBUTION IN A METAL GATE MOSFET WITH A NEW RAMAN SIMULATION METHOD

Tetsuya Tada[1], Vladimir Poborchii[1], Hiroshi Arimoto[1], Akira Satoh[1], Koichi Fukuda[1], Kazuhisa Fujita[2], and Toshihiko Kanayama[1]

[1]National Institute of Advanced Industrial Science and Technology (AIST)
1-1-1 Higashi, Tsukuba, Ibaraki 305-8562, Japan
[2]ASTOM R&D
2-3-13 Minami, Wako-shi, Saitama 351-0104 Japan

INTRODUCTION

Micro-Raman spectroscopy is one of the powerful techniques to measure the local stress of Si in a non-destructive manner [1-3]. However, it is impossible to characterize the stress quantitatively only from Raman shifts since the stress is a tensor quantity composed of six independent components.

To solve this issue, one estimate the stresses by comparing the measured Raman shifts and those calculated with the stress tensors obtained with the finite element method (FEM) stress simulations [4-7].

In nanoscale structures, however, the excitation and Raman scattering light intensity distributions are strongly modified by the sample structures, which has a large impact on the Raman spectra [8]. Thus, the simple comparison between the measured Raman shifts and those calculated using the stress tensors with the FEM stress simulation does not give the correct stress distribution in nanoscale regions.

In this paper, we show the newly developed Raman simulation method combined with an FEM stress simulation and a Finite-difference time-domain (FDTD) electromagnetic simulation to take account of light distribution for precise analysis of local stress distribution with micro-Raman spectra of Si nanodevice structures [9]. We demonstrate the usefulness of this method by analyzing the stress distribution in the source/drain (S/D) regions near the metal gate measured with polarized UV micro-Raman spectra in a W/TiN gate MOSFET.

EXPERIMENTAL RESULTS AND THE SIMULATION

The used sample structure, a SiN/W/TiN/ HfSiON/SiO2 gate stack, is illustrated in Fig.1. The thicknesses of the SiN, W, and TiN layers were 50 nm, 70 nm, and 10 nm, respectively. The gate length was 600 nm. Figure 2 shows scanning electron micrographs of the sample used in the Raman experiments of the top view (a), and the cross sectional view cleaved along Line A (b).

Polarized Raman measurements were performed using a UV confocal Raman microscope equipped with oil immersion micro-objective lens with *xx*- (both the polarization directions of excitation and detection lights are perpendicular to the side wall of the gate electrode) or *yy*- (both the polarization directions of excitation and detection lights are parallel to the side wall of the gate electrode) configuration. The excitation wavelength was 364 nm. The diameter of the probed area was about 120-150 nm. The peak positions of the measured spectra were determined by Lorentz curve fittings.

WE–09

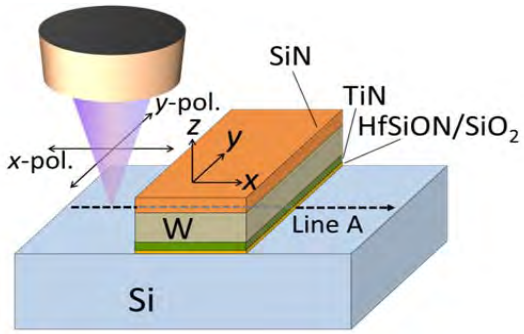


FIGURE 1. The sample structure used in the present work.

In Fig.3, the spatial variation of the Raman shifts of Si measured along Line A is plotted as a function of the probe positions with the *xx*- (□) and *yy*-polarization configurations (○). As seen, the Raman shifts increase as the probe positions come closer to the gate edge. However, the Raman shift increase for *yy*-configuration is much smaller than that for *xx*-configuration near the gate.

The difference of Raman spectra between *xx*- and *yy*-configurations can be explained by the polarization dependence of the distribution of the light intensity near the gate edge. Figure 4 shows the 2D maps of the electric field intensities calculated with the 2D FDTD simulations for the light sources of *x*- and *y*-polarizations, which indicates the sample structure strongly modify the light distribution in nanometer scale near the gate

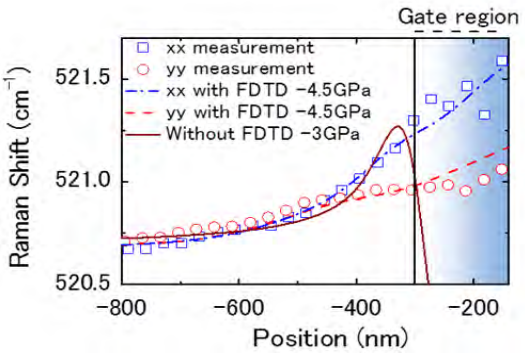


FIGURE 3. The spatial variation of the Raman shifts of the Si along Line A for the experimental results with *xx*-(□) and *yy*-polarization configuration (○). The simulation results are also shown for those with (dashed-dotted line for *xx*- and dashed line for *yy*-polarization configurations) and without FDTD simulations (solid line).

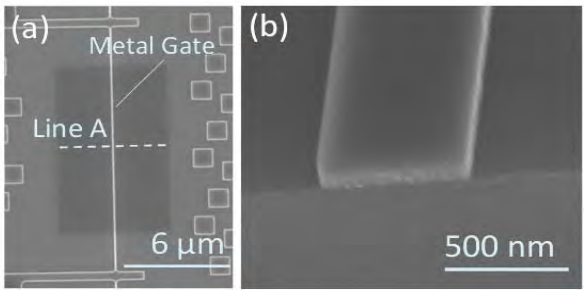


FIGURE 2. Scanning electron micrographs of the sample used in the Raman experiments of the top view (a), and the cross sectional view cleaved along Line A (b).

edge. The light intensity for the *y*-polarization is very week in the S/D region within ~50 nm of the gate edge, in contrast to that for the *x*-polarization. The FEM simulation shows that the metal gate exerts compressive stress intensively in the S/D regions within the ~50 nm of the edge. Thus, the FDTD and FEM simulations results indicate that the Raman signals from the intensively strained area contribute little to the Raman spectra measured with the *yy*-configuration, resulting in the smaller Raman peak shift than that with the *xx*-configuration.

The spatial variation of the Raman shifts along Line A was simulated using the developed Raman simulation process. In the simulation, the excitation light distribution was first obtained by the FDTD simulation for a polarized light source with a Gaussian profile (full width at half maximum, FWHM: 120 nm) located 70 nm above the gate. Then, the Raman scattering intensity was evaluated using Si Raman tensors and the calculated excitation light intensity at each mesh point in the

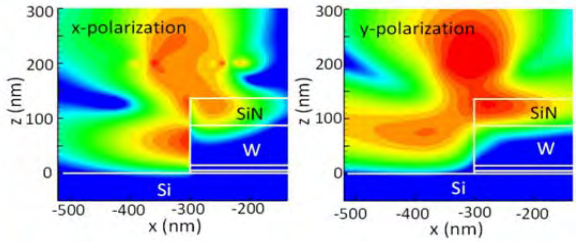


FIGURE 4. The 2D maps of the electric field intensities calculated with the FDTD simulations for the light sources of *x*- and *y*-polarizations. Light sources are located just above the gate edge.

WE–09

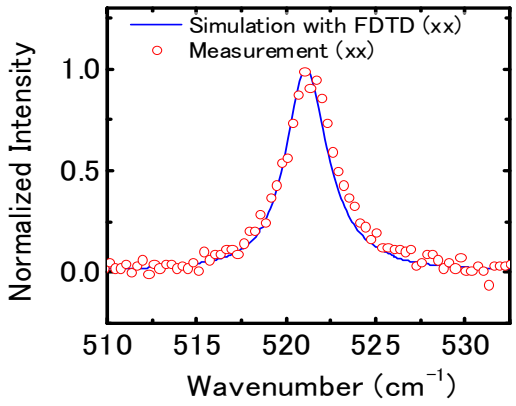


FIGURE 5 Comparison of an experimental Raman spectrum with the results of the simulation with the FDTD procedure for the *xx* polarization at a probe position of −300 nm.

sample. We assumed that each mesh point in Si emits Raman scattering light with a Lorentzian spectrum with an FWHM of 2.5 cm^{-1} and a peak wavelength calculated using the stress tensor components computed by the FEM. Finally, the Raman spectra were obtained by integrating the Raman scattering light intensity over the line 70 nm above the gate using the FDTD simulation.

To fit the simulation results with the FDTD to the measured Raman data, the initial internal stress of the gate is assumed to be −4.5 GPa. As seen in Fig.3, the simulations with the FDTD reproduce well the polarization dependence of the spatial variation of the Raman shifts and the Raman spectrum (Fig. 5). However, to fit the simulation result without the FDTD, we should assume the initial stress of the gate to be −3 GPa (solid brown line in Fig.2). Here, the simulation without the FDTD procedure cannot deal with polarization dependence, and we consider only the *xx*-polarization data, since the *yy*-polarization data contain few signals from the regions near the metal gate.

The internal stress of the tungsten film used in the gate is −4.3 GPa, which was estimated with wafer bending measurement. This value agrees well with the estimation by the simulation with the FDTD but not that without the FDTD, which means that the simulation without the FDTD gives the wrong Raman shift distribution near the gate edge.

SUMMARY

We have developed the new Raman simulation method utilizing the FDTD electromagnetic simulation and the FEM stress simulation for the precise local stress analysis of Si devices. This method can take account of the nanoscale modification of light distribution caused by the sample structures, which has a significant impact on the Raman spectra especially in the Si nanodevices.

Thus, the FDTD analysis in the Raman simulation process is essential for the precise stress analysis of Si nanodevices. We have estimated the correct stress value in the metal gate MOSFET structure with this simulation method.

REFERENCES

1. T. Tada, V. Poborchii, and T. Kanayama, J. Appl. Phys., **107**, 113539 (2010).
2. V. Poborchii, T. Tada, and T. Kanayama, Appl. Phys. Lett., **94**, 131907 (2009).
3. I. De Wolf, Semicond. Sci. Technol. 11, 139 (1996).
4. A. Yagishita, T. Saito, S. Matsuda, and Y. Ushiku, Jpn. J. Appl, Phys. **36**, 1335 (1997).
5. M. Yoshikawa, M. Maegawa, G. Katagiri, and H. lshida, J. Appl. Phys. **78**, 941 (1995).
6. E. Bonera, M. Fanciull, and G. Carnevale, J. Appl. Phys. **100**, 033516 (2006).
7. A. Satoh, T. Tada, V. Poborchii, T. Kanayama, S. Satoh, and H. Arimoto, Jpn. J. Appl. Phys. **51**, 016603 (2011).
8. V. Poborchii, T. Tada, and T. Kanayama, Appl. Phys. Lett. **94**, 131907 (2009).
9. T. Tada, V. Poborchii, and T. Kanayama, Appl. Phys. Lett. **101**, 243511 (2012).

KEYWORDS

Raman spectroscopy, Si device, Stress Simulation, FDTD simulation

AUTOMATED STRAIN MEASUREMENT USING NANOBEAM DIFFRACTION COUPLED WITH PRECESSION

A. Darbal*, R. Narayan*, C. Vartuli**, G. Lian**, S. Nicolopoulos*** and J. K. Weiss*,

*AppFive, LLC, 1095 W. Rio Salado Pkwy, Suite 110, Tempe, AZ 85281, USA
** Texas Instruments, 13121 TI Boulevard, Dallas, TX 75243, USA
***NanoMEGAS SPRL, Blvd Edmond Machtens 79, B-1080 Brussels, Belgium

INTRODUCTION

Measurement of strain with high spatial resolution and high precision in semiconductor devices is critical to monitor the designed strain distributions. For this purpose, spot diffraction patterns acquired using nanobeam illumination in the transmission electron microscope (TEM) have been used previously. Such patterns can be acquired at high spatial resolution compared to other strain measurement techniques, and the experiment is relatively straightforward to perform on most modern microscopes [1].

Previous studies using nanobeam diffraction have used the measurement of shift in individual diffraction spots to measure strain. In order to improve strain measurement precision, it is desirable to fit entire strained diffraction patterns to unstrained reference patterns. However, the presence of strong dynamical effects in electron diffraction makes such a fitting difficult. Because of the dynamical effects, spot intensity distributions are strongly dependent on local specimen thickness, so there is often little similarity between diffraction patterns from different areas. This particular challenge can be overcome by combining nanobeam diffraction with beam precession [2]. With precession, the incident beam is tilted and rotated at a high frequency (typically about 100 Hz) so that the acquired diffraction pattern is an average of all orientations within the precession cone. Dynamical effects are reduced as the incident beam is not exactly on axis and fewer beams are excited simultaneously. The use of precession also enables the collection of higher-order reflections, which are more sensitive than lower-order reflections to small changes in lattice parameters. The combination of these features makes nanobeam diffraction coupled with precession an attractive method for automated strain measurement.

METHODS

The electron microscopy was performed on a 200kV Zeiss Libra L200 TEM equipped with a field emission gun (FEG), operated in the Scanning TEM (STEM) mode. A NanoMEGAS DigiSTAR unit was used to produce precession and descanning of the electron beam. An AppFive TopSPIN data acquisition system was used to acquire electron diffraction patterns using a CCD camera while synchronously positioning the electron beam in various patterns on the specimen. A cross section sample of a blanket SiGe layer grown on a single-crystal Si substrate was prepared using Focused Ion Beam milling. The high angle annular dark field

WE–10

(HAADF) STEM image of the Si/SiGe cross section is shown in Fig. 1. Nanobeam diffraction profiles were acquired in both longitudinal (along the SiGe layer) and transverse (perpendicular to the Si/SiGe boundary) directions (Fig. 1).

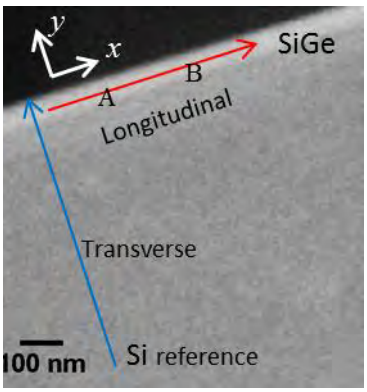


FIGURE 1. HAADF STEM image of the Si/SiGe multilayer.

A proprietary algorithm developed by AppFive was used to calculate the strain at each position of the electron beam. Diffraction patterns from strained regions of the specimen were numerically distorted in order to produce an optimum match with a reference diffraction pattern obtained from the unstrained Si region (see Fig. 1).

Results And Discussion

Diffraction patterns, with and without precession, from two points marked A and B in the STEM reference image (Fig. 1) are shown in Fig. 2. By comparing these patterns obtained from seemingly identical regions, one can see the improvement in the pattern quality when precession is included. The diffraction patterns without precession contain a small number of low-order spots that are not very sensitive to strain. Also, the spot intensities change dramatically at each position due to small changes in specimen thickness or bending. This causes problems for the automated processing algorithms, which can have significant systematic errors due to matching the wrong spots between different patterns. Additionally, less than one quarter the number of spots appear in the unprecessed diffraction patterns compared to the precessed patterns, which would lead to considerably higher statistical uncertainty in results calculated from unprecessed diffraction patterns.

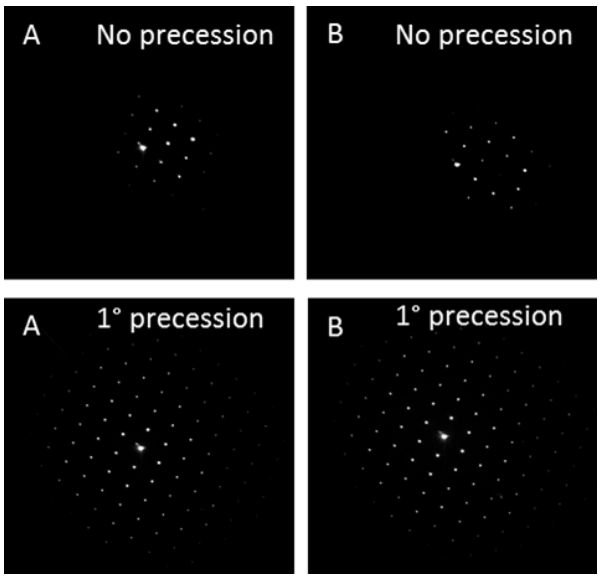


FIGURE 2. Diffraction patterns from points A and B in Fig. 1, without precession (top) and with 1° precession (bottom).

Figs. 3 and 4 show the strain profiles measured using diffraction patterns acquired with 1° precession. The transverse profile (normal to the Si/SiGe interface) was acquired with a step size of approximately 8 nm and a longitudinal profile (along the SiGe layer) was acquired with a step size of approximately 30 nm. The transverse profile shows that the Si layer far from the SiGe is unstrained and there is a sharp increase in tensile strain in the normal direction immediately inside the SiGe layer. On the other hand, strain in the longitudinal direction ε_{xx} is very small, which is consistent with the fact that the SiGe layer is coherent with the substrate. The longitudinal profile shows that the strain is relatively constant along the SiGe layer. The average normal strain ε_{yy} in the longitudinal profile was 1.22% and the standard deviation was 0.02%. It was not possible to obtain any physically meaningful results using the same automated algorithm for processing diffraction patterns acquired without precession,

due to the significant differences in the intensity distributions as shown in Fig. 2.

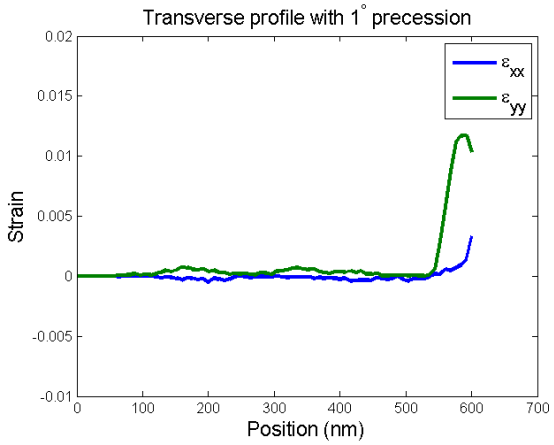


FIGURE 3. Transverse strain profile.

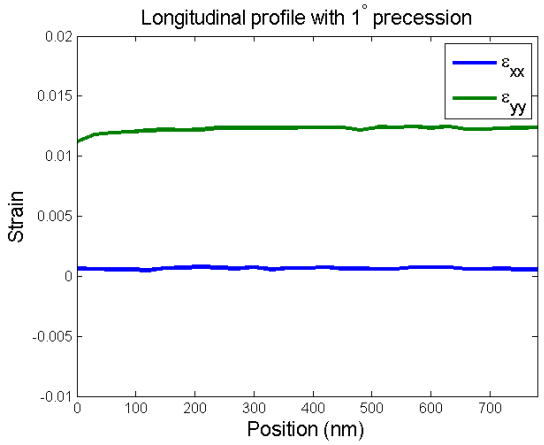


FIGURE 4. Longitudinal strain profile.

The spatial resolution of this method depends on the size of the electron probe. With most modern FEG TEMs, one can expect to produce an electron probe diameter smaller than 5 nm, although there are special compensations necessary to maintain that probe size with precession. Other precession nanobeam experiments in the TEM (for example, orientation mapping) have achieved a spatial resolution down to approximately 1 nm [3]. It is reasonable to expect similar spatial resolution with strain mapping using nanobeam diffraction.

Because of the insensitivity of precession electron diffraction (PED) towards small changes in specimen thickness, this method for strain measurement does not impose any stringent requirements on specimen preparation, as opposed to other TEM strain measurement techniques. Furthermore, spot intensities in PED do not vary with small local orientation changes in the crystal. These features make it possible to design computer algorithms that can measure strain using PED patterns with no manual input needed to identify the spots or to specify the principal strain directions.

CONCLUSION

We have demonstrated automated strain mapping using nanobeam electron diffraction coupled with precession. The analysis of the precession electron diffraction patterns to produce strain distributions required no user input. With this technique, we observed that the strain in the SiGe blanket layer was 1.22% in the direction perpendicular to the Si/SiGe interface. Strain along the direction parallel to the interface was close to zero, as expected in a coherent interface. The precision of strain measurements with this method was 0.02%. Without precession, automated strain determination from spot patterns was not possible with the current algorithm.

REFERENCES

1. D. Cooper et al., *Journal of Physics: Conference Series* **326** 012025 (2011).
2. R. Vincent, P.A. Midgley, *Ultramicroscopy* **53** 271-282, (1994).
3. D. Bhattacharyya et al, *Acta Mater.* **59** 3804–3816 (2011).

KEYWORDS

Strain measurement, TEM, nanobeam, electron diffraction, precession

WE–11

OPTICAL DYNAMIC PICOCALORIMETER FOR FAST THERMODYNAMIC MEASUREMENTS

Brian G. Burke & David A. LaVan

Materials Measurement Science Division, National Institute of Standards and Technology, Gaithersburg, Maryland, USA
david.lavan@nist.gov

INTRODUCTION

We have developed a new measurement technique for non-contact thermodynamic measurements based on optical heating and optical detection of bilayer microcantilevers. This method is capable of rates exceeding 10^6 °C/s and has heat sensitivity of 18 pJ for a dynamic measurement with 3 kHz bandwidth measured in air. By tracking resonant frequency shifts, the method has already achieved mass resolution of 0.1 pg. This approach is capable of coupled mass and thermal measurements, allowing direct measurement of mass evolution during experiments and characterization of the specific heats and specific heat capacities of nano-scaled samples.

BACKGROUND

Prior work on bilayer cantilevers demonstrated 1 pJ heat sensitivity [1,2] using exothermic reactions to generate heat or were heated using a heat bath from ohmic heaters. That work was extended to 150 fJ sensitivity at long measurement times (tens of minutes which can be expressed as 0.008 Hz bandwidth) [3]. We have already [4] extended the sensitivity to 18 pJ measured with 3 kHz bandwidth, which is equivalent to a sensitivity of 30 fJ at 0.008 Hz. Improvements to the electronics and instrument design are being implement with greater sensitivity and faster rates expected.

METHOD

Bilayer cantilevers were produced using silicon microfabrication methods ranging in size from 1 μm wide by 5 μm long to 2 μm wide by 10 μm long.

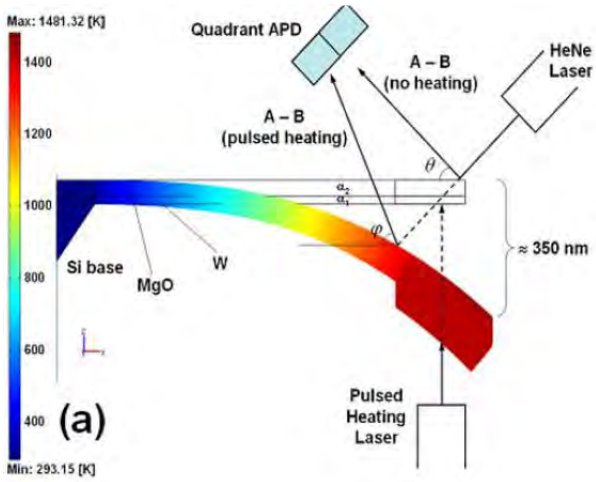


FIGURE 1. Illustration of the setup with superimposed Finite Element Modeling (FEM) results for a 5 μm² microcantilever. Displacement shown for modeled heating using a 10 mW 1.0 μs laser heat pulse in vacuum.

Tungsten and magnesium oxide were selected as the initial materials for the bi-material based on a number of requirements including high reflectivity (measuring laser side), high absorbance (heating laser side), high melting points, resistance to degradation and appropriate difference in thermal expansion. These cantilevers are substantially

WE–11

smaller than typical AFM cantilevers and require higher speed detectors to take advantage of their short thermal time constant.

RESULTS

Figure 2 provides an example of the resonant frequency observed in deflection noise density measurements on 2 μm wide by 10 μm long cantilever exposed to 5 heating cycles in air. The resonant frequency shift is 5.05 kHz and is equivalent to a mass change of 1.91 pg. Digital lock-in amplifiers can detect much smaller frequency shifts than this and instruments employing methods such as phase-locked loops will improve even further upon the sensitivity to mass changes during a measurement.

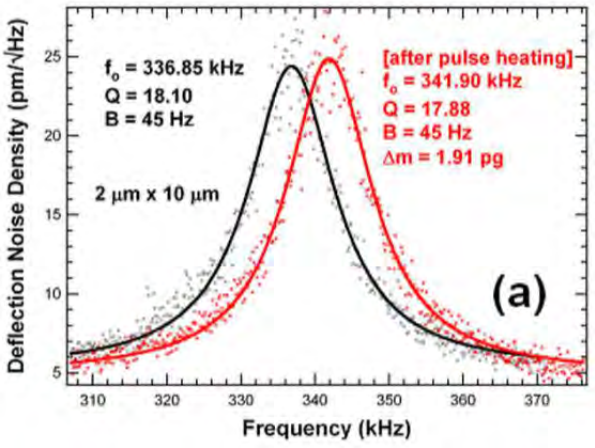


FIGURE 2. Measured resonant frequencies of a 20 μm² microcantilever showing a combination of ablation and oxidation after five cycles of laser heating in air.

Figure 3 shows an illustration of the measured displacements of the same size cantilevers as used in Figure 2 subject to laser pulse heating. Here, a 167 μs laser heating pulse was used and the entire heating and cooling cycle recorded during a 1 ms experimental period. It is interesting to note deflection peaks occurring at the beginning and end of the heating cycle which we attribute to the radiation pressure from the heating laser – this component of the signal may be useful as an internal check for the laser power and cantilever stiffness.

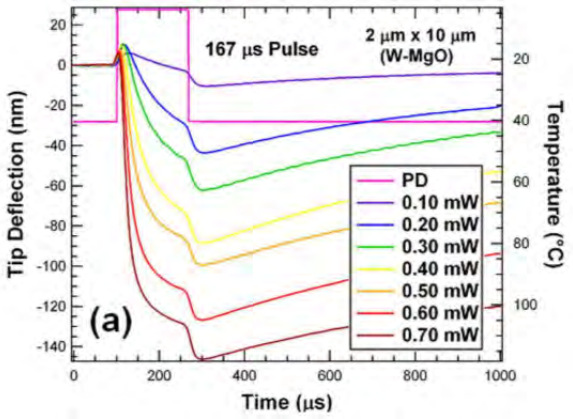


FIGURE 3. Measured heating response of a 20 μm² microcantilever as a function of laser power in air.

Research was performed in part at the NIST Center for Nanoscale Science and Technology. Certain commercial equipment, instruments, or materials are identified in this document. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the products identified are necessarily the best available for the purpose.

REFERENCES

1. R. Berger, Ch. Gerber, J. K. Gimzewski, E. Meyer, and H. J. Guntherodt, Appl. Phys. Lett. 69, 40 (1996)
2. J. K. Gimzewski, Ch. Gerber, E. Meyer, and R. R. Schlittler, Chem. Phys. Lett. 217, 589 (1993)
3. J. R. Barnes, R. J. Stephenson, C. N. Woodburn, S. J. O'Shea, M. E. Welland, T. Rayment, J. K. Gimzewski, and Ch. Gerber, Rev. Sci. Instrum. 65, 3793 (1994).
4. B. G. Burke, D. A. LaVan, R. S. Gates, and W. A. Osborn, Appl. Phys. Lett. 101, 243112 (2012)

Keywords

picocalorimetry, nanocalorimetry, picocalorimeter, nanocalorimeter, optical, laser, non-contact, thermal measurement, thermodynamic, material, properties

WE–12

ACCURACY AND RESOLUTION OF NANOSCALE STRAIN MEASUREMENT TECHNIQUES

Will Osborn[1,*], Lawrence Freidman[1], Mark Vaudin[1], Steve Stranick[1], Michael Gaither[1], Justin M. Gorham[1], Victor Vartanian[2], Robert Cook[1]

[1] Materials Measurement Science Division, National Institute of Standards and Technology, Gaithersburg, MD†
[2] 3D enablement Center Metrology, Sematech, Albany, NY

INTRODUCTION

The microelectronic and micro-electro-mechanical systems (MEMS) industries are developing smaller structures, placing them closer together, and utilizing a wider range of materials to gain the desired device properties. As a consequence, there is an increasing need to measure strain in the materials forming and surrounding devices. There are two experimental techniques that are particularly promising for making strain measurements in materials such as silicon at length scales smaller than 250 nm: Confocal Raman Microscopy (CRM) and Electron Backscattered Diffraction (EBSD). This work describes ongoing efforts at NIST to establish an experimental basis for the accuracy of measured strains and the spatial and strain resolutions of both techniques.

STRAIN MEASUREMENT TECHNIQUES

Both CRM and EBSD are measurement techniques that are widely employed for other purposes, but can also be used for strain measurement. CRM strain measurement is a specialized form of Raman spectroscopy. In our experiments, when coherent light is backscattered from a solid, a fraction of the scattered light undergoes a chemical Raman shift that is caused by inter-atomic vibrations. Because the frequency of these vibrations is a function of the strain in the material, difference in the Raman shift between two regions can be attributed to a strain difference between two positions with identical chemistry. The details of piezo Raman shifts are well described[1], but in practice this technique requires excellent spectral resolution, temperature stability, and knowledge of the phonon deformation potentials of the material being measured.

EBSD is a diffraction technique implemented in a Scanning Electron Microscope (SEM). The SEM provides an electron beam incident on the sample surface that in turn provides a "sub-surface" source of backscattered electrons, many of which have a kinetic energy very near that of the incident beam. Some of the backscattered electrons will diffract from the crystal structure of the sample to form a diffraction pattern. This pattern can be used to determine the orientation of the crystal, but can also be compared to patterns acquired from different points to determine the relative strain of the crystal between the points.

SAMPLES

As an industrially relevant material and a frequent source of strain in devices, patterned $Si_{1-x}Ge_x$ films are chosen as a test case. Two separate types of samples are in use: Reference Material (RM) 8191 prototypes that have low spatial resolution patterning and a large $Si_{1-x}Ge_x$ pad for X-ray Diffraction (XRD); and high spatial resolution fins mimicking a commercial process. The RM 8191 samples are prototypes of a reference

WE–12

material under development by NIST, and the layout of the chip is shown in Fig. 1. The first generation of prototypes utilizes three $Si_{1-x}Ge_x$ compositions, x = {0.2, 0.3, 0.4}, with two thicknesses at each composition. Thickness is used to give nominally coherent and relaxed samples from each composition so that chemical and strain effects can be separated.

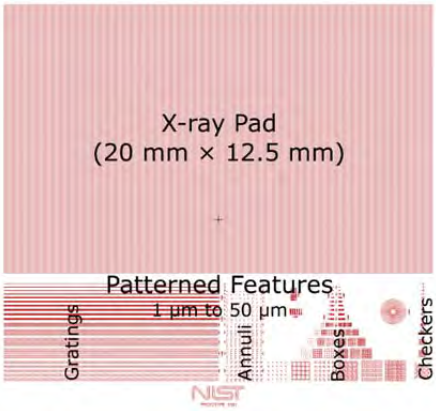


FIGURE 1. Features and layout of the RM 8191 prototype, including a large XRD and XRR pad.

The high spatial resolution lines are groups of $Si_{1-x}Ge_x$ capped fins with widths ranging between 50 nm and 150 nm, with a pitch near 350 nm. These structures have a significant over-etch, causing the Si between the $Si_{1-x}Ge_x$ lines to be completely unstrained, and allowing the Si underneath the $Si_{1-x}Ge_x$ to elastically accommodate a fraction of the strain across the line.

Accuracy of Strains

Both CRM and EBSD are best implemented as relative strain measurement techniques, so to assess the accuracy of the measured strains, the RM 8191 structure is used. The incorporation of the large X-ray pad allows XRD and X-ray Reflectivity measurements to be made on chips before and after patterning to ensure that (1) the stress state is known with small uncertainty and (2) that the processing did not damage the $Si_{1-x}Ge_x$ layer. The result of performing EBSD on the 50 µm lines and analyzing the data with cross-correlation software is presented in Fig. 2. The coherency factor of the films, η, ranges from 1 for coherent to 0 for relaxed.

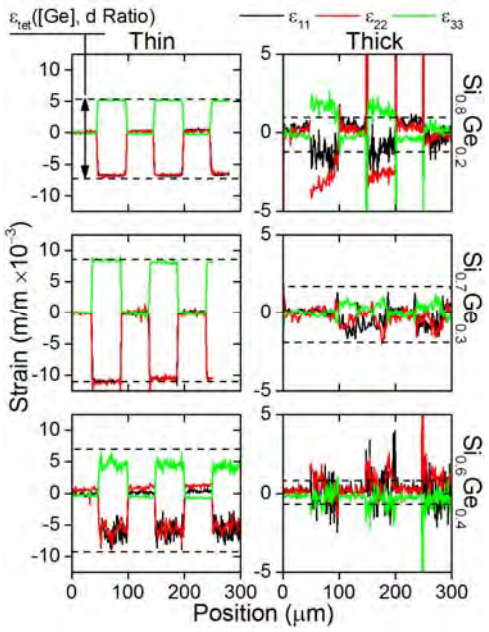


FIGURE 2. EBSD measured strains profiles across 50 µm lines of RM 8191 prototypes.

The analysis method for EBSD provides the six components of the strain tensor; however, it is not capable of determining volumetric strain, ε_{vol}. Thus, an unknown constant can be added to ε_{11}, ε_{22}, and ε_{33}, allowing ε_{11} and ε_{22} to be "zeroed out" in the $Si_{1-x}Ge_x$ regions (where $\varepsilon_{11}=\varepsilon_{22}=0$ for $\eta=1$). To address this issue and simplify the results, the metric used to assess the accuracy of the technique is the tetragonal strain, which is determined as $\varepsilon_{tet} = \varepsilon_{33} - \frac{\varepsilon_{11}+\varepsilon_{22}}{2}$ from EBSD, and can be calculated by combining X-ray Photoelectron Spectroscopy composition measurements and XRD strain measurements to determine η and ε_{tet}. The agreement of the dashed lines in Fig. 2 with the plateaus corresponding to the $Si_{1-x}Ge_x$ lines ε values indicates the strain accuracy for each sample. Similar work is being performed for using CRM.

Spatial Resolution

The features incorporated into RM 8191 are similar to sizes found in commercial MEMS, but are quite large compared to structures found in microelectronics. To explore the spatial resolution capabilities of CRM and EBSD, measurements were

WE–12

made on smaller structures. Fig. 3 shows the results of these studies on 9 adjacent 143 nm wide $Si_{0.7}Ge_{0.3}$ capped fins with a pitch of 360 nm. The CRM data presented was collected with a 488 nm excitation source, and so significant intensity from the unstrained Si substrate is present in the Raman spectra. The value plotted is the wavenumber difference between the Si-Si vibration from the unstrained silicon and the Si-Si vibration in the $Si_{1-x}Ge_x$ region.

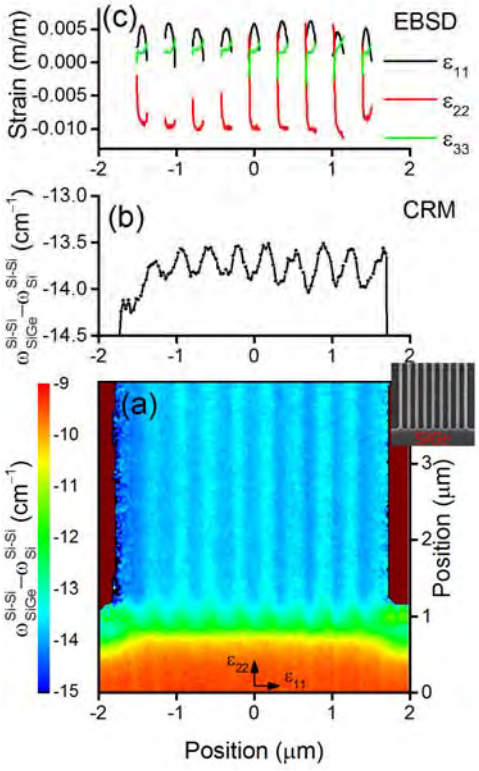


FIGURE 3. CRM mapping and EBSD line scans across 143 nm wide lines. The offset SEM micrograph shows the structures with a 4 μm field of view.

Fig. 3(b) shows the average of 10 horizontal scans from (a) as a line profile. Although it is too early for final conclusions, it is clear that: (1) the lines are relaxed compared to the equibiaxial region at the bottom of Fig. 3(a); (2) there is sufficient spatial resolution to distinguish between lines even with a laser spot size large than the line width; and (3) there is a consistent and measurable strain profile across the lines.

Fig. 3(c) shows the strain analysis from EBSD patterns collected from a dimensionally identical $Si_{0.6}Ge_{0.4}$ sample. The expected relaxation causes a significant departure from the equibiaxial strain state ($\varepsilon_{11} \neq \varepsilon_{22}$). Once again, final conclusions are premature, but: (1) the spatial resolution is more than sufficient to measure variations across 143 nm wide lines; (2) the magnitudes of the measured strains are in line with expectation.

CONCLUSIONS

Both CRM and EBSD show great promise for measuring strain in MEMS and electronic structures. The spatial resolution of EBSD is intrinsically superior, but CRM is capable of measuring structures at and below 150 nm. The strain accuracy, strain resolution, and spatial resolution of both techniques are being assessed.

REFERENCES

1. E. Anastassakis, A. Pinczuk, E. Burstein, *Solid State Communications* **8**, 133-138 (1970).
2. A. Wilkinson, G. Meaden, D. Dingley, *Ultramicroscopy* **106**, 307-313 (2006).

† Official contributions by the National Institute of Standards and Technology are not subject to copyright.

KEYWORDS

Strain Measurement, Stress Measurement, CRM, EBSD, XRD, SiGe, Reference Material

WE–13

FULL WAFER SPATIALLY RESOLVED ADHESION TESTING OF ULK-FILMS WITHOUT SAMPLE PREPARATION

Ude D. Hangen, Andy Romano, David Vodnick

*Hysitron, Inc. * 9625 West 76th Street * Minneapolis, MN 55344*

INTRODUCTION

The thin ULK films applied in modern electronics devices are cutting edge engineering products. While an increasing porosity is beneficial for the reduction of the dielectric constant κ the applied film still needs to be robust enough to support the mechanical and thermo-mechanical stresses during the manufacturing process including the CMP steps. The large mismatch of elastic properties between the ULK-film and the bulk substrate makes the interface susceptible to failure by cracking. The Youngs-modulus mismatches by a factor of 10 with a ULK–film typically reaching 10GPa to 20GPa and the underlying substrate material with a modulus between 100GPa and 200GPa. Problems of thin film adhesion or the related dielectric breakdown topic are known but the pattern of failure is random. Films are believed to behave sufficiently uniform throughout the wafers. The assumption was not confirmed by actual testing and it is therefore possible that the deposited films are less homogenous than expected. This originates from variations of thickness and different process conditions between the wafer center and the border. Therefore a metrology tool is needed to probe the thin film behavior with high spatial resolution.

NANOMECHANICAL TESTING

Nanoindentation testing and nanoscratch testing should be viewed as complementary measurement techniques to typical characterization techniques of ULK thin films. The porosity measurement by ellipsometry [1] and the adhesion measurement by 4-point-bending [2] are examples of well-established techniques used in ULK-film metrology that are time consuming and special in preparation. Therefore these tests are usually only used to characterize the wafer once.

The reduced modulus and hardness found by nanoindentation testing is correlating with different aspects of the porous film as it is sensitive to the porosity itself [3]. High porosity films show low hardness and reduced modulus values and vice versa. The critical force determined in scratch test can be correlated to the thin film adhesion; alternatively the extent of an interfacial crack generated with a wedge indenter can be monitored to quantify the adhesion strength [4]. The advantages of nanoindentation and nanoscratch are these tests can be performed on a microscopic area of a few μm^2. This allows performing thousands of tests per wafer without a special sample preparation necessary. In future mechanical tests on test structures in the scribe are possible.

WE–13

METROLOGY EQUIPMENT USED

The experiments were performed with a TI-950A nanoindenter for metrology by Hysitron, Inc. Minneapolis. The TI-950A uses the most advanced electrostatic transducer and digital controller technology to perform highly sensitive measurements in the nano-regime of indentation (0-200nm[5]). Measurements of hardness H and reduced modulus E_r can be reproduced with a standard deviation around <2% on a flat sample at 10nm penetration depth. Reproducing accurate values of hardness and reduced modulus at such a small penetration depth is of large importance to be able to extract mechanical properties out of ULK film thicknesses of 200nm. Moreover a high reproducibility in measurements is the precondition to characterize the local variation in film properties.

MECHANICAL TESTS PERFORMED

Fig. 1 shows typical indentation experiments with a Cube Corner indenter and scratches with a 1µm radius probe performed with a ramp in the normal force from 0 to 1500µN. A small force drop in the lateral force is related to the blister formation – the delamination of the ULK film from the substrate material. The normal force at this point is the critical force that is monitored. The instrument's in-situ SPM imaging capability was used to confirm that the initial critical event corresponds to film delamination while the much larger event that follows is due to film spalling. It is therefore important that the instrument used to perform the tests be able to detect the relatively subtle onset of delamination as opposed to the much more obvious film spalling event.

WAFER MAPPING

A series of 1884 nanoindentation tests were performed to determine the homogeneity of a ULK film´s mechanical properties on a single wafer. The thickness of the ULK was 200nm. Figure 2 shows the results. The notch of the wafer is on the lower end of the property map. The hardness and modulus varied by ~10-15% across the surface of the wafer. Although there was some degree of axial symmetry to the properties, there were also more localized regions of variability that were not necessarily symmetric about the center[Fig2]. It is interesting to notice that the Modulus Contour Map shows a significantly difference to the Hardness contour in the center of the wafer. Since the volume probed for the hardness and modulus value is different the difference indicates a densification of the porous film close to the substrate in the center of the wafer [5].

A series of 1884 scratch tests were performed on the same wafer with a small offset from the position used for the indentations. The critical force was detected by an automated routine. The adhesion values show a different uncorrelated pattern from the hardness and modulus contour map. The highest critical forces are found close to the notch of the wafer.

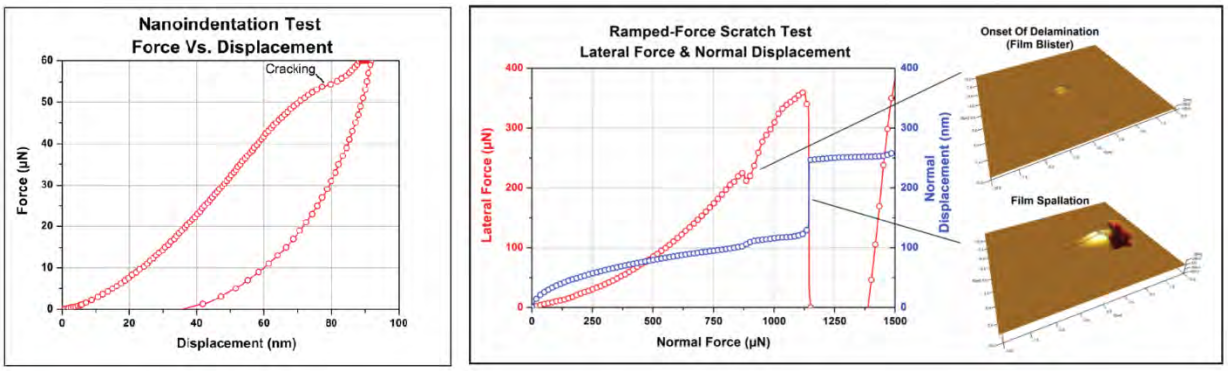


FIGURE 1. (a) Representative force-displacement curve from an indent on a ULK film.
(b) Representative data from a nanoscratch test showing how the critical load was determined.

WE–13

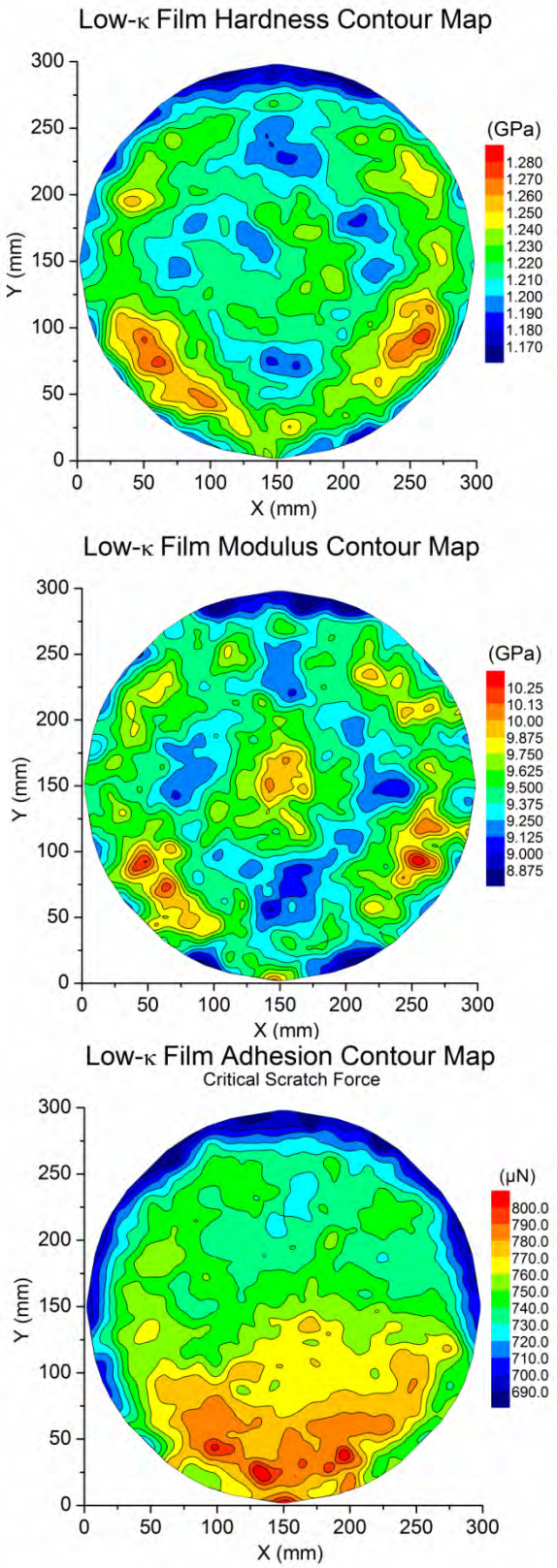


FIGURE 2 Mechanical Wafer Property Maps

SUMMARY

The wafer mapping results demonstrate that the mechanical mapping is a suitable method to monitor local changes in the deposited ULK thin films. All values vary by 10 to 15% over the full wafer range; but the local variation is in a range of 1%.

REFERENCES

1. A. Bourgeois, A. Brunet Bruneau, V. Jousseaume, N. Rochat, S. Fisson, B. Demarets, J. Rivory *Thin Solid Films* 455-456, 2004, pp 366-369
2. R.H. Dauskardt, M. Lane, Q. Ma, N. Krishna En*gineering Fracture Mechanics*, Vol 61, 1, 1998, pp 141–162
3. K.Vanstreels and A.M.Urbanowicz; *J.Vac.Sci. Technol*. B, Vol. 28, No. 1, Jan/Feb 2010
4. Hangen, U.D.; Yeap, K.-B.; Vodnick, D.; Zschech, E.; Li, H.; Vlassak,J. , *AIP Conference Proceedings* 1395, 240 (2011)]
5. ISO 14577; definition of nano-regime

KEYWORDS

Adhesion, Porosity, Elastic modulus, Hardness, Indentation, Scratch

WE–14

DESIGN OF TEST STRUCTURE FOR 3D-STACKED INTEGRATED CIRCUITS (3D-SICS) METROLOGY*

Lin You, Jung-Joon Ahn and Joseph J. Kopanski

Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology
Gaithersburg, MD 20899, USA

INTRODUCTION

As the further miniaturization and performance enhancement of electronic system is more and more demanded by the semiconductor society, the traditional planar (2D) electronic interconnection and packaging shows its difficulties to follow up the semiconductor roadmap. To walk through such limitations, 3D Stacked Integrated Circuits (3D-SICs) draw tremendous research interests and has been widely studied. [1] However, comparing with the traditional 2D circuit, the 3D-SICs are facing some challenges such as Through Silicon Vias (TSVs) and Back-end of line (BEOL) issues. [2-4] Consequently, a better understanding of the electric and magnetic fields as well as the capacitances between multi-levels of metal lines can definitely assist in the future 3D circuit design regarding cross-talk and reliability issues.

On the other hand, on the metrology point of view, the traditional Scanning Probe Microscopy (SPM) technologies showed mature capabilities of acquiring the surface metrology. However, the additional features such as subsurface imaging is certainly required in support the 3D-SICs development. Recently, several techniques, such as Scanning Microwave Microscopy (SMM), Electrostatic Force Microscopy (EFM) have shown their promising capability of subsurface characterization on different semiconductor devices. [5, 6]

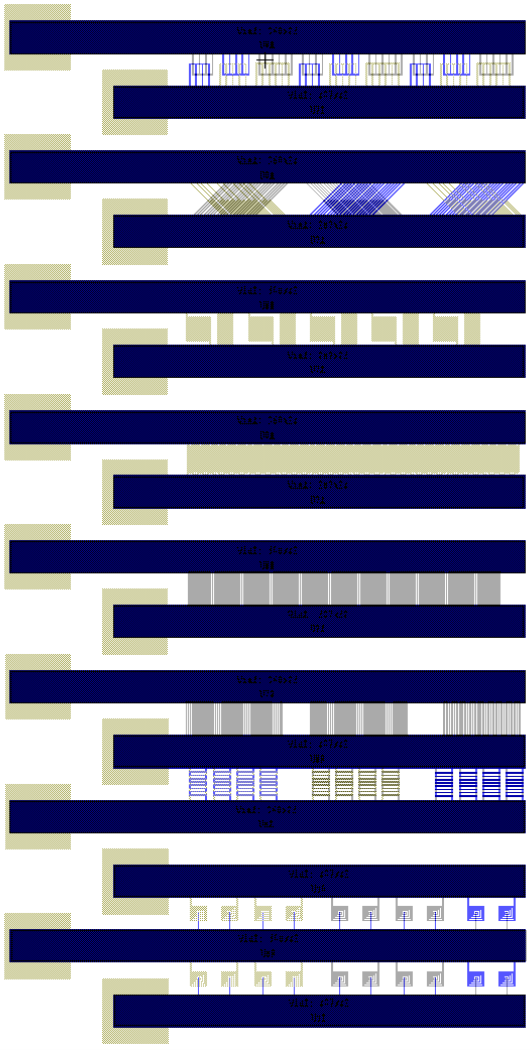


FIGURE 1. Overview of a single period of the test structure layout

WE–14

In the work plan, we will finally build up and optimize our unique SPM subsurface metrology as well as the estimation of its limit by comparing the experimental and simulation results. As the first step, we show the design of the multi-level test chip including several well-known buried structures. The single chip will be integrated on a thumb-nail size chip. The pads will be bonded on a Printed Circuit Board (PCB) allowing the external bias accesses. Different feature parts can be biased separately to simulate a Device Under Test (DUT).

TEST CHIP DESIGN CONCEPT

One period of the design layout overview is shown in Fig. 1. As the chip will be characterized by various SPM techniques, the bonding pads (big squares on the left side in Fig. 1) are designed only on one side of the chip to avoid cantilever crash. To keep the number of bonding pads, two rows of I/Os are put instead of one. The wide metal stripes (50 um thick) minimize the potential drop and keep the fine features working under same bias. The test chip including several well-known buried metal line structures, such as:

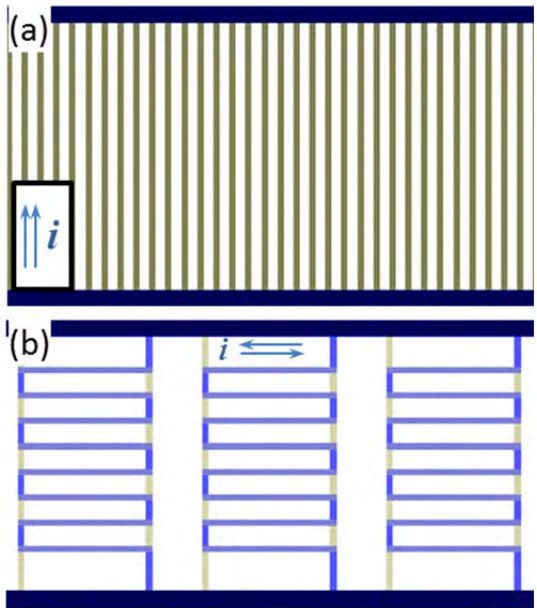


FIGURE 2. Parallel wires at different levels layout in (a) same current direction (b) reverse current directions.

PARALLEL WIRES AT DIFFERENT LEVELS

The structure can be seen in Fig. 2. This part simulates that the parallel metal lines buried at different level inside the silicon substrate. Fig. 2(a) simulates the case that the two lines have the same direction of current flow. Please note that the wires at different levels are overlapped in the layout. To simulate the current flows in reverse condition, the design is shown in Fig. 2(b). As all the lines have the same current direction (top to bottom or reverse), the overlapped horizontal parts of the wire has the reversed current flow inside.

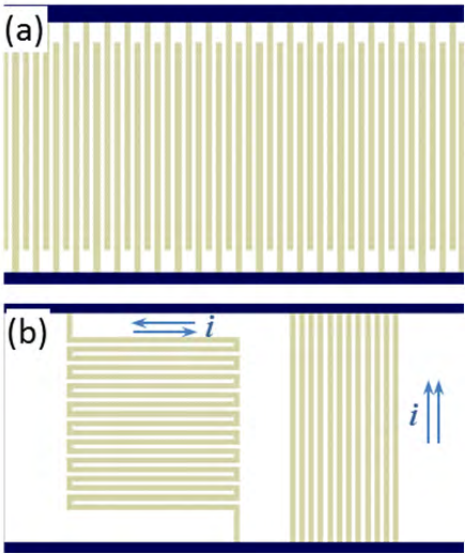


FIGURE 3. Parallel wires at the same level layout for (a) different potential simulation (b) current flow simulation.

PARALLEL WIRES AT THE SAME LEVEL

This part simulates the parallel metal lines at the same level, which could be buried inside the silicon substrate or not. In Fig. 3(a), the potential influences from close neighbor wires can be simulated. The upper and lower wires biases can be tuned differently to estimate such influences. The left part of Fig. 3(b) shows the current flow in the reverse direction while the right part simulates current flow in the same direction. Due to electromagnetic effect, the neighbor wires are expecting different electrical properties.

WE–14

PERPENDICULAR WIRES AT DIFFERENT LEVELS

In this structure, perpendicular lines at different levels can be simulated. In Fig. 4(a), the upper part of the wire can have potential differences with the lower part of wire. The surface potential information can be collected by Kelvin Force Microscopy (KFM). Different bias can be applied to the perpendicular wires at the different levels to observe the electrical field influence from the subsurface structures.

In the Fig. 4(b), the metal lines at different levels are rotated at 45° in contradict ways to create a 90° of cross-line. As the upper and lower stripes can be biased separately, the cross talk of multi-level lines can be simulated in both AC and DC voltage. In addition, some parts of lines (upper right and lower right) are not crossed and can be taken as reference

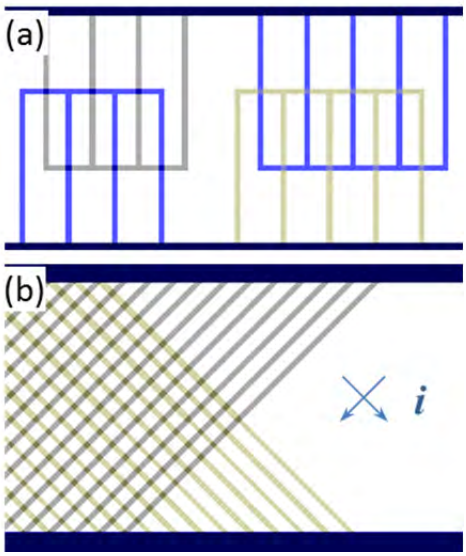


FIGURE 4. Perpendicular wires at different layers for (a) different potential simulation (b) current flow simulation.

ELECTROMAGNETISM FEATURES

Nano-loop layout is designed to create the surface/subsurface electromagnetic field. The magnitude of the magnetic field can be tuned by the applied current. The magnetic force can be detected by the Magnetic Force Microscopy (MFM). The loops are created in two reverse directions to created reverse magnetic field.

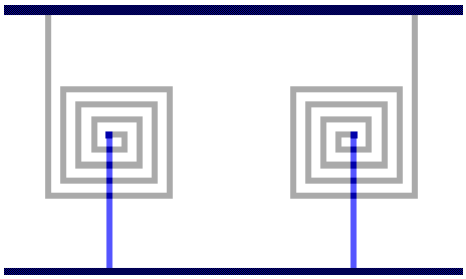


FIGURE 5. Nano-loop layout to produce magnetic field

REFERENCES

1. E. Beyne, presented at the *VLSI Technology, Systems, and Applications, 2006 International Symposium on*, (2006).
2. E. J. Marinissen and Y. Zorian, presented at the *Test Conference, 2009. ITC 2009. International*, (2009).
3. D. Z. Pan, L. Sung Kyu, K. Athikulwongse, J. Moongon, J. Mitra, P. Jiwoo, M. Pathak and Y. Jae-seok, presented at the *Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific*, (2012).
4. K. Sakuma, P. S. Andry, C. K. Tsang, S. L. Wright, B. Dang, C. S. Patel, B. C. Webb, J. Maria, E. J. Sprogis, S. K. Kang, R. J. Polastre, R. R. Horton and J. U. Knickerbocker, *IBM Journal of Research and Development* **52** (6), 611-622 (2008).
5. C. Plassard, E. Bourillot, J. Rossignol, Y. Lacroute, E. Lepleux, L. Pacheco and E. Lesniewska, *Physical Review B* **83** (12), 121409 (2011).
6. M. Zhao, X. Gu, S. E. Lowther, C. Park, Y. C. Jean and T. Nguyen, *Nanotechnology* **21** (22), 225702 (2010).

NOTE

* Official contributions by the National Institute of Standards and Technology are not subject to copyright.

KEYWORDS

3D-SICs, BEOL, MFM, KFM, SWMM, Subsurface characterization

WE–15

A NEW PROGNOSTIC TOOL FOR TSV RELIABILITY ASSESSMENT USING RF SIGNALS

Chukwudi Okoro[1*], Pavel Kabos[4], June W. Lau[2], [3]Jan Obrzut, Klaus Hummler[5], Yaw S. Obeng[1]

[1]*Semiconductor and Dimensional Metrology Division,*
[2]*Metallurgy Division,*
[3]*Polymers Division,*
National Institute of Standards and Technology (NIST),
100 Bureau Drive, Gaithersburg, MD 20899
[*]*Phone: 301-975-2040,* [*]*Email: chukwudi.okoro@nist.gov*

[4]*Electromagnetic Division,*
National Institute of Standards and Technology (NIST),
325 Broadway, Boulder, CO 80305

[5]*SEMATECH,*
257 Fuller Road, Albany, NY 12203

INTRODUCTION

Three dimensional stacking of chips achieved by using through-silicon via (TSV) has gained much attention recently, as it enables increased chip miniaturization and higher chip performance [1]. Due to the complexity associated with the integration of TSVs, most studies conducted so far have focused on solving the many processing related concerns plaguing its adoption. The challenges include, Cu-pumping [2], electrodeposition of Cu [3], wafer thinning and bonding [4], TSV proximity to transistors [5], stress / strain characterization [6] and much more.

In recent times, a few reports regarding TSV reliability, such as TSV electromigration [7] and thermal cycling studies [8], [9], based on DC resistance (R_{DC}) measurement have appeared in the open literature. However, there appears to be discrepancies in the published data, thus, the need for more independent studies.

A study performed on solder joint reliability has shown that the use of R_{DC} in reliability studies results in late or delayed prognostics in comparison to the use of radio frequency (RF) signals [10]. The RF-based approach has been used by [11] for back-end-of-line (BEOL) interconnect studies, and they found it to be sensitive to the degree of void damage in Al and AlCu metal lines. This makes using RF signals as a metrology tool for studying TSV interconnect reliability performance a worthwhile approach. Indeed, many recent studies have used RF signals to monitor TSV performance, by evaluating changes in their impedance [12]. However, the emphasis of those studies has been focused on best practices in TSV design. The studies were conducted on as-fabricated state, without applying thermal stress to the TSVs.

WE–15

In this work, RF signals were used as a prognostics tool for the assessment of the impact of thermal cycling on the performance of Cu TSVs. In order to understand the observed RF signal degradation with thermal cycling, other complimentary analysis techniques were also used, such as R_{DC} measurements, the transmission electron microscopy (TEM) and the focused ion beam (FIB).

We used a two-level stacked dies for this study. The TSVs were 5.5 µm in diameter and 50 µm deep and were located at the top chip. The top and the bottom chips were bonding using Benzocyclobutene (BCB). The studied RF test structure is a daisy chain of 60 TSVs, having a ground-signal-ground (GSG) configuration.

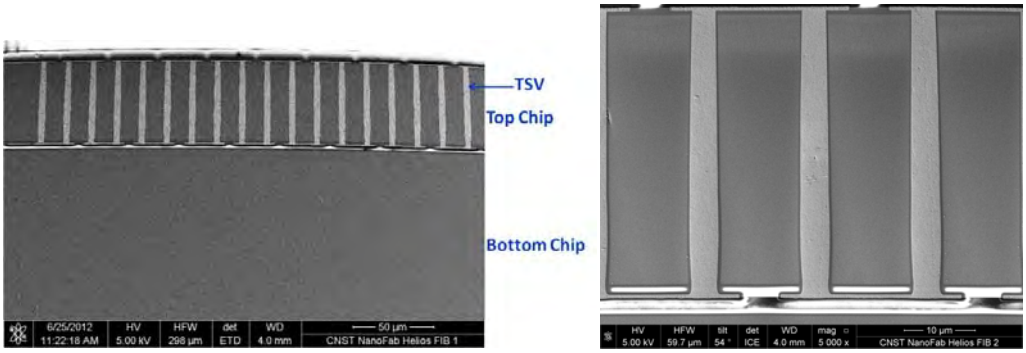
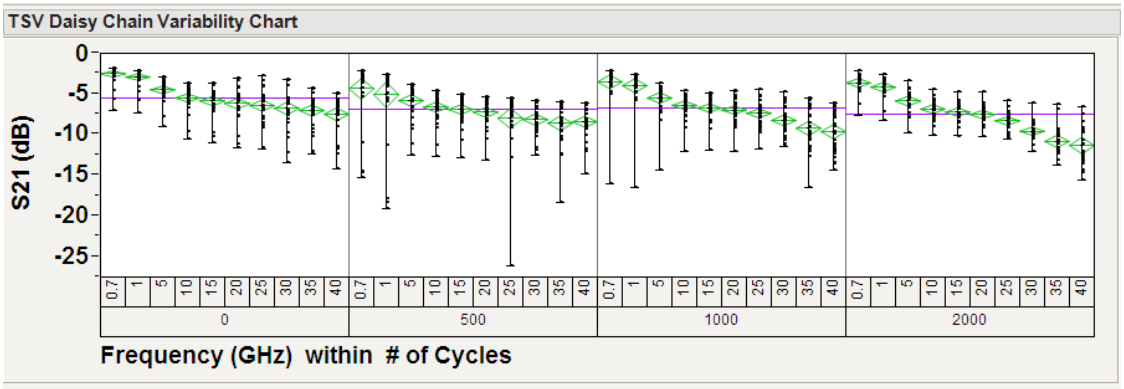


FIGURE 1. SEM cross-sectional image of the stacked chip, showing the signal TSV daisy chain.

The RF test structures were measured using the vector network analyzer (VNA), and their four component scattering-parameter (S-parameter) data were obtained. Measurements were first taken in the as-received state, prior to thermal cycling, to determine their baseline RF signal characteristics. Thereafter, the test structures were subjected to thermal cycling, as the samples were repeatedly heated and cooled from 30C to 150C. RF and R_{DC} measurements were performed every 500 thermal cycles, for up to a maximum of 2000 thermal cycles.

It was found that the signal integrity of the TSV daisy chain degrades with increasing number of thermal cycles, as shown in Figure 2. This trend is attributed to the presence of defects in the structure caused by cyclic stressing during thermal cycling.



WE–15

FIGURE 2. Variability analysis of the effect of the attained number of thermal cycles on transmission coefficient (S_{21}). The reported error bars represent ± three times the standard deviation of the thirty-four samples that were measured. The shown variability is a composite of sample-to-sample variability and systematic experimental variability.

The transmission coefficient was observed to be averagely constant from 500 - 1000 cycles. This indicates that the failure mechanism at play stabilizes, thus resulting in the observed constant transmission coefficient from 500 – 1000 cycles. However, at 2000 cycles the transmission coefficient increases further, which indicates the acceleration in the prevailing active failure mechanism or the introduction of a different failure mechanism between 1000 and 2000 cycles.

Further analysis performed using R_{DC} measurement technique showed similar trends, as the resistance of the TSV chain increased with the number of thermal cycles. This trend is attributed to the growth of voids in the test structure, as well as interface de-cohesion as confirmed from TEM and FIB analysis.

Based on the obtained results from this study, it is shown that the use of RF signals as a metrology tool for the study of the reliability of TSV interconnects is complimentary to the traditional R_{DC} measurement technique; however, it is much more informative and sensitive to the presence of discontinuities in the TSV structure.

REFERENCES

[1] C. Okoro *et al*, ECTC, June 2007, Reno, USA, 249
[2] C. Okoro *et al*, AIP Conf. Proc., Nov. 2010, Vol. 1300, 214
[3] C. Huyghebaert *et al*, ECTC, June 2010, Las Vegas, 1083
[4] B. Swinnen *et al*, IEDM, 2006, 371
[5] A. Mercha *et al*, IEDM Dec. 2010, San Francisco, CA, 2.2.1
[6] C. Okoro *et al*, IITC, May 2008, San Francisco, 16
[7] T. Frank *et al*, IPRS 2011, 3F.4.1
[8] T. Frank *et al*, ECTC, June 2010, Las Vegas, 321
[9] M. G. Farooq *et al*, IEDM, Dec. 2011, Washington DC, 7.1.1
[10] D. Kwon *et al*, ECTC, Lake Buena Vista, FL, May 2008, 606
[11] S. Foley *et al*, Microelectron. Reliab., Vol. 40, 2000, 87
[12] Joohee Kim *et al*, IEEE Trans. CPMT, vol. 1, 2011, 181

KEYWORDS

Through-silicon via (TSV), Radio Frequency (RF), Back end-of-line (BEOL), interconnect, Reliability Assessment

WE–16

TSV Reveal Height and Bump Dimension Metrology by the TSOM Method: From Nanometer to Micrometer Scale

Victor Vartanian[a], Ravikiran Attota[b], Steve Olson[c], Robert Edgeworthd, Iqbal Ali[a], Craig Huffman[a], Pete Moschak[c], Harry Lazier[c], and Elizabeth Lorenzini[c]

[a]*SEMATECH, 257 Fuller Road, Suite 2200, Albany, NY, 12203, USA*

[b]*Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD, 20899, USA*

[c]*College of Nanoscale Science and Engineering (CNSE), SUNY Albany, assignee to SEMATECH*

[d]*Intel assignee to SEMATECH*

Introduction

Through-focus scanning optical microscopy (TSOM) [1-4] is a method for conventional optical microscopes to collect dimensional information at the nanometer scale. By combining 2D optical images captured at several through-focus positions, TSOM transforms conventional optical microscopes into 3D metrology tools with nanometer-scale sensitivity for feature dimensions ranging from nanometers to micrometers.

TSOM has demonstrated an ability to provide lateral and vertical measurement sensitivity of less than a nanometer, comparable to the dimensional measurement sensitivity of other critical dimension (CD) metrology tools such as CD-SEM (scanning electron microscopy) and OCD (optical CD). The technique can measure features far smaller than the diffraction limit of an optical system because it captures much richer three-dimensional optical data at many z-heights (i.e., through focus). Additionally, TSOM appears to decouple the measurement of profile dimensional changes at the nanoscale, such as small perturbations in sidewall angle and height, with little or no ambiguity.

In this work, we will assess the extendibility of TSOM from the nanometer to micron scale by measuring 3D interconnect features such as 5 µm diameter through-silicon via (TSV) reveal pillars in the 3-5 µm height range, as well as C4 and micro-bumps with diameters of 35 to 100 µm. Measurement sensitivity to small changes in feature dimension will be assessed by simulations as well as by experimental data.

Extendibility of TSOM from Nanometer to Micron Feature Sizes

The exceptional z-height resolution of TSOM, as well as rapid measurement time, is particularly important for high volume manufacturing of 3D interconnect applications, for which cost is also a concern. For example, TSOM has demonstrated sensitivity to nanometer-scale changes in height, with an acquisition time of only a few seconds. These two attributes make TSOM particularly advantageous for 3D-stacked IC measurements of TSV reveal structures, as well as C4 bumps and microbumps. Because current instruments have several limitations, performing 3D metrology at

WE–16

micron scales with nanometer sensitivity is difficult. For example, OCD tools require numerous features within the interaction volume of the incident beam, which is not possible with the micron-scale feature sizes and pitches associated with 3D IC applications. CD-SEM measurement time is not compatible with whole wafer defect inspection.

TSOM Applied to Through-Silicon Via Reveal Features

TSV reveal wafers were used to determine sensitivity to changes in TSV height and diameter. TSVs are typically fabricated using a process shown below:

1) Etch TSVs to 50 µm deep from the wafer surface.

2) Deposit an oxide liner and a diffusion barrier.

3) Plate TSVs with Cu.

4) Flip the wafer over and bond to a carrier wafer.

5) Grind and CMP the Si down to 3-5 microns above the TSVs.

6) With Tetra-Methyl Ammonium Hydroxide (TMAH), wet etch the remaining Si and expose the Cu pillars.

The revealed Cu pillars are presented in Figure 1, showing the intact oxide liner surrounding the Cu pillar.

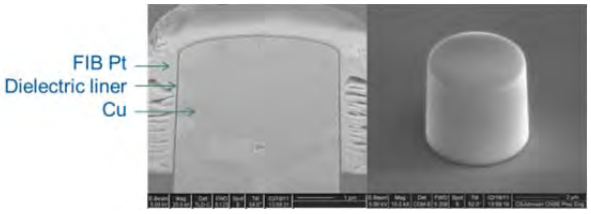


FIGURE 1. A Focused ion beam (FIB)/SEM image (left) shows a revealed TSV; tilt SEM image (right) shows a smooth Si surface.

Simulation studies indicate that the differential TSOM image (DTI—the difference between two TSOM images—, the "reference feature" and the "perturbed" feature) exhibits a detectable difference in maximum and minimum optical intensities, or optical intensity range (OIR). The OIR absolute difference in the maximum and minimum optical intensities is useful as a quantitative comparison. Using 546 nm illumination, Figure 2 demonstrates a detectable OIR for a 5 nm difference in pillar diameter (top left DTI) and a 5 nm difference in pillar height (top right DTI) compared to a 5 µm diameter pillar that is 3 µm above the Si substrate. An experimentally measured DTI is shown on the bottom.

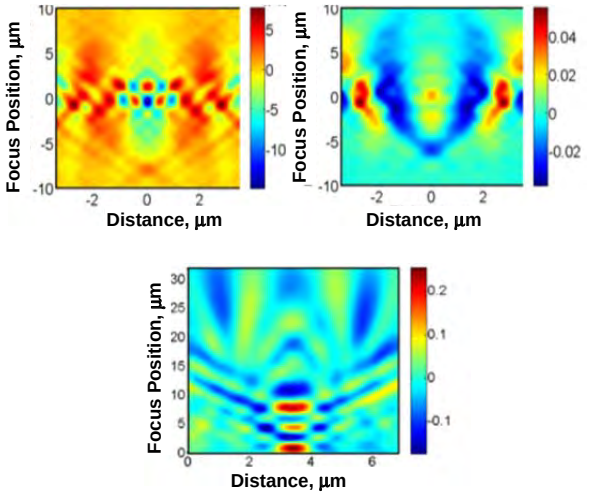


FIGURE 2. Simulated differential TSOM image for a 5 nm difference in pillar diameter (top left DTI) and for a 5 nm difference in pillar height (top right DTI) for a 5 µm diameter pillar that is 3 µm above the Si surface. An experimental DTI is shown in the bottom. Illumination wavelength is 546 nm.

The paper will compare experimental TSOM measurements with other reference metrology tools such as profilometry and SEM for dimensional information.

TSOM exhibits sensitivity to small dimensional differences between adjacent TSV reveal structures, as shown in Figure 3. Each TSV reveal structure was imaged and the OIR was measured as 16 x 10^{-2}, which is 5X the noise floor (~3 x 10^{-2}). Thus, TSOM could be a good high-speed process-variability inspection tool in HVM of bumped wafers.

WE–16

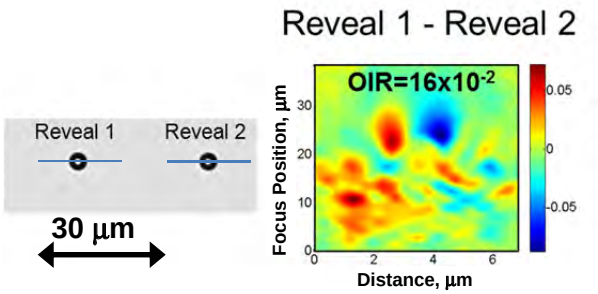


FIGURE 3. Measurements made on Cu reveal pillars within the same die indicate relatively small dimensional differences as shown by the relatively small OIR (16 x 10^{-2}).

C4 AND MICROBUMP METROLOGY USING TSOM

C4 and microbump wafers were also used to evaluate the utility of TSOM on micron-sized features. Wafer bumping (C4 or microbump) is a method for forming interconnects between integrated circuits and microelectromechanical systems (MEMS) and external circuitry using solder bumps that are deposited onto chip pads. Solder bumps are deposited on the pads on the top of the wafer during the final wafer processing step. To mount the chip to external circuitry such as a circuit board or another chip or wafer, the wafer is flipped over so that its top side faces down and its pads aligned with corresponding pads on the external circuit. Solder is then flowed to complete the interconnect. Before the wafer is flipped over, it undergoes optical inspection and metrology to determine whether any bumps are missing or bridged and whether the bumps are coplanar and are the correct size to ensure good connectivity to the pads. A top-down optical image of C4 bumps is presented in Figure 4 showing various defects.

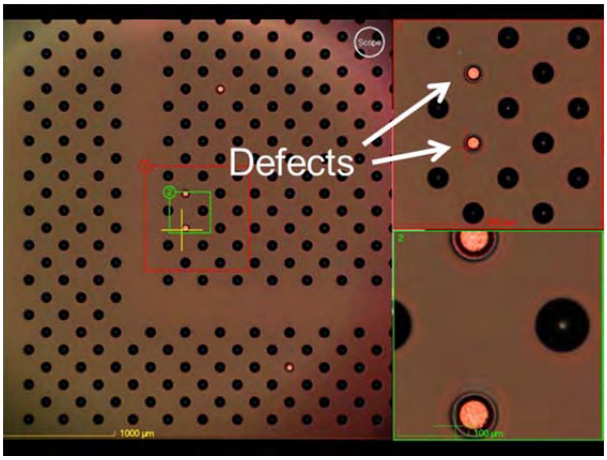


FIGURE 4. Top-down optical image showing C4 bumps including defective bumps.

The availability of a high speed, low cost bump inspection tool is critical for HVM of 3D-IC applications.

REFERENCES

1. R. Attota, R. M. Silver, and J. Potzick, *Optical illumination and critical dimension analysis using the through-focus focus metric*, Proc. SPIE, 6289, p. 62890Q-1-10 (2006).
2. R. Attota, R. M. Silver, and B. M. Barnes, *Optical through-focus technique that differentiates small changes in line width, line height, and sidewall angle for CD, overlay, and defect metrology applications*, Proc. SPIE 6922, 6922OE-1-13, (2008).
3. E. Brown, *Nanoscale dimensioning is fast, cheap with new NIST optical technique*, NIST Tech Beat, October 28, http://www.nist.gov/public_affairs/techbeat/tb2008_1028.htm#tsom (2008).
4. R. Attota, T. A. Germer, and R. M. Silver, *Through-focus scanning-optical-microscope imaging method for nanoscale dimensional analysis*, Optics Letters, Vol. 33, Issue 17, pp. 1990-1992 (2008).

KEYWORDS

TSOM, through-focus scanning optical microscopy, metrology, 3D interconnect, through-silicon via, TSV

WE–17

DEFECT METROLOGY OF EPITAXIAL GE ON PATTERNED SI WAFERS USING AN INLINE HRXRD TOOL

M. Wormington[a], P.Y. Hung[b], M.-H. Wong[b], C.T. Schamp[d], A. Giladi[c], M. Klinov[c], W.-E Wang[b], G. Bersuker[b], P. D. Kirsch[b], and R. Jammy[b]

[a] *Jordan Valley Semiconductors, 3913 Todd Lane, Suite 106, Austin, TX 78744, USA*
[b] *SEMATECH, 257 Fuller Road, Suite 2200, Albany, NY 12203, USA*
[c] *Jordan Valley Semiconductors, Zone #6, Ramat Gavriel, Migdal Ha'Emek 23100, Israel*
[d] *Novati Technologies, 2706 Montopolis Drive , Austin, TX 78741*

INTRODUCTION

The shift in consumer and enterprise trends from the desktop to mobile devices and cloud computing puts ever increasing demands on CMOS technology to offer lower power consumption and higher performance. High mobility channel materials such as Ge and III-V are strong contenders to replace Si at the 11 nm technology node or beyond [1-2]. The intrinsically higher carrier mobility and injection velocity of these materials have the potential to enable more aggressive scaling of the power supply voltage (V_{DD}) without compromising performance. These materials, however, must be integrated on Si substrates to take advantage of Si-based high-volume manufacturing (HVM) platforms. Nevertheless, direct deposition of Ge or III-V on Si results in a highly defective material due to the large lattice mismatch with the Si substrate (4% for Ge and >8% for III-V). One promising integration approach is to use an aspect ratio trapping (ART) structure whereby the Ge or III-V is grown inside shallow isolation trenches formed by a dielectric film (typically SiO_2), which limits the dislocation propagation through the film thickness, and confines defects within the lower portion of the trench. This approach is expected to result in high quality channel materials in the top portion of the Ge or III-V layer [3-5] intended to be used as the device channel. Employing this technique, Park *et al.* [6] reduced the threading dislocation density in Ge ART structures from a typical level of 10^8 cm^{-2} down to 10^6 cm^{-2}. Waldron *et al.* [7] also demonstrated the potential of HVM of III-V ART structures in a 200 mm Si process flow.

The high resolution X-ray diffraction (HRXRD) technique, in particular, the reciprocal space mapping (RSM) approach, has shown potential for non-destructive monitoring of the defect density of Ge or III-V on both ART-patterned silicon wafers and conventional epitaxial-grown blanket wafers [3-4]. However, a typical RSM measurement takes several hours and, while valuable for materials and process development, is not practical for (inline) production monitoring. This paper demonstrates the use of an inline HRXRD technique for the characterization of structural defects in the Ge ART structures. The extracted defect densities are shown to match those of transmission electron microscopy (TEM) performed on the same samples.

EXPERIMENTAL

SAMPLES

The ART samples studied in this work were fabricated on 200 mm on-axis Si(001) substrates. A

WE–17

550 nm SiO_2 layer was first formed by thermal oxidation, followed by lithographic patterning and plasma dry etch. Two samples with different pitches and aspect ratios were targeted: sample 150, which has a 150 nm Ge trench and 450 nm SiO_2, and sample 350, which has a 350 nm Ge trench and 1050 nm SiO_2. Thus, sample 150 has a narrow pitch and a higher aspect ratio than sample 350.

High Resolution X-ray Diffraction

HRXRD measurements were done using a Jordan Valley JVX7200 X-ray metrology tool as described by Wormington *et al* [8]. Measurements of the symmetric 004 Bragg reflection were done using the FastHRXRD mode in which the incident beam slit is opened wide and the diffracted intensity distribution is acquired simultaneously in about 30 s. In addition, RSMs were collected by using a narrow slit to reduce the incident beam divergence to about 0.02 deg. The position of this slit in the beam was then scanned to adjust the incidence angle from -3 to +1 deg with respect to the substrate peak position without changing the spot position on the sample. The diffracted intensity over a range of about 4 deg was then acquired at each step of the slit as is done in a conventional, parallel beam diffractometer. Measurements were with the X-ray beam both parallel and perpendicular to the ART structure to look for asymmetries in the defect distribution.

To verify the FastHRXRD data, we compared the results with those obtained from the RSM data and from TEM imaging.

Transmission Electron Microscopy

Plan-view and cross-sectional TEMs were collected to provide complementary information about defect distribution. The cross-sectional orientation imaged along the [110] ART axis direction gives a defect profile in the Ge from the top coalesced layer down to the bottom of the trench; the plan-view orientation imaged normal to the surface along the [001] direction reports defects residing throughout the thickness of the TEM sample, which is on the order of 100 nm, therefore mainly revealed the defect reside in the coalesced layer.

Results and Discussion

Two types of defects were detected in the TEM images shown in figure 1: stacking faults (SFs), which have a "boxy" appearance, and threading dislocations (TDs), which look like wavy lines on the TEM.

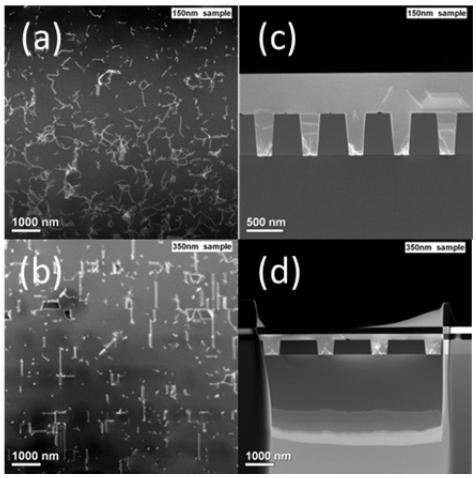


FIGURE 1. ADF-STEM micrographs of plan–view TEMs (a) top left: sample 150, (b) bottom left: sample 350. Cross section TEMs (c) top right: sample 150, (d) bottom right: sample 350.

The plan-view TEMs show that threading dislocation was dominant in the narrower trench sample (sample 150), whereas SFs are dominant in the wider trench sample (sample 350). The trench width also impacts the thickness of the coalesced Ge after CMP. In particular, sample 150 has a thicker coalesced layer (~500 nm) than sample 350 (~230 nm). The defect densities determined from analysis of the TEM images are given in table 1.

TABLE 1. Defect density from TEM measurements.

Sample	*Defect density (cm^{-2})*
150	Cross section: 2.2 x 10^8 in top 100nm and 3x10^9 for the epitaxial Ge film Plan view: total 2x10^9
350	Cross section: 0 in top 100nm and 2x10^9 for the epitaxial Ge film Plan-view: total 1.7x10^9 (TD 3.6x10^8, SF 1.3x10^9)

Figures 2 show the FastHRXRD data for the symmetric 004 reflection measured with the X-ray beam perpendicular to the ART trenches for sample 150. The angular position of the Ge Bragg peak gives the strain relaxation of Ge and its full width half maximum (FWHM) is related to the crystal quality. For quantitative analysis, we performed peak fitting to accurately extract the peak position and FWHM. The diffraction signal from sample 150 is highly asymmetric, requiring two Gaussian peaks to achieve a good fit to the data. Zaumseil et al. [5] reported a similar asymmetric peak shape in conventional ω/2θ scans and assigned the (weaker) peak with the larger angular separation from the Si substrate peak to Ge in the trenches and the peak with the smaller angular separation (also stronger) to the coalesced Ge layer. The peak position of the Ge in the trenches indicates that the material is essentially fully relaxed, *i.e.,* has bulk lattice parameters. The peak position of the coalesced Ge layer is due to a small in-plane tensile strain ε_{xx} = 0.19% due to the mismatch in the coefficient of thermal expansion (CTE) between Ge and SiO_2.

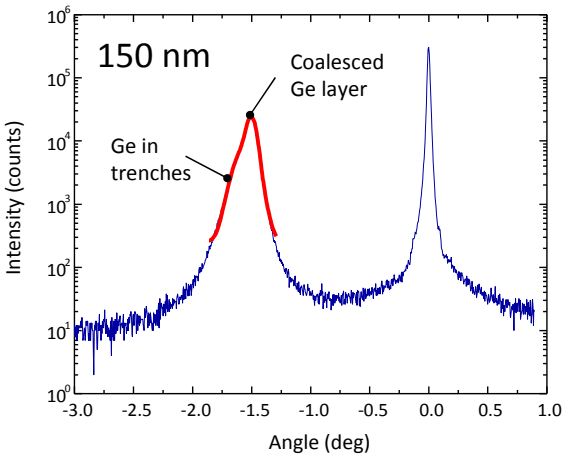


FIGURE 2. FastHRXRD diffraction data collected with the X-ray beam perpendicular to the trenches for sample 150, the broad (red) line is the sum of the two Gaussians used to fit the peak.

For sample 150, the FWHMs of the Ge signals from the trench layer is broader than the coalesced layer (not shown), indicating that the trench Ge has poorer crystal quality, which agrees with our TEM results and a previous publication [6]. The Ge diffraction peak from sample 350 is more symmetrical and can be fitted as a single Gaussian function possibly due to the much thinner coalesced layer. The FWHMs were similar both parallel and perpendicular to the trenches indicating an isotropic distribution of defects in the Ge.

TABLE 2. Defect density from FastHRXRD measurements. Values are average of measure

Sample	***FWHM (deg) [Defect density (cm^{-2})]***
150	Coalesced layer: 0.093 [3.8 x 10^8] Trench layer: 0.205 [1.9 x 10^9]
350	0.255 [2.8 x 10^9]

The defect density in the Ge from the HRXRD data was estimated using the simple model proposed by Ayers [9] for GaAs on Si which relates the FWHM of the omega rocking curve, β (rad), to the threading dislocation density, D (cm^{-2}),

$$D \sim \frac{\beta^2}{4.36b^2} \qquad (1)$$

where $b = a/2$ <110> (~ 4 Å) is the Burgers vector of the dislocations.

Essentially the threading dislocations create a distribution of tilts within the crystal lattice that broaden the diffraction peak. Hence D provides an estimate of the volume averaged defect density in the Ge under the assumption that threading dislocations are the dominant defects. The quantity β is defined for an ω-scan on a conventional diffractometer not the peak width in the FastHRXRD data. However, for reasonably thick layers (> 100 nm) the peak for imperfect (high TDD) epilayers is dominated by the tilt distribution and using the FastHRXRD peak width yields defect densities that are within 10% of those obtained from Q_x data extracted from the RSMs, which is within the level of uncertainty of the analysis method itself.

Comparing the HRXRD with TEM results we see that the defect density for both techniques is in reasonable agreement. The defect density the coalesced layer of sample 150 is one order of magnitude lower than that in the trench area,

WE–17

indicating that the current ART design confined the defect in the trench region. The overall defect density in the trenches is around 10^9 cm^{-2}, which agrees with most of the published defect density data for Ge deposited on Si.

Comparison Between FastHRXRD and RSM Results

Figures 3a and b show RSMs for samples 150 and 350, respectively. RSM provides more information than FastHRXRD measurements, but the acquisition time is very long (a few hours/map) limiting the technique to R&D applications.

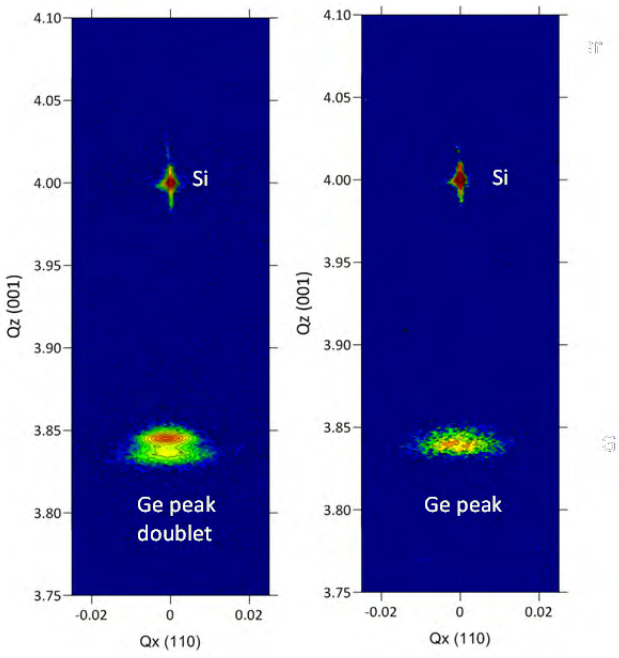


FIGURE 3. Reciprocal space maps (RSMs) around the symmetric 004 Bragg reflection from Si measured using a JVX7200 X-ray metrology tool. Left: RSMs from sample 150. Right: RSMs from sample 350.

The map in figure 3b shows that the Ge peak broadening in the FastHRXRD measurements of sample 350 is due to scattering in the Q_x direction due to tilts induced by the defects at the bottom of the trenches. For sample 150 there is also broadening of the Ge peak in the Q_z direction as a result of the different lattice parameters of the material in the trenches and coalesced material.

Summary and Conclusion

We have demonstrated the capability of an inline HRXRD metrology tool to monitor the defect density of ART samples by studying Ge ART samples with different pitches and aspect ratios. The defect density extracted from FastHRXRD is comparable to the values obtained using RSMs and TEM analysis. With a typical measurement time of ~30 seconds, this tool provides fast and non-destructive feedback to support optimization of the ART processes in the R&D phase; it is also expected to enhance fabrication yield. This study demonstrates that the trench width in the Ge ART can affect defect type and density, as well as thickness of the coalesced Ge layer. In particular, when the Ge trench width is increased from 150 nm to 350 nm, the dominant defect type changes from threading dislocations to stacking faults. The post-CMP coalesced Ge layer also becomes thinner as the trench is widened.

References

1. T. Krishnamohan, D. Kim and K. Saraswat, in Fundamentals of III-V Semiconductor MOSFETs, edited by S. Oktyabrsky and P. D. Ye (Springer, New York, 2009), pp.7-30.
2. M.J.H. van Dal et al., IEDM (2012) section 23.5, publication pending
3. E.A. Fitzgerald and N.Chand, *Electron. Mater.*, **20**, 839 (1991)
4. E.A. Fitzgerald et al., *J. Vac. Sci. Technol., B* **7**, 782 (1989)
5. Zaumseil et al., *J. Appl. Phys.,* **106**, 093524 (2009)
6. J. S. Park et al., *Electrochemical and Solid-State Letters*, **12** ,H142 (2009).
7. Waldron et al., *ECS Trans.,* **45**, 115 (2012).
8. M. Wormington, et al., AIP Conf. Proc. 1395, 198 (2011).
9. Phillips, P.J., et al., *Ultramicroscopy*, **111**, 1483 (2011).
10. J.E. Ayers, *J. Cryst. Growth.,* **135**, 71 (1994)
11. Leonhardt et al., *J. Appl. Phys.*, **110**, 073516 (2011)

Keywords

Aspect ratio trapping, ART, Ge, III- , high-resolution XRD, defect density, TEM

WE–18

XPS tool matching and Optimization for EUV optics Contamination Studies

Yudhishthir Kandel*, Mihir Upadhyaya*, Gregory Denbeaux*, Cecilia Montgomery**

*College of Nanoscale Science and Engineering, University at Albany, SUNY, 257 Fuller Rd, Albany, NY 12203
**SEMATECH, 255 FullerRd, Albany, NY 12203

INTRODUCTION

The lithography industry is making a transition from Deep Ultra Violet (DUV) lithography using 193nm radiation to EUV (Extreme Ultra Violet) radiation using 13.5nm (92 eV) of radiation. EUV radiation has very little transmittance in air and requires high vacuum for operation. EUV radiation is ionizing and can be absorbed by trace amount of contaminants present on the optics surface, hence adversely affecting the performance of the exposure tool. Photoresist, a radiation sensitive polymer coating, outgasses in vacuum during the exposure which can leave residue on the optical surfaces [1]. Some of the residue can be cleaned while some residue may be permanently left behind. It is necessary to measure the amount of non-cleanable residue left after exposing each photoresist so a proper evaluation could be made on the contaminating properties for each sample. This is paramount to the protection of expensive optics.

An evaluation procedure was designed and developed according the specification from ASML[2] at a custom Resist Outgassing and eXposure (ROX) tool at the College of Nanoscale Science and Engineering [3, 4, 5]. A witness plate is impinged with 800μA/cm^2 300 eV electron beam. At the same time a wafer coated with photoresist under evaluation is exposed using EUV photons in the same chamber. During exposure the outgassed byproduct gets deposited onto the surface of the witness plate. The thickness of the contamination is measured using a spectroscopic ellipsometer and then cleaned with atomic hydrogen. The remaining, residual contaminant on the witness plate is what we classify as the non-cleanable contamination. We then use XPS to measure the atomic concentration of the non-cleanable contamination.

XPS MEASUREMENT

ASML specification requires each species on the surface of the witness plate be measured within 0.1% of the measurement as compared to one certified by ASML. There were several issues encountered in setting up the XPS measurement procedure. Variations in measurement from one tool to another, variations in measurement of a tool over time and user handlings, and sample modification over time due to shipping, handling and X-ray exposure.

TOOL TO TOOL VARIATION

ASML requires we use Al Kα radiation that is capable of sampling 8-10 nm of sub-surface volume for analysis. There were no detailed guidelines on the transmission function calculations, relative sensitivity factors, peaks and background determination. Tool manufacturers have differing methods and numbers for these parameters, so matching is a challenge. As soon as angle between irradiation and signal collection is varied from ideal

WE–18

collection angle of about 54 degrees, relative sensitivity factors needs to be corrected accordingly. Calculation of transmission function is dependent on the choice of relative sensitivity factors of the peaks used for deriving such equation. As a result, tool transmission function, peak background subtraction, and selection or determination of relative sensitivity factors needs to be done consistently between tools to have comparable results.

We did a comparative study of different transmission functions, relative sensitivity factors and background choices as suggested in the literature as well as by the equipment manufacturers. We found the transmission function measured at constant pass energy assuming the correctness of modified Wagner relative sensitivity factors [6] and Shirley background [7] subtraction. We measured 7 peaks of pure metal and stoichiometric samples of S, Ag, Cu, Au, and Ru. A custom MATLAB code was written to carry out the analysis procedure.

Great care was taken to make sure the analysis across the tool is done at the same spot. Relative sensitivity factors were corrected for the angle offset from the ideal angle. This produced the best matching results.

Tool	S2p	W4d5	P2p	Ru3D	O1s	N1s	Si2s
Quantera II	3.4	0.3	1.1	47.9	41.3	5.5	0.4
Thermo Scientific	5.7	0.2	1.4	46.5	39.3	6.2	0.7

VARIATIONS WITH THE SAME TOOL

Results would fluctuate even when measured by the same tool using the same method for scanning and analysis due to the statistical fluctuations in the number of electrons collected by the detector. It is therefore necessary to scan for multiple times and take an average to achieve the desired precision.

The amount of signal collected also depends on the pass energy and the dwell time in addition to the number of scan cycles used. The greatest pass energy was selected that would provide the required peak width resolution to distinguish between the closest peaks expected in these samples. The x-ray source might deteriorate over time owing to the degradation of anode, monochromator or the electron beam source. The reduced x-ray intensity would inversely affect the statistics of the measurements.

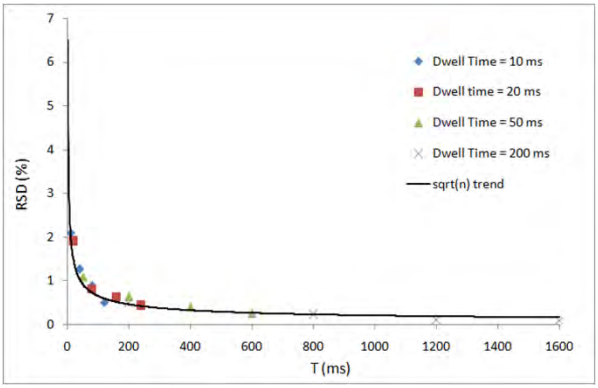


FIGURE 1. Relative standard deviation as a function of the total acquisition time per point. Energy step size of 0.2 eV and pass energy of 224 eV was used. Anode setting of 300 µm 65 W 18 kV was used.

We experimentally determined the scan parameter that would give 0.1% standard deviation for Au4f peak. Figure 1, shows the error accumulated as a function of total scan time used for a scan. Noise in the data was measured to be proportional to square root of the total signal collection time. This information along with the calculated transmission function and manufacture provided and angle offset corrected relative sensitivity factors were used to optimize the

WE–18

number of scan for each peak. It allowed us to achieve the desired accuracy at the least amount of time.

REFERENCES

1. Yu-Jen Fan, Leonid Yankulin, Alin Antohe, Petros Thomas, Chimaobi Mbanaso, Rashi Garg, Yunfei Wang, Andrea Wüest, Frank Goodwin, Sungmin Huh, Patrick Naulleau, Kenneth Goldberg, Iacopo Mochi, Gregory Denbeaux, *"Effect of Carbon Contamination on the Printing Performance of Extreme Ultraviolet (EUV) Masks"*, Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures), **28**, Issue 2, pp. 321-328 (2010).
2. N. Harned, *International Symposium on Extreme Ultraviolet Lithography*: Miami, Florida, 17-20 October 2011.
3. Chimaobi Mbanaso, Seth Kruger, Craig Higgins, Yashdeep Khopkar, Alin Antohe, Brian Cardineau, Gregory Denbeaux, *"Mass spectrometer characterization of reactions in photoresists exposed to extreme ultraviolet radiation",* Proc. SPIE **7969**, Extreme Ultraviolet (EUV) Lithography II, 79692J, 2011.
4. A. Antohe, C. Mbanaso, Y.-J. Fan, L. Yankulin, R. Garg, P. Thomas, G. Denbeaux, E. C. Piscani and A. F. Wüest, *"EUV resist outgassing: scaling to HVM intensity",* Proc. SPIE **7271** - The International Society for Optical Engineering, , pp. 26-1-7 (2009).
5. Genevieve Kane, Yudhi Kandel, Mihir Upadhyaya, Yashdeep Khopkar, Horace Bull, Chris Deitrick, Greg Denbeaux, Dominic Ashworth, Chandra Sharma, Jaewong Sohn, Dan Craft, Bill Colman *Witness plate outgassing update in Albany SEMATECH and CNSE,* IEUVI Resist TWG, Brussels Sept. 2012.
6. Wagner, C.D., et al.. *Empirical atomic sensitivity factors for quantitative analysis by electron spectroscopy for chemical analysis.* Surface and Ineterface Analysis, 1981. **3**(5): p. 211-225.
7. Shirley, D.A., *High resolution X-ray photoemission spectrum of the valance bands of gold,* Physical Review B, 1972. **5**(12): p.4709-4714.

KEYWORDS

EUV, Optics, XPS, Outgassing, Contamination, Tool matching

WE–19

CROSS SPECTRUM NOISE SPECTROSCOPY FOR DEEP LEVEL TRAP DETECTION IN NANO-SCALE SEMICONDUCTOR DEVICES

Deepak Sharma[1,3], Sergiy Krylyuk[1,4], Abhishek Motayed[1,4], Qiliang Li[2,3], Albert V. Davydov[1]

1. National Institute of Standards and Technology, Material Measurement Laboratory, Gaithersburg, MD 20899 USA
2. National Institute of Standards and Technology, Physical Measurement Laboratory, Gaithersburg, MD 20899 USA
3. Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030 USA
4. IREAP, University of Maryland, College Park, MD 20742 USA

INTRODUCTION

It is well recognized that deep energy levels may detrimentally affect the performance of semiconductor devices. However, application of traditional methods to study deep levels, such as deep level transient spectroscopy (DLTS) [1], photo-induced current transient spectroscopy or low frequency noise (LFN) spectroscopy, often becomes impractical for nano-scale devices. It turns out that by measuring the noise spectra of the dc current flowing through a uniform semiconductor biased with a small dc voltage, we can estimate energy, time-constants, and density of the generation-recombination (G-R) centers present in the sample [2]. Low-frequency noise or "spontaneous fluctuations" in current through semiconductors exists due to the stochastic nature of the conduction process and was first studied in details by A. Van Der Ziel [3]. Later, the theory of fluctuations due to Shockley-Read-Hall (SRH) centers in Si junction field-effect transistors (FETs) was successfully developed by Lauritzen and Shah [4]. Copeland finally demonstrated the equations necessary for extraction of the trap parameters in n-type GaAs [5]. This theory was further refined and employed by F. Scholz for measuring noise in Si MOSFETs for characterization of the deep and shallow levels in Si [6].

NOISE MEASUREMENT SETUP

In LFN spectroscopy, the accurate measurements of the noise signal in low-current nanowire devices such as FETs are extremely challenging because the device noise, which is proportional to the dc current, becomes comparable with the instrumental noise of the measurement setup. To overcome these issues, we have implemented a LFN measurement method based on dual-channel cross-spectrum analysis technique (Figure 1) [7, 8]. This effectively reduced the power spectral density (PSD) by three

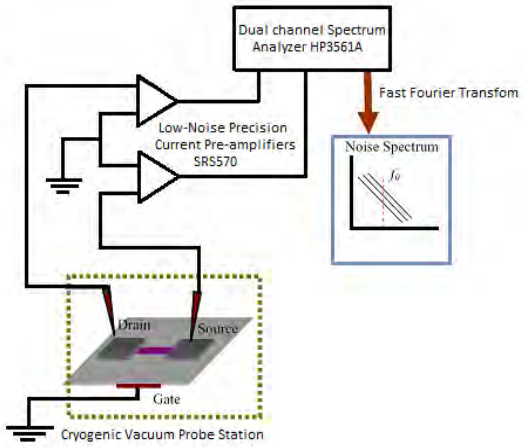


FIGURE 1. Dual channel cross spectrum noise measurement setup.

Sample	Energy (eV)	Concentration (cm^{-3})	Capture cross section value of electrons (cm^2)	Capture cross section value of holes (cm^2)
A, p-SiNWs	E_v+0.23	≈1x10^{16}	5.7x10^{-19}	5.0x10^{-19}
B, n-SiNWs	E_c-0.43	≈1x10^{12}	6.1x10^{-15}	5.3x10^{-15}

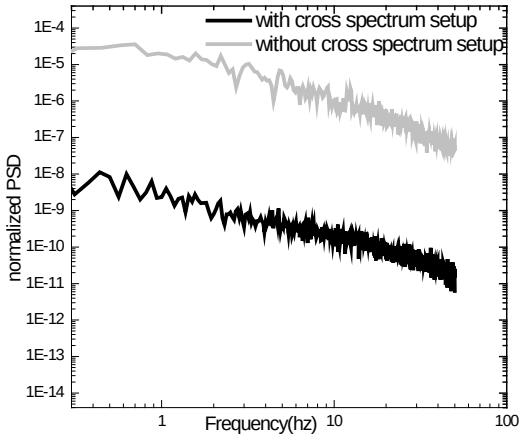


FIGURE 2. Noise measurement data of a single SiNW using two different techniques.

orders of magnitude by reducing the parasitic background 1/f noise, enabling high sensitivity measurements (Figure 2). The new method was applied to probe deep levels in Si nanowires (SiNWs) grown by the Vapor- Liquid-Solid (VLS) mechanism using Ni catalyst. Metal catalysts employed in the VLS growth are known to be sources of unintentional impurities in NWs which can deteriorate the electronic properties of NW devices. In particular, nickel impurities in p-Si form acceptor levels located about 0.23 eV above the valence band edge, while in n-Si substitutional Ni forms acceptor level around 0.35 eV below the conduction band [9]. We fabricated two sets of FETs using p-type (Sample A) and n-type (Sample B) doped SiNWs. Noise measurements were performed in 80 K to 320 K temperature range. The PSD spectra showed clear Lorentzian peaks due to the G-R processes. Temperature-dependent noise analysis indicated that the traps responsible for the G-R noise correlate well with the deep-levels introduced by Ni atoms diffused in SiNWs during the growth. Table 1 lists the parameters of deep traps calculated from our measurements which are in a good agreement with the values for Ni impurity reported in the literature [9].

CONCLUSIONS

This study identifies the LFN spectroscopy as an alternative to DLTS and optical measurements for characterization of deep-levels in semiconductor nanowire materials and demonstrated the fact that optimization of noise measurement technique can be very useful in estimating the quality of semiconductor nano-scale devices.

REFERENCES

1. D. K. Schroder, *Semiconductor Material and Device Characterization*, John Wiley & Sons, New York, 1998.
2. F. Scholtz, J. M. Hwang, and D. K. Schroder, *Solid-State Electronics*, **31**, 205-217 (1988).
3. A. Van Der Ziel, *Fluctuation Phenomena in Semiconductors*, New York Academic Press Inc., 1959.
4. P. Lauritzen and C. T. Shah, *IEEE Trans. Electron Devices*, **10**, 334-335 (1963).
5. J. A. Copland, *IEEE Tran. Electron Devices*, **18**, 50-53 (1971).
6. F. Scholtz, J. M. Hwang, and D. K. Schroder, *Solid-State Electronics*, **31**, 205-217 (1988).
7. G. Cannatà, G. Scandurra, and C. Ciofi, Rev. Sci. Instrum. **80**, 114702 (2009).
8. M. Sampietro, L. Fasoli, and G. Ferrari, *Rev. Sci. Instrum.* **70**, 2520 (1999).
9. A. G. Milnes, *Deep Impurities in Semiconductors*, Wiley, New York, 1973, pp. 12.

KEYWORDS

Noise, nanowire, defects, deep levels, traps.

DEVELOPMENT OF HIGH RESOLUTION TOPOGRAPHIC CHARACTERIZATION AT DIE SCALE BY INTERFEROMETRY

F. Dettoni[1,a], C. Beitia[2], S. Gaillard[1], O. Hinsinger[1], F. Bertin[2], M. Rivoire[1]

[1] *STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France.*
[2] *CEA, Leti, campus MINATEC, 17, rue des Martyrs, 38054 Grenoble Cedex 9, France.*

[a] *e-mail: florent.dettoni@st.com, Phone: +33 4 38 78 11 02, Fax: +33 4 38 78 30 34*

INTRODUCTION

Metrology requirements in the semiconductors industry have considerably gained in importance during the last decade [1]. Indeed, the monitoring through metrology of critical process step is required raising a need for innovative metrology tools. One major metrology issue is to image, at the die-scale, the topography with a nanometric z-resolution. In this context, a technique capable of imaging the topography of area of a few square centimeters with a nanometric sensitivity and a micrometric lateral resolution is highly desirable.

This need arises mainly from the chemical mechanical polishing (CMP) process. Indeed, due to the increasing number of process steps and the increasingly stringent specifications involved in the fabrication of new devices CMP is recognized as a critical process [2]. Furthermore CMP process performance has a direct impact on photolithography process windows that is a key parameter in the semiconductors industry.

Thanks to image stitching, interferometry can meet such requirements. Indeed interferometry is endowed with both a nanometric vertical and micrometric lateral resolution. In addition interferometry is fast. Nevertheless problems induced mainly by the die scale must be solved. These problems are: (i) transparent overlayers; (ii) die scale leveling; (iii) validation of stitching algorithm; and (iv) reliability of the measure at the die scale.

In a previous work [3] the aforementioned problems have been solved for die size less than 1 cm^2. In this paper we deal with die area of few square centimeters for which we propose new metrological solutions.

EXPERIMENTAL

In this study we have used two interferometers and a profilometer. The first interferometer is a WYKO NT9300 from Bruker. The interferometer operates in a phase-shifting mode (λ = 533 nm) using a Michelson configuration. The attainable field of view is 2.4 mm×1.8 mm, the vertical resolution is 1 nm and the lateral resolution is 3.6 µm.

The second interferometer is a Fizeau interferometer from Zygo Corporation. This interferometer operates in a phase shifting mode (λ = 632.8 nm). The circular field of view has a diameter of 150 mm, the vertical resolution is 20 nm and the lateral resolution is 100 µm. The profilometer is a high resolution profilometer HRP-340 from KLA-Tencor with a 2 µm radius stylus.

This study is done on 300 mm wafers after CMP of an advanced technology node.

RESULTS AND DISCUSSIONS

(i) First, a 30-nm opaque cap layer of tantalum is deposited on the surface. This layer is mandatory to suppress the spurious contribution of interference occurring in the thin dielectric overlayers. The impact of the Ta layer on the topography is checked, using an atomic force microscopy, at the single transistor scale and, using a mechanical profilometer, at the die scale. The results (not presented here) show that the topography of the Ta capping layer fully conforms to the topography of the underlying surface making it possible to evaluate the potential of interferometry.

(ii) In a second part we focus on the die-scale leveling issue (Figure 1.). Indeed at this scale, different contributions make up the low frequency content of the topography. The detrimental contributions must be identified and suppressed.

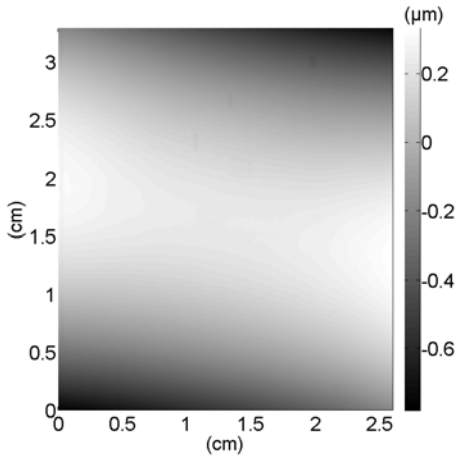


FIGURE 1. High resolution topographic characterization at the die-scale by Michelson interferometry without leveling

Wafer scale deformation is the main component of the detrimental contributions. We show that usual leveling methods like tilt, modal tilt or sphere tilt removing are not efficient to suppress this contribution. The leveling method, consisting in selecting three areas supposedly at the same level, fails as well. To solve this problem, more sophisticated corrections are investigated.

At the die-scale, other contributions to deformation are induced by the chuck design and the vacuum sample holder. These contributions are addressed, discussed and quantified. We show that chuck impact is essentially due to vacuum and requires specific attention. This contribution needs to be taken into account as well in the proposed corrections.

(iii) The next problem to be addressed is the fine tuning of the stitching algorithm parameters used to obtain the die image from a set of field of view. This has been studied by comparing the stitched image with a full die image obtained using the Fizeau interferometer. We demonstrate that, when appropriated recipe is used, image stitching is reliable up to size as large as 9 cm^2.

(iv) Finally we assess, using the mechanical profilometer, the Michelson Interferometer accuracy at both the micrometric and the die scale (Figure 2.).

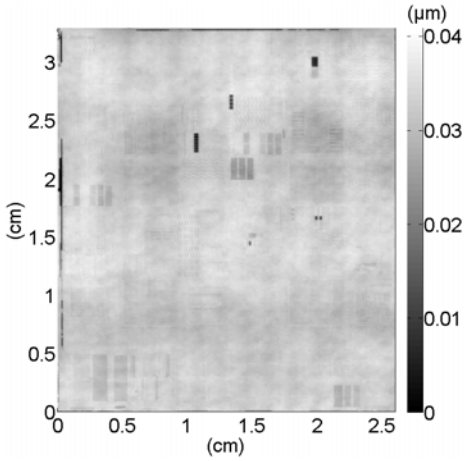


FIGURE 2. High resolution topographic characterization at the die-scale by Michelson interferometry with leveling

Both techniques possess the same lateral and vertical resolutions but, at the die-scale, mechanical profilometry is time consuming. Nevertheless it can be used as reference technique when proper methodology is used. To make a consistent comparison we apply the same leveling algorithm for both mechanical profilometry and interferometry raw data. This comparison allows us to observe very good correlations at both

micrometric and die scale between the two techniques.

An important point is to assess the influence of the leveling on the true sample topography. As shown in figure 3, the leveling method consisting in selecting two or three areas supposedly at the same level works efficiently at the micrometric scale (visually checked). We observe that at die-scale both the leveling method and the checking method are not adapted.

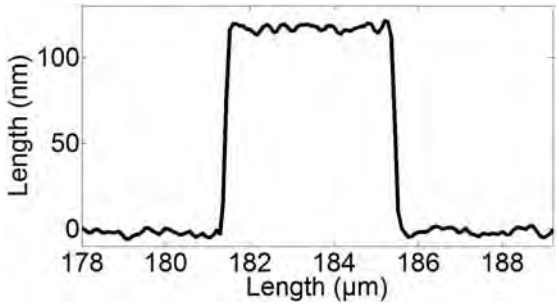


FIGURE 3. Representation of HRP scan at the micrometric scale after classic leveling

In the case of leveling by polynomial fit, a mean square can be used as goodness of fit indicator. Figure 4. shows that the presence of pattern involves numerous surface variations rendering both this leveling method and this indicator unreliable. Indeed we observe that using of polynomial of higher degree leads to enhance the goodness of fitness. This is due to the fact that the model does not discriminate between pattern-related topology and spurious contribution. Consequently the leveling by polynomial fit and its goodness of fit indicator are no more reliable.

These issues raise a demand for non-classical leveling method for topographic characterization of patterned surface at the die scale.

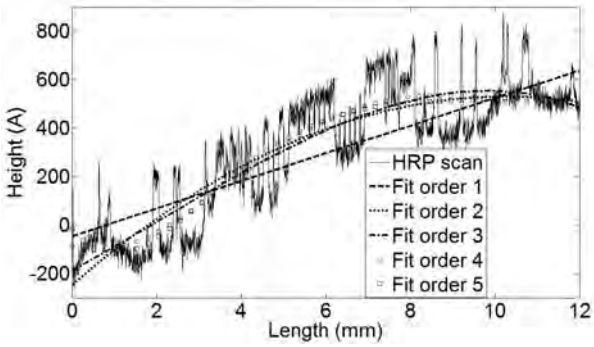


FIGURE 4. Representation of single HRP scan at the die scale and evolution of fit curve depending on the order of fit

CONCLUSION

This work demonstrates that Michelson interferometry is well suited for high resolution (vertical ≈ 1 nm, lateral ≈ microns) topography characterization at the die-scale (few square centimeters). Nowadays, the presence of transparent multilayer hampers optical-based metrology method. However we demonstrate that a Ta cladding layer resolves this problem. We also show that metrology problems induced by the die scale can be solved for area as large as 9 cm^2. We show that conventional algorithms break down to level die-scale topography images and we propose better suited methods.

REFERENCES

1. T.G. Mathia et al., Recent trends in surface metrology, *Wear* **271**, 2011, pp. 494-508.
2. K. Devriendt et al., Poly-Open and metal gate CMP steps in RMG processing on planar and 3D device architectures, *International Conference on Planarization Technology 2011 proceeding*, 2011, pp. 536-538.
3. F. Dettoni et al., Interferometry a direct die level characterization technique, *International Conference on Planarization Technology 2012 proceeding*, 2012, pp. 153-158.

KEYWORDS

Interferometry, characterization, dies, metrology, topographic, high-resolution.

WE–21

DEVELOPMENT OF THREE-DIMENSIONAL RAMAN SPECTRA ANALYSIS SYSTEM FOR TCAD STRESS SIMULATION IN FINFET STRUCTURES

Hiroshi Arimoto[1], Akira Satoh[1], Vladimir Poborchii[1], Tetsuya Tada[1], Koichi Fukuda[1], Koji Usuda[2], Kazuhisa Fujita[3], and Toshihiko Kanayama[1]

[1]*National Institute of Advanced Industrial Science and Technology (AIST)*
1-1-1 Higashi, Tsukuba, Ibaraki 305-8562, Japan
[2]*Green Nanoelectronics Center (GNC), AIST West*
16-1 Onogawa, Tsukuba, Ibaraki 305-8569, Japan
[3]*ASTOM R&D*
2-3-13 Minami, Wako-shi, Saitama 351-0104 Japan

INTRODUCTION

Stress control is a critical issue in developing advanced CMOS devices. Accurate stress simulation is indispensable for understanding the actual amount of stress in the channel region of devices. Micro-Raman spectroscopy is a useful technique for evaluating the local stress and calibrating stress simulations [1-3]. Although stress cannot be characterized quantitatively from only the Raman shifts, Raman shifts can be calculated using stress tensors obtained from a stress simulation [4]. This suggests that stress simulations can be calibrated by adjusting the stress parameters or the profiles of the device structure to be measured so that the calculated Raman shifts may agree with the measured ones. For precise calculations of Raman shifts, the propagation of excitation and scattered light should be strictly simulated. To make this possible, we combined a two-dimensional finite-difference time-domain (FDTD) electromagnetic simulation with a finite element method (FEM) stress simulation [5].

The Raman spectra analysis of FinFET structures should be treated three-dimensionally, because this sort of structure has a big effect on Raman shifts. In this paper, we describe an extended for three–dimensional simulation of such a system and a comparison of the calculated Raman spectra with measured results for a fin-like structure.

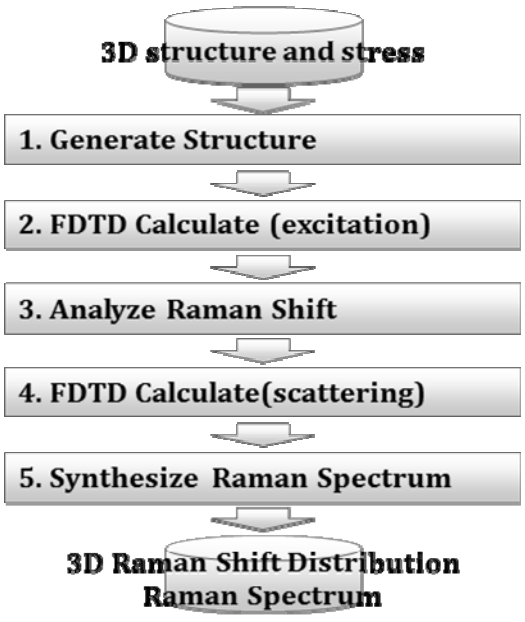


FIGURE 1. Flow diagram of Raman spectra analysis.

WE–21

Simulation Procedure

Figure 1 shows the flow diagram of the three-dimensional Raman spectra analysis system. It consists of the following sections: 1. Structure and stress reading section, 2. FDTD calculation section for incident excitation light, 3. Raman shift analysis section (calculates the wavelength of Raman scattered light from different mesh points on a sample on the basis of the stress distribution), 4. FDTD calculation section for scattered light, and 5. Raman spectra analysis section. The analysis results are visualized with a three-dimensional viewer. This system allows loading of three-dimensional TCAD simulation results of structure and stress. A three-dimensional FDTD calculation of the whole structure would take a huge amount of CPU time. To avoid this problem the system performs separate FDTD calculations for each wavelength classified on the basis of the Raman shift distribution. This reduces the CPU time because the separate FDTD calculations can be executed in parallel. To avoid interference between the scattered light from different mesh points, the calculations of the flashes are repeated with different phases until the accumulated light distributions saturate.

Simulation Results

Figure 2 shows the absorbed light intensity distribution under the excitation light in a fin-like structure which is under stress of silicon-germanium alloy (SiGe) at both ends. The polarization of the excitation is parallel to the fin. The intensity distribution of excitation light is modulated in this structure; the excitation light wraps around the sidewall and the absorbed intensity is especially strong close to the edges.

Figure 3 shows the electric field distributions of scattered lights that are classified into groups of different wavenumbers: 523.57, 523.37, and 523.17 cm^{-1}. As the strength of stress varies depending on the location, the Raman scattering light is accordingly scattered at different wavelengths. The FDTD calculations for each classified light were executed by repeating the flash with a different phase until the accumulated light distributions saturated.

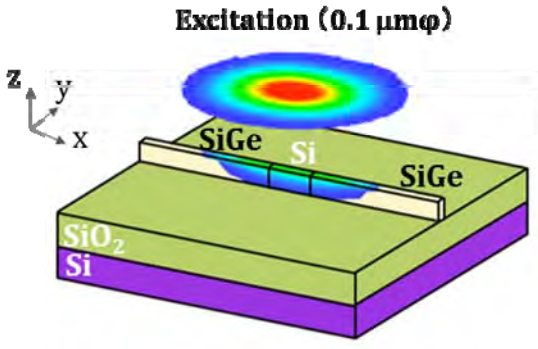


FIGURE 2. Absorbed light intensity distribution in the FinFET structure.

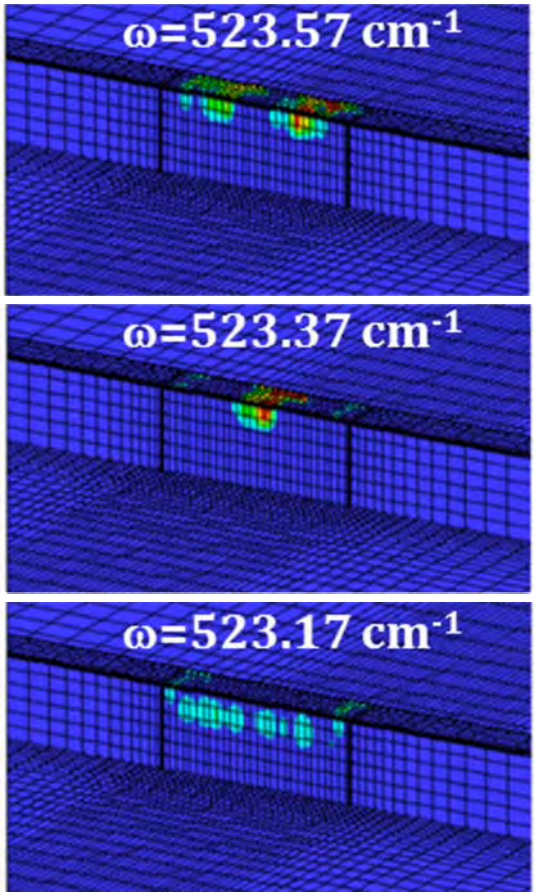


FIGURE 3. Electric field distribution of scattered light of different wavenumbers.

WE–21

Figure 4 shows the Raman spectrum synthesized from the FDTD calculations of scattered light by convoluting their Lorentzian Raman spectra. It would, then, become equivalent to the actually measured Raman spectrum. It took 20 hours (total CPU time) to obtain this spectrum. The calculation consisted of six wavenumber groups with 10 iterations and used 16 computing nodes executing in parallel. Figure 5 shows the relative change in the intensity and the Raman shift with iterations. The Raman spectrum saturates after 10 iterations.

Figure 6 compares the calculated Raman spectra with measured results [6] for a 50-nm-wide strained silicon on insulator (SSOI) structure with the scattered light polarization parallel (xx) to that of the excitation light. The calculated Raman spectra matched the measured ones.

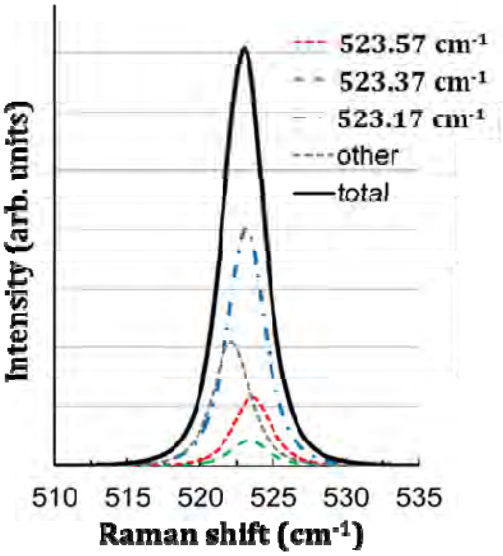


FIGURE 4. Raman spectrum synthesized from FDTD calculation of scattered light.

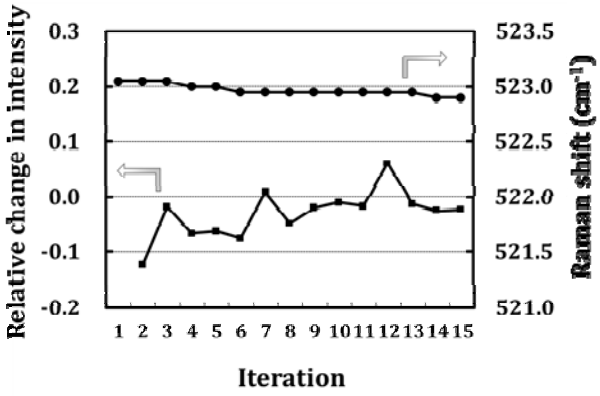


FIGURE 5. Relative change in intensity and Raman shift with iterations

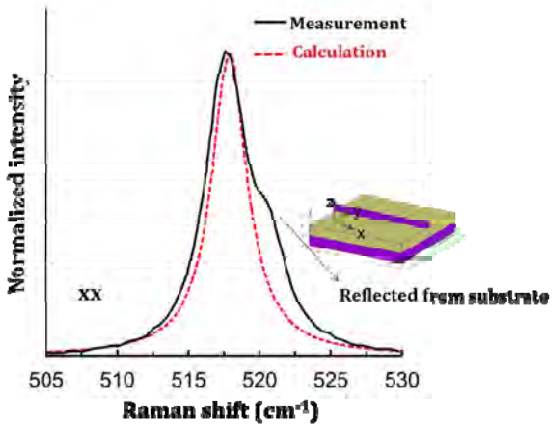


FIGURE 6. Comparison of calculated Raman spectra with measured results for a patterned SSOI structure.

CONCLUSIONS

We developed a three–dimensional Raman spectra analysis system combining an FDTD electromagnetic simulation and TCAD stress simulation. This system enables us to accurately calculate a Raman spectrum reflecting nanometer scale modulation effects in the light intensity distribution due to the device structure. The calculated Raman spectra matched the measured results for a 50-nm-wide strained silicon on insulator (SSOI) structure.

REFERENCES

1. V. Poborchii, T. Tada, and T. Kanayama, Appl. Phys. Lett., 94 (2009) 131907.
2. T. Tada, V. Poborchii, and T. Kanayama, J. Appl. Phys., 107(2010) 113539.
3. A. Satoh *et al.*, Jpn. J. Appl. Phys., 51(2012) 016603.
4. A. Yagishita, T. Saito, S. Matsuda, and Y. Ushiku, Jpn. J. Appl, Phys. **36** (1997) 1335.
5. T. Tada *et al.*, SSDM2012, Kyoto.
6. V. Poborchii *et al.*, Appl. Phys. Lett., 99 (2011) 191911.

KEYWORDS

Raman, TCAD, Stress, FDTD simulation, FinFET

WE–22

Characterization of SiO_2/Si Interface Quality by Photoluminescence

Shiu-Ko Jang Jian[1], Chih-Cherng Jeng[1], Ting-Chun Wang[1], Chih-Mu Huang[1], Ying-Lang Wang[1], and Woo Sik Yoo[2]

[1]Taiwan Semiconductor Manufacturing Company, Ltd.,
No. 1-1, Nan-Ke Rd., Science-Based Industrial Park, Tainan, 741-44, Taiwan
[2]WaferMasters, Inc., 254 East Gish Road, San Jose, CA 95112, USA

INTRODUCTION

Ultra thin, high quality gate oxide films are essential in fabricating advanced CMOS devices. [1] Low temperature, high quality oxidation techniques have been actively investigated in the industry for several decades. [2,3] The quality of the gate oxide is mainly characterized by electrical characteristics of the CMOS devices.

Subtle and unexpected gate oxide quality variations in the production line can negatively impact device yield significantly. To minimize the negative impact through process optimization and monitoring, development of an effective and practical non-contact in-line monitoring technique for gate oxide integrity and oxide/Si interface quality, is strongly desired.

In this paper, ultra thin gate oxides prepared by three different low temperature formation techniques were prepared and characterized using multiwavelength room temperature photoluminescence (RTPL) spectroscopy. The application of RTPL spectroscopy for in-line monitoring of oxide integrity was investigated.

EXPERIMENT

Ultra thin (1.5 ~ 2.0 nm thick) oxide films were grown on 300 mm Si (100) wafers using three different low temperature oxidation techniques, at RT or 350°C. Table 1 shows the oxide thickness and oxide preparation techniques.

Room temperature photoluminescence spectra of three wafers were measured in the wavelength range of 900 ~ 1400 nm under 650 and 827 nm focused laser beam excitation. The excitation laser beam spot size was in the range of 50 ~ 100 μm in diameter. The laser power at the wafer surface was 20 ~ 50 mW. The RTPL signal was integrated for 1 s per measurement point. For wafer mapping, up to 16,645 points (2 mm intervals with 3 mm edge exclusion) were measured.

TABLE 1. Description of wafers.

Wafer ID	SiO_2 (nm)	Preparation Technique
Wafer A	2.0	Remote Plasma at 350°C
Wafer B	1.5	Immersed Plasma at RT
Wafer C	2.0	Steam in Furnace at 350°C

WE–22

RESULTS AND DISCUSSIONS

RTPL spectra of the center of Wafer A under 650 and 827 nm excitation were plotted in Fig. 1 (a). Strong RTPL signals were measured under 827 nm excitation. The typical asymmetric interband RTPL spectra, with a peak wavelength at ~1400 nm, were measured. Very weak RTPL signals were measured from the same measurement site, under 650 nm excitation. The probing depth of RTPL depends on the excitation wavelength. It deepens as excitation wavelength gets longer because the absorption coefficient gets smaller as the excitation wavelength shortens, Estimated probing depths for Si, under 650 and 827 nm, are ~ 4.0 and ~10.0 μm, respectively. [4,5]

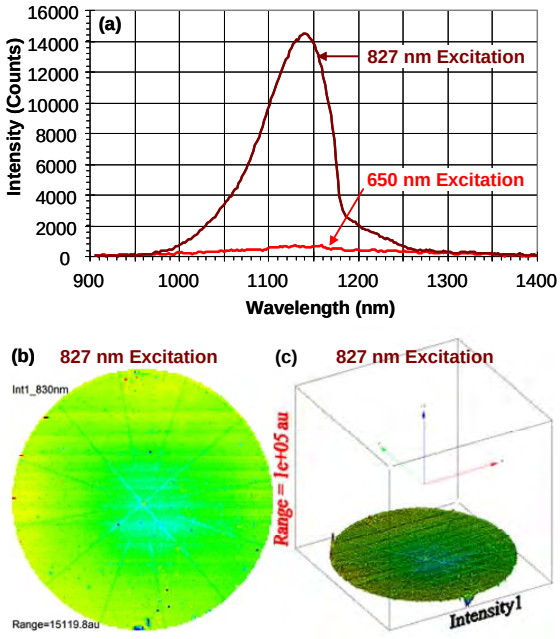


FIGURE 1. RTPL spectra of Wafer A under 650 and 827 nm excitation (a), 2D RTPL wafer map (b) and 3D RTPL wafer map under 827 nm excitation.

For Si wafers with thermal oxide grown at high temperatures (>1000°C) RTPL signals are 5~10 times stronger than for Si wafers with a native oxide layer and a oxide layer prepared at low temperatures. Poor oxide film quality and/or poor SiO_2/Si interface, significantly weakens the RTPL signal. RTPL signals under shorter excitation wavelengths, with shallower probing depths, are more sensitive because the probing volume is strongly influenced by the quality of the oxide film and SiO_2/Si interface.

Figure 1 (b) and (c) show 2D and 3D RTPL intensity wafer maps under 827 nm excitation. For RTPL wafer mapping, 15,101 points were measured for each excitation wavelength. They showed reasonably uniform RTPL intensity across the wafer. This suggests the remote plasma oxidation (Wafer A) process at room temperature resulted in relatively uniform SiO_2/Si interface quality.

The same measurements were repeated for Wafer B and Wafer C for comparison. Since the RTPL intensity significantly varies between wafers, all RTPL intensity was normalized to the RTPL intensity of Wafer A for easy comparison. Figure 2 (a) and (b) show normalized RTPL intensity of the three wafers and RTPL intensity ratio under different excitation wavelengths.

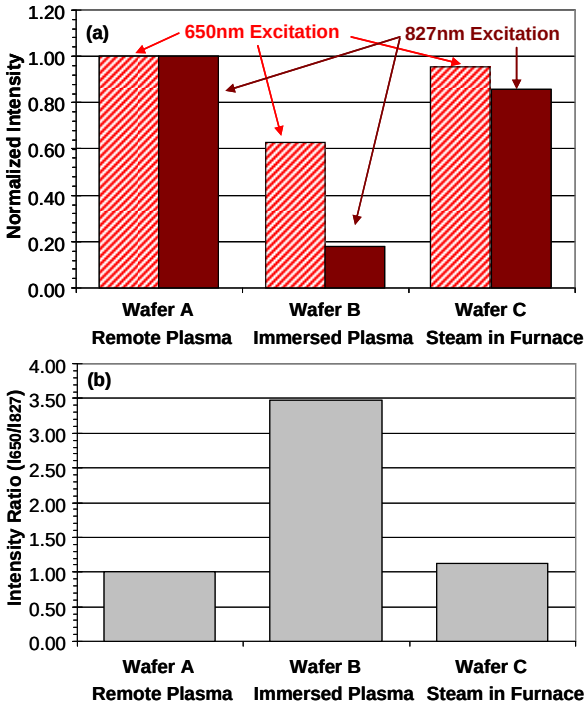


FIGURE 2. Normalized RTPL intensity of wafers A, B and C under 650 and 827 nm excitation (a) and their RTPL intensity ratio (I_{650}/I_{827}) (b).

Relative RTPL intensity (Fig. 2 (a)) among Si wafers with different low temperature oxide layers indicates the quality of the SiO_2/Si interface and potential damage of the Si wafers, within the probing depths.

As seen in Fig. 2 (a), Wafer A, with a remote plasma oxide layer, showed the highest RTPL intensity under both excitation wavelengths. Wafer B, with oxide grown in immersed plasma, showed significant RTPL intensity drops under both excitation wavelengths. It suggests that the SiO_2/Si interface and bulk Si quality are significantly compromised by plasma damage during oxide growth. Wafer C, with steam oxide in a furnace at 350°C, showed slightly weaker RTPL intensity than that from Wafer A. Slight decrease of 827 nm excited RTPL intensity can also be noticed.

The RTPL intensity ratio (I_{650}/I_{827}) (Fig. 2 (b)) can be used as a good indicator of relative crystalline damage distribution, in the depth direction. High values in the intensity ratio (I_{650}/I_{827}) can be interpreted as the presence of larger damage in the bulk Si. When the bulk damage is large, the RTPL intensity under all excitation wavelengths tends to be smaller because the RTPL signal is mainly from interband transitions of Si, regardless of excitation wavelengths.

Judging from the excitation wavelength dependence of RTPL intensity and its ratio (I_{650}/I_{827}), the low temperature oxide quality and bulk Si damage can be interpreted in the following order.

Oxide Quality: Wafer A > Wafer C > Wafer B

Si Bulk Damage: Wafer B > Wafer C > Wafer A

Electrical performance of devices using different low temperature oxide films showed good inverse correlation between the oxide quality determined by RTPL and device leakage current. Wafers with higher RTPL intensity and balanced intensity ratios (I_{650}/I_{827}) showed smaller leakage current values.

Traditionally, physical dimensions and physical properties of ultra thin oxide films have been characterized to optimize and monitor oxidation processes in semiconductor device manufacturing. However, the monitored physical dimensions and parameters of ultra-thin oxides prepared under non-equilibrium process conditions were not necessarily in good correlation with device performance. As the RTPL signal is from Si with an SiO_2 layer and interface characteristics, this technique should have practical value regarding the nature of the SiO_2/Si interface, a characteristic not easily discerned with other techniques.

SUMMARY

Multiwavelength RTPL measurements were performed on ultra thin low temperature oxide films on Si wafers. We have found that the RTPL characterization results reflect the quality of the SiO_2/Si interface and correlates with electrical properties of devices fabricated on the same structures. The RTPL technique can be very useful for in-line monitoring of low temperature oxidation processes and of the integrity of the SiO_2/Si interface.

REFERENCES

1. E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology,* New York: John Wiley & Sons, 1982, Chap. 1.
2. L. K. Wang, D. S. Wen, A. A. Bright, T. N. Nguyen and W. Chang, *IEDM '89 Technical Digest* 463 (1989).
3. D. Hiller, R. Zierold, J. Bachmann, M. Alexe, Y. Yang, J. W. Gerlach, A. Stesmans, M. Jivanescu, U. Müller, J. Vogt, H. Hilmer, P. Löper, M. Künle, F. Munnik, K. Nielsch, and M. Zacharias, M. P. Brown and K. Austin, *J. Appl. Phys.* **107**, 064314 (2010).
4. W. S. Yoo, T. Ueda, T. Ishigaki, and K. Kang, Ion Implantation Technology, *AIP Conf. Proceedings,* **1321**, 204 (2010).
5. W. S. Yoo, T. Ueda, T. Ishigaki, K. Kang, M. Fukumoto, N. Hasuike, H. Harima and M. Yoshimoto, *J. Electrochem. Soc.*, **158**(1), H80 (2011).

KEYWORDS

ultra thin oxide, SiO2/Si interface, in-line monitoring, room temperature photoluminescence (RTPL)

Thursday, March 28

Registration

8:00 AM – 8:30 AM

Beyond CMOS Metrology

Session Chair: Luigi Colombo, TI

8:30 AM
Metrology for a Post-CMOS World: an Overview 237
Tom Theis, NRI

9:00 AM
X-ray Photo Electron Spectroscopy of Nanomaterials–Graphene and III-V Interfaces 240
Robert M. Wallace, UT Dallas

9:30 PM
Issues with Characterization of Graphene Field Effect Transistors 243
Eric Vogel, GIT

10:00 AM
Coffee Break and Poster Viewing

10:30 AM
Overview on the Characterization for RRAM Technologies 246
Vincent Jousseaume, CEA Leti

11:00 AM
Microwave Electrical Measurements of Individual Magnetic Devices for Spintronics, MRAM, and NonBoolean Architectures 249
Matthew Pufall, NIST

Metrology for Patterning

Session Chair: George Thompson, Intel

11:30 AM
Overview of Next Generation Lithography - Advanced Patterning, EUV & Self Assembly. 252
Stefan Wurm, Global Foundries

12:00 PM
Metrology Tools as Basis for Photo Mask Repair and Mask Performance Improvement 255
Klaus Edinger, Carl Zeiss

12:30 PM
Lunch and Poster Viewing

Atom Probe Tomography: a Special Frontiers Session

Session Chair: Wilfried Vandervorst, IMEC

2:00 PM
Frontiers of Atom Probe Microscopy 257
Karen Henry, Intel

2:30 PM
Laser-Tip Interaction 260
Angela Vella, GPM- Université de Rouen, and Janusz Bogdanowicz, Imec-KULeuven

3:00 PM
Coffee Break and Poster Viewing

3:30 PM
Tip Shape Evolution and Reconstruction 266
David Larson, Cameca Instruments, Inc.

4:00 PM
Novel Evaporation Control Concepts and Imaging 267
Ty Prosa, Cameca Instruments, Inc., and Matthieu Gilbert, IMEC

4:30 PM
Quantifying Performance 268
Karen Henry, Intel, and Wilfried Vandervorst, IMEC

4:50 PM
Summary

5:00 PM – 6:00 PM
Poster Session (with Wine and Cheese)

Poster Presentation

TH-01, Complementary Methodologies for Thin Film Characterization in One Tool – a Novel Instrumentation for 450 mm Wafers 269
Ina Holfelder[1], Philipp Hönicke[1], Andreas Nutsch[1,2], and Burkhard Beckhoff[1]
[1]Physikalisch-Technische Bundesanstalt, Abbestr 2-12, 10587, Berlin, Germany
[2]previously Fraunhofer IISB, Schottkystrasse 10, 91058 Erlangen, Germany

TH-02, Soft X-Ray Characterization of DSA Block Copolymers 272
Daniel Sunday, Wen-Li Wu, and R. Joseph Kline
National Institute of Standards and Technology (NIST), Gaithersburg MD

TH-03, HAXPES for Non-Destructive Analysis of Chemistry at Buried Interfaces in Advanced Gate Stacks 275
Paul Risterucci[1], Eugénie Martinez[1], Rachid Boujamaa[2], Jörg Zegenhagen[3], Blanka Detlefs[3], Mickael Gros-Jean[2], Catherine Dubourdieu[4], and Olivier Renault[1]
[1]CEA, LETI, MINATEC Campus, GRENOBLE Cedex 9, France
[2]STMicroelectronics, 850 rue Jean Monnet, Crolles, France
[3]European Synchrotron Radiation Facility, Grenoble, France
[4]LMGP, CNRS, Grenoble INP, Grenoble, France

TH-04, WITHDRAWN 278

TH-05, Charge-Based Capacitance Measurements Circuits for Interface with Atomic Force Microscope Probes 279
Joseph Kopanski, M. Yaqub Afridi, Chung Jeong, Michael Lorek, Timothy Kohler, and Curt. A. Richter
Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD 20899, USA

TH-06, Vibrating Sample Magnetometry Study of High-Permeability Dielectrics on Nanomagnets . . 282
Peng Li[1], Gyorgy Csaba[1], Michael Niemier[2], X. Sharon Hu[2], Joseph J. Nahas[2], Wolfgang Porod[1], and Gary H. Bernstein[1]
[1]Center for Nano Science and Technology, Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, USA
[2]Department of Computer Science and Engineering, University of Notre Dame, Notre Dame, IN 46556, USA

TH-07, Pore Size Evaluation of Low-κ Thin Films by Using X-Ray Porosimetry 285
Yong-Qing Chang, Bo-Ching He,Hsin-Chia Ho, and Wei-En Fu
Center for Measurement Standards, Industrial Technology Research Institute 321, Sec.2, Kuangfu Rd., Hsinchu, 30011, Taiwan

TH-08, New Experiments and Applications Made Possible by a Low Temperature 4-Tip STM with UHV-SEM Navigation 288
Andreas Bettac, Berndt Guenther, Juergen Koeble, Fred Henn, and Albrecht Feltz
Omicron NanoTechnology GmbH, Limburger Str. 75, D-65232 Taunusstein, Germany

TH-09, Local Measurements of Graphene Electronics Using Gate Mapping Tunneling Spectroscopy . 291
Jungseok Chae[1,2], Yue Zhao[1,2], Suyong Jung[1,2,3], Andrea F. Young[4], Cory R. Dean[5,6], Lei Wang[6], Yuanda Gao6, Kenji Watanabe[7], Takashi Taniguchi[7], James Hone[6], Kenneth L. Shepard[5], Phillip Kim[4], Nikolai B. Zhitenev[1], and Joseph A. Stroscio[1]
[1]Center for Nanoscale Science and Technology, National Institute of Standard and Technology
[2]Maryland NanoCenter, University of Maryland
[3]Korea Research Institute of Standards and Science
[4]Department of Physics, Columbia University
[5]Department of Electrical Engineering, Columbia University
[6]Department of Mechanical Engineering, Columbia University
[7]Advanced Materials Laboratory, National Institute for Materials Science

TH-10, Graphene as Transparent Electrode for Direct Observation of Hole Photoemission from Silicon to Oxide 293
Rusen Yan,[1,2], Qin Zhang[1,2], Oleg A. Kirillov[1], Wei Li[1,3], James Basham[1], Alex Boosalis[1,4], Xuelei Liang[3], Debdeep Jena[2], Curt A. Richter[1], Alan Seabaugh[2], David J. Gundlach[1], Huili G. Xing[2], and N. V. Nguyen[1]
[1]Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, Maryland 20899, USA
[2]Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, USA
[3]Key Laboratory for the Physics and Chemistry of Nano Devices, Peking University, Beijing, China
[4]Department of Electrical Engineering and Nebraska Center for Materials and Nanoscience, University of Nebraska-Lincoln, Lincoln, Nebraska 68588, USA

TH-11, Direct Measurement of the Intrinsic Dirac Point of Graphene 297
Kun Xu[1,2], Caifu Zeng[3], Qin Zhang[1,4], Rusen Yan[1,4], Peide Ye[2], Kang Wang[3], Alan C. Seabaugh[4], Huili Grace Xing[4], John S. Suehle[1], Curt A. Richter[1], David J. Gundlach[1], and N. V. Nguyen[1]
[1]National Institute of Standards and Technology, Gaithersburg, Maryland
[2]Purdue University, West Lafayette, IN
[3]University of California, Los Angeles, Los Angeles, CA
[4]University of Notre Dame, Notre Dame, IN

TH-12, Revelation of Pattern Formation in Single Ferromagnetic CoFeB Film by Using the Giant Spin Hall Spin Torque. 300
Wanjun Jiang, Pramey Upadhyaya, Li-Te Chang, Kin L. Wong, Jing Zhao, Tianxiao Nie, Murong Lang, Robert N. Schwartz, and Kang L. Wang
Device Research Laboratory, Electrical Engineering Department, University of California, Los Angeles, California, USA, 90095

TH-13, Measure the Charge Storage Speed and Endurance of Redox-Active Molecules 303
Hao Zhu[1, 2], Christina A. Hacker[2], Curt A. Richter[2], Hui Yuan[1,2], Haitao Li[1,2], Oleg Kirillov[2], Dimitris Ioannou[1], and Qiliang Li[1,2]
[1]Dept. of Electrical and Computer Engineering, George Mason University, Fairfax, VA,
[2]Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD

TH-14, The Statistic Characteristics of Switching Parameters for Ta2O5-X Based RRAM 306
Haitao Li[1,2], Curt A. Richter[2], Oleg Kirillov[2], Hao Zhu[1,2], Hui Yuan[1,2], Qiliang Li[1,2]
[1]Dept. of Electrical and Computer Engineering, George Mason University, Fairfax, VA,
[2]Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD

TH-15, Interactions Between Two Independently Contacted and Rotationally Aligned Graphene Layers. 310
Christopher Corbet, Kayoung Lee, Babak Fallahazad, Emanuel Tutuc, and Sanjay Banerjee
The Microelectronics Research Center, The University of Texas at Austin, 10100 Burnet Road, Building 160, Austin Texas, 78758

TH-16, FinFET Sidewall Roughness Measurement and Correlation to Device Performance 313
A. F. Bello[1], Aaron Cordes[2], Abhijeet Paul[1], Shogo Mochizuki[3], Chun-Chen Yeh[4], and Huiming Bu[4]
[1]Technology Research Group, GLOBALFOUNDRIES, 257 Fuller Rd., Suite 3100, Albany, NY
[2]Sematech, 257 Fuller Rd., Suite 2100, Albany, NY
[3]Renesas, 257 Fuller Rd., Suite 3100, Albany, NY
[4]IBM Microelectronics, 257 Fuller Rd., Suite 3100, Albany, NY

TH-17, Optical Scatterometry for In-Die Sub-Nanometer Overlay Metrology 317
Henk-Jan H. Smilde[1], Martin Jak[1], Arie den Boef[1], Mark van Schijndel[1], Murat Bozkurt[1], Andreas Fuchs[1], Maurits van der Schaar[1], Steffen Meyer[1], Stephen Morgan[1], Jon Wu[1], Vincent Tsai[1], Frida Liang[1], Cathy Wang[1], Kaustuve Bhattacharyya[1], Guo-Tsai Huang[2], Chih-Ming Ke[2], and Kai-Hsiung Chen[2]
[1]ASML Netherlands B.V., De Run 6501, 5504 DR Veldhoven, The Netherlands
[2]TSMC Ltd, 8, Li-Hsin Rd. 6. Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.

TH-18, CD-SAXS for 3D Dimensional Metrology on 32 nm Pitch Line Patterns 320
Daniel F. Sunday1, Wen-li Wu[1], Scott List[2], and R. Joseph Kline[1]
[1]Materials Science and Engineering Division, National Institute of Standards and Technology, Gaithersburg, MD 20899
[2]Intel Corporation, Hillsboro, OR 97124

TH-19, On Sub-10 nm 3D CD-SEM Metrology 322
András E. Vladár, John S. Villarrubia, Bin Ming, and Michael T. Postek
National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899-8212, USA

TH-20, CD Metrology Gaps Analysis from the 22 nm Node Onwards 324
Benjamin Bunday
SEMATECH, 257 Fuller Rd, Albany NY, 12203 USA

TH-21, Fabrication and Characterization of Standards for Atomic Force Microscope Tip Width Calibration 327
Ronald Dixson[1], Craig McGray[1], Boon Ping Ng[2], Ndubuisi G. Orji[1], and Jon Geist[1]
[1]NIST Semiconductor and Dimensional Metrology Division, 100 Bureau Drive, Gaithersburg, MD 20899
[2]Singapore Institute of Manufacturing Technology, 71 Nanyang Drive, Singapore 638075

TH-22, Shallow Probe: Non-Destructive Compositional Metrology for Films and Structures 331
Mona P. Moret, Anna Meura, Anne-Sophie Robbes, and Michel Schuhmacher
CAMECA, 29 quai des Grésillons, 92 622 Gennevilliers, France

TH-23, Device-Level Electrical Characterization Using Ferromagnetic Resonance of Magnetic Multilayers 333
Eric R. Evarts, Matthew R. Pufall, and William H. Rippard
Magnetics Group, Electromagnetics Division, NIST, 325 Broadway, Boulder, CO 80305

9–1

METROLOGY FOR A POST-CMOS WORLD: AN OVERVIEW

Thomas N. Theis

IBM Research, T.J. Watson Research Center, PO Box 218, Yorktown Heights, NY 10598 USA

INTRODUCTION

Precision in metrology leads precision in manufacturing. This must be so, because controlling any manufacturing process for reproducibility and yield requires feedback loops involving measurement. To quote Lord Kelvin, "If you can not measure it, you can not improve it." [1] One cannot build what one cannot "see". But manufacturers do not just adopt and exploit advances in metrology. They promote and sometimes even demand the advances. One industry in particular has driven these advances more than any other in the last half century – the worldwide semiconductor electronics industry.

This industry has, of course, accustomed us to the idea of exponentially compounding improvements in the minimum lithographic dimension – the smallest patterned feature size that can be routinely reproduced in manufacturing. Less widely appreciated is the fact that semiconductor electronics has driven vast improvements in control of purity, composition, and structure of materials, and in the control of all the additive and subtractive processes used to structure materials into devices and integrated circuits. This progress has been largely motivated by the economic imperative to continuously shrink the devices of information technology, particularly the Complementary Metal Oxide Semiconductor (CMOS) field-effect transistor. However, CMOS technology is clearly approaching some important physical limits. Since roughly 2003, the inability to reduce power supply voltages along with device dimensions, combined with economic constraints on areal power density and total power, has forced designers to limit clock frequencies even as devices have continued to shrink. This plateauing of a critical performance metric for computing reduces the economic incentive to further shrink the CMOS field-effect transistor. Even the most optimistic engineers see rapidly approach limits to further miniaturization.

New channel materials, new device structures, and novel circuits cannot fundamentally alter this situation. *The device physics must change in a fundamental way* if we are to realize faster, denser digital logic with very low power dissipation. The continued vitality of the information technology revolution, and the continued push of manufacturing precision toward nanometer dimensions, will depend on it. Without such a fundamental advance, the industrial impetus for further advances in metrology will also be greatly reduced. Fortunately, there is no shortage of new digital switch concepts based on physical principles which avoid the fundamental voltage-scaling limit of the field-effect transistor.

THE NANOELECTRONICS RESEARCH INITIATIVE

The Nanoelectronics Research Initiative (NRI) is a consortium of leading semiconductor companies established in 2005 to guide and fund fundamental research at U.S. universities with the goal of finding the "next switch" to replace the CMOS transistor for

9–1

storing and manipulating digital information. The National Institute of Standards and Technology (NIST) and the National Science Foundation (NSF) have partnered with NRI to fund this research. Four geographically distributed university research centers, funded by industry and by an award from NIST, form the core of the program. Each center explores a few selected device concepts and contributes to research comparing the capabilities of these devices. Although no single device has yet emerged as a clear winner with the potential to eclipse the field-effect transistor, results are sufficiently promising that NIST and the industrial sponsors have recently renewed their commitment to NRI. Based on the learning to date, a vision for the next five years of research has emerged.

Device Benchmarking

The research vision has been influenced by the results of increasingly sophisticated device performance benchmarking studies carried out by the university research centers. The latest comparative analysis, involving the key university investigators for each device concept and led by I. Young and D. Nikinov of Intel, has just been published [2]. Applying a uniform methodology and set of engineering assumptions across all considered device concepts, the authors draw some important conclusions. First, they find that tunneling field-effect transistors (TFETs) stand out in both energy and delay. Second, they find that of the various spintronic devices studied, those based on spin transfer torque (STT) switching of magnetic orientation are both slow and dissipate more energy in switching, while devices based on voltage-controlled switching of magnetic orientation (magnetoelectric devices) are similarly slow but dissipate less energy in switching.

NRI-supported research, as well as research under the Semiconductor Research Corporation's new STARnet centers, will reflect these developments. The TFET is promising as a fast, low-power device because it switches by a novel mechanism that avoids the voltage-scaling limit of the conventional field effect transistor. Other new device concepts, promising similar advantages of fast switching with low supply voltage, have emerged from the NRI centers in the last year or so and will be further explored and developed. The spintronic devices all switch by magnetic precession. Switching speed is therefore expected to be limited by the low magnetic precession frequencies in ferromagnetic materials. More important, this switching mechanism is not energy efficient when driven by spin transfer torque (STT) from a spin-polarized current. The benchmarked magnetoelectric devices promise much better energy efficiency. Newly-proposed and demonstrated mechanisms for switching of magnetization, such as voltage control of magnetic anisotrophy [3] and the giant spin Hall effect [4] are of great interest and will be further explored and developed.

Metrology For A Post-CMOS World

Before any of these potential post-CMOS devices can be considered for manufacturing, countless exploratory devices must be built, tested, modeled, and understood. Properties of novel materials must be measured and improved. Novel device structures must be fabricated and characterized. Recalling Lord Kelvin's admonition about the need be able to measure what one wishes to improve, this research invites and sometimes demands advances in metrology. Metrology has thus been and will continue to be a key component of the NRI research program. Each of the university research centers supports a strong characterization and nano-metrology component with a focus on measuring those material properties and device characteristics most relevant to understanding the potential of each exploratory device.

For example, a new low-voltage device concept proposed and explored by the NRI INDEX (Institute for Nanoelectronics Discovery and Exploration) center is based on the unique charge transport properties of p-n junctions in graphene monolayers and bilayers. Thus, among many techniques explored by INDEX researchers for characterization of graphene, the development of improved Kelvin Probe Force Microscopy to image the potential variation across nanoscale graphene p-n junctions is very important. The measurements test and constrain models for the junction potential profile,

9–1

and these models are crucial to device design. INDEX researchers are also exploring and demonstrating spin-logic devices with magnetic elements switched by spin diffusion. They are therefore improving techniques for sensing spin diffusion and transport in graphene and other 2D materials

The NRI SWAN (Southwest Academy for Nanoelectronics) center is attempting to demonstrate another graphene-based device, the Bi-layer Pseudospin FET or BiSFET. If the theoretically predicted materials physics can be confirmed, switching in this device will involve the formation of a novel condensed electronic state in certain bi-layer graphene structures. Fabrication of the requisite structures pushes the limits of nanofabrication technology. SWAN researchers have therefore devoted much creativity and effort to characterizing the nanostructure of graphene as a function of growth conditions.

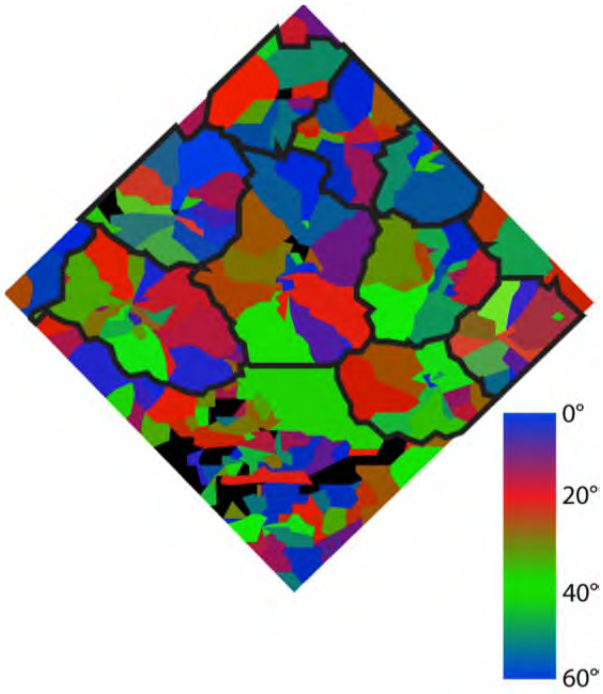


FIGURE 1. Grain orientation map of a graphene film obtained by electron diffraction. Figure used with permission of Prof. Moon Kim, UT Dallas.

For example, electron diffraction patterns obtained with a transmission electron microscope were used to accurately determine grain orientation in graphene. Repeating the measurement, point by point, allowed construction of grain-orientation maps that yield much valuable information about the growth process. **Figure 1** shows such a map, color coded for grain orientation. The grain orientations and shapes provide information regarding nucleation points and formation of grain boundaries during film growth.

This and other characterization techniques developed by SWAN researchers are having a dramatic impact on the understanding and control of graphene synthesis, enabling the exploration of many new device concepts, including, but not limited to the BiSFET.

Conclusion

The NRI centers bring together researchers who can push the frontiers of materials systhesis and exploratory device fabrication, characterization, and modeling. The above-mentioned examples illustrate some ways in which this research is enabled by advances in metrology. If NRI is ultimately successful in its goal of finding the "next switch" to replace the CMOS transistor, the demands of the electronics industry on metrology will would be amplified along with the economic imperative to manufacture the new devices with shrinking dimensions and greater precision.

References

1. http://zapatopi.net/kelvin/quotes/
2. D. E. Nikonov and I. A. Young, Proc. IEDM, December 2012.
3. T. Maruyama, *et al.*, Nature Nano **4**, 158 (2009).
4. L. Liu, *et al.*, Science **336**, 555 (2012).

Keywords

Manufacturing, metrology, nanoelectronics, precision, post-CMOS

9–2

X-RAY PHOTOELECTRON SPECTROSCOPY OF NANOMATERIALS– GRAPHENE AND III-V INTERFACES

Robert M. Wallace

Department of Materials Science and Engineering
University of Texas at Dallas

INTRODUCTION

Interest in high-mobility materials has been renewed as a result of the anticipated performance requirements for CMOS technology, including power, speed and reliability. [1] Among the materials under consideration, graphene and III-V compound semiconductors are under particular scrutiny. In addition to scaled MOSFETs, alternative devices are under exploration,[2] including single particle tunneling (e.g. TFET) [3] and exciton condensates (e,g, BiSFET). [4] A key component in any of these nanoscale devices is the dominance of their surfaces and interfaces with device components such as dielectrics and contacts. X-ray Photoelectron Spectroscopy (XPS) is well established to study the interfacial chemistry of these materials and provides insight on potential defect formation that would impact device performance.

In this paper, we summarize our recent efforts examining the surfaces and interfaces of graphene and III-V compound semiconductors in contact with dielectrics. We present *in-situ* and *ex-situ* studies of surfaces and interfaces, demonstrating the importance of interfacial control in the understanding of film growth mechanisms. We then stress utilization of in-situ deposition and characterization methods with a goal of correlation to device behavior.

EXPERIMENTAL METHODS

Figure 1 shows the UHV system employed to conduct in-situ deposition and analysis on high mobility materials. The system incorporates a number of thin film deposition capabilities, processing (plasma treatments, anneals, atomic-H exposure), and analysis methods. [5] It is seen that the combination of multiple deposition techniques in conjunction with surface/interface analysis provides a powerful opportunity to fundamentally understand technologically relevant device interfaces. In particular the ability to prepare a surface, and alter it in a controlled manner which is still reminiscent of a device fabrication process, is particularly important.

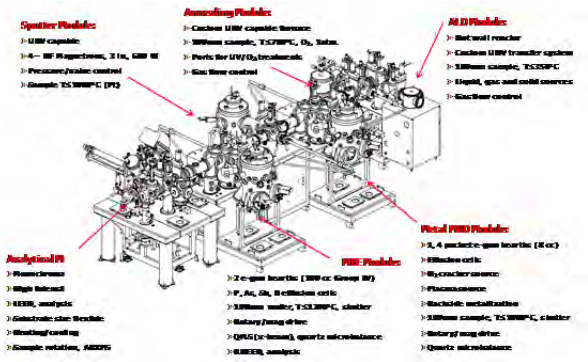


FIGURE 1. Ultrahigh vacuum cluster system for in-situ investigations of high-mobility materials.

9–2

RESULTS

In-situ vs. Ex-situ Analysis

The study of atomic layer deposition (ALD) on III-V surfaces has revealed potentially important reaction pathways to control deleterious surface oxidation on compound semiconductors, such as GaAs and InGaAs.[6] In-situ studies have shown that the ALD precursor can readily reduce surface oxides during the thermal ALD process, referred to as a "self-cleaning" process. [7] In contrast, ex-situ analyses of similar high-k stacks have suggested that the self-cleaning process does *not* occur. [8] Such apparent contradictions have been shown to originate from the exposure of the high-k/III-As sample to the atmosphere, as seen in Fig. 2.

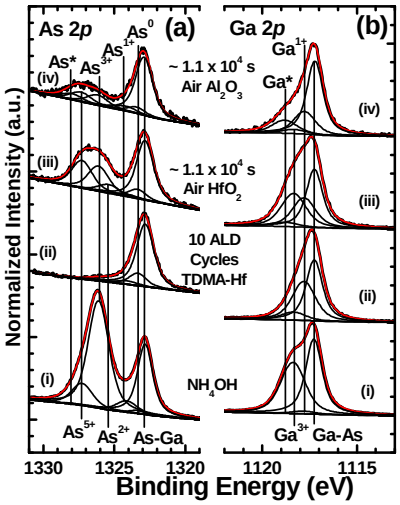


FIGURE 2. Photoelectron spectra after (i) NH_4OH treated, (ii) 10 ALD cycles of TDMA-Hf/H_2O, (iii) 1.1×10^4 s air exposure, (iv) 10 cycles Al_2O_3 after 1.1×10^4 s air exposure for the As 2*p* and Ga 2*p* core-level features. Interfacial oxide re-growth is greater for the HfO_2/GaAs system in comparison to the Al_2O_3/GaAs system under these growth conditions. Reprinted with permission from [8]. Copyright (2012), American Institute of Physics

The GaAs surface exposed to an NH_4OH treatment clearly shows surface oxidation from the wet chemical exposure. Exposure of this interface to a TDMA-Hf ALD process results in the clear reduction of As- and Ga-oxides (and the growth of Hf-oxides). Subsequent exposure of this surface to the atmosphere results in reoxidation – a result that could be misconstrued as evidence for a lack of interfacial oxide "self cleaning." It is also seen in Fig. 2 (spectra (iv)) that an Al_2O_3 film deposited by ALD provides a better barrier to surface reoxidation than HfO_2.

HIGH-K ON GRAPHENE

Growth of high-k films on graphene presents specific challenges due to the relatively inert behavior of the graphene surface basal planes. Several methods have recently been explored to functionalize the graphene surface sufficiently to enable deposition of high-k dielectrics by ALD methods. [9] Among these, ozone exposure has been demonstrated to produce conformal Al_2O_3 films on graphene, while not resulting in detectable damage based on Raman and device measurements. [10,11] In addition to effects of surface contamination serving as nucleation sites, [12,13] weakly bound species during the ALD process appear to impact the efficiency of film nucleation and growth.

This may be seen in Figure 3, where in-situ studies of ALD Al_2O_3 growth on graphite are examined under full cycle and half-cycle conditions which should nominally result in identical growth. The difference between the growth cycles entails a N_2 purge sequence between precursors for a normal full-cycle process, while this purge is interrupted during half-cycle studies for XPS interrogation.

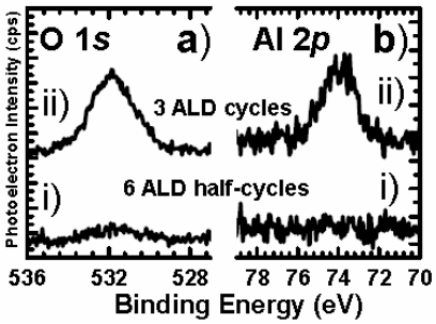


FIGURE 3. Photoelectron spectra of (a) O1*s* and (b) Al 2*p* regions for (i) half-cycle vs. (ii) full-cycle ALD of Al_2O_3. Reprinted with permission from [9]. Copyright (2012), American Institute of Physics.

9–2

The longer interruption to interrogate the surface by XPS clearly results in less Al_2O_3 growth, and suggests that weakly bound species are present during the ALD process which are transient, but necessary for conformal film growth. We will also show purge time studies which support this interpretation.

SUMMARY

In-situ studies provide a powerful characterization tool to enable a more fundamental understanding of interfaces relevant for device technologies. We will present several other examples on compound semiconductors and graphene demonstrating the power of such analysis.

ACKNOWLEDGMENTS

The author gratefully acknowledges the research assistants and colleagues who contributed to the work, including Prof. D. Akinwande, Ms. A. Azcatl, Prof. S. Banerjee, Dr. B. Brennan, Dr. L. Colombo, Mr. H. Dong, Prof. S. Datta, Prof. C. Hinkle, Mr. D. Hinojos, Dr. S. McDonnell, Dr. A. Pirkle, Prof. R. Ruoff, Prof. A. Seabaugh, Prof. E. Tutuc, Prof. E. Vogel, Mr. X. Qin, and Mr. D. Zhernokletov. The work is supported by NIST and the NRI MIND and SWAN Centers, the FCRP MSD Center, the AFOSR (AOARD grant No. FA2386-11-1-4077), and the NSF under award No. ECCS 0925844.

REFERENCES

1. For example, see the *International Technology Roadmap for Semiconductors*, (2011).
2. K. Bernstein, R. K. Cavin, III, W. Porod, A. Seabaugh, and J. Welser, "Device and Architecture Outlook for Beyond CMOS Switches," *Proceedings of the IEEE*, **98(12)** 2169-2184 (2010).
3. A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE*, **98(12)** 2095-2110 (2010).
4. L. F. Register, X. Mou, D. Reddy, W. Jung, I. Sodemann, D. Pesin, A. Hassibi, A. H. MacDonald, and S. K. Banerjee, "Bilayer Pseudo-Spin Field Effect Transistor (BiSFET): Concepts and Critical Issues for Realization," *ECS Transactions*, **45(**4), 3–14 (2012)
5. R.M.Wallace, "In-Situ Studies of Interfacial Bonding of High-κ Dielectrics for CMOS Beyond 22nm," *Electrochemical Society Transactions* **16(5)**, 255-271 (2008).
6. C.L.Hinkle, E.M.Vogel, P.D.Ye and R.M.Wallace, "Interfacial Chemistry of Oxides on $In_xGa_{(1-x)}As$ and implications for MOSFET applications," *Current Opinion in Solid State and Materials Science*, **15**, 188-207 (2011); and references therein.
7. C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, "GaAs interfacial self-cleaning by atomic layer deposition," *Applied Physics Letters* **92**, 071901 (2008).
8. S. McDonnell, H. Dong, J. M. Hawkins, B. Brennan, M. Milojevic, F. S. Aguirre-Tostado, D. M. Zhernokletov, C. L. Hinkle, J. Kim, and R. M. Wallace, "Interfacial oxide re-growth in thin film metal oxide III-V semiconductor systems," *Applied Physics Letters*, **100**, 141606 (2012); and refs. therein.
9. S. McDonnell, A. Pirkle, J. Kim, L. Colombo and R. M. Wallace, "Trimethyl-Aluminum and Ozone Interactions with Graphite in Atomic Layer Deposition," *Journal of Applied Physics*, **112** 104110 (2012); and refs. therein.
10. B. Lee, G. Mordi, M. J. Kim, Y. J. Chabal, E. M. Vogel, R. M. Wallace, K. J. Cho, L. Colombo and J. Kim, "Characteristics of High-k Al2O3 Dielectric Using Ozone-Based Atomic Layer Deposition for Dual-Gated Graphene Devices," *Applied Physics Letters* **97**, 043107 (2010).
11. S. Jandhyala, G. Mordi, B. Lee, G. Lee, C. Floresca, P-R. Cha, J.H. Ahn, R. Wallace, Y. Chabal, M. Kim, L. Colombo, K. Cho, J. Kim, "Atomic Layer Deposition of Dielectrics on Graphene Using Reversibly Physisorbed Ozone," *ACS Nano*, **6**, 2722 (2012).
12. A. Pirkle, J. Chan, A. Venugopal, D. Hinojos, C. W. Magnuson, S. McDonnell, L. Colombo, E. M. Vogel, R. S. Ruoff and R. M. Wallace, "The effect of chemical residues on the physical and electrical properties of chemical vapor deposited graphene transferred to SiO2," *Applied Physics Letters*, **99**, 122108 (2011)
13. J. Chan, A. Venugopal, A. Pirkle, S. McDonnell, D. Hinojos, C. Magnuson, R. Ruoff, L. Colombo, R. Wallace, E. Vogel, "Reducing Extrinsic Performance Limiting Factors in Graphene Grown by Chemical Vapor Deposition," *ACS Nano* **6**, 3224 (2012)

KEYWORDS

High mobility, High-k, in-situ, III-V, Graphene

9–3

ISSUES WITH ELECTRICAL CHARACTERIZATION OF GRAPHENE FIELD EFFECT TRANSISTORS

Eric M. Vogel[1,2], Archana Venugopal[2,3], and Luigi Colombo[3]

[1]*School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, GA 30332*
[2]*The University of Texas at Dallas, Richardson, TX 75080*
[3]*Texas Instruments, Incorporated, Dallas, TX 75243*

INTRODUCTION

The primary test vehicle used to evaluate materials (e.g. graphene, metal contacts, gate dielectrics) associated with graphene device fabrication is a relatively simple test structure consisting of graphene transferred to an insulating substrate with the bulk Si substrate as the back gate and deposited metal source-drain contacts. For this device, the extracted effective mobility is used to gauge the impact of the gate dielectrics or graphene type, and the extracted contact resistance is used to gauge the effect of metal processes. While the use of the Field Effect Transistor (FET) test structure is common, there have been few investigations to systematically determine whether assumptions associated with characterizing the transport properties of graphene using this test structure are valid. This paper will review our recent work[1-3] on the transport properties of graphene transistors.

EXPERIMENTAL

Single-layer graphene flakes from natural graphite were transferred onto thermal oxide with different thicknesses (15, 90, and 300 nm) grown on p-type Si wafers (doping ~ 10^{17}/cm^3) using a dry oxidation process. A standard two step electron beam lithography process was then used to etch the graphene flakes to desired dimensions and to define test structures. Contacts to the graphene transistors were made using nickel deposited at room temperature by electron beam evaporation followed by a liftoff process.

RESULTS AND DISCUSSION

MODEL FOR TOTAL RESISTANCE

We have use a simple model described elsewhere for the total resistance (R) of a typical FET.[2-4] There are four primary parameters that are extracted by fitting the experimental R vs. back gate voltage (V_{bg}) with the model: the Dirac or minimum conductivity voltage (V_{Dirac}), the contact resistance (R_c), the intrinsic carrier concentration (n_0), and mobility (μ). Figure 1 shows experimental and modeled R vs. V_{bg}, as well as each of the primary parameters extracted for this case. The model is observed to fit the experimental data well over the entire range of V_{bg}. We have previously shown that the mobility extracted using the Hall technique and the Drude model are equivalent to the mobility extracted using this model at moderate to high field for measurement temperatures ranging from 4 to 300 K.[3] The constant mobility model was adopted for the remainder of the results presented in this paper.

9–3

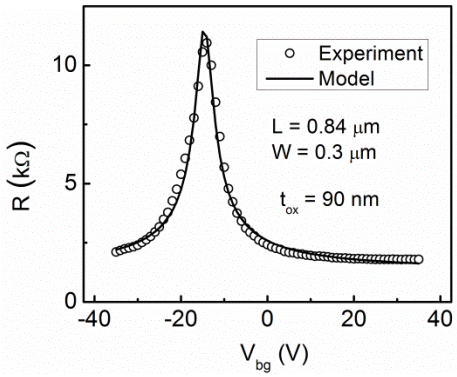


FIGURE 1. Comparison of the measured total resistance and modeled total resistance as a function of V_{bg}. The following parameters were extracted: μ = 3291 cm^2/Vs, n_0 = 4.6x10^{11} cm^{-2}, R_c = 1221 Ω, and V_{Dirac} = -14.6 V. Reprinted from Solid State Communications, **152**/15, A. Venugopal, L. Colombo, E. M. Vogel, Issues with Characterizing Transport Properties of Graphene Field Effect Transistors, 1311-1316, Copyright (2012), with permission from Elsevier.

EXTRACTED MOBILITY

Figure 2 shows the extracted μ as a function of L for several W.[3] The mobility is observed to increase and saturate with increasing channel length as previously reported.[5, 6] For L less than several micrometers, the channel resistance is independent of the channel length. One possible reason is that the electrons or holes in graphene travel across the channel without scattering (quasi-ballistic) so that R_{ch} is no longer linearly proportional to L.[5, 6] Another possible reason is that the metal contacts may perturb the channel region near the contacts.[7]

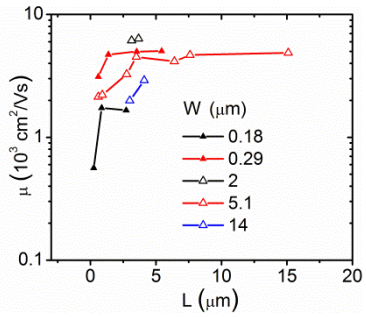


FIGURE 2. Extracted mobility as a function of channel length for different channel widths. Reprinted with permission from A. Venugopal *et al.*, Journal of Applied Physics 109, 104511, (2011). Copyright 2011, American Institute of Physics.

Figure 3 shows the extracted μ as a function of W for several different channel length and for three different thickness of SiO_2 (t_{ox}).[3] We hypothesize that the extracted μ has a relationship with W caused by two different phenomena. For very small W, less than several hundred nanometers, the extracted μ decreases with decreasing W. This has previously been attributed to scattering by the edge of the graphene channel.[8] For channel lengths of several micrometers, the μ decreases with increasing W and eventually saturates at large W. Recently, several researchers have demonstrated a large increase in carrier concentration at the edges of a graphene strip.[9-11] This charge accumulation results in a conductivity and extracted mobility that depends on the channel width. We also observe that the extracted μ for W of several micrometers decreases with decreasing t_{ox} which is expected for this electrostatic phenomenon. For t_{ox} of 15 nm, the extracted μ at several micrometers width is approximately the same as that of W ~10 μm.

These results strongly suggest that small bottom t_{ox} and large L and W should be used when comparing mobility of graphene devices.

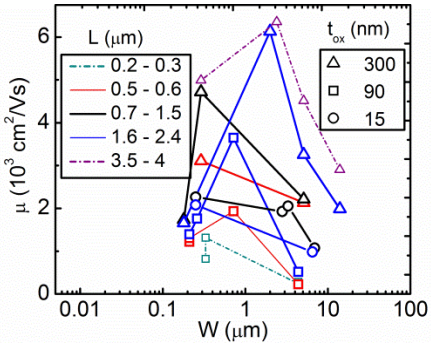


FIGURE 3. Extracted mobility as a function of channel width for different channel lengths and oxide thicknesses. Reprinted with permission from A. Venugopal *et al.*, Journal of Applied Physics 109, 104511, (2011). Copyright 2011, American Institute of Physics.

EXTRACTED CONTACT RESISTANCE

As described in the model section, the second parameter which strongly impacts R is R_c. We have used the transfer length method to determine R_c.[2] It is commonly assumed that R_c is linearly proportional to the width of the contact.[12] However,

9–3

the dependence of R_c on the width of the contact has not been reported for graphene.

Typically, the width of the contact is determined by the width of the defined graphene, W, as the metal contacts completely cross the graphene. Figure 4 shows that the extracted R_c is approximately independent of W for the range of W shown. If the current is being injected uniformly over the width of the contact, then there should be greater than a factor of 10 ratio in R_c over the range of W shown. These results are consistent with enhanced carrier injection at the edge of the graphene. One possible explanation for this result is that the previously described electrostatic accumulation of carriers along the edge of graphene is dominating carrier injection. Another possibility is that the defective nature of the edge of graphene enhanced carrier injection..

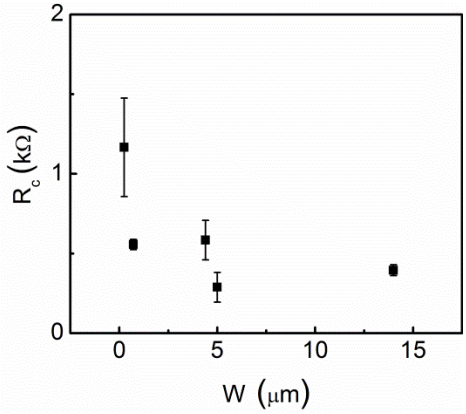


FIGURE 4. TLM extracted contact resistance as a function of contact width for Ni contacts on monolayer graphene. Reprinted from Solid State Communications, **152**/15, A. Venugopal, L. Colombo, E. M. Vogel, Issues with Characterizing Transport Properties of Graphene Field Effect Transistors, 1311-1316, Copyright (2012), with permission from Elsevier.

CONCLUSIONS

The primary parameters which affect the total resistance of a graphene field effect transistor are the mobility and contact resistance. While mobility is typically assumed to be independent of device length and width, we find that this is not the case. Our results indicate that large devices should be used to appropriately determine channel mobility. The extracted contact resistance is found to be weakly dependent on the width also suggesting that carriers are primarily injected from the contact edges.

ACKNOWLEDGMENTS

This work is supported by funding from the SRC NRI SWAN center, a Texas Instruments diversity CMOS fellowship, and NSF MRSEC: The Georgia Tech Laboratory for New Electronic Materials (Award #0820382).

REFERENCES

1. Portions reprinted from Solid State Communications **152** (15), A. Venugopal, L. Colombo and E. M. Vogel, Issues with characterizing transport properties of graphene field effect transistors, 1311-1316, Copyright (2012), with permission from Elsevier.
2. A. Venugopal, L. Colombo and E. M. Vogel, Applied Physics Letters **96** (1), 013512 (2010).
3. A. Venugopal, J. Chan, X. Li, C. W. Magnuson, W. P. Kirk, L. Colombo, R. S. Ruoff and E. M. Vogel, Journal of Applied Physics **109** (10), 104511 (2011).
4. S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc and S. K. Banerjee, Applied Physics Letters **94** (6), 062107 (2009).
5. Y. W. Tan, Y. Zhang, K. Bolotin, Y. Zhao, S. Adam, E. H. Hwang, S. Das Sarma, H. L. Stormer and P. Kim, Physical Review Letters **99** (24), 246803 (2007).
6. C. Zhihong and J. Appenzeller, IEDM Tech. Digest, 509 - 512 (2008).
7. T. Mueller, F. Xia, M. Freitag, J. Tsang and P. Avouris, Physical Review B **79** (24), 245430 (2009).
8. Y. Yinxiao and R. Murali, IEEE Electron Device Letters **31** (3), 237-239 (2010).
9. F. T. Vasko and I. V. Zozoulenko, Applied Physics Letters **97** (9), 092115 (2010).
10. P. G. Silvestrov and K. B. Efetov, Physical Review B **77** (15), 155436 (2008).
11. A. A. Shylau, J. W. Klstrokos and I. V. Zozoulenko, Physical Review B **80** (20), 205402 (2009).
12. K. Nagashio, T. Nishimura, K. Kita and A. Toriumi, Applied Physics Letters **97** (14), 143514 (2010).

KEYWORDS

Graphene, transistors, electrical, characterization

9–4

OVERVIEW ON THE CHARACTERIZATION FOR RRAM TECHNOLOGIES

V. Jousseaume, P. Noé, E. Souchier, P. Calka, E. Martinez, H. Grampeix, G. Rodriguez, M. Bernard, E. Henaff, M. Tessaire, A. Salaun, A. Roule, P. Gergaud, F. Fillot, F. Pierre, D. Mariolle, N. Chevalier, M. Veillerot, J.P. Barnes, G. Ghezzi, V. Delaye, D. Lafond, G. Audoit, F. Aussenac, N. Rochat, C. Licitra, J.F. Nodin, C. Carabasse, E. Jalaguier, E. Vianello, G. Molas, V. Sousa, L. Perniola, C. Guedj, F. Bertin, A. Chabli, S. Maitrejean and B. De Salvo

CEA, LETI, Minatec campus, 17 rue des Martyrs, 38054 Grenoble, France

INTRODUCTION

Emerging non-volatile memory technologies based on resistance change such as Phase Change RAM (PCRAM), Conductive Bridge RAM (CBRAM) or Oxide Resistive RAM (OxRRAM) are considered as promising alternatives in order to replace flash memory in a near future. The performance optimization of these devices is related to material and stack optimization. This requires a precise characterization at a nanometer scale of the materials (stoichiometry control, doping, crystallography …) and of the interfaces. Another challenge is to elucidate the switching mechanisms of these new memories by using specific characterization protocols illustrated in this paper.

PHASE-CHANGE MEMORY

Chalcogenide phase change materials (PCMs), such as GeTe and $Ge_2Sb_2Te_5$ (GST), are excellent candidates for use in resistive memories thanks to rapid reversible phase transformation (10th of ns) between amorphous and crystalline states complemented by a large variation of resistivity (or optical reflectivity). In memory cells (figure 1(a)), switching from the crystalline (low resistivity) to the amorphous (high resistivity) phase is obtained by applying a short and high current pulse which locally melts the material. A longer and lower pulse is used for crystallization.

Regarding material characterization, specific methods are required in order to follow the switching mechanism. When enough phase change material is present, the recording of resistivity or reflectivity evolution with temperature gives useful information (figure 1(b)).

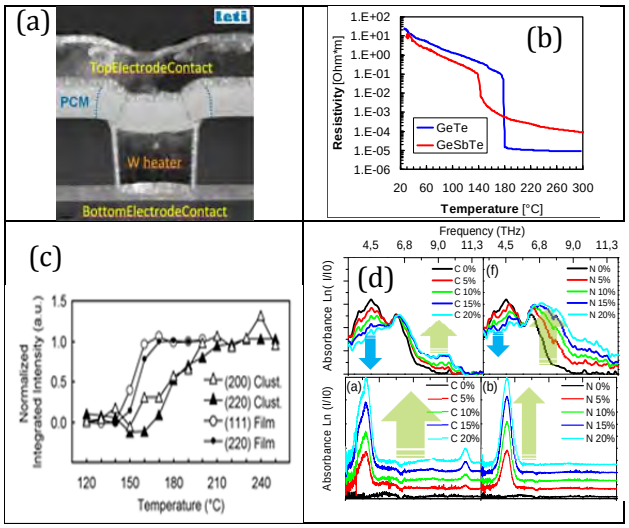


FIGURE 1. (a): TEM cross section of a PCRAM device with GeSbTe. (b): Thin film resistance measurements for $Ge_2Sb_2Te_5$ and GeTe alloys as a function of temperature. (c): crystallization of cluster studied by *in situ* XRD. Normalized integrated intensities for GST clusters (220) and (200), and GST film (111) and (200), diffraction peaks as a function of temperature. (d): LF and HF FTIR absorbance spectra of as-deposited a-GeTeC (left) and a-GeTeN (right) thin films as a function of dopant concentration.

If the mass of studied materials is reduced, X-ray diffraction experiment with high flux (typically synchrotron based experiment) can be required as shown in figure 1(c) for GST nanoclusters (see ref [1] for more details).

9–4

A more fundamental challenge is the precise understanding of the physics responsible for phase change materials properties and, from an application point of view, how we can play with. The introduction of C and N "dopants" were investigated to increase significantly the crystallization temperature of GeTe and GST, with a beneficial increase of the retention time and significant RESET currents reduction [1]. The introduction of dopants in GeTe strongly modifies its properties but the origin of this phenomenon remains unclear. The analysis of Pair Distribution Function obtained by XRD and of vibrational modes by FTIR coupled with *ab initio* simulations allows the investigation of the effect of dopant on the local structure of the amorphous phase [2-3]. The incorporation of C or N drastically affects the mechanical properties of a-GeTe (figure 1(d)). The modification of the vibrational modes goes with an increased number of mechanical constraints leading altogether to a more stressed rigid structure giving a good explanation to the stabilization of a-GeTe by doping.

CONDUCTIVE-BRIDGE RAM

Another promising technology under development for next generation non-volatile memory is the Conductive Bridge RAM (CBRAM). In this case, the device is composed of a solid electrolyte thin film (mainly chalcogenides or oxides) sandwiched between an oxidizable metallic anode (usually Ag or Cu) and an inert cathode. It is expected that, under the influence of an electric field, metallic ions are produced at the anode and migrate through the electrolyte to form a conducting channel. The formation process can be reversed by applying a bias with opposite polarity (bipolar switching). The existence of a conducting filament was evidenced in integrated devices (after cycling) by Energy Filtered TEM (figure 2(a)) [4]. One of the most promising solid electrolyte consists of a thin amorphous film of GeS_2 with a thin Ag layer subsequently dissolved using a photodissolution process. On bulk materials, previous studies have shown that the incorporation of Ag in GeS_2 leads to the formation of Ag_2S nanospheres which would be responsible for ionic conduction in the electrolyte. Unfortunately, the same studies on thin PVD films do not systematically exhibit such crystalline nanospheres, either because the phases are amorphous or too small.

CBRAM devices suffer from data retention issues supposed to be due to the early dissolution of the conductive path [4]. To overcome this problem, one of the solutions investigated consists in the incorporation of "dopants" in the chalcogenide matrix.

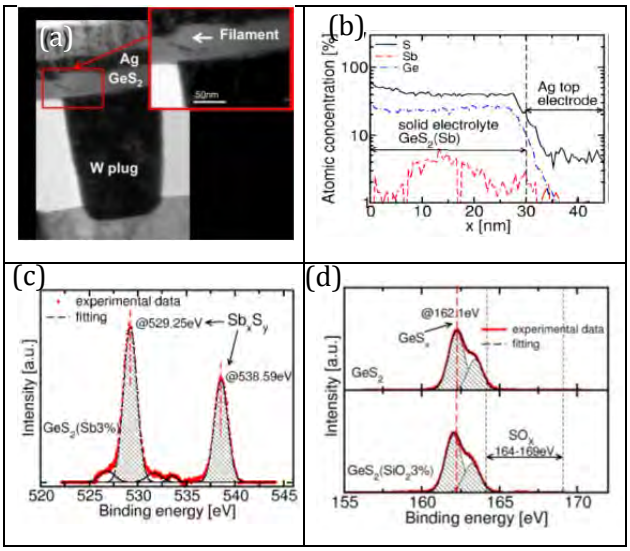


FIGURE 2. (a) TEM cross section of a CBRAM device with GeS_2 electrolyte after SET operation [4] (b) EDX profile of the GeS_2(Sb)/Ag stack (c) XPS spectra of GeS_2(Sb3%) sample putting in evidence Sb-S bonds and (d) XPS spectra of GeS_2 and GeS_2($SiO_2$3%) samples [4].

Figures 2(c) and 2(d) show XPS results performed on doped GeS_2 thin films. The presence of Sb-S bonds is observed in the GeS_2-Sb samples, while in the case of SiO_2 doping, neither Si nor O seems to be bonded to S. The improvements of data retention is only observed in the case of Sb doped GeS_2 devices. In this case, it is expected that Sb reduces the available unbonded S atoms (sites where Ag atoms preferably move to) thus limiting the Ag diffusion. Finally, in-situ experiments could be helpful to better understand the switching mechanism in CBRAM, but these experiments are difficult (the set and reset occurs in a few ns and the conductive filament is at the nanometer scale) [5].

OXIDE-RESISTIVE RAM

Transition Metal Oxide can also present resistive switching in Metal-Insulator-Metal (MIM) structures. Reversible resistive switching was observed in various binary oxides, such as NiO, TiO_2, HfO_2 and Ta_2O_5. Unlike CBRAM, either unipolar (switching triggered by voltage amplitude - not its polarity) or bipolar (switching depends upon voltage polarity) behaviors can be found depending of the studied stack [6]. However,

9–4

despite numerous efforts, the driving mechanism for the resistive switching effect in OxRRAM devices is still under debate. One of the models commonly invoked involves a "filamentary conducting path" in which the resistive switching originates from the formation and rupture of conductive filaments in an insulating matrix [6]. This is confirmed by direct observations of localized conductive regions made on TiO_2 [7] and HfO_2 [8]. C-AFM experiments offer the possibility to produce and analyze these individual conductive paths (figure 3(a) and 3(b)). HR-TEM observations confirm that electroforming (the first write operation) is a local phenomenon starting and propagating through grain boundaries (figure 3(c)). The nature of the conductive filament is also debated. The resistance switching mechanism in HfO_2 OxRRAM is often related to the oxygen vacancies migration towards the oxide/top electrode interface. Unfortunately, the characterization of oxygen vacancy diffusion under electrical field is really tricky and in-situ electrical switching during TEM experiments remains challenging. In these HfO_2 OxRRAM, ex-situ STEM-EELS results (not shown) enlighten the existence of an oxygen-deficient region containing a high density of oxygen vacancies at the top interface [8].

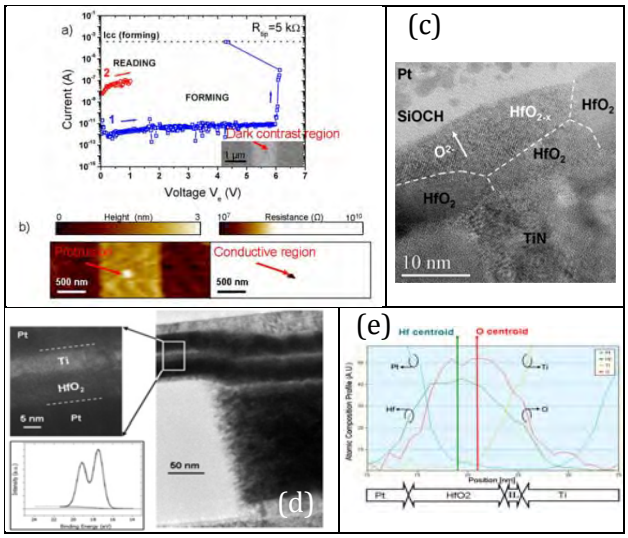


FIGURE 3. (a) I(V) characteristics performed on HfO_2 with C-AFM, Inset: SEM image of the HfO_2 surface after electrical stress [8]. (b) Topography and resistance maps measured by SSRM on the switched HfO_2 (c) HR-TEM image of the HfO_{2-x} conductive region. (d) HR-TEM image of Pt/HfO_2/Ti integrated devices, Inset: Hf 4f XPS spectrum for HfO_2 (10 nm) on Pt [10]. (e) Atomic composition of the active layers in as fabricated device measured by EDX [10].

Ex-situ HAXPES based on the use of synchrotron radiations to study deeply buried interfaces, was also successfully used before and after switching to highlight the importance of oxygen deficiency after the electroforming [9]. Finally, the switching can be improved by tuning the oxygen vacancy distribution in the dielectric layer or at the top metal/oxide interface. However, although it was suggested that the profile of O vacancies in HfO_2 can be controlled by a buffer layer (such as Ti [figure 3(d) and 3(e)]) several questions related to the switching mechanisms are remaining [10]. Unfortunately, direct proofs of the role of the oxygen during the set and the reset are still missing.

CONCLUSION

Efforts are still necessary before introducing new resistive memories in production. In the case of RRAM, there is a consensus that it will require material and stack optimization with a careful control of their properties (oxygen vacancies, doping, crystallography). The future investigations should also be focused on improving the physics of the switching mechanism especially in term of kinetics information. A strategy consisting in combining physical and electrical characterization techniques will be helpful: the use of C-AFM for local-scale characterization of conducting filaments, in-situ switching experiments to dynamically monitor the material changes with HAXPES or HR-TEM to characterize the bulk composition and the interfaces.

REFERENCES

1 S. Maitrejean et al, IEEE IITC (2012).
2. G. Ghezzi et al, Appl. Phys. Lett. **99** (2011) 151906.
3. P. Noé et al., EPCOS12 (2012).
4. E. Vianello et al. IEDM (2012).
5. S.-J. Choi, Adv. Mat. 23(2011) 3272.
6. R. Waser and M. Aono, Nature Mater. **6** (2007) 833.
7. G.H. Kim et al., Appl. Phys. Lett. **98** (2011) 262901.
8. P. Calka et al., Nanotechnology (2013).
9. M. Sowinska et al., Appl. Phys. Lett. **100** (2012) 233509.
10. C. Cagli et al. IEDM (2011).

KEYWORDS

Memory, Resistive switching, PCRAM, CBRAM, OxRRAM

ACKNOWLEDGEMENTS

The authors would like to thank J.-Y. Raty (Liège University) for *ab initio* simulations of PCMs, F. Hippert (CNRS-LNCMI), N. Boudet (ESRF), M. Maret (CNRS-SIMAP) and F. D'Acapito (CNR-IOM-OGG) for synchrotron-based experiments, C. Vallée, P. Gonon, C. Mannequin (CNRS-LTM) for their contibution on OxRRAM.

9–5

MICROWAVE ELECTRICAL MEASUREMENTS OF INDIVIDUAL MAGNETIC DEVICES FOR SPINTRONICS, MRAM, AND NONBOOLEAN ARCHITECTURES

Matthew R. Pufall, Eric R. Evarts, and William H Rippard

Magnetics Group, Electromagnetics Division
NIST, 325 Broadway, Boulder, CO 80305

INTRODUCTION*

Nanometer-scale spintronic devices based on magnetic materials are being explored for applications ranging from memory to logic, driven by the promises of low energy operation, nonvolatility, and novel functionality. Spintronic devices based on the spin-transfer torque effect are a true nanotechnology, in that they show emergent behavior as device dimensions decrease. As a consequence, the function of a device can also depend on the details of the magnetic properties such as magnetization, anisotropy, and defects, at nanometer length scales. Spin transfer torques can cause large-angle, nonlinear magnetization dynamics of amplitudes not readily accessible via applied fields, dynamics that are sensitive to the details of the local magnetic properties. We have developed new electrical metrologies that utilize magnetoresistance and the spin transfer torque effect to quantify the high frequency behavior of fully functional individual devices, and are able to correlate these behaviors with particular magnetic processes.

For MRAM elements, we measure read disturb rates and write error rates at 1 part in 10^6 accuracy and correlate these errors with device-level ferromagnetic resonance spectra of magnetic modes and with measured real-time switching traces. For spin torque oscillators (STOs) that are being considered as elements in NonBoolean logic architectures, we have developed several measurement methods that probe the nanoscale magnetic and electrical environment, such as: a) measurement of microwave spectra vs. field to probe magnetization and anisotropy variations of a continuous thin film on a length scale of 50 nm; b) measurement of the frequency (phase) noise spectra of an individual STO, showing Gaussian and excess $1/f$ noise; c) measurement of phase locking to impressed ac signals, and the time to achieve locking; d) measurement spin wave radiation from an STO, and of coupling between adjacent STOs via spin waves.

RESULTS

In the following section we present some of our measurements of spin torque switched MRAM devices patterned at NIST, as well as measurements of STO dynamics and phase locking, results that will be expanded upon in the presentation.

* Official contributions by the National Institute of Standards and Technology are not subject to copyright.

9–5

SPIN TORQUE MRAM

Over the past several years, spin torque MRAM (STT-MRAM) has moved from the laboratory to demonstration product.[1-3] with read and write performance testing moving from tens of events to greater than 10^6. New physics has emerged particularly in the infrequent events measured in write error rate (WER) testing, in which the performance of some devices can deviate significantly from the "macrospin" or single magnetic domain model.

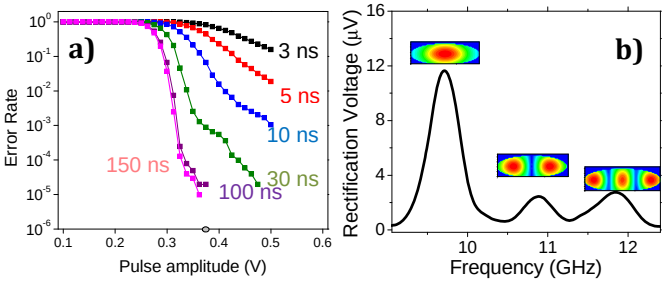


FIGURE 1. a) WER of 50 nm x 150 nm device; b) Sample ST-FMR spectra of the same device at $\mu_0 H$ = 0.8 T out of plane. Inset ellipses are micromagnetic simulations of the normal modes of oscillation for this field. Red indicates greater magnetization motion, blue lesser motion.

Fig. 1a shows the WER of a 50 nm x 150nm elliptical magnetic tunnel junction device, with a stack consisting of (thicknesses in nm) bottom/Ta(5)/PtMn(15)/CoFe(2.3)/Ru(0.8)/CoFeB(2.5)/MgO(0.87)/CoFeB(1.5)/Ta(1)/top. The top layer is called the "free layer" and can switch between two stable states along the long axis of the ellipse, depending on the direction of the current pulse injected into the device. As seen in the figure, the write error rates with increasing voltage for devices with in-plane magnetization can deviate from the single exponential predicted by the single domain, (dual potential well) model. Using spin-torque, we can measure the normal modes of oscillation of a single device using spin-torque induced ferromagnetic resonance (spin torque FMR). An ac current is injected into the device, producing an ac spin torque that induces precession and an ac resistance change, and a rectification voltage is produced by the combined ac resistance and current.

As seen in Fig. 1b, multiple peaks are visible as a function of frequency, indicating that the device is not acting as a single domain. Similar spectra are seen for all devices of this size. Nonetheless, in many devices the WER distributions appear as those expected for a single domain. However, we can correlate variations in these spectra with variations in write error rates. Furthermore, we are able to do real-time high-bandwidth (13 GHz) measurements of magnetization trajectories of these infrequent events. These measurements support the idea that these events result from deviations from single-domain behavior, and that nanostructure in the device is affecting function.

METROLOGIES FOR STOS FOR NONBOOLEAN ARCHITECTURES

Nanocontact spin torque oscillators are based on a localized, large-angle magnetization excitation in one layer of a continuous spin valve multilayer. This excitation is caused by an injected dc current that becomes spin-polarized as it traverses the spin valve structure, transferring spin angular momentum from one layer to the other and causing coherent oscillations in the thinner layer. These oscillations are large amplitude (precession cone angles approaching 90°), with typical frequencies in the tens of gigahertz, are narrowband (1 MHz), and are tunable by the magnitude of dc current. These excitations are intrinsically a nanoscale effect, requiring high current densities (10^7 A/cm^2) to induce coherent precession.[4] The resulting excitation is localized under the 50-100 nm diameter nanocontact, but is coupled to the surrounding magnetic film, into which spin waves can radiate.

We have shown that these oscillators are nonlinear, exhibiting frequency pulling and phase locking[5] to injected ac currents. Furthermore, we have shown that STOs respond nonlinearly to spin

9–5

waves: Two STOs made to the same magnetic film can mutually phase lock via spin waves, and to a lesser extent dipolar coupling.[6] Furthermore, an STO can be used as a local magnetoresistive sensor to detect spin waves radiated from a nearby STO.[7]

As narrowband, current tunable, nonlinear microwave oscillators, along with their back-end of line CMOS compatibility, STOs have garnered interest as the basic elements in oscillator-based NonBoolean architectures. However, substantial metrology challenges must be met for this development to move forward. Fundamentally, these challenges are due to the fact that while the general properties of these oscillations are understandable from the point of view of a single domain model, the details are not. Because of the nonlinear nature of the excited mode, analytical or computational models of this mode and its interaction with the surrounding environment—and variations/defects in this environment—are currently lacking.

To aid in the development of these models, we have developed electrical measurement methods to better quantify the local magnetic environment, and the nonlinearities of these devices. For example, we use spin-torque FMR to parameterize the net effective magnetic field seen under the nanocontact, and measure how this field varies with field direction as a measure of the inhomogeneity of the magnetic layer.[8] We find that at the length scales of STOs, magnetic films can show variations on the order of 1 mT to 10 mT. Furthermore, our results suggest that these variations can have a substantial effect on the *nonlinear* excited mode, producing output frequency variations far greater than those expected for such effective field variations.

Another probe of the local magnetic environment is the color of the frequency noise spectrum. This spectrum can also act as a measure of the intrinsic relaxation processes of the oscillator. We have developed methods to measure the frequency noise spectrum of the pW-nW output powers of STOs over several decades. We have found that the color of the frequency noise exhibits Gaussian white noise, as expected for an oscillator at finite temperature, but an excess $1/f$ noise component not predicted by models. Furthermore, this $1/f$ component varies with free layer composition.[9]

For synchronization and relative phase control of large arrays of oscillators as is required in oscillator-based associative memories,[10] the nonlinearities that drive STO coupling to injected ac currents and incident spin waves must be better understood. We have developed measurement methods to parameterize this nonlinearity in several ways. First, we have measured the locking range of the STO as a function of injected ac current amplitude and harmonic number, for comparison to oscillators. Second, we have made real-time measurements of the time to lock to an injected microwave pulse. Together, these measurements form an initial parameterization of the nonlinear coupling of STOs to currents, and are useful inputs to and comparisons with analytical or computational models. Similar measurements are planned for mutual phase locking via spin waves, as this coupling is in principle driven by a different nonlinear mechanism.

REFERENCES

1. J. Slonczewski and J. Sun, J. Magn. Magn. Mat. **310**, 169–175 (2007).
2. M. Gajek, et al., *Appl. Phys. Lett.* **100**, 132408-132411 (2012);
3. J. Sun, et al., *Phys. Rev. B* **84**, 064413-064422 (2011).
4. W. Rippard, et al., *Phys. Rev. Lett.* **92**, 90–93 (2004).
5. W. Rippard, et al., *Phys. Rev. Lett.* **95**, 10-13 (2005).
6. S. Kaka, et al., *Nature* **437**, 389–92 (2005).
7. M. Pufall, et al., *Phys Rev. Lett.* **97**, 087206–9 (2006).
8. M. Pufall, W. Rippard, S. Russek, and E. Evarts, *Phys. Rev. B* **86**, 094404–10 (2012).
9. M.W. Keller, et al,, *Appl. Phys. Lett.* **94**, 193105-8 (2009).
10. F. Hoppensteadt and E. Izhikevich, *Phys. Rev. Lett.* **82**, 2983–2986 (1999).

KEYWORDS

STT-MRAM; magnetics; spintronics; microwave measurements; ferromagnetic resonance; nonlinear oscillators; NonBoolean;

10–1

Overview of Next Generation Lithography - Advanced Patterning, EUV & Self Assembly

Stefan Wurm and Mark Neisser

SEMATECH, 257 Fuller Road, Suite 2200, Albany, NY 12203, U.S.A.

Introduction

Over the past ~40 years optical lithography has been enabling two dimensional scaling of critical dimension (CD) feature sizes from ~6 μm down to ~22 nm. As prescribed by Raleigh's law, this was accomplished through decreasing the imaging wavelength λ, increasing the numerical aperture (NA) of the optical projection system, and through patterning process improvements. Per Raleigh's equations [1], imaging resolution is limited to 0.25 λ/NA, where the maximum NA is determined by the refractive index of the immersion fluid. For ArF immersion at 193 nm, that fluid is water, with a refractive index of 1.44. The smallest half pitch that can possibly be resolved is about 34 nm. Actual constraints of real tools and lithography processes mean that one can approach this number, but not hit it exactly. Therefore, for advanced patterning at the 32 nm half-pitch the industry introduced double patterning lithography (DPL), where the pitch of a printed pattern is doubled by chemical processes on etched structures or by actually exposing and etching the same layer twice. This concept can be extended to multiple patterning lithography (MPL), but the cost increases significantly. The preferred industry alternative to MPL is extreme ultraviolet lithography (EUVL), which uses 13.5 nm radiation, as it would allow the industry to go back to a single patterning solution at 22 nm half-pitch. However, EUVL still has challenges to overcome before it is manufacturing ready. Both MLP and EUVL technologies could benefit from assist technologies such as directed self-assembly (DSA).

DSA uses certain types of polymers that separate into different phases when annealing. With appropriate polymers, the polymer structure will determine the dimensions and general morphology of the blocks. In the absence of constraints or directing forces, this phase separation process is called "self assembly;" it will provide random arrangements of lines, cylinders, or whatever phase shape is formed. If some type of constraint can be applied, more regular patterns can be made. For example, if the self-assembly is constrained between parallel linear walls, a pattern of lines can be assembled, or if there is a pattern of holes self-assembly may give smaller holes within those holes. This directing of the patterns formed by applying constraints is called "directed self assembly" or "DSA."

Metrology capabilities providing the means of measurement needed to enable patterning solutions and to support them in manufacturing have been critical in the past. Today's advanced lithography manufacturing technology heavily relies on sophisticated imaging and process simulation, which in turn requires large amounts of measurement data to be acquired on a routine basis to ensure process stability. Accurate, precise, and fast measurement of critical parameters is indispensable to meet today's manufacturing

10–1

challenges in advanced lithography process and equipment control. The timely availability of new metrology capabilities will be critical to support the introduction of new lithography technologies for sub 22 nm half-pitch. The following sections describe the key metrology challenges for multiple patterning, EUV lithography, and for DSA.

ADVANCED PATTERNING

The main metrology challenges of DPL and MPL are the expected ones of measuring very small features and defects that get smaller each year. However, there are additional measurements needed since there can be dual and/or multiple distributions of CDs, overlay, etc. (one distribution for each exposure plus measurement related to the relative placements and sizes of each exposure or additional pattering step). But these metrology challenges should not be underestimated. Table 1 shows some key lithography specifications from the 2011 International Technology Roadmap for Semiconductors (ITRS) [2] for the next 10 years. Clearly, precisions on the order of 0.1nm will be needed in future measurements. What is more, the specification shown for minimum patterned defect size is the expected measurement capability, not the desired capability. There is room for improvement in the current and expected capabilities for defect identification and characterization.

EUV LITHOGRAPHY

EUVL lithography needs to meet the same requirements shown in Table 1 except for the MPL related ones shown in the bottom two rows. However, the physics of producing and imaging EUV radiation brings new metrology challenges. EUV operates at a wavelength of 13.4nm, which is 14X smaller than 193 nm, is readily absorbed in air and drives a very different light/matter interaction. The EUV light path needs to be all in vacuum and optical designs have to be reflection-type instead of transmission-type using near normal and grazing incidence mirrors.

Mask and lens mirrors are made of dozens of layers with thicknesses less than the EUV wavelength in order to use interference properties to produce EUV Bragg reflectors. Any non-uniformity in these structures can produce aberrations in optical elements or defects in masks. Preliminary work has shown that buried mask defects much smaller than a printed feature can give unacceptable defects in the printed pattern. The metrology tool infrastructure and methodology for detecting and assessing the severity of mask defects other than actually printing wafers and measuring the printed patterns is still in development. This includes commercial actinic mask blank inspection, actinic and e-beam based patterned mask inspection and an EUV areal imaging tool.

TABLE 1: Key ITRS lithography specification driving metrology requirements.

Specification in (nm)	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
Minimum line CD	20	18	17	15	14	13	12	11	10	9	8
Minimum hole dimension	32	28	25	23	20	18	16	14	13	11	10
Minimum patterned defect size	20	20	20	10	10	10	10	10	10	10	10
Minimum hole CD uniformity	1.2	1.0	0.8	0.6	0.5	0.5	0.4	0.4	0.3	0.3	0.3
Double patterning CD uniformity	0.6	0.4	0.3	0.3	0.3	0.3	0.2	0.2	0.2	0.2	0.2
Spacer defined CD uniformity		0.4	0.3	0.3	0.3	0.3	0.2	0.2	0.2	0.2	0.2

10–1

Another EUV challenge is light sources. The need for high source power for the exposure tools themselves is well known and there is a focused industry effort underway to develop better EUV sources for exposure tools. But EUV metrology tools would also benefit from brighter sources. The necessary power is much smaller than that of an exposure tool, but the space and cost constraints are much smaller too.

Directed Self Assembly

In a DSA process, typically a film of block copolymer is applied onto a wafer, baked to anneal and generate the domains of different phases, and then etched. It is desirable to inspect the annealed pattern before it is etched to make sure the features are the correct size and in the correct locations, because after etch, the wafer will probably not be reworkable and will have to be scrapped if the annealed patterns weren't correct. But this inspection requirement means determining the physical structures of contiguous phases that might not be that different chemically. For example, one might be inspecting a pattern of lamellae of polystyrene alternating with polymethylmethacrylate where the width of the lamellae is between 12 and 18 nm and the mixing zone in between the phases is 1 or 2 nm thick. This is a significant metrology challenge by itself. Complicating this measurement is the need to understand the three dimensional structure of the lamellae. The pattern may look perfect when the lamellae are looked at from the top of the film, but the lamellae may be tapered, or even connected at the bottom of the film. So top down inspection will not suffice to say the annealed pattern is correct.

Another difficult issue is pattern registration. Features such as holes (formed by phase separated cylinders) and lines (formed by vertical lamellae) have to be aligned to circuit elements below them. But measuring this alignment can require measuring the position of phases in the annealed film with features that are below and obscured by the annealed film. This is another challenge, especially since position will have to be controlled to less than 20% of an already small feature size.

Another DSA metrology issue is defects. The free energy differences that drive the annealing process are small and finely balanced. Contamination of a guiding pattern can affect the phase annealing and cause unwanted patterns to form. On the other hand, some sorts of defects can be present and not affect the finished pattern at all because a small gap in an aligning feature may still leave the desired pattern as the lowest free energy state. Not enough is known yet about what types of defects are critical to self assembly. Learning about this will require characterizing very small defects, some of which might be merely changes in substrate surface energy, and testing their effect on the self assembly process. This will require defect identification and analysis of very small defects, which is a considerable challenge.

Summary

The industries ability to continue two dimensional scaling towards ever smaller feature sizes critically depends on the simultaneous availability of advanced lithography technologies and metrology capabilities that can support their manufacturing introduction. For the new patterning techniques on the horizon, such as EUV, MLP, and DSA, this will require new metrology techniques and new inspection tools. Buried defects, three dimensional profiles and characterization of phase domains are among the key lithography / metrology challenges that need to be addressed by the semiconductor industry.

References

[1] Lord Rayleigh, *Phil. Mag. (5)* **8**, 261 (1879) and B. J. Lin *Proc. SPIE* **633** 44 (1986)

[2] http://www.itrs.net/Links/2011ITRS/Home2011.htm

Keywords

Advanced lithography, double patterning, multiple patterning, extreme ultraviolet lithography, direct self assembly

10–2

METROLOGY TOOLS AS BASIS FOR PHOTO MASK REPAIR AND PERFORMANCE IMPROVEMENT

Klaus Edinger

Carl Zeiss SMS GmbH, Industriestr. 1, 64380 Rossdorf, Germany

INTRODUCTION

Driven by the consumer market and keeping pace with Moore's law, integrated circuit components are continuously shrinking in dimension. To make smaller circuit features, the microelectronic industry has implemented new techniques such as immersion lithography and multiple patterning and is currently introducing Extreme-Ultraviolet (EUV) lithography for high-volume chip manufacturing. With this trend of extending optical lithography the requirements on the quality of the photo mask as part of the optical system have increased dramatically.

In order to improve process control and mask performance Carl Zeiss SMS has developed several closed loop applications: For example, data generated by mask metrology tools such as aerial imaging or registration and overlay measurement are used as input for an ultra-short pulse laser based system. The laser system can write intra-volume shading elements inside the bulk material of the mask. By adjusting the density of the shading elements, the light transmission through the mask is locally changed in a manner that improves critical dimension uniformity across the wafer. On the other hand, the laser system can also be used to generate a locally varying lateral strain field in order to correct registration and overlay errors.

For reticle fabrication mask repair and validation has become a fundamental part of the production process and focused electron beam induced processing has evolved as state of the art technology for repairing advanced photo masks[1].

ELECTRON BEAM BASED MASK REPAIR

Focused electron beam induced processing is a high resolution nanostructuring technique for local deposition and etching of materials. In the MeRiT® mask repair tool the high resolution electron beam of an SEM is used to induce chemical reactions at the mask surface. A suitable precursor gas is dispensed through a nozzle in close vicinity to the incident beam. Depending on the precursor chemistry, a reaction is induced by the electrons, leading to either a deposition caused by fragmentation of precursor molecules or to a reaction between the adsorbed molecules and the substrate material, resulting in volatile products and thus etching of the substrate material. Since the reaction is confined to the area exposed by the electron beam, this technique allows high resolution nanostructuring with feature sizes well below 50 nm.

ABSORBER DEFECT REPAIR

Currently used 193nm lithography photo masks consist of a 6 inch quartz plate with a sub 100 nm thick absorber on top. The absorber material can be either complete opaque (binary mask) or can transmit a small amount of light which is phase shifted by 180 degree and thus enhancing the

10–2

contrast of the image projected onto the wafer (attenuated phase shift mask PSM). Defects on patterned mask can either be missing absorber material (clear defect) in which case material needs to be added. The added material not only must resemble the optical properties of the missing absorber, but also has to be durable towards harsh cleaning procedures and extended UV exposure. The other type of defect is absorber material in areas that should be transparent (opaque defect). Here, the material, which can also have lateral variations in height, has to be selectively removed without damaging the underlying quartz substrate. After the repair the repair quality is verified by an aerial imaging system (AIMS™) which emulates the scanner and thus allows a quantitative determination of the photolithographic process window. An example of a clear defect repair is shown in figure 1.

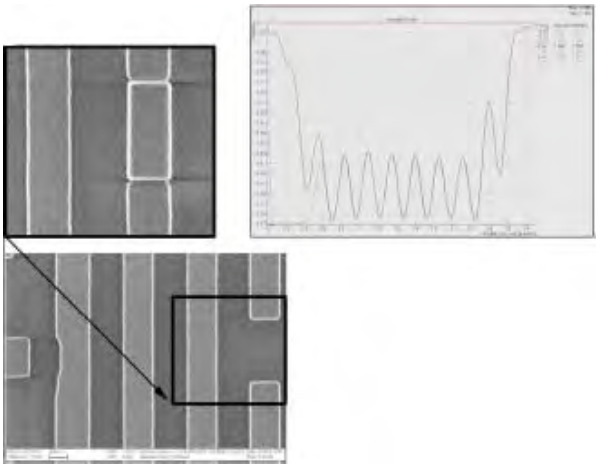


FIGURE 1. SEM image of a programmed defect on an attenuated phase shift mask (lower left). SEM image of the repair (upper left) and corresponding AIMS™ measurement (upper right)

EUV Mask Repair

The scheduled transition from 193 nm lithography to Extreme Ultra-Violet (EUV) lithography introduces reflective optics which poses significant challenges to the optics including the photo masks itself. The more complex nature of the optics (Bragg multilayer mirrors at 13.6 nm wavelength, operated under vacuum), and the increased complexity of manufacturing steps involved, increase the number of possible sources for defects. Small embedded particles causing deviations from smoothness of the multilayer as shallow as 3 nm, can significantly change phase and intensity of the reflected light and are therefore already critical. As a consequence repair capability is required for defects in the absorber layer and for defects in the mirror[2].

Since a repair of the multilayer itself is not feasible a compensation technique is used, where the center of the multilayer bump or pit is located and the absorber around the defect is removed to compensate for the light intensity drop at the defect site. Since this shallow multilayer defects can be invisible in the SEM image a vacuum compatible atomic force microscopy (AFM) measurement system has been integrated into the vacuum chamber next to the electron column. A successful compensational repair is shown in figure 2.

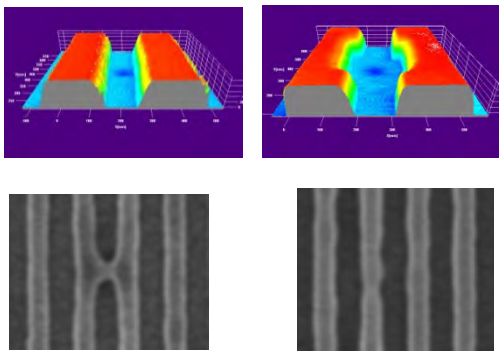


FIGURE 2. Example of a successful compensation repair of a multilayer pit defect. Top: AFM images before (left) and after repair (right). Bottom: SEM images of the developed resist after wafer printing before (left) and after repair (right)

References

1. I. Utke, S. Moshkalev and P. Russell, *Nanofabrication Using Focused Ion and Electron Beams: Principles and Applications*, Oxford University Press, *2012,* 349 -380.
2. M. Waiblinger, T. Bret, R. Jonckheere, D. van den Heuvel, Proceedings of SPIE **8522**, 85221M (2012).

Keywords

Mask repair, EUV multilayer, focused electron beam induced processing, aerial imaging

11–1

FRONTIERS OF ATOM PROBE MICROSCOPY

Karen T. Henry

Intel Corporation

INTRODUCTION

As transistor dimensions continue to shrink, the ability to measure the position and composition of individual atoms becomes increasingly important. CMOS technologies today incorporate complex three-dimensional geometries comprised of several materials to achieve the desired performance. With fewer dopant atoms within such devices and film thicknesses approaching less than a nanometer, atom probe tomography (APT) is a natural complement to current generation microscopy techniques such as transmission electron microscopy (TEM) and secondary ions mass spectrometry (SIMS). The use of focused ion beam (FIB) sample preparation methods and the development of laser-assisted APT have led to significant advances in the characterization of semiconductor materials at the atomic level. This discussion will overview advances in the APT technique that have allowed for the atomic-scale characterization of multi-layers, oxide films, and semiconductor materials and devices.

ATOM PROBE OVERVIEW

APT combines a time-of-flight mass spectrometer with a point projection microscope capable of atomic-scale imaging. The technique is based on the successive removal of single surface atoms from a very sharp needle-shaped sample. By applying a standing DC voltage to the sample, the surface atoms with the highest electric field strength are ionized and removed from the tip surface. This physical process is referred to as field evaporation [1]. In conventional APT, the standing DC voltage is held below the field evaporation threshold of the surface atoms and voltage pulses are applied to raise the field above the threshold to trigger a field evaporation event.

To study materials with electrical conductivities lower than metals, laser pulses can be used to trigger a field evaporation event. In laser-assisted APT, a short, spatially confined temperature rise at the specimen apex lowers the field evaporation threshold and leads to field evaporation at a given DC voltage. Once a field evaporation event occurs, the elemental identity is determined by time-of-flight (TOF) mass spectrometry and the atomic coordinates are determined by a position-sensitive detector. Based on the ion TOF and its position on the detector, the atomic identity and position within the sample volume can be reconstructed.

SPECIMEN PREPARATION

Electropolishing has been the traditional method for fabricating the needle-shaped specimen geometry necessary for APT analysis [1]. However, advancements in FIB-based systems and sample preparation methods now provide an alternative method to fabricate specimens from a specific region of interest in a variety of materials [2-3]. The combination of ion beam milling and high-resolution SEM imaging provides the flexibility to locate a buried region of interest, remove unwanted materials, and position the apex of the specimen at a specific site as shown in Figure 1.

11–1

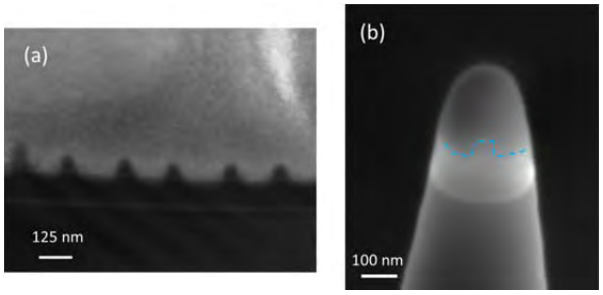


FIGURE 1. (a) – (b) Positioning a region of interest within a specimen using FIB-based preparation techniques.

Atomic-scale Dopant Mapping

The mapping of dopant distributions with high spatial resolution has been recognized as an important part of the roadmap for the design of future transistors [4]. As transistor dimensions continue to shrink, the challenge to understand and characterize both the implant depth and potential migration within the nm-scale dimensions of actual devices has intensified. APT offers a unique combination of high analytical sensitivity coupled with high spatial resolution.

Currently, secondary ion mass spectrometry (SIMS) is heavily relied upon in the industry to measure dopant profiles. The analyzed sample volume required to achieve maximum sensitivity is not constrained, with analyzed areas often several hundred square microns. Square microns of material cannot be analyzed by APT and thus does not compete with SIMS for sensitivity at the micron scale. However, at the nano-scale, APT is ideally suited to investigate dopant distributions of device-level volumes. Prosa et al. demonstrate APT measurements can provide accurate and precise measurements of dose when best practices for analysis are followed [5]. Figure 2 shows a direct comparison between SIMS and APT of the National Institute of Standards and Technology (NIST) SRM-2134 arsenic implant in silicon depth profile.

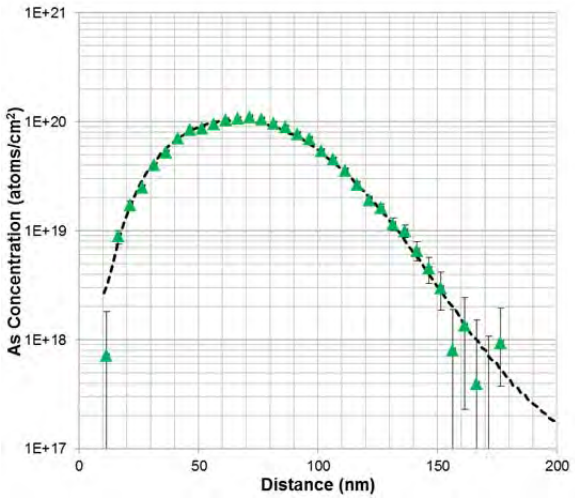


FIGURE 2. A representative As dopant profile. Green triangles are APT data points with 1σ error bars based on counting statistics and background subtraction. The dashed black line is the SIMS profile for comparison.

These results illustrate that APT is capable of atomic-scale dopant mapping and in combination with SIMS can provide a comprehensive picture of dopant distributions.

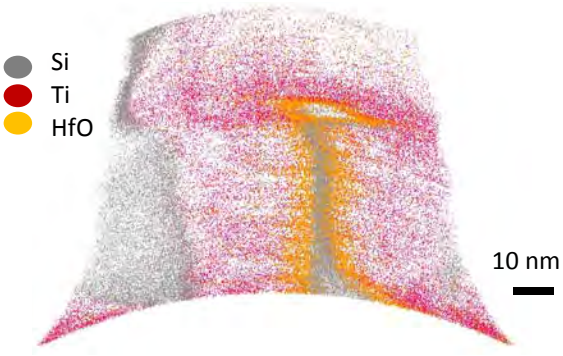
Silicon Device Analysis

To achieve desired performance in today's CMOS technologies, complex three-dimensional geometries comprised of several materials have been developed. In these highly engineered devices, slight process variations can affect the structural and material properties such as dimensions, interface roughness and dopant distribution. Advanced metrology techniques with high spatial resolution and sensitivity are needed to characterize and control these parameters. APT is seen as a potential candidate for providing 3D chemical imaging of device-level volumes.

The test structures used to illustrate the use of APT for silicon device analysis consist of an array of fins as shown in Figure 1. Specimens were prepared using a FIB-based technique where a single fin was isolated for analysis. Figure 3 shows the analyzed volume after 3D reconstruction. This image depicts the complete structure analyzed starting from the poly-silicon cap to the base of the Si-fin. Distortions

11–1

of the Si-fin and gate structure are observed in the reconstruction. These artifacts are expected when analyzing 3D heterogeneous structures. Although the appearance of the reconstruction is distorted, useful information can be extracted such as intermixing of the layers comprising the gate structure or the lateral distribution of dopants and impurities.



The development of advance reconstruction algorithms and the use of correlative techniques such as transmission electron microscopy (TEM) are needed to improve the quality of the data.

Summary

The introduction of laser-assisted APT combined with the development of advanced specimen preparation methods has extended the application base of this technique beyond metallurgy. With high spatial resolution and three-dimensional chemical mapping capabilities, APT will provide information not available by any other microscopy technique. The few examples provided illustrate how laser-assisted APT can be used in the development of semiconductor materials and devices.

References

1. M.K. Miller, A. Cerezo, M.G. Hetherington and G.D.W. Smith, *Atom probe field-ion microscopy*. Oxford, Oxford University Press, 1996.
2. K. Thompson, D. Lawrence, D.J. Larson, J.D. Olson, T.F. Kelly and B. Gorman B *Ultramicroscopy* **107**, 131 (2007).
3. M.K. Miller and K.F. Russell, *Ultramicroscopy* **107**, 761 (2007).
4. ITRS, International Technology Working Groups International Technology Roadmap for Semiconductors, www.itrs.net (2010).
5. T.J. Prosa, D. Olson, B. Geiser, D.J. Larson, K. Henry and E. Steel, *Ultramicroscopy*, **In press** (2012).

Keywords

Atom probe, dopants, characterization

11–2

LASER-TIP INTERACTION PART ONE : PROBING THE THERMAL RESPONSE OF A SILICON FIELD EMITTER BY ULTRA-FAST LASER ASSISTED ATOM PROBE TOMOGRAPHY

Angela Vella [1], Elena P. Silaeva [1,2,] Jonathan Houard [1], Tatiana E. Itina [2], and Bernard Deconihout

1 Groupe de Physique des Materiaux UMR CNRS 6634 and CORIAUMR CNRS 6614- UFR Sciences Site du Madrillet, Avenue del'Universit´e - B.P. 12 76801 Saint Etienne du Rouvray, France

2 Laboratoire Hubert Curien, UMR CNRS 5516/Universit´e Jean Monnet,18 rue Benoˆıt Lauras, 42000 Saint-Etienne, France

INTRODUCTION

The optical properties of non-metallic field emitters are strongly affect by the static electric field applied to the tip, as theoretically studied by Tsong in 1979 [1] and more recently by authors [2]. Tsong suggested that the conduction and valence bands at the surface of a doped semiconductor at room temperature are bent under a huge positive electric field. As a result, the high density of holes at the surface changes the properties of the material at the surface, which becomes semi-metallic. However, all models developed in the different domains of laser-tip interaction to evaluate the contribution of the thermal and optical effects neglect the band bending due to the static field, in band- gap materials.

In this presentation, we show, theoretically and experimentally, that the high static electric field can confine the absorption at the surface of a silicon tip, where the band bending takes place. This confinement of the absorption increases the contrast between the temperature of the surface and that of the bulk (tip apex and tip shank). This contrast is at the origin of an ultra-fast thermal pulse, which is probed by time-resolved measurements using Laser assisted Atom Probe Tomography (La-APT).

THEORETICAL MODEL

To describe the transient response of the silicon tip to the field during the interaction with the laser pulse, we use the drift-diffusion approach. In the presence of a positive electric field, the photo-generated holes start moving toward the surface, whereas the electrons move in the opposite direction.

This effect leads to a significant increase in the hole density at the surface with respect to its bulk value.

At the surface, accumulated holes can significantly absorb laser energy.

The temperature at the surface of the tip is determined by the processes of heating and heat dissipation in the bulk. The heating is caused by the transfer of energy from the carriers to the lattice

11–2

through carrier-phonon coupling and carrier recombination. Because of fieldinduced charge separation and very low density of electrons at the surface the surface recombination becomes negligible and the temperature time evolution is determined by the thermalization process between hot holes and the lattice. The energy transferred to the lattice depends on the hole temperature and its density.

Experimental Results

To verify the confinement of the absorption at the surface, a linear 3D atom probe assisted by femtosecond laser.

Using an autocorrelation setup, two laser pulses with a variable temporal delay are slightly focused onto the tip. Figure 1 shows the evolution of the evaporation rate φ as a function of the delay τ between the pulses.

A very fast decay is observed experimentally as a function of the delay between pulses: the evaporation rate is divided by a factor two in less than 5 ps.

Fitting the data by our theoretical model a cooling time of only 1.7 ps is obtained. This time incredibly short and can only be related to a near-surface optical absorption and heating. Hence, the measurement of this short cooling time is a experimental evidence of the influence of the band bending due to the high electric field on the optical properties of the tip and its following heating and cooling process.

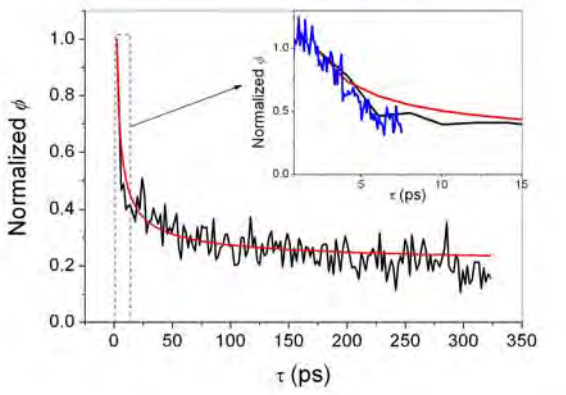


FIGURE 1. Normalized evaporation rate as a function of the delay between pulses using autocorrelation (black curve). In the inset, blue (black) line corresponds to the evaporation rate measured at short (long) delay time and red line correspond to the fit.

References

1. T. Tsong, Surface Science 81(1), 28–42 (1979).

2. E P Silaeva, A Vella, N Sevelin-Radiguet, G Martel, B Deconihout and T E Itina New Journal of Physics 14 **(2012) 113026**

Keywords

Atom probe tomography, laser-nanotip interaction

11–2

LASER-TIP INTERACTION PART TWO: LIGHT ABSORPTION BY NANOSCALE SEMICONDUCTING TIPS IN LASER-ASSISTED ATOM PROBE TOMOGRAPHY

J. Bogdanowicz[1,2], M. Gilbert[2], S. Koelling[2,3] and W. Vandervorst[1,2]

[1]*Instituut voor Kern- en Stralingsfysika, KU Leuven, Celestijnenlaan 200D, B-3001 Leuven, Belgium*

[2]*IMEC, Kapeldreef 75, B-3000 Leuven, Belgium*

[3] *Fraunhofer-CNT, Königsbrücker Str. 180, 01099 Dresden, Germany*

INTRODUCTION

Atom Probe Tomography [1,2] (APT) is an analysis technique based on the emission of ionized species from a nanoscale conical tip with a sub-100-nm apex radius. Due to the high constant voltage applied to the sample, a strong electric field just below the field-evaporation threshold (~ 10-50 V/nm) is generated at the tip apex [3]. An electric pulse (voltage-pulsed APT, typically used for good electrical conductors) or a sub-picosecond laser pulse (laser-assisted APT, typically for poor conductors) is then used to trigger the emission. The evaporated ions, after being accelerated in the electric field onto a position-sensitive detector, are chemically identified by time of flight mass spectrometry. This allows for the full compositional analysis of three-dimensional volumes with sub-nanometer resolution. While the evaporation mechanism of voltage-pulsed APT is well understood [4], the impact of the laser on a nanoscale tip during a laser-assisted APT experiment is still under intense investigation [5-17]. The latter is indeed considerably influenced by the light absorption properties of the conical tip as well as by the nonlinear dynamics of the carriers/heat generated in the tip by the laser pulse. These complex effects control the evolution of the surface of the nanoscale object and, hence, the time dependence (i.e. final mass resolution) and nature (single or multiply charged ions, clusters,...) of the emitted species. A clear and quantitative understanding of these phenomena is therefore required in order to fully exploit the power of the laser-assisted APT technique and to transition from an experimental, intuition-based operation and interpretation towards an optimized and quantitative analysis.

In this paper, we propose to focus on the first phase of the laser-tip interaction, i.e. develop a model to explain physically and quantify the absorption of the laser pulse by a conical semiconducting tip. We start by generalizing the analytical Mie theory of light scattering and absorption by cylindrical objects to the case of a conical tip. This first-order theory shows that absorption in a conical tip occurs preferentially at well defined locations of the tip, as confirmed experimentally by the presence of sharply localized holes in tips illuminated with high-power pulses. The theory is then refined and discussed to account for experimental observations which disagree with the first-order model.

11–2

LOCALLY RESONANT ABSORPTION IN CONICAL TIPS

A rigorous analytical solution to the problem of the interaction between light and a conical object does not exist, which explains why most investigations have so far been based on time-consuming finite-difference time-domain simulations [10-14]. It has, however, recently been demonstrated that an approximate analytical theory can be developed based on Mie theory of light scattering and absorption by infinite cylinders [18]. This solution has the advantage of explaining the physics underlying this phenomenon [19].

According to Mie theory, the electric field coupled into an illuminated cylinder is strongly enhanced for sharply defined values of the cylinder radius (Fig. 1). This resonant behavior is the result of the constructive interference between the transmitted and (multiply) internally reflected waves inside the cylinder, as also occurs in thin films of specific thicknesses. Yet, following [19], a cone with a small angle (<5-10°) interacts electromagnetically as a stack of cylinders with a radius varying slowly along the axis z of symmetry. The internal field shown in Figure 1 can therefore also be understood in first order as the field inside a conical tip as a function of its local radius. In other words, conical tips interact resonantly with light at sharply defined locations of the cone, where the local radius corresponds to one resonance of Mie theory.

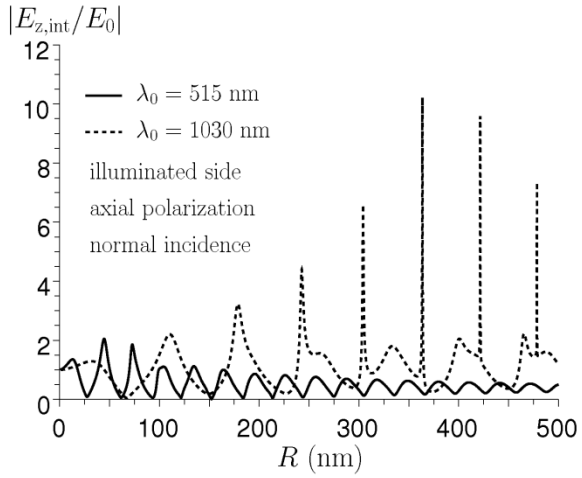


FIGURE 2. Resonance behavior of the internal electric field oriented along the symmetry axis z of a silicon cylinder of radius R illuminated with an incident electric field of amplitude E_0 and wavelengths $\lambda_0 = 515$ nm (full line) and $\lambda_0 = 1030$ nm (dotted line). The incidence (resp. polarization) is normal (resp. parallel) to the cylinder axis. The shown values are on the illuminated side.

These theoretical considerations are confirmed by Figure 2, where a Scanning Electron Microscopy (SEM) image of a silicon tip after high-fluence (~ 100 mJ/cm²) IR irradiation shows that high power illumination creates sharply localized holes in the tip at the very locations of the Mie resonances.

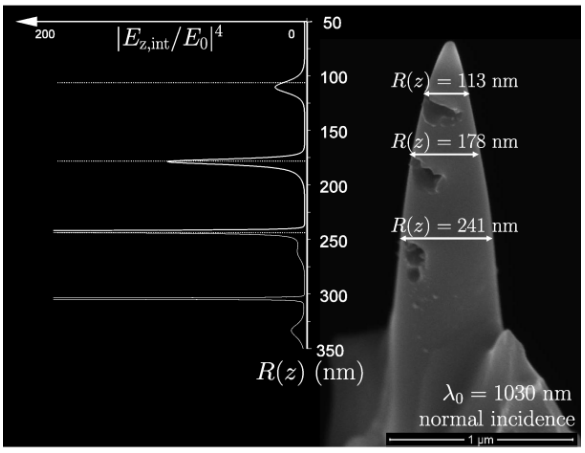


FIGURE 2. (left) Theoretical value of $|E_{z,int}|^4$ along the illuminated side of an IR-irradiated conical silicon tip with 10° cone angle as a function of the local radius $R(z)$. (right) Silicon tip irradiated with a high-fluence (~100 mJ/cm²) IR pulsed laser. Resonance absorption occurs in the cross-sections with $R(z)$ ~113, 178 and 241 nm. The tip is tilted 45° with respect to the primary beam of the SEM.

11–2

REFINED THEORY

The power of the above theory lies in its ability to explain with a simple analytical formulation the impact of a laser pulse as used in an APT experiment on the tip as a function of the basic parameters such as the laser wavelength or polarization.

However, further experimental observations seem to infer that the model should be refined. To begin with, as illustrated in Figure 3, if the cone angle is reduced, multiple holes appear in the resonant Mie cross-sections. We explain this interference phenomenon by the presence of extra waves generated by the geometrical perturbation (cylinder to cone) and propagating through the cone. Second, the one-sided shape of the holes of Figs. 2 and 3 cannot be accounted for by the proposed model, which expects multiple holes distributed along the circumference of the resonant cross-sections [18]. We therefore propose a transient absorption model where interband transitions dominate at the onset of the pulse, generating a very high concentration of excess carriers. In the course of the pulse, the intraband transitions therefore drastically increase such that they eventually dominate the absorption mechanism. Finally, the carrier/heat diffusion(less) behavior is also discussed in light of the sharpness of the holes.

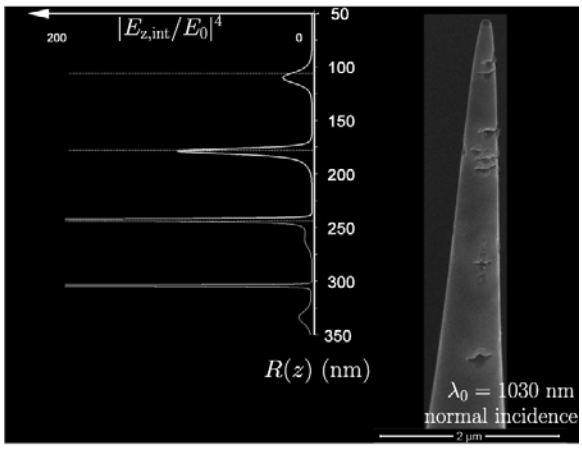


FIGURE 3. (left) Theoretical value of $|E_{z,\mathrm{int}}|^4$ along the illuminated side of an IR-irradiated conical silicon tip with 5° cone angle as a function of the local radius $R(z)$. (right) Silicon tip irradiated with a high-fluence (~100 mJ/cm²) IR pulsed laser. Multiple holes are observed in the resonant cross-sections. The tip is tilted 45° with respect to the primary beam of the SEM.

REFERENCES

1. M.K. Miller, A. Cerezo, M.G. Hetherington and G.D.W. Smith, Atom Probe Field Ion Microscopy (Oxford University Press, 1996).
2. D. Blavette, A. Bostel, J.M. Sarrau, B. Deconihout and A.Menand, Nature **363**, 432 (1993).
3. P.J. Smith and D.A. Smith, Philosophical Magazine **21**, 907 (1970).
4. R. G. Forbes, Applied Surface Science **87-88**, 1 (1995).
5. B. Gault, F. Vurpillot, A. Bostel, A. Menand, and B. Deconihout , Appl. Phys. Lett. **86**, 094101 (2005);
6. A. Cerezo, G. D. W. Smith, and P. H. Clifton, Appl. Phys. Lett. **88**, 154103 (2006)
7. F. Vurpillot, B. Gault, A. Vella, M. Bouet, and B.Deconihout, Appl. Phys. Lett. **88**, 094105 (2006).
8. A. Vella, B. Deconihout, L. Marrucci, and E. Santamato, Phys. Rev. Lett. **99**, 046103 (2007)
9. J. Houard, A. Vella, F. Vurpillot, and B. Deconihout, Appl. Phys. Lett. **94**, 121905 (2009)
10. J. Houard, A. Vella, F. Vurpillot, and B. Deconihout, Phys. Rev. B **81**, 125411 (2010)
11. J. Houard, A. Vella, F. Vurpillot, and B. Deconihout, Phys. Rev. B **84**, 033405 (2011)
12. S. Koelling, N. Innocenti, A. Schulze, M. Gilbert, A. K. Kambham, and W. Vandervorst, J. Appl. Phys. **109**, 104909 (2011)
13. S. Koelling, M.Gilbert, J. Goossens, A. Hikavyy, O. Richard, and W. Vandervorst, Surf. Interf. An. **43,** 163 (2011)
14. A. Vella, N. Sevelin-Radiguet, J. Houard, and B. Deconihout, Appl. Surf. Sci. **258**, 9202 (2012)
15. E. P. Silaeva, N. S. Shcheblanov, T. E. Itina, A. Vella, J. Houard, N. Sevelin-Radiguet, F. Vurpillot, and B. Deconihout, Appl. Phys. A, doi:10.1007/s00339-012-7189-7 (2012)
16. E. P. Silaeva, A. Vella, N. Sevelin-Radiguet, G. Matel, B. Deconihout and T. E. Itina, New J. Phys. **14**, 113026 (2012)
17. A. Vella, E. P. Silaeva, J. Houard, T. E. Itina, and B. Deconihout, Ann. Phys., doi: 10.10002/andp.201200182 (2012)

11–2

18. C. F. Bohren and D. R. Huffman, *Absorption and scattering of light by small particles* (Wiley, New York, 1983)
19. J. Bogdanowicz, M. Gilbert, N. Innocenti, S. Koelling, B. Vanderheyden, and W. Vandervorst, to be published in Opt. Express

KEYWORDS

Semiconductor materials; Absorption; Laser-Assisted

Atom Probe Tomography; Mie theory.

11–3

ATOM PROBE TOMOGRAPHY RECONSTRUCTION

D. J. Larson, B. P Geiser, T. J. Prosa & T. F. Kelly
CAMECA Instruments, Inc., 5500 Nobel Drive, Madison, WI USA 53711

INTRODUCTION

Atom probe tomography data are collected as individual ions. Data reconstruction consists of calculating 3D positions in specimen coordinates (denoted in this work as lower case xyz) from a time-series of 2D positions in detector coordinates (denoted in upper case XY). The standard reconstruction methodology [1-6] involves calculating a magnification in order to convert the detector hit positions (X and Y) into specimen-space coordinates in x and y (where x and y are contained in the plane normal to the specimen axis at the current apex position). In the small field-of-view limit, magnification (M) is considered proportional to the distance between the sample and the detector and inversely proportional to the product of the radius of curvature of the specimen, R, and the image compression factor (ICF), Figure 1, which defines the projection center and is most often treated as a single point for the entire field of view:

$$M = \frac{d}{ICF \cdot R}$$

It is generally accepted that the nominal value of the *ICF* is between one and two and, on average, its deviation from unity is due to the effects of the shank region of the specimen compressing the electric field lines inwards toward the detector (i.e., away from a simple radial projection), as shown in Figure 1. The z coordinate values are obtained by projecting to the surface of a geometrical model of the apex assuming the magnification computed above. For each reconstructed atom, the z coordinate of the spherical model is adjusted by a small increment computed by assuming that the volume of the reconstructed atom was removed uniformly from the entire apex. The z increment is also a function of a number of other instrumental and materials parameters [1, 2] such as flight-path length, *d*, detection efficiency, *ε*, detector area, *A*, and atomic volume, Ω:

$$\Delta z = \frac{\Omega d^2}{A \varepsilon ICF^2 R^2}$$

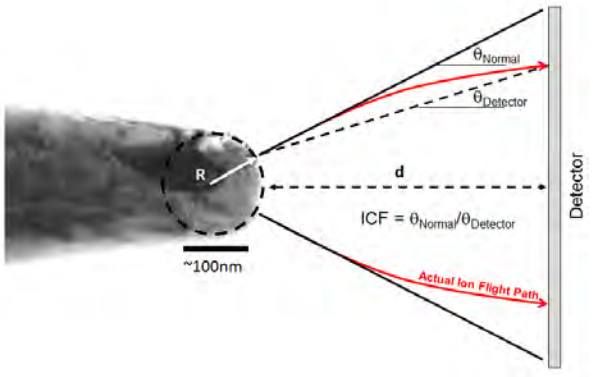


FIGURE 1. Schematic of the geometrical relationship between the tip radius, R, and the image projection factor, ICF.

Prior to the advent of wide-field-of-view instruments [7], the geometric assumptions described by Blavette [8], and later applied by Bas [1], were widely considered the standard global reconstruction technique. The Bas model assumes that the original shape of acquired volumes is small enough in lateral extent to be considered cylindrical and the radius of curvature of the specimen is determined atom-by-atom from the specimen voltage. In the early reconstructions, the shank angle was assumed to be zero in the calculation of the volume increment, although Walck published a description of specimen geometry that could be

11–3

used to compute depth increments that are appropriate for a wide field of view and included shank-angle effects [9]. These effects were later taken into account by Geiser et al. [4].

A complete review of the current state of APT reconstruction, which currently is a topic of much research within the community, is beyond the scope of the current work, but some relevant references are provided for the interested reader [2-4, 6, 10-20].

LIMITATIONS

The most common reconstruction algorithm for APT data reconstruction has two main limitations: the field evaporated surface is reconstructed as a hemispherical shape (with initial radius R0), and the atomic volume/depth increment (Δz above) is not dependent on the X or Y variables.

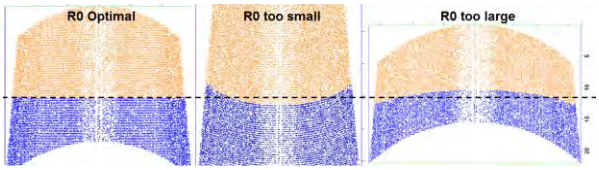


FIGURE 2. Field evaporation simulation showing the effects of intimal reconstruction radius, R0.

In Figure 2, a field evaporation simulation [21] illustrates the effects of the reconstruction radius on a simple planar interface (no evaporation field difference between the two colored regions). The accuracy of the reconstruction of the interface is obviously very sensitive to the choice of initial radius. A combination of simulated evaporated shape, simulated detector hitmap and experimental data is shown in Figure 3 for the more probable case where elements with different evaporation fields are present and the evaporated shape is non-hemispherical [16]. The resultant detector hitmap is non-uniform (Figure 3b) and experimental data of this type (Figure 3c) exhibit both types of effects observed in Figure 2.

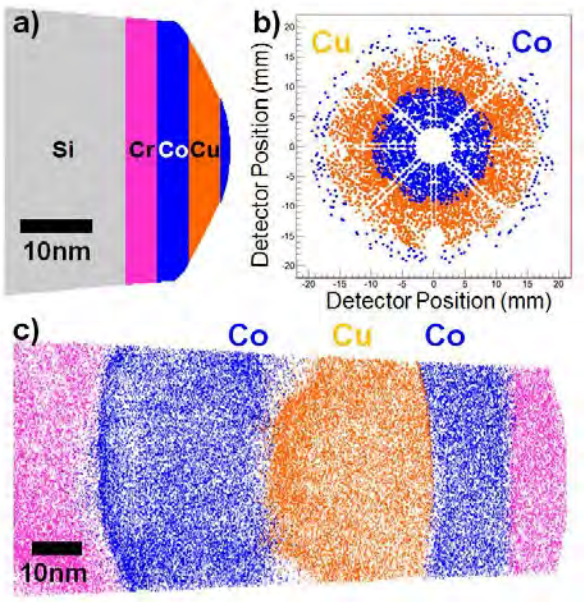


FIGURE 3. Field evaporation simulation showing (a) a non-hemispherical evaporated shape, (b) a non-uniform density detector hitmap and (c) experimental data showing the curvatures effects seen in Figure 2.

POTENTIAL SOLUTIONS

Methods to deal with these limitations include post reconstruction density correction [14, 22], methods which operate within the limits of the hemispherical projection [15, 18, 19] and methods which remove the hemispherical limitation [20] . We will briefly discuss an example of the latter type in the remainder of this abstract.

One potential method to improve reconstruction, which is not constrained by a hemispherical specimen shape or by a constant volume/depth increment across the detector, uses a field evaporation simulation to create a sequential set of transforms to map ions from detector space to specimen space [20]. The user must assume the structure to be evaporated and simulate the evaporation in order to create the transforms. Examples are shown in Figure 4 for a 1000-ion-deep slice of a low-field-on-high-field bilayer structure. The transforms provide the magnification (radial transform) and surface height position (depth transform) for any detector hit position (x axes in Figure 4). The solid lines in Figure 4

11–3

approximately indicate the results for a reconstruction which the hemispherical model.

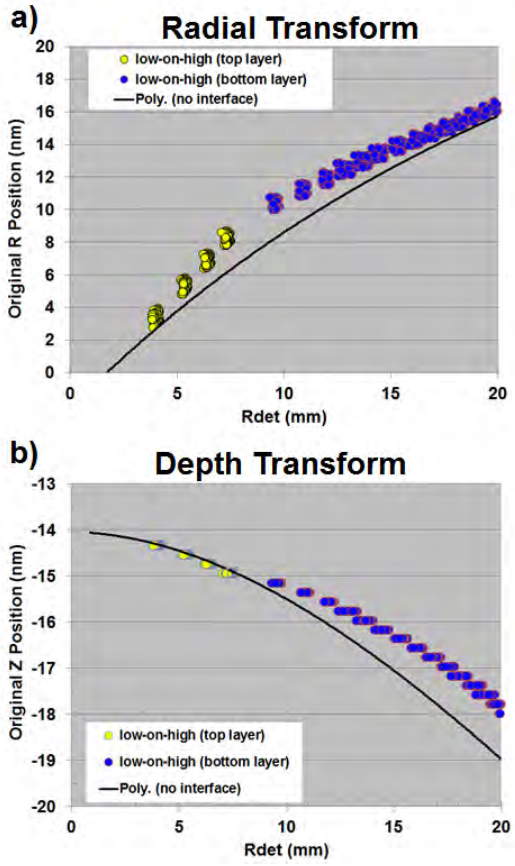


FIGURE 4. (a) Radial and (b) depth transforms for the case of a low-field-on-high-field bilayer [20].

Figure 5 compares the results for a standard reconstruction [1] and the simulation-based transform method [20] for the case of a low-field-on-high-field bilayer. The larger field of view shown at the interface position in figure 5b is indicative of the actual blunter specimen shape (lower magnification and thus larger field of view) at this point in the evaporation sequence. The result is a more accurate reconstruction which does not result in the low density region shown in the center of Figure 5a.

Application of this method both to high-on-low field and low-on-high field cases results in a mean XYZ error improvement in positioning accuracy by a factor of ~two [20]. Since we cannot accurately simulate very large radius specimens (the current simulations were performed with 20 nm radius specimens) due to computational resource constraints, we anticipate that the application of this method to experimental data will require scaling the ion sequence number by $(Rtip/Rsim)^2$. We expect to have to scale the Rorig and Zorig transfer function values by (Rtip/Rsim) and also to take into account several other standard variables such as atomic volume and detector efficiency, in order to apply this method to experimental data.

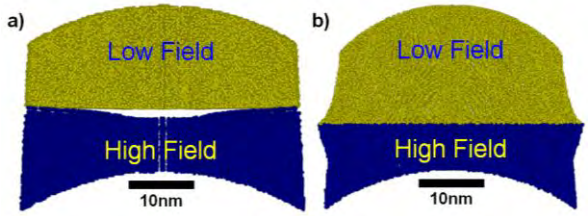


FIGURE 5. Effect of transforms on simulated data. a) conventional reconstruction and b) reconstruction using transforms of Figure 4.

KEYWORDS

Atom probe tomography, Data reconstruction

REFERENCES

[1] P. Bas, et al., Appl. Surf. Sci., **87/88** (1995) 298.
[2] B. Gault, et al., Micros. Microanal, **14** (2008) 296.
[3] B. Gault, et al., J Appl Phys, **105** (2009) 034913/1.
[4] B.P. Geiser, et al., Microsc. Microanal., **15** (2009) 292.
[5] M.K. Miller, Atom Probe Tomography: Analysis at the Atomic Level, Kluwer Academic/Plenum Publishers, New York, 2000.
[6] B. Gault, et al., Ultramicroscopy, **111** (2011) 448.
[7] T.F. Kelly, et al., Microsc. Microanal., **10** (2004) 373.
[8] D. Blavette, et al., Revue Phys. Appl., **17** (1982) 435.
[9] S.D. Walck, et al., J. de Physique, **47-C2** (1986) 451.
[10] B. Gault, et al., Microsc. Microanal., **15** (2009) 10.
[11] T.C. Petersen et. al., J Appl Phys, **105** (2009) 103518.
[12] E.A. Marquis, et al., J. Microsc., **241** (2011) 255.
[13] B. Gault, et al., Ultramicroscopy, **111** (2010) 448.
[14] F. De Geuser, et al., Surface and Interface Analysis, **39** (2007) 268.
[15] D.J. Larson, et al., J. of Microsc., **243** (2011) 15.
[16] D.J. Larson, et al., Ultramicroscopy, **111** (2011) 506.
[17] D.J. Larson, et al., Microsc. Microanal., **17** (2011) 740.
[18] F. Vurpillot, et al., Ultramicroscopy, **111** (2011) 1286.
[19] B. Gault, et al., Ultramicroscopy, **111** (2011) 1619.
[20] D.J. Larson, et al., Microsc. Microanal., **18** (2012) 953.
[21] B.P. Geiser, et al., Micros. Microanal., **15** (2009) 302.
[22] F. Vurpillot, et al., Surface and Interface Analysis, **36** (2004) 552.

11–4

NOVEL EVAPORATION CONTROL CONCEPTS AND IMAGING PART ONE: NOVEL EVAPORATION CONTROL CONCEPTS

T.J. Prosa, D.R. Lenz, T.R. Payne, E. Oltman, J.H. Bunton, R.M. Ulfig & D.J. Larson

CAMECA Instruments, Inc., 5500 Nobel Drive, Madison, WI 53711 USA

INTRODUCTION

Modern atom probes utilize some form of automated acquisition algorithm to control data collection [1]. Ideally, this automated control adjusts conditions to optimize analysis yield, data quality, and acquisition time; however, current algorithms merely utilize some form of voltage manipulation in order to maintain a desired detection rate. Presumably, the motivation for voltage control of detection rate has been 1) ease to implement, 2) maintaining a constant evaporation field for homogeneous materials, and 3) providing data of uniform data quality (data characteristics such as mass resolving power, out-of-time events, background, multi-hit probability, preferential evaporation, etc.). It is conceivable though that alternate control strategies could lead to improved performance. During this presentation we will discuss the current LEAP® evaporation control, which is representative of current commercial control algorithms, and discuss the future of acquisition control with supporting data and examples when possible.

VOLTAGE CONTROL

The basis for voltage control is illustrated in Fig. 1. Here the target detection rate is established and the voltage increases or decreases dependent on the average measured rate during some previous acquisition time window. As shown in the figure, when the target detection rate is changed from 3% to 14%, the voltage quickly increases to raise the actual rate. Note that the actual rate is not immediately achieved. The rate at which the set point is achieved and the propensity to overshoot or undershoot the target are standard issues for control algorithms. The parameterization of the LEAP control algorithm allows the user to optimize the efficiency for reaching and maintaining the set point by modifying the algorithm parameters.

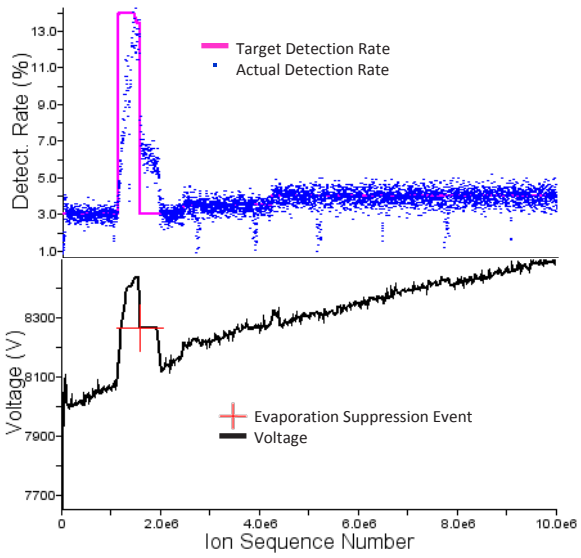


FIGURE 1. (top) Target and actual detection rate and (bottom) voltage evolution for the same 10 million detected events.

11–4

In terms of optimizing analysis yield or data quality, current algorithms are blind. They merely try to hold the evaporation process relatively constant, but this is only true for homogeneous materials. Multi-phase materials or layered structures can present widely varying local evaporation and field effects. Alternative control procedures might allow for improved yield and/or data quality dependent on acquisition information other than the detection rate.

Over time, the LEAP algorithm has evolved to include a fast response feature termed Interface Evaporation Control (IEC). When a high number of consecutive instrument pulses result in an evaporation event (for example 9 out of 10 pulses when the target rate is set for 1 out of 100 pulses) the instrument immediately lowers the voltage by some set amount. This occurrence is illustrated in Fig. 1 by the red plus sign. The idea is that highly correlated events may precede specimen failure and by quickly reducing the field, specimen failure might be avoided. Original implementations of this feature were done in software and so the response was moderately fast. Next generation implementations will move this feature to firmware to make it as fast as possible.

Constant Flux

One commonly suggested approach to improve data quality is constant evaporation flux control. Because a specimen blunts during acquisition, the imaged surface area of the specimen also increases. A number of data quality metrics (background for example) are expected to depend both on data rate and image area. By holding the evaporation rate per unit area constant (flux), one might collect data with more uniform background content.

The approach is illustrated in Fig. 2. Here a specimen analysis is started with the normal voltage control algorithm. Once 10 million ions have been collected, the specimen was slightly repositioned and constant flux mode was initiated. In this case, the basic control algorithm is still detection rate; however, a flux calculation is performed and the target data rate is adjusted to maintain a constant flux. In this example, the data rate doubles from 2% to 4% while the voltage evolves from 5 kV to 8 kV.

While this approach has the potential to improve data quality, the analysis yield is expected to decrease when compared to the standard algorithm because the data are collected at a higher average relative field. This yield danger is especially apparent for multi-layered structures. When a material is analyzed progressing from a low-field material to high-field material, the voltage is increased to accommodate. A simple constant flux algorithm would interpret the voltage increase as an increased surface area thereby reducing the flux and requiring a further increase in the target data rate to keep the flux constant—exactly the opposite approach one would take to obtain high yield through such an interface. Utilization of a constant flux algorithm for inhomogeneous materials may require user intervention or a smart algorithm that can recognize the differences in material (chemistry) and make appropriate adjustments.

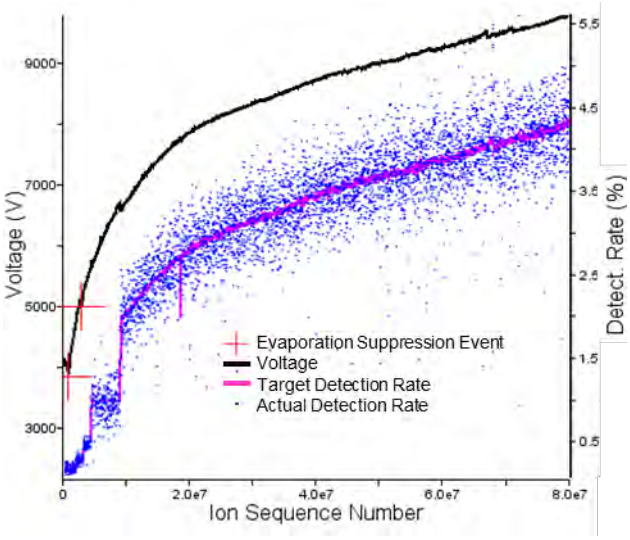


FIGURE 2. An example of evaporation control based on constant flux. Starting at ~10 million ions, the data rate is adjusted so that a constant number of ions per unit area is emitted from the imaged surface per unit time.

Constant Apex Temperature

The advent of laser-pulsed APT introduced another set of control parameters. In terms of

11–4

complexity, constant laser pulse energy is easy to implement; however, as the analysis of any APT specimen proceeds, the tip blunts, which modifies the heated volume and heat transport properties continually. This typically results in decreased apex temperatures (increasing the required evaporation field) for fixed pulse energy as the analysis proceeds. This is undesirable from both yield and data quality perspectives.

One can monitor the apex temperature indirectly by way of observed charge state ratios (CSRs) in the mass spectrum [2,3]. Laser-pulsed APT takes advantage of the fact that the required evaporation field is generally reduced as a function of increasing temperature. This reduced operating field results in increased specimen survivability (the stress on the specimen varies as the square of the field). Because the observed CSR depends strongly on the field at the time of evaporation, it provides an indication of relative apex temperatures.

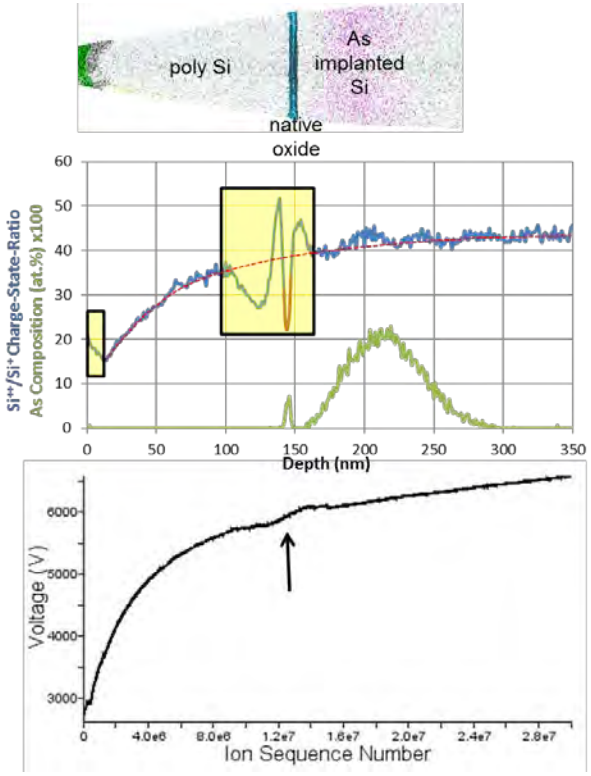


FIGURE 3. (top) An atom map showing the structure of an analyzed, capped arsenic-implanted material. The charge-state-ratio evolution (middle) and voltage evolution (bottom) are discussed in the text.

An example of CSR variation is shown in Fig. 3. The specimen is an arsenic-implanted silicon wafer that has had a 190 nm thick layer of poly-silicon and a small amount of nickel added to the surface as capping material to protect it during specimen preparation. This specimen is mostly Si, but with a layer of native oxide that is known to require significantly higher evaporation field. Using the Si++/Si+ CSR to monitor the apex temperature below the Ni cap, one observes an interesting trend. The general trend follows the dashed-red curve which is interpreted as a steady cooling of the apex temperature as the specimen blunts. The CSR during analysis through the oxide region is complex. Here, a combination of non-uniform tip shape and simultaneous analysis of two materials with differing evaporation fields makes it difficult to use the CSR as a proxy for apex temperature. As with the constant flux approach, one would need to use caution using such an approach in general to modify laser pulse energy with the goal of achieving constant apex temperature by way of CSR.

Scripted Control

It seems clear that an algorithm moving beyond simple voltage control to manipulate data rate might require utilization of multiple pieces of acquisition information. The implementation discussed here for constant flux control is a scripted algorithm. That is, the algorithm kernel is still voltage control based on data rate, but surrounding that core is a control structure (scripts) that modify the target data rate based on the logic of the control structure. This approach for adjusting the core algorithm is suitable for a smart CSR algorithm as well. A complex control structure could monitor things like local chemistry, identify interfaces or estimate local evaporation rates and adjust data rate and laser pulse energy to ensure analysis conditions that do not negatively impact yield. If done well, then this sort of approach may actually enhance yield, improve data quality, and minimize acquisition time all in an automated fashion.

11–4

References

1. M.K. Miller, *Atom Probe Tomography*, Kluwer Academic/Plenum Publishers, New York, 2000.
2. G. L. Kellogg, *J. Appl. Phys.* **52**, 5320-5326 (1981).
3. E.A. Marquis et al*., J. Appl. Phys.* **104**, 084914 (2008).

Keywords

Atom probe, instrument control, field evaporation

11–4

NOVEL EVAPORATION CONTROL CONCEPTS AND IMAGING PART TWO: IMAGING BORON IN SILICON BY FIELD ION MICROSCOPY

Matthieu Gilbert[a], Wilfried Vandervorst[a,b]

[a] *Imec, Kapeldreef 75, B-3001 Leuven, Belgium*
[b] *Instituut voor Kern- Straling fysika, K.U.Leuven, Leuven, Belgium*

INTRODUCTION

The main driving force in the micro-electronics industry is the continuous down scaling of devices which does require an accurate tuning of the electrical properties. This is usually done by controlling the amount of active impurities and their in-depth distribution. At present dopant distributions should have a depth extension of only a few nanometers with a very abrupt gradient necessitating metrology with high depth resolution.

Despite the recent developments of the laser assisted atom probe (APT) towards atomic scale 3D-characterization of semiconductor [1,2], the relatively low detection efficiency (50-60%) and the laser induced thermal atom vibrations represent a limitation to image small clusters containing only a few atoms.

In this paper we present an alternative approach based on field ion microscopy (FIM), which allows to achieve better performance than APT, as demonstrated for the case of boron in silicon. The increased performance arises from the absence of the laser interaction as well as from the fact that FIM provides images with 100% detection efficiency. The technique will only be applicable for those cases where the absence of mass information (no time of flight spectrometry) is compensated by differences in evaporation field such as the case for boron and silicon (64V/nm vs. 33V/nm, respectively). This difference provides a clear contrast between both species and allows us to demonstrate that boron atoms can be imaged in silicon without any ambiguity and that the contrast between the two can be used to collect a concentration profile.

PRINCIPLE OF FIM AND 3DFIM

The principle of field ion microscopy (FIM) is based on the field ionization of gas atoms in the proximity of atoms on a tip and their projection onto a position sensitive detector [3,4]. Typically the specimen is shaped like a tip with an end radius in the range of 50-100 nm. The sample is cooled down to cryogenic temperature in the range of 15-80K and biased at a high voltage (kV range). An imaging gas (H_2, Ne) is introduced in the analysis chamber with a pressure of about 1-2 10^{-5} mbar which becomes ionized when the electric field around the tip exceeds its field ionization value. (10-40 V/nm). The electric field at the surface of the tip varies according to the atomic roughness at the surface and hence the gas is locally ionized at atomic protrusions where the electric field is the highest. The ionized species are then projected onto a position sensitive detector leading to an image which represents a magnified view of the tip apex. The contrast within the image originates from the different amount of ionised gas atoms

11–4

originating from each position at the surface of the specimen. Higher field regions such as atomic protrusions, edges and local variations in workfunction (dopants, phases, poles,..) lead to a higher field ionisation probability and thus contrast relative to low field regions. As the magnification can be as large as ~ 1 million, atomic resolution within the image becomes accessible [3,4].

Whereas originally FIM provided a static image of the tip surface, recently the concept of 3D-FIM was proposed [5]. The principle is to record consecutive FIM images as a movie during dynamic FIM whereby conditions are chosen such that also atoms from the sample are evaporated. Within the assumption that this can be viewed as the consecutive removal of individual atomic layers, each image within the movie provides information on a deeper lying layer and thus can be used to construct a depth profile of the sample. In order to obtain a 3D-representaion of the analysed volume, a stacking algorithm were used whereby the depth increment is calculated assuming a constant evaporation rate, taking into account the curvature of the tip for a flattening of the surface (as the hemispherical surface is projected onto a flat detector).

RESULTS

To demonstrate the capabilities of dynamic FIM and to validate the reconstruction algorithm, a sample containing boron delta layers separated with 3 nm silicon was investigated. This structure was covered with 100 nm of silicon as a cap layer to protect the structure during specimen preparation with the focused ionbeam [6]. The sample was measured using hydrogen as imaging gas and was cooled down to 80 K. Boron atoms are seen on the detector as bright spots and hence brightness filters can be used to identify their location. Figure 1a shows a typical FIM image of the tip surface containing B-atoms. The dashed circle marks the position of a series of large, bright spots representative for the Boron atoms within the delta layer. When the successive pictures recorded during the analysis are piled up into one 3D-volume, the B distribution within delta layers is revealed (figure 1b). The representation can be further refined by a flattening of the curvature through the reconstruction process leading to a clear identification of the Boron delta layers (figure 1c).

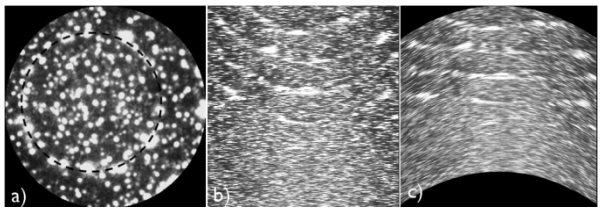


FIGURE 1. FIM picture of boron delta layers in silicon. A) image as recorded by the detector (black circle through large white spots indicates the position of the B-atoms from delta layer); b) cross sectional view of stacked images showing the delta layers (lines with bright contrast); c) cross sectional view after reconstruction and flattening of the layers.

Within the present investigation we rely on the assumption of a constant field of view within the microscope and thus a constant magnification for all pixels. In that case it's easy to link the number of bright pixels with the number of boron atoms on the surface and hence to determine its concentration based on the variation in brightness.

Using the known silicon thicknesses between each delta layer as depth calibration one derive a depth increment 0.0135 nm/picture and the brightness variation as concentration variation, one can compare the FIM-based B-profile with SIMS (O^{2+} with an energy impact of 250eV) and Atom Probe data as shown in figure 2. The apparent discrepancy with SIMS is very interesting and indicative for the different sensitivity to the sample roughness for SIMS vs APT en FIM as a result of their very different sampling area. When the same delta layer structure without the rough cap is analysed, a close agreement between SIMS and APT is obtained.

The depth resolution appears to be much better in FIM than in atom probe because in Atom Probe, the depth resolution of the boron delta layers is decreased due to the field evaporation differences between Si and B leading to local magnification effect [7]. Although such artifacts would also be expected for FIM measurements, their effect can be less as in FIM, surface atoms are imaged by the gas atoms created **above** the surface and **before** the

11–4

Boron atoms leave the surface, while in AP the image corresponds to the B-atoms evaporated **from** the sample surface making them more sensitive to trajectory aberrations in the reconstruction and hence also in the depth profile.

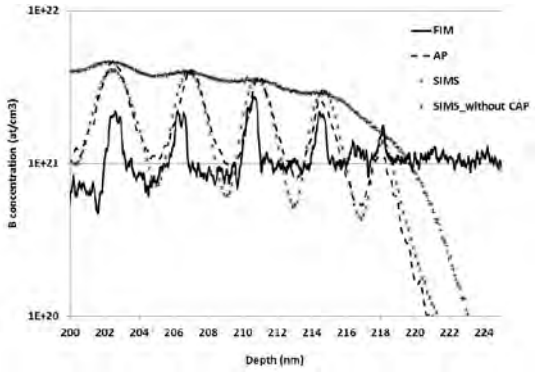


FIGURE 2. B profiles as measured with SIMS, APT and extracted from FIM brightness depth profiles. The SIMS profile for the sample with cap layer is extensively broadened by the surface roughness.

Looking closely at the concentration profiles we observe that the FIM profile is not yet fully quantitative. A more refined algorithm for converting the brightness variations will be necessary. Moreover one cannot exclude that at high concentrations, two large bright spots merge and will be considered as due to one individual B-atom.

Finally, an important point to consider is the sensitivity of the brightness profiles. At present the profiles show sensitivity orders of magnitude lower than APT. This can be partially explained by the limited encoding of the brightness levels (ranging from 0-255) which limits the sensitivity. The overall background in the image corresponds at present to a concentration of about 1E21 at/cm^3. This high background value is determined by the evaporation rate (the evaporation rate varies with the electric field) and the imaging gas used in this experiment. This is still very far from the theoretical limit : assuming a single boron atom on the surface could be identified and since the total number of atoms present on the surface is theoretically close to 10^5, a detection limit should be in the range of 5E17 in silicon. Optimization of the contrast interpretation and background noise will be necessary to reach that target.

CONCLUSION

It has been shown that 3D field ion microscopy can be performed on semiconductor materials and provides results with superior depth resolution as compared to SIMS and APT. The imaging process relies on differences in field evaporation which are characteristic for the elements contained in the sample. In the case of boron atoms in silicon, we have demonstrated that boron atoms (high field evaporation species) could easily be separated from Si atoms and that their position can be identified. Assigning brightness variations to concentration variations, and using a dedicated reconstruction algorithm, it was possible to compare the brightness profile with the SIMS profile. The results indicate a superior depth resolution versus SIMS (in particular in the case of rough samples) but equally well outperform APT profiles. An improvement of the data quality and reduction of the bckground, requires more intense studies on the influence of the operating parameters (base temperature, imaging gas, laser field assisted evaporation), more refined reconstruction and filtering algorithms.

REFERENCES

1. S.Koelling, M.Gilbert, J.Goossens, A. Hikavyy, O.Richard and W.Vadervorst, Surface and Interface Analalysis (2010).
2. T.Philippe, S.Duguay, D.Blavette, Ultramicroscopy,vol 110, issue 7, (2010), 862-865.
3. M. Miller, A. Cerezo, M. Hetherington, and G. Smith, Atom Probe Field Ion Microscopy, Oxford, 1996.
4. T.T.Tsong, Atom Probe Field Ion Microscopy, Field emission and surfaces and interfaces at atomic resolution, Cambridge university press 1990.
5. F.Vurpillot, M.Gilbert and B.Deconihout, Surf. Interface Anal. 2007; 39: 273–277.
6. D.J.Larson, M.K.Miller, R.M.Ulfig, R.J.Matyi, P.P.Camus, T.T.Kelly, Ultramicroscopy 73 (1998) pp. 273-278.
7. E.Cadel, F.Vurpillot, R.Larde, S.Duguay, and B.Deconihout, J.Appl. Phys. 106, 044908 (2009).

KEYWORDS

Field ion microscopy, imaging boron, depth profile.

11–5

QUANTIFYING PERFORMANCE

Karen Henry[1] and Wilfried Vandervorst[2]

[1]*Intel*

[2]*IMEC*

Abstract not available at time of press.

TH–01

COMPLEMENTARY METHODOLOGIES FOR THIN FILM CHARACTERIZATION IN ONE TOOL – A NOVEL INSTRUMENTATION FOR 450 MM WAFERS

Ina Holfelder[1], Philipp Hönicke[1], Andreas Nutsch[1,2], Burkhard Beckhoff[1]

[1]*Physikalisch-Technische Bundesanstalt, Abbestr 2-12, 10587, Berlin, Germany*

[2]*previously Fraunhofer IISB, Schottkystrasse 10, 91058 Erlangen, Germany*

INTRODUCTION

The scaling down of critical dimensions for the manufacturing of nanoelectronics demands for the continuous introduction of new materials. The request for validation, assurance, and support materials analysis results using differing analytical methods is driving the integration of multiple methods into one tool. This paper shows the success of complementary metrology and proposes an integrated metrology approach for reliable characterization of structure and composition.

CHARACTERIZATION OF THIN HIGH-K LAYERS USING VARIOUS METHODS AND LABORATORIES

Samples, previously designed as reference samples, were employed for demonstration of the success of complementary metrology. The substrates were silicon wafers with diameters of 100 mm. Plasma Assisted Atomic Layer Deposition (PA-ALD) was used to create Al_2O_3 layers on silicon. A formation of a SiO_2 layer between the Si substrate and the high-k layer is expected. The root cause is most likely the cleaning and transfer process prior to deposition. In addition, the formation of a very thin hydrocarbon surface layer is to be expected. The root cause for this layer is most likely surface contamination from the environment.

For thin layer characterization, probably the most challenging issue is figuring out the mass deposition which is the product of thickness and density, also representing electron densities for scattering. As there are several solutions providing similar results, the identification of the appropriate material parameters at a specific energy and the corresponding thickness demand for the use of an approach using more than one analytical technique.

The ellipsometry measurements were performed using a Woollam M-2000DI rotating compensator spectroscopic ellipsometer. The X-Ray Reflectivity measurements were performed with an X'Pert pro MRD from Panalytical with CuKα excitation. The Grazing Incidence X-Ray Fluorescence measurements were performed using an Atomika 8300W with WLβ excitation and in the PTB laboratory at BESSY, where a plane grating monochromator beamline provides high spectral

TH–01

purity and high photon flux in the photon energy range from 78 eV to 1.86 keV.

The layer thicknesses and material parameters validated by several analytical techniques demonstrate the successes of the use of complementary metrology. (see Figure 1)

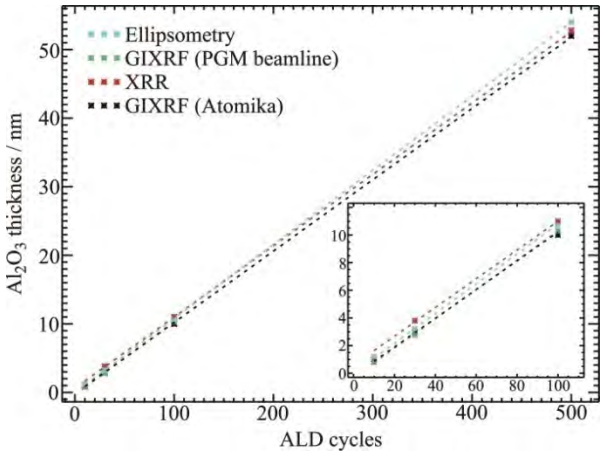


FIGURE 1. Complementary analysis of Al_2O_3 layers on silicon with varying thicknesses. The determined thicknesses of X-Ray Reflectivity (XRR), Total Reflection, as well as Grazing Incidence X-Ray Fluorescence (TXRF or GIXRF) and Ellipsometry are in accordance with each other.

The goal of this approach was to achieve reliable and reproducible results using various excitation energies and analytical techniques. This is a challenge when taking into account that the selection of material parameters at different excitation energies has a considerable impact on the evaluated results.

The measurements show an accordance of the thicknesses determined by the analytical techniques and at different laboratories. But one should keep in mind that open issues remain, such as the description of the surface contamination by water and an appropriate model for the interfaces. Currently, the achieved results are in accordance but the use of additional analytical techniques e.g. chemical analysis of the surface and the interface, is expected to explain the differences in the results and observed offsets. This has not been performed yet.

Design of the 450 mm Metrology Platform

For the analysis of surfaces and materials, light sources in different spectral ranges, e.g. X-rays or infrared light, are used for diffraction, scattering or excitation of fluorescence. The use of appropriate detectors in scattering, or fluorescence geometry is indispensable. Highly precise metrology demands accurate positioning of the sample with respect to the sources and the detectors. The handling unit for samples and the automation are main contributors to the semiconductor metrology equipment cost. For this reason, the approach of integration of multiple analytical techniques has advantages with respect to cost aspects and handling steps. Affording high quality analysis for 450 mm wafers, a design study of the 450 mm analytical platform was performed. This design study integrates seven complementary analytical methods into one metrology chamber. Five methods rely on X-ray characterization methods, such as Total Reflection X-Ray Fluorescence Analysis (TXRF), Grazing Incidence X-Ray Fluorescence Analysis (GIXRF/XRF), X-Ray Reflectometry (XRR), X-Ray Diffractometry (XRD), and Grazing Incidence Small Angle X-Ray Scatterometry (GISAXS). Furthermore, the two methods of spectroscopic ellipsometry and vacuum UV reflectometry using the spectral range of ultra-violet to infrared were supplemented. A novel 5-axis positioning system was designed and patented enabling integration of all analytical methods into one chamber under vacuum or atmospheric conditions.

The goal of the design study was to highlight all aspects, e.g. economic and scientific, of the design and realization of a metrology platform for wafers with a diameter of 450 mm. The criteria studied are

- analytical performance of the methods, which includes the determination of structural and compositional information including material parameters of surfaces on wafers with a diameter of 450 mm
- complementarity of the analytical techniques, which means the usage of different analytical

techniques to assess the surface for improve of reliability and traceability of the results

- tool performance (e.g. spatial resolution, measurement speed, mechanical components)
- costs

Based on these criteria the above discussed different analytical techniques were analyzed and benchmarked (see Table 1) and the design of the metrology platform was performed.

Heart of the metrology platform is a patented stage enabling the integration of all these techniques in approx. 1 m^2 footprint (see Figure 2).

FIGURE 2. CAD model of the analytical platform for 450 mm wafers (design study)

TABLE 1. Overview on application, specification, measurement time and estimated cost for the in the metrology platform integrated analytical techniques.

Method	Application	Spatial resolution	Acquisition time	Strenght of the method	Costs per Method
TXRF	elemental (B-U) contamination	1mm^2 / 1cm^2	50 s – 1000 s / point	highest sensitivity on smooth surfaces	~ 300 k€
GIXRF / XRF	depth profiling, nanolayer analysis	0.5 mm^2 / 1cm^2	100 s – 5 h / point	depth sensitivity	~ 300 k€
XRR	layer thickness	to 1 mm^2	1000 s – 5 h / point	nanolayer characterization	~ 300 k€
XRD	crystal structure	0.5 mm^2 / 1cm^2	1000 s – 5 h/ point	lattice constant / stochiometry	~ 300 k€
GISAXS	nanostructures	0.5 mm^2 / 1cm^2	10 min / frame	particle size distribution	~ 600 k€
Ellipsometry	layer thickness, optical constants	35 µm × 35 µm	10 s / 1 min / point	fast layer characterization	~ 300 k€
Vacuum UV Reflectrometry	layer thickness	3 mm - 50 µm	3s-10s /point	fast nanolayer characterization	~ 500 k€

ACKNOWLEDGEMENTS

This work was partially supported by the European Commission and BMBF under the FP 7 ENIAC Initiative EEMI 450 contract no. 13N10988 and the European Commission under the FP6 Program through the Integrated Infrastructure Initiative “ANNA”, contract no. 026134-RII3

REFERENCES

1. A. Nutsch, M. Lemberger, P. Petrik,, AIP Conf Proc 1395 (2011) 193-197

TH–02

Soft X-ray Characterization of DSA Block Copolymers

Daniel Sunday, Wen-Li Wu, R. Joseph Kline

National Institute of Standards and Technology (NIST), Gaithersburg MD

Introduction

One of the greatest challenges facing the semiconductor industry in the next decade is the patterning of sub 10 nm features for integrated circuit components. The fundamental limitations on feature sizes patterned with traditional optical lithography, coupled with the slow development of an EUV source of sufficient intensity, have pushed the semiconductor industry to consider alternative technologies.[1] The directed self assembly (DSA) of block copolymers (BCP) is being explored as a supplement approach to be used in concert with existing technologies. In DSA a chemical template is patterned on a surface (typically through the use of e-beam or liftoff techniques) and a BCP with a smaller, but commensurate, pitch is assembled on top of that template. The contrast in affinities between the BCP components and the template components drives the BCP to register with the underlying pattern and amplify it significantly.[2] This BCP layer is then used as an etch mask to transfer the patterned features into the underlying substrate. Careful control over the final shape of the BCP components is necessary to enable the process to reach the level of precision and consistency required by the semiconductor industry. There are a wide variety of factors which will influence the BCP shape. For example enhanced affinity of one component for the substrate or surface will lead to enrichment of the attracted component in that region and depletion throughout the remainder of the film, resulting in a strain on the interface which may lead to both distortions in the interfacial profile and enhanced roughness.[3] These competing interactions will lead to complex features that need to be characterized and their origins understood in order to gain improved control over the assembly process and subsequent etch steps. This will be impossible without a reliable method for in-situ characterization of patterned BCPs. To this end we have developed a variation on the small angle scattering technique which is capable of resolving the detailed interfacial structure of DSA BCPs.

CD-SAXS and Soft X-rays

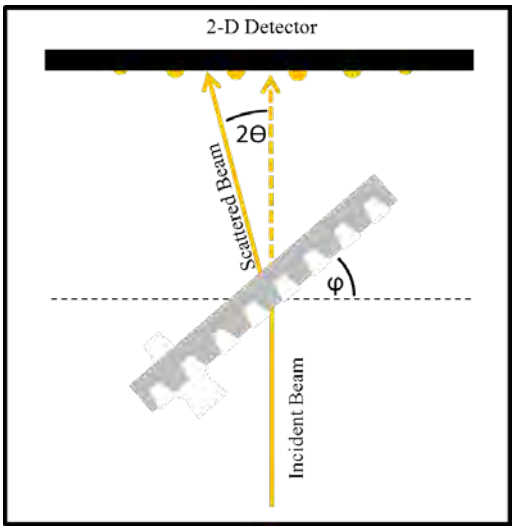


FIGURE 1. CD-SAXS geometry, the sample angle (φ) is rotated around normal incidence, changing the q space explored by the scattering.

Critical-dimension SAXS (CD-SAXS) is a measurement technique where a periodic

TH–02

nanostructure is placed on a rotation stage and measurements are taken over a range of sample angles, the measurement geometry is shown in Figure 1. Rotating the sample allows information about both the vertical and horizontal composition profiles to be obtained from the scattering pattern.[4] The images taken at individual angles are reconstructed into a 2-D scattering map which can be fit using an inverse approach to provide detailed information on the nanostructure shape. This technique has been shown to be successful at evaluating complex line-gratings consisting primarily of etched silicon. The obstacle to adapting this technique for measurements of BCP's lies in the extremely poor contrast between the organic components. This may be overcome by using soft x-rays near an atomic absorption edge where the contrast becomes chemical bond specific and may be tuned through careful control over the incident energy.[5] We will show that by using soft x-rays for the CD-SAXS measurement we can reconstruct detailed structural information from the scattering profile.

BCP Interfacial Profile Characterization

A series of BCP's consisting of PS-PMMA were assembled on templates patterned with an E-beam.[6] These samples were delaminated and placed on SiN windows in order to conduct the measurement. Measurements were taken using both hard (17 KeV) and soft (282 eV) x-rays in order to demonstrate the improvement in contrast obtained with the soft x-ray version of CD-SAXS. The hard x-ray measurements resulted in up to the fifth order diffraction peak being observed, whereas the soft x-ray measurements result in diffraction peaks up to the 10th order. These higher order peaks are critical for effectively defining detailed features in the BCP shape, as they reduce the uncertainty associated with the inverse fitting approach (where the uncertainty is determined with a Monte-Carlo Markov Chain (MCMC) sampling algorithm). Examples of the BCP shape obtained from the hard and soft x-ray measurements are presented in Figure 2. The features associated with the hard x-ray measurements result in a high degree of uncertainty, particularly around the substrate and the surface, two areas critical to the etch process. The fits obtained from the soft x-ray measurements result in extremely low uncertainties, resulting from the additional higher order peaks. The outlined structure shows the shape of the PMMA block, being the stronger scattered in both measurements. We observe an enrichment of PMMA around the substrate, whereas the PS was enriched near the surface. The strain induced by this component distribution results in the width oscillation seen in the profile, where the PMMA layer expands until it reaches an inflection point around a height of 20nm and then contracts as it approaches the surface. In addition to the interfacial profile observed, this measurement provides information on the sidewall roughness by measuring the rate of decay in the scattering intensity. This roughness measurement contains contributions from both the line edge and line width roughness.

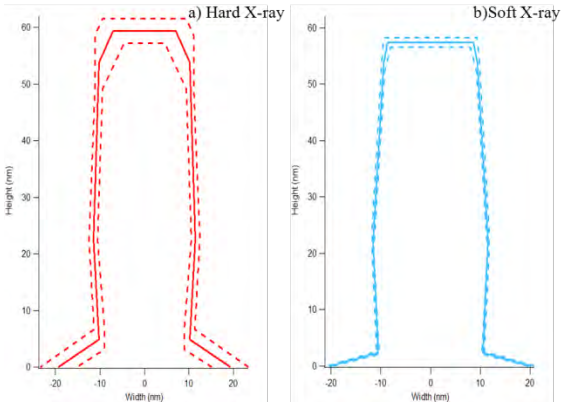


FIGURE 2. Examples of interfacial profiles determined from soft X-ray CD-SAXS with both hard and soft x-rays. Solid lines represent best fit to scattering pattern, dashed lines represent 95% confidence intervals.

References

1. The International Technology Roadmap for Semiconductors. (http://www.itrs.net/, 2011).

TH–02

2. Edwards, E. W., Montague, M. F., Solak, H. H., Hawker, C. J. & Nealey, P. F. *Advanced Materials* **16**, 1315–1319 (2004).
3. Wang, Q., Nath, S. K., Graham, M. D., Nealey, P. F. & de Pablo, J. J. *The Journal of Chemical Physics* **112**, 9996-10010 (2000).
4. Hu, T. et al. *Journal of Applied Physics* **96**, 1983 - 1988(2004).
5. Wang, C. et al. *Nano Letters* **11**, 3906–3911 (2011).
6. Stein, G. E., Liddle, J. A., Aquila, A. L. & Gullikson, E. M. *Macromolecules* **43**, 433–441 (2010).

KEYWORDS

DSA, Block Copolymers, X-ray, Soft X-ray

TH–03

HAXPES For Non-Destructive Analysis of Chemistry at Buried Interfaces In Advanced Gate Stacks

Paul Risterucci[1], Eugénie Martinez[1], Rachid Boujamaa[2], Jörg Zegenhagen[3], Blanka Detlefs[3], Mickael Gros-Jean[2], Catherine Dubourdieu[4] and Olivier Renault[1]

[1]CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France.
[2]STMicroelectronics, 850 rue Jean Monnet, Crolles 38926, France.
[3]European Synchrotron Radiation Facility, 6 rue Jules Horowitz, Grenoble F-38000, France.
[4]LMGP, CNRS, Grenoble INP, 3 parvis L. Néel, BP 257, Grenoble 38016, France.

INTRODUCTION

Non-destructive analysis of the chemistry at buried interfaces is of prime importance in nanoelectronics and an important new field in photoelectron spectroscopy (XPS). This is addressed by the recently developed HAXPES (HArd X-ray PhotoElectron Spectroscopy) technique. This tool is now available at 3rd generation synchrotron radiation storage rings with high-energy excitations ranging from 2 to 20 keV and high kinetic energy (<15keV) electrostatic electron analyzers. The development of HAXPES paved the way to non-destructive characterization of gate stacks in technologically relevant conditions without any kind of sample preparation that would modify the buried interfaces. This enables the development and optimization of advanced devices with a higher reliability. Current improvements are aimed at further increasing the depth sensitivity. This is highlighted here by the analysis of high-k/metal gate stacks with increasing thicknesses of the top metal gate.

EXPERIMENTAL

GATE STACK SAMPLES

The studied samples were prepared in a gate-first integration process on 300 mm Si(100) wafers. After a HF-SC1 clean, a thin SiON interfacial layer (IL) was formed by oxidation of the silicon substrate with in-situ steam generation (ISSG) at 1025°C, followed by decoupled plasma nitridation (DPN) and post nitridation anneal (PNA). Then, a 1.7 nm-thick HfSiON film was deposited by metal organic chemical vapor deposition of HfSiO followed by DPN and PNA and finally, the sample was capped with a LaO_x layer by physical vapor deposition (PVD). Two LaO_x thicknesses were investigated: 0.4 and 1.0 nm, referenced as La04 and La10, respectively. The metal gate stack was composed of a 6.5 nm TiN film deposited by PVD followed by a 30 or 50 nm-thick amorphous Si (a-Si) film deposited using chemical vapor deposition (CVD) with a maximum thermal budget of 600°C. Figure 1 shows the final multi-layer stack. Reference samples without LaO_x capping layers (La00) were also prepared. To simulate the

TH–03

transistor fabrication process, high temperature activation annealing was performed at 1065°C under N2 for 1.5 s on some wafers. Such a thermal budget leads to the crystallization of a-Si into polycrystalline silicon (Poly-Si). HAXPES measurements were performed with and without this top Si layer. In the latter case, the Si top layer was chemically removed with tetramethyl ammonium hydroxide (TMAH).

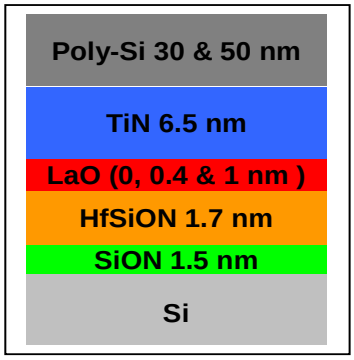


FIGURE 1. Schematic of the Poly-Si/TiN/LaO_x/HfSiON/SiON/Si stacks (La00: x = 0 nm; La04: x = 0.4 nm; La10: x = 1.0 nm).

HAXPES ANALYSIS CONDITIONS

HAXPES measurements were performed at the undulator beamline ID32 at the European Synchrotron Radiation Facility (ESRF, Grenoble, France) using photon energies ranging from 3.81 to 18 keV. Photoelectrons were detected at a take-off angle of 80° with respect to the sample surface (i.e., close to normal emission). An overall energy resolution of 0.3 eV was achieved at low energy (3.81 keV) with the help of a high resolution Si (311) double crystal post-monochromator and a SPECS PHOIBOS 225 high resolution photoelectron spectrometer [1]. The energy resolution was less good (< 4 eV) to the benefit of higher count rate at higher photon energies (12, 15 and 18 keV).

GATE STACKS WITH TIN

The high-k/metal gate stacks were first studied after removal of the top Si layer, i. e. with a 6.5 nm-thick TiN metal gate. Then the effect of the insertion of a LaO_x thin capping layer was investigated. These HAXPES measurements were performed at 3.81 keV. Diffusion of Lanthanum towards the underlying layers is expected after high temperature annealing [2]. Related changes regarding the high-k/Si chemistry are visible in the silicon core level spectra. As the Si 2*p* and La 4*d* lines overlap, the Si 1s core level is more appropriate for analyzing the chemistry of the buried layers and interfaces. Figure2 shows the Si 1s core level spectra obtained for the annealed samples as a function of LaOx thickness.

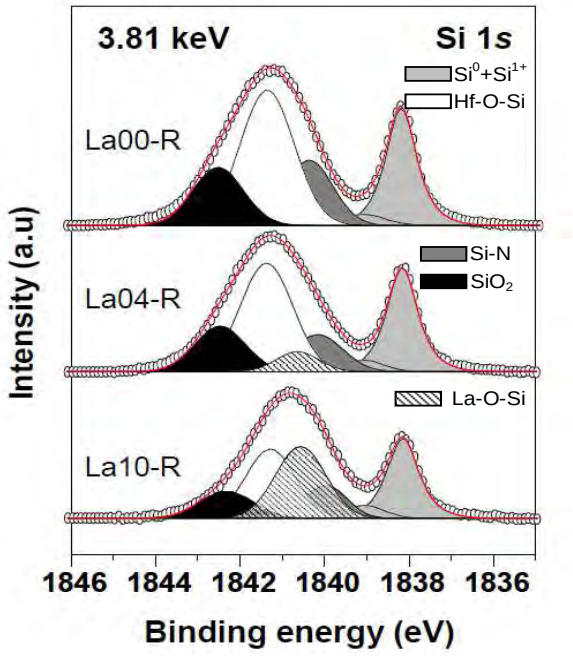


FIGURE 2. HAXPES Si 1s core level spectra measured for the TiN/LaO_x/HfSiON/SiON/Si stacks after spike anneal at 1065°C with a photon energy of 3.81 keV (La00-R: x = 0 nm; La04-R: x = 0.4 nm; La10-R: x = 1.0 nm).

All the spectra were fitted with Gaussian peaks after a Shirley-type background subtraction. The bulk Si^0 1s substrate emission is located at a binding energy of 1838.2 eV. In a previous paper [2], we showed that the Si 1s core level spectra can be deconvoluted with different components attributed to silicates, sub-oxides and nitride states. They are identified, for the reference sample without LaOx, with their

TH–03

chemical shift relative to the bulk silicon Si^0: i) Si^{1+} (+0.9 eV), ii) Si-N ((+2.2 eV), iii) Si^{3+} in Hf silicate oxinitride (+3.3 eV) and iv) Si^{4+} in SiO_2 (+4.4 eV). After insertion of La into the gate stacks, an additional component appears at an energy shift of 2.6 eV relative to the bulk Si^0. This new component is ascribed to La-O-Si bonds[3] and its amplitude exhibits a clear enhancement after spike anneal as the LaO_x thickness increases from 0.4 to 1.0 nm. Concomitantly, we observe a decrease of the SiO_2 component, indicating a shrinking of the interfacial layer with increasing LaO_x thickness. Consequently, these results show that formation of La silicate occurs during the 1065°C spike anneal as a result of La diffusion into the high-k and SiON interfacial layers.

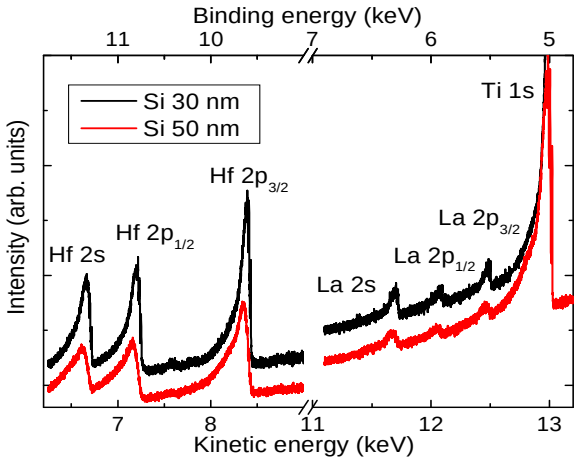


FIGURE 3. HAXPES survey spectra measured at 18 keV for 30 and 50 nm-thick poly-Si capping layers.

GATE STACKS WITH TIN / POLY-SI

The high-k/metal gate stacks were then studied with the full top metal gate, i. e. including 30 or 50 nm layers of Si. Only the gate stacks including the 1 nm-thick LaO_x layer were analyzed, before annealing. The first objective was to test the capabilities of HAXPES, in terms of counting rate and depth sensitivity. Wide-range XPS spectra were recorded at different photon energies (12, 15 and 18 keV) selected as to increase gradually the sampling depth.

Figure 3 shows HAXPES spectra measured at 18 keV for 30 and 50 nm-thick poly-Si capping layers. Good counting statistics was obtained despite the drastic decrease of photoelectric cross-sections. The Ti 1s peak is detected in both cases, thus indicating that the depth sensitivity is sufficient to probe the buried TiN layer. Both spectra exhibit core levels from buried elements such as Hf (Hf 2p and 2s) and La (La 2p and 2s) with satisfying intensity. A non-destructive analysis of ultra thin buried layers and interfaces is still possible through a very-thick top layer (36.5 or 56.5 nm). This is a clear demonstration of the capabilities of HAXPES in terms of bulk sensitivity and a real advantage for artefacts-free results on technologically relevant structures.

CONCLUSION

We highlight here the capabilities of HAXPES for non-destructive and accurate analysis of advanced high-k/ metal gate stacks. The chemistry of the high-k/Si interface was investigated after LaO_x insertion. A demonstration of the in-depth sensitivity was also done by working at high excitation energies (up to 18 keV). Ultra thin (1 nm) layers buried under more than 50 nm-thick top metal gates were successfully analyzed.

This work was partially supported by the European EUREKA/CATRENE program in the frame of the CT206 UTTERMOST project. We gratefully acknowledge technical support at ID32 by Helena Isern and Lionel André.

REFERENCES

1. J. Zegenhagen et al., *J. Electron Spectrosc. Relat. Phenom* **178**, 258 (2010).
2. R. Boujamaa et al., *J. of Appl. Phys.* **111**, 054110 (2012).
3. K. Kakushima et al., *Appl. Surf. Sci.*. **254**, 6106 (2008).

KEYWORDS

HAXPES, high-k/metal gate stacks, capping layers, La

TH–04

Withdrawn

TH–05

CHARGE-BASED CAPACITANCE MEASUREMENTS CIRCUITS FOR INTERFACE WITH ATOMIC FORCE MICROSCOPE PROBES[1]

Joseph Kopanski, M. Yaqub Afridi, Chong Jiang, Michael Lorek, Timothy Kohler, and Curt A. Richter

Semiconductor and Dimensional Metrology Division
National Institute of Standards and Technology
100 Bureau Dr., stop 8120
Gaithersburg, MD 20899-8120 USA

INTRODUCTION

An essential metrology for emerging nanoelectronic devices and their constitute materials is the measurement of their electrical characteristics and properties[1]. Devices or material test structures can be connected to bonding pads and electrically contacted via mechanical probes or wire bonded into packages. This conventional approach requires quality device contacts, additional processing overhead, and devotion of a large proportion of the device substrate to bonding pads (usually on the order of 50 μm x 50 μm each), especially if statistical data on a large number of devices is required. Bonding pads also introduce large capacitances (≈ 100 fF) relative to the device capacitances, distorting device characteristics and complicating interpretation. An alternative approach has been to directly access the device with a conducting atomic force microscope (AFM) probe and utilize techniques such as conducting AFM (c-AFM) for current-voltage and resistance measurements, various implementations of Kelvin force microscopy for surface potential measurements, and scanning capacitance microscopy (SCM) for local capacitance-voltage measurements. Using an AFM tip as a local and mobile probe of electrical properties is largely non-destructive, allows partially processed devices to be measured, and allows probing device substructures that are not otherwise directly accessible.

We have invested considerable effort into improving SPM based tools for this kind of in-vivo electrical characterization of nanoelectronic devices and materials. In previous workshops, we have reported on SCM for dopant profiling [1], optimization of Kelvin force microscopy for surface potential measurements [2], and the development of carbon nanotube (CNT) terminated tips for improved spatial resolution. SCM has proven a convenient technique for qualitative capacitance measurements. Quantitative extraction of two-dimensional dopant profiles is dependent on a good physical model of the SCM measurement and knowledge of the semiconductor material being imaged. True quantitative capacitance measurements at the nanoscale prove more difficult. The small capacitances to be measured can be swamped by the stray capacitance of probes and wires. The small values can be below the resolution of even the best integrated capacitance meters. For these reasons, we are pursuing the charge based capacitance measurement (CBCM) technique [4] because it is highly sensitive to small

[1] Official contributions by the National Institute of Standards and Technology are not subject to copyright.

TABLE 1. CBCM Configurations available on the test chip.

Type of Device	Reference Branch Capacitors (Area)	Measurement Branch Capacitors (Area)	Notes
1. Basic CBCM circuit	None	MOS (16 to 1600 λ^2)	Large range
2. CBCM with bias control	None	MOS (16 to 1600 λ^2)	with bias control
3. CBCM with bias control	None	None	"SCM on a Chip"
4. CBCM with bias control	MOS (16 to 1600 λ^2)	MOS (16 to 1600 λ^2)	balanced branches
5. CBCM with bias control	MOS (all 144 λ^2)	MOS (100 to 182 λ^2)	Medium capacitors
6. CBCM with bias control	MOS (all 1406 λ^2)	MOS (1260 to 1681 λ^2)	Large capacitors
7. Basic CBCM circuit	Metal-metal (16 λ^2)	Metal-metal (16 to 44 λ^2)	Small capacitors

capacitances and capable integration onto an AFM tip, thereby reducing stray and wire capacitance to the bare minimum. The CBCM technique has previous been applied to the measurement of metal-to-metal capacitance in back end of the line (BEOL) multi-level metal interconnect processes [4]. Usually, these devices are integrated on the same chip as the devices to be measured, with either a single CBCM per device, or a multiplexer interfacing multiple devices with a single CBCM circuit.

The goal of this work is to interface a single CBCM circuit interfaced with an AFM tip, providing a mobile capacitance meter with unparalleled probe placement precision and high accuracy, quantitative capacitance measurement capability.

CHARGE BASED CAPACITANCE MEASUREMENT (CBCM)

The charge based capacitance measurement (CBCM) was original developed to measure the capacitance between metal levels on an integrated circuit [4]. The CBCM circuit contains two branches, a measurement branch and a reference branch. The measurement branch contains the device under test (DUT) and all the wiring needed to make connections. The reference branch contains the same wiring, but not the DUT. By comparing the current in the two branches, the capacitance of the DUT can be extracted from the stray capacitance of the wiring. Each branch contains two gates; one of which is gated on when the DUT is charged, but is gated off when the device is discharged. A current meter in series with the DUT will only see the average charging current and hence measure a net dc current, I_{avg}, which is proportional to the DUT capacitance, C_m, applied dc voltage, V_{dd}, and the ac measurement frequency, f:

$$C_m = \frac{I_{avg}}{V_{dd} f}$$

Our devices are based on a refined CBCM design using transmission gates [5] and additional circuitry to enable a dc bias on the capacitor under test [6].

The concepts of this work have been tested using three custom integrated circuits fabricated by the MOSIS design service. Chip 1 consisted of series of small MOS and metal-insulator-metal capacitors accessible by both traditional probe stations and

TH–05

AFM probes [7]. This chip provided a convenient vehicle to compare traditional capacitance meters and probe based capacitance measurements. Chip 2, the subject of this paper, consists of various implementations of CBCM circuits and integrated test capacitors. Chip 3, under design, consists of metal-to-metal test structures implemented in the interconnect metal that provide arrays of calculable capacitances, electric fields, and magnetic fields. These structures will allow us to precisely calibrate the CBCM circuits on devices without bonding pad contacts. The CBCM test chip consists of eight series of CBCM circuits, briefly described in Table 1. Devices were chosen to cover capacitances ranging from around 200 aF to 1 pF. Series 3 takes both the reference branch and measurement branch of the CBCM circuit out to bonding pads. These devices will be connected through a differential amplifier to test different methods of interfacing the CBCM with an AFM tip to form an "SCM on a Chip."

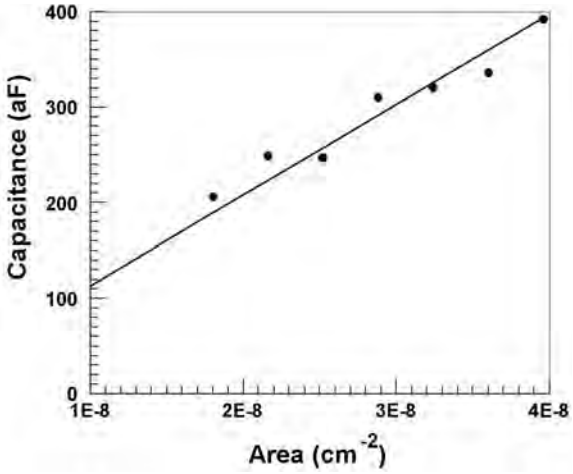


FIGURE 1. Capacitance extracted from CBCM current-voltage measurements of the metal-to-metal capacitances (series 7) on the test chip.

RESULTS

The metal-to-metal devices, series 7 from Table 1, present the most challenging set of capacitance measurements on the test chip. Capacitances for these 7 devices were extracted by measuring the current-voltage characteristics with a dc bias voltage from 2 to 5 V and a gate switching frequency of 1 MHz. Reproducibility of extracted capacitance was within 20 aF for the seven devices, with some small changes with switching frequency and switching waveform shape. Figure 1 shows the average capacitance values for the 7 devices plotted versus the area of the metal-to-metal capacitors. The plotted line is the theoretical capacitance value calculated using an assumed intermetal low k dielectric constant of 2.4 and the extracted dielectric thickness of 224 nm. Additional measurements on the MOS devices are underway.

Chong Jiang, Michael Lorek, and Timothy Kohler were summer undergraduate research fellows (SURF) sponsored by an NSF REU grant.

References

1. J. J. Kopanski, J. F. Marchiando, J. Albers, and B. G. Rennex, Characterization and Metrology for ULSI Technology, D. G. Seiler, A. C. Diebold, W. M. Bullis, T. J. Shaffner, R. McDonald, and E. J. Walters, Eds. (AIP, New York, 1998), pp. 725-729.
2. J. J. Kopanski, P. McClure, and V. Mancevski, Frontiers of Characterization and Metrology for Nanoelectronics, D. G. Seiler, A. C. Diebold, R. McDonald, C. M. Garner, D. Herr, R. P. Khosla and E. M. Secula Eds. (AIP, New York, 2009), pp. 212-216.
3. J. J. Kopanski, I. Sitnitsky, V. Vartanian, P. McClure, and V. Mancevski, Frontiers of Characterization and Metrology for Nanoelectronics, D. G. Seiler, A. C. Diebold, R. McDonald, A. Chabli, and E. M. Secula Eds. (AIP, New York, 2011), pp. 123-127.
4. J. C. Chen, B. W. McGaughy, D. Sylvester, C. Hu, *Proc. IEEE IEDM*, 1996, pp. 69-72.
5. L. Vendrame, L. Bortesi, A. Bogliolo, *Proc. 7th IEEE Signal Propagation on Interconnects Workshop* (Sienna, Italy, 2003).
6. T. Sutory and Z. Kolka, *Proc. 1st Intl Conf Mixed Design*, (Ciechocinek, Poland, 2007), pp. 501-505.
7. C. A. Richter, J. J. Kopanski, C. Jiang, Y. Wang, M. Y. Afridi, X Zhu, D.E. Ionnou, and Q. Li. Frontiers of Characterization and Metrology for Nanoelectronics, D. G. Seiler, A. C. Diebold, R. McDonald, C. M. Garner, D. Herr, R. P. Khosla and E. M. Secula Eds. (AIP, New York, 2009), pp. 328-332.

KEYWORDS

AFM-based capacitance measurement, CBCM, Charge cased capacitance measurement, C-V measurements, Electrical characterization

TH–06

VIBRATING SAMPLE MAGNETOMETRY STUDY OF HIGH-PERMEABILITY DIELECTRICS ON NANOMAGNETS

Peng Li[1], Gyorgy Csaba[1], Michael Niemier[2], X. Sharon Hu[2], Joseph J. Nahas[2], Wolfgang Porod[1], and Gary H. Bernstein[1]

1 Center for Nano Science and Technology, Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, USA

2 Department of Computer Science and Engineering, University of Notre Dame, Notre Dame, IN 46556, USA

INTRODUCTION

Nanomagnet logic (NML) is a novel paradigm to realize low power, non-volatile digital logic[1]. Low-power operation is the most important benefit of NML, as calculations show that if 10^{10} magnets switch 10^8 times/s, the power dissipation from switching of magnets[2] is expected to be ~0.1 W. NML operation relies on magnetic ordering; to initiate this process, hard-axis fields are required to place the magnets into a metastable state for re-evaluation. Figure 1 shows a possible way to use on-chip, field-generating wires and yokes to generate this field[3]. Resistive losses in the wires are the dominant power dissipation source in this scheme. In order to achieve low-power NML operation, magnets should switch at the lowest possible fields. Pietambaram, *et al*. showed that switching fields of magnetic random access memory (MRAM) elements could be lowered if covered by enhanced permeability dielectric (EPD) films[4]; the EPD concentrates the external field, and thus decreases the required current needed to switch an MRAM cell. This suggests that EPDs can be used to reduce the clock energy associated with NML circuit elements as well. However, the geometries and the switching modes of nanomagnets are different in NML than in MRAM, so we seek to understand how EPDs will affect NML devices when subjected to hard axis fields. This study is based on the work in reference 5.

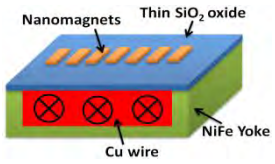


FIGURE 1. Schematic of clock circuitry.

EXPERIMENT

To understand the behaviors of both standalone and coupled nanomagnet elements, we fabricated two samples using high-resolution electron-beam lithography, followed by metal deposition and lift-off. Samples 1 and 2 are composed of standalone and coupled nanomagnets, respectively, with dimensions 60 nm × 120 nm × 20 nm. About 10^7 nanomagnets were prepared in each sample in order to achieve the minimum volume of magnetic material that can be measured using a Microsense vibrating sample magnetometer (VSM)[6]. Fig. 2 shows the layouts of (a) standalone and (b) paired (coupled) nanomagnets, as well as scanning electron microscope (SEM) images of both samples (c, d). In order to avoid interactions, the patterns in both samples are placed more than 600 nm apart, as shown in the SEM images.

The EPD films are a dielectric (MgO) matrix with embedded nanometer-size CoFe particles. Fig. 3(a) shows a scanning transmission electron microscope (STEM) image of a single CoFe layer, which is an aggregate of discrete particles (the dark spots in the

TH–06

image) with diameters of 5 nm ±1 nm. Fig. 3(b) is a magnetization curve that confirms the superparamagnetic (hysteresis-free) characteristics of the EPD films.

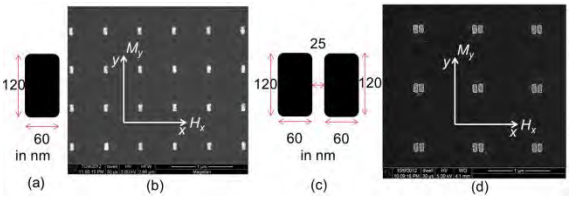


FIGURE 2. Details of structures in simulations and experiments. (a) layout of one magnetic unit of sample 1. (b) SEM of sample 1. (c) Layout of one unit of sample 2. (d) SEM of sample 2.

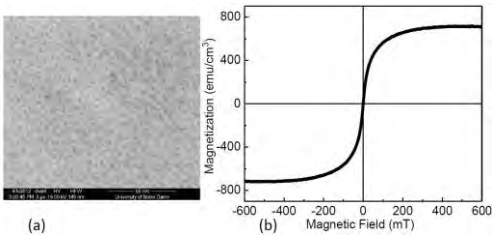


FIGURE 3. Characterization results of EPD films. (a) STEM image of a CoFe layer. (b) Magnetization curve.

In the clocking process of NML, a hard-axis directed field, i.e., nulling clock field, is applied to place magnets into the metastable state; in this case, easy-axis (y) magnetization of the magnets is zero (M_y =0; see Fig. 2(b)(d) for directions). By monitoring the magnetization in the easy-axis (y) of the nanomagnets while sweeping a hard-axis (x) external field, an M_y vs. H_x curve can be measured, thus the nulling clock field can be read from the curve. Such measurements can be secured by the vector coils in the Microsense VSM[6,7].

M_y vs. H_x curves not only provide the most relevant information for the clock operation, but also it is the most straightforward to measure, as the M_y component comes solely from the nanomagnets, and the EPD films provide no magnetization component vertical to the applied field.

All M_y vs. H_x curves are measured as described below. First, we magnetize the sample along the easy axis (y) with a 1 T field. Then, starting from zero, we gradually apply an external field along the hard axis of the magnets along the positive x-direction (stopping at 200 mT). Then we sweep the field in the opposite direction to -200 mT.

RESULTS AND DISCUSSION

Switching Behavior Of Nanomagnets With No EPD Films

OOMMF[8] was used to help illustrate the switching processes of nanomagnets in our arrays. The magnets in the simulations have rounded corners that best approximate the shapes of the fabricated magnets. Fig. 4(a) shows the switching curves of both standalone and coupled magnets. Magnetization states appear in the insets. For the standalone case (Figs. 2(a) and 2(b)), after the array is magnetized along the y axis, the magnets have a strong M_y component (stage A); with an increasing hard-axis field in the positive x-direction, M_y gradually decreases, and when the field reaches 160 mT, all of the magnetization points right, and M_y =0 (stage B). When the field sweeps back to zero, the magnets turn up or down randomly, so M_y remains at zero (stage C). Finally, when the field is increased in the negative x-direction (toward -200 mT), the magnetization states of the devices in the array point left, and M_y stays at zero.

The switching process of the coupled magnets is similar to that of the standalone case. However, the coupling field between the two magnets is another field component driving them toward the hard-axis direction, and reduces their net switching fields. This is reflected in the slopes of the curves. In addition, when the external field is zero (stage C), the magnetization of the two coupled magnets are aligned antiferromagnetically.

Figure 4(b) shows the experimental magnetization along the easy axis normalized to the nominal nanomagnet volume. The experimental data agree well with the simulations regarding the clock fields at which the magnetization goes to zero (i.e., the minimum field required to null the magnets), as well as the slopes of the curves. The starting M_y values are slightly lower than the values in the simulations. A likely cause is that the volume of the fabricated nanomagnets is not precisely known, and also the end domain states of the magnets strongly depend on their shapes, which

TH–06

cannot be controlled perfectly in the fabrication process.

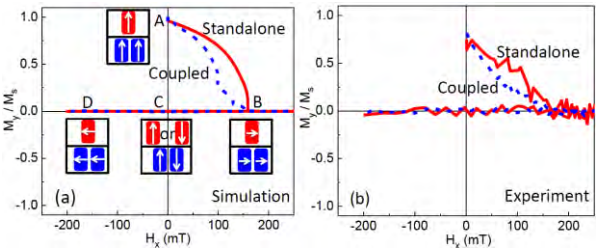


FIGURE 4. M_y vs. H_x curves of nanomagnets with no EPD films. (a) Simulated curves. The insets demonstrate the states of standalone and coupled magnets at different fields. (b) Experimental curves.

Switching Behavior Of Nanomagnets With EPD Films

After the samples are covered with EPD films, the nanomagnets switch at much lower fields. Fig. 5 shows experimental M_y vs. H_x curves for both standalone and coupled magnets. For the standalone case, the EPD films have lowered the nulling clock field from 160 mT to 65 mT (~60% reduction). Note that the remanent values of M_y are the same before and after the deposition of the EPD films, which echoes previous experiments[9]. This confirms that EPDs do not add any residual background magnetic bias to the NML switching characteristics. The same trend is seen in the sample of coupled magnets, where the nulling clock field decreases to 40 mT from 160 mT, a 75% reduction. This indicates that EPD films may not only reduce the switching fields of magnets, but also modify the coupling field between them. Work to understand the effect of EPD films on the coupling fields is in progress.

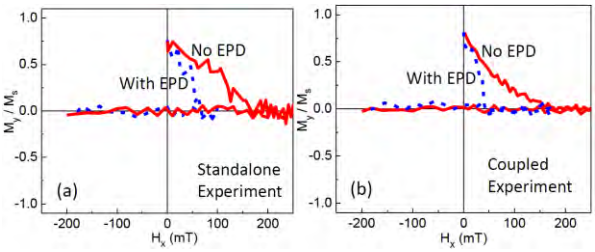


FIGURE 5. Experimental M_y vs. H_x curves of nanomagnets. (a) Standalone magnet sample (1) with and without EPD films. (b) Coupled magnet sample (2) with and without EPD films.

We have investigated the effect of EPD films on the switching behaviors of standalone and coupled magnets. This is the first-of-its-kind measurement to test the effect of EPD films on the nulling clock field in nanomagnet logic. The experimental results have shown that EPD films reduce the nulling clock fields of standalone and coupled magnets by 60% and 75%, respectively. The 75% reduction in switching field translates to a potential 94% reduction in NML power consumption. Moreover, the remanent magnetization of the nanomagnets is unchanged by the addition of EPDs, which suggests that EPDs do not contribute undesirable remanence to the NML circuit.

References

1. A. Imre, G. Csaba, L. Ji, A. Orlov, G. H. Bernstein and W. Porod, *Science* **311**, 205-208 (2006).
2. G. Csaba, A. Imre, G. H. Bernstein, W. Porod, and V. Metlushko, *IEEE Trans. Nanotechnol.*, **1**, 209-213 (2002).
3. M. T. Alam, M. Siddiq, G.H. Bernstein, M. Niemier, W. Porod, and X. S. Hu, *IEEE Trans. Nanotechnol.*, **9**, 348-351 (2010).
4. S. V. Pietambaram, N. D. Rizzo, R. W. Dave, J. Goggin, K. Smith, J. M. Slaughter, and S. Tehrani, *Appl. Phys. Lett.*, **90**, 143510-143510-3 (2007).
5. P. Li, G. Csaba, M. Niemier, X. S. Hu, J. Nahas, W. Porod, and G. H. Bernstein, *J. Appl. Phys.*, under review, 2012.
6. [Online]. Available: http://www.microsense.net/products-vsm-accessories.htm
7. P. Li, G. Csaba, V. Sankar, X. Ju, E. Varga, P. Lugli, X. S. Hu, M. Niemier, W. Porod, and G. H. Bernstein, *IEEE Trans. Magn.*, **48**, 4402-4405 (2010).
8. M. J. Donahue and D. G. Porter, OOMMF User's Guide (National Institute of Standards and Technology, Gaithersburg, MD, 1999), Interagency Rep. NISTIR 6376.
9. P. Li, G. Csaba, V. K. Sankar, X. S. Hu, M. Niemier, W. Porod, and G. H. Bernstein, *Proc. Device Research Conf.*, 129-130 (2012).

Keywords

Vibrating sample magnetometry, nanomagnets, nanomagnet logic, high permeability dielectrics

TH–07

PORE SIZE EVALUATION OF LOW-*K* THIN FILMS BY USING X-RAY POROSIMETRY

Yong-Qing Chang, Bo-Ching He, Hsin-Chia Ho and Wei-En Fu*

Center for Measurement Standards, Industrial Technology Research Institute
321, Sec.2, Kuangfu Rd., Hsinchu, 30011, Taiwan

INTRODUCTION

Successful fabrication of future generations of integrated circuits demands materials with lower dielectric constant k values to decrease cross talk and RC delay. Introduction of micropores (>2 nm) by desorption of organic molecules from a dense $Si0_2$ matrix achieves dielectric constant values as low as 2.05 but also decreases mechanical strength [1,2]. Silicon dioxide (SiO_2) has been the interlayer dielectric in the inter-connect of integrated circuits. However, the dielectric constant of SiO_2 cannot sufficiently prevent cross talk between closely spaced copper wires in the latest generation of semiconductor devices. To address this problem, materials with lower dielectric constants (low-k) are being developed [3,4]. State-of-the-art nonporous low-k dielectric materials typically have k values ranging from 2.6 to 3.0 while retaining mechanical strength, but these need to be further reduced to 2.2 or below in the next few years [5,6] according to 2011 ITRS low-k road map. Therefore determining the pore size and pore size distribution (PSD) of these thin films is key to optimizing the processing conditions for implementation in the future device generations [7]. By using X-ray reflectivity combined with the mass flow control system, porosity and pore size distributions can be derived non-destructively. Compared with TEM and SAXS (Small angle X-ray scattering), the so-called X-ray porosimetry is easier, faster and reproducible.

X-RAY POROSIMETRY COMBINED WITH MASS FLOW CONTROL SYSTEM

The refractive index of X-rays is slightly less than unity, giving rise to total external reflection (TER) in angles less than the critical angle of the film. Description of the refractive index with respect to depth, z, is given by (1),

$$n(z) \approx 1 - \frac{2\pi r_e}{k^2}\rho_e(z) - i\frac{\lambda u(z)}{4\pi} = 1 - \delta - i\beta \quad (1)$$

where r_e is the classical electron radius, k is the wave vector in the z-direction, $\rho_e(z)$ is the electron density, λ is the X-ray wavelength and u(z) is the absorption coefficient [2].

Due to the porous structure of porous thin films, the refractive index of thin films would change after trapping toluene molecule substances in the pores. At grazing incidence angles and small wave vector transfer, X-ray probes are sensitive to the electron density profile of the thin film system. The electron density of the thin film and substrate are determined by the critical angles via [8], as (2) below

$$\theta_c = \lambda\sqrt{\frac{r_e\rho_e}{\pi}} \quad (2)$$

Combined with the X-ray reflectivity and the mass flow control system, from the air and toluene-saturated conditions, one can calculate the total amount of toluene adsorbed [8] by,

$$\rho_{film} = \rho_w(1 - P) + \rho_{toluene} * P \quad (3)$$

TH–07

Here, ρ_{film} is the average density of the film under toluene/air vapor ratio, ρ_{wall} is the density of the wall material between the pores, P is the porosity of the saturated film, $\rho_{toluene}$ is the mass density of the condensed toluene ~0.865 g/cm^3 at 20 °C.

After curve fitting of a series of ρ_{film} with Gauss function simulation, the fitting result of the individual film density v.s. specific vapor ratio is defined. Converting vapor ratio into pore size through Kelvin's equation, as below

$$r_c = -\frac{2V_m r}{RT}\frac{1}{\ln(P/P_0)} \quad (4)$$

Based on Eq. (4), the pore size distribution is obtained.

EXPERIMENTAL DETAILS

The overall system consists of a main X-Ray Reflectivity (XRR) goniometer, a rapid heating plate (Anton Paar DHS 1100), a mass flow control equipment (1000 sccm in total), N_2 carrier gas, a sealed sample stage with X-ray windows made of Kapton polymers, a pump, and a spectrometer (with a DUV-UV source) to quantify the toluene/air ratio.

The low-k SiO_2 sample was first held at 400 °C (based on NIST Webbook, [9]) for 10 min to remove the remained toluene and other impurities in the pores. The rapid heating process was performed on the Domed Hot Stage (DHS 1100, Anton Paar). The heating rate is 200 °C/min, and the cooling rate is 60 °C/min in air ambiences.

The reflectivity measurements were later performed on a Philips X'Pert PRO MRD Reflectivity/Diffractometer with a designed sealed chamber of Kapton X-ray windows. A metal-ceramic Cu Long Fine Focus X-ray tube set to 45 kV and 40 mA was used for the generation of X-rays. The incident and reflected X-ray beams were conditioned using an X-ray mirror and a parallel plate collimator.

At the beginning of measurements, the 100 sccm air flow filled in the sealed chamber with carrier gas N_2 to perform the alignment procedure. For the following variant vapor ratio of toluene to air, 30 sec of pumping and ventilation needs to execute to reduce and restore the chamber pressure to 1 atm. Vapor ratio of 3 % for each interval was stabilized for 3 minutes to reach equilibrium. The steps were repeated until the film is toluene saturated, i.e. no changes on critical angles of films.

TABLE 1. Mass density changes with vapor ratio applied.

Vapor ratio (% toluene)	Mass density (g/cm3)	Vapor ratio (% toluene)	Mass density (g/cm3)
0.00	1.050	0.15	1.210
0.03	1.070	0.18	1.276
0.06	1.070	0.21	1.330
0.09	1.101	0.24	1.390
0.12	1.167	0.27	1.400

TH–07

Results And Discussions

Figure 1 shows the reflectivity spectrum of porous thin films with a increment of 3 % of toluene to air ratio. With increasing toluene molecules absorbed in the films, the average film density is increasing as well, as shown in Table 1. The original plot shows the increasing critical angles from ~ 0.14° to ~0.167°. The average film density curve was obtained by X-ray software based on the algorithm of global solutions. In this work, Gauss function was used for the density curve fitting since the pores were assumed to be isolated and uniformly distributed for the physical vapor deposited (PVD) film. The X-ray analysis software analyzed the film based on a three layer model (SiO_2/SiOCH/SiOCH).

Figure 2 indicates the main pore size is 13 Å derived from Gauss function simulation of series of film density values based on the toluene adsorption experimental results. The pore size was converted by Kelvin's equation to replace the vapor ratio. Meanwhile, the porosity was obtained as 38% ~ 40% on film saturation state, as the equation (5) below.

$$P\,\% = \frac{\rho_{sat} - \rho_{air}}{\rho_{toluene}} * 100\% \qquad (5)$$

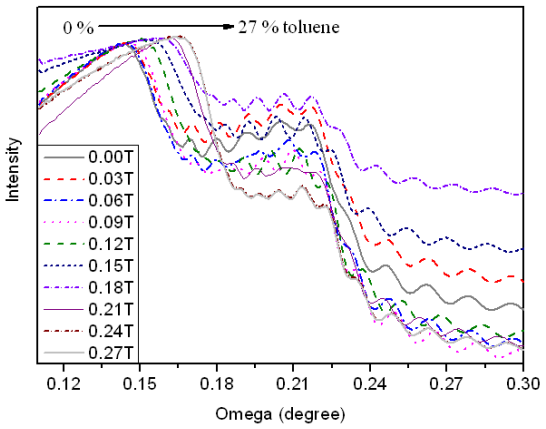


FIGURE 1. The toluene adsorption curves of porous thin films from 0.00% to 0.27% (saturated).

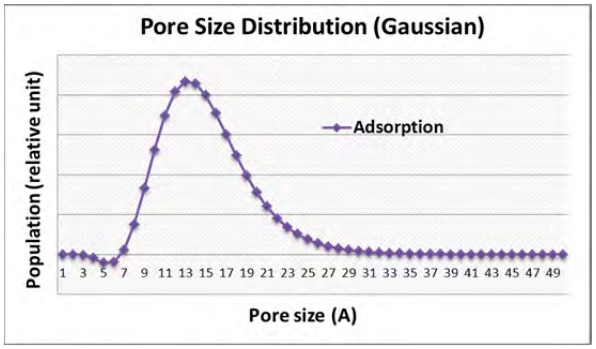


FIGURE 2. The pore size distribution of porous thin films based on Gauss curve fitting and Kelvin's equation conversion.

Conclusions

The porosity and the pore size distribution of porous low-k thin films were analyzed under the combined apparatus of the XRR and mass flow control system. The main pore size was obtained as 13 Å in diameter based on the results of Gauss function curve fittings. The porosity was around 38% ~ 40% under toluene saturated adsorption of the film.

References

1. A. Grill and V. Patel, J. Appl. Phys., **94**, 3427-3435 (2003).
2. C. M. Settens and V. K. Kamineni, AIP Conf. Proc., **1173**, pp. 163-167 (2009).
3. M. Morgen and E. T. Ryan, Rev. Mater. Sci. **30**, 645 (2000).
4. A. Grill and D. Edelstein, Advanced Metallization Conference 2001 (AMC 2001) (Materials Research Society, Warrendale, PA, 2001) , p.253.
5. H. J. Lee and E. K. Lin, Chem. Mater. **14**, 1845 (2002).
6. A. Grill and V. Patel, Appl. Phys. Lett. **79**, 803 (2001).
7. Hae-Jeong Lee and Christopher L. Soles, J. Appl. Phys., **95**, No. 5 (2004).
8. Hae-Jeong Lee and Christopher L. Soles, J. Appl. Phys. **100**, 064104 (2006).
9. NIST Webbook: http://webbook.nist.gov/cgi/cbook.cgi?ID=C108883&Mask=4

Keywords

X-ray reflectivity, pore size distribution, porosity, thin films

TH–08

New Experiments and Applications Made Possible by a Low Temperature 4-Tip STM with UHV-SEM Navigation

Andreas Bettac, Berndt Guenther, Juergen Koeble, Fred Henn and Albrecht Feltz

Omicron NanoTechnology GmbH, Limburger Str. 75, D-65232 Taunusstein, GERMANY

Introduction

A major challenge in the development of novel devices in nano- and molecular electronics is their interconnection with larger scale electrical circuits required to control and characterize their functional properties. Local electrical probing by multiple probes with STM precision can significantly improve efficiency in analyzing individual nano-electronic devices without the need of a full electrical integration [Ref. 1-7]. Recently we developed a new microscope stage that merges the requirements of a SEM navigated 4-probe STM and at the same time satisfies the needs for high performance SPM at low temperatures.

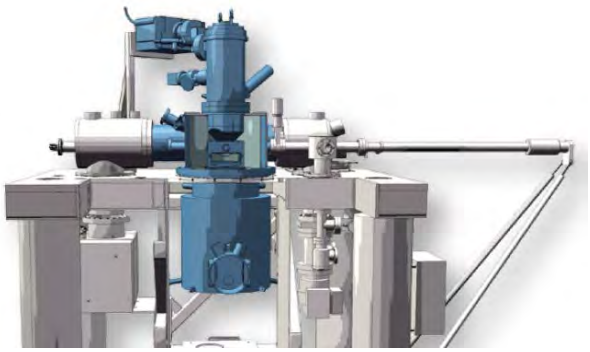


FIGURE 1. Schematic showing the low temperature 4-tip STM (LT NANOPROBE) concept. LHe/LN2 bath cryostats at the bottom, SEM column at the top.

SEM imaging and tip navigation

For the navigation of four independent STM probes, simultaneous SEM imaging is indispensable to bridge dimensions from the mm- down to the nm-scale. The SEM enables a large field of view for probe coarse positioning as well as fine positioning and rapid localization of small structures with its high resolution capabilities. As a suitable tool for that purpose, the UHV Gemini column offers unsurpassed resolution under true UHV conditions. In combination with the Low Temperature UHV NANOPROBE, the in-lens Secondary Electron Detector (SED) represents a key advantage.

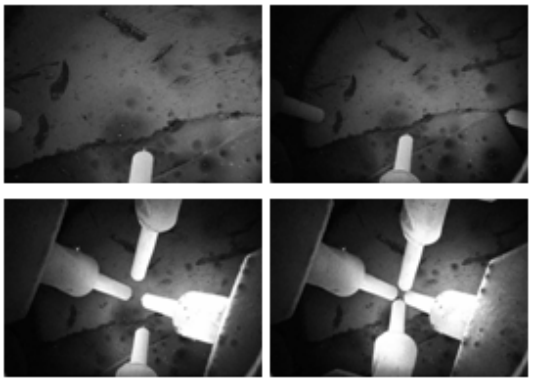


FIGURE 2. Sequence of SEM images taken at T < 5 K. Coarse positioning of the four STM probes under SEM navigation.

TH–08

Only one small access port in the thermal shield compartment of the microscope stage (at T <5 K) is needed, thus minimizing thermal impact, while still offering a suitable signal for high resolution SEM imaging.

THE MICROSCOPE STAGE

Cooling the whole microscope to LHe temperatures requires an extremely compact stage with only 100x100 mm in size - a real challenge if 4 STMs need to be fully functional, independent and highly stable.

An efficient thermal shield compartment allows for temperatures well below 5 K, extremely low thermal drift and thermal equilibrium of sample and probes. In addition, the integration of high resolution SEM navigation requires a small SEM working distance and thus makes a dedicated STM concept indispensable. A sophisticated shared stack scanner allows for a very compact and flat design, while ensuring highly linear, orthogonal and stable STM scanning characteristics. For sophisticated STM measurements, like dI/dV spectroscopy, the microscope stage employs an effective eddy current damped spring suspension.

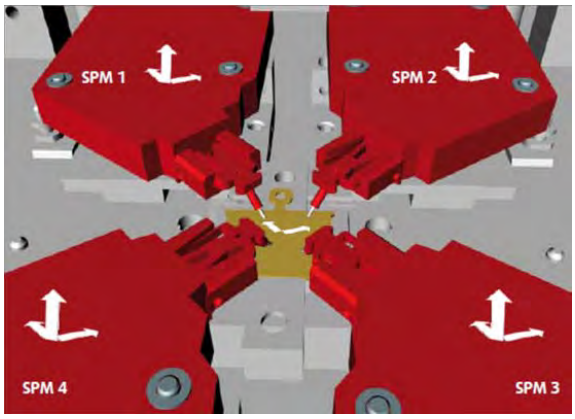


FIGURE 3. Schematic showing the four dedicated and independent STM modules.

The microscope stage carries four individual SPM modules with independent and guided 3D coarse positioning of XYZ = 5x5x3 mm. The sample can be independently positioned by XY = 4x4 mm. Fine positioning and STM imaging with atomic resolution is achieved by shared stack scanners with XY=1x1 µm scan range at LHe temperatures. A fast and secure tip and sample exchange is crucial for ease of use and high throughput: individual probe modules are moved to a tip exchange position and spring loaded tip carriers can easily be exchanged by wobble-stick.

FIRST RESULTS: 4-PROBE MEASUREMENTS AND STM PERFORMANCE

STM is the key to advancing probing technology into the nanometer scale. It ensures extremely accurate probe positioning and STM-based safe tip approach of fragile probe tips having diameters in the range of a few ten´s of nanometers or less. STM imaging is required for final precise positioning of the probe tip when it shadows nm-sized structures in the SEM field of view or if the structures are even smaller than accessible by SEM.

All four STM modules of the LT NANOPROBE are designed to achieve atomic resolution on metal surfaces with pm stability and thus open up the route for new experiments beyond local electrical probing.

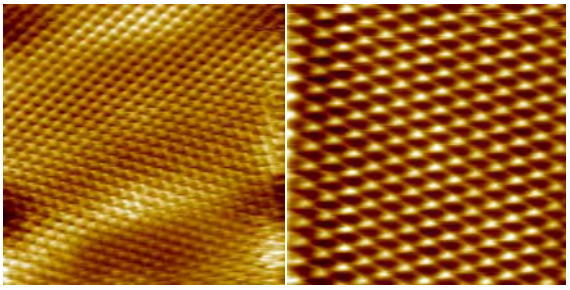


FIGURE 4. STM measurements with atomic resolution on metal surfaces Au(111) (left) and Ag(111) (right) at a temperature of T<5K.

The low sample temperature, the very low lateral and vertical drift and a high vertical mechanical stability make experiments like dI/dV-spectroscopy, atom-/molecule-manipulation or new fascinating experiments like tunneling spectroscopy

TH–08

from one STM tip via a floating sample to a second or to all 3 other STM tips possible.

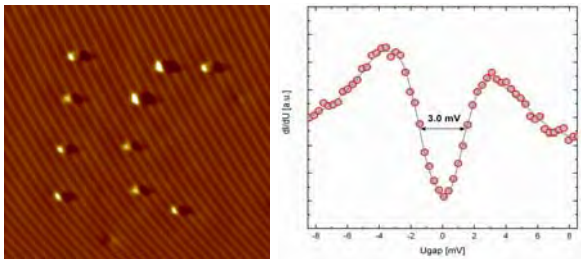


FIGURE 5. Left: atom manipulation of Ag atoms/clusters on at Ag(111) surface at T<5K
Right: Scanning tunneling spectroscopy measurement at temperatures below 5 K, spectrum shows the superconducting energy gap of the Nb tip on a Au(111) sample. U_{GAP}=80mV, I_{SET}=40nA, f_{MOD}=540Hz, U_{MOD}=140µV

Besides, the standard and new kind of STM experiments with one or multiple tips, the LT NANOPROBE was designed for 4 point characterization measurements of nanostructures. In this case, the 4 STM tips will be positioned above the nanostructure under SEM control.

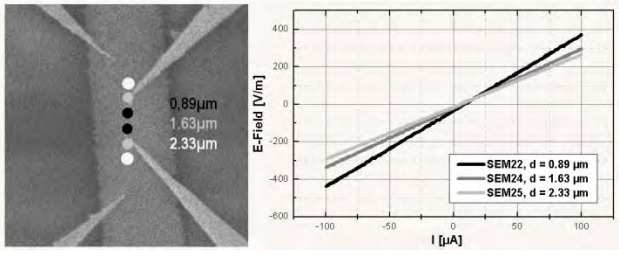


FIGURE 6. Left: The 4 tips were navigated at a temperature of below 5K under complete SEM control. After placing the tips on the Fe-nanowire, the conductivity of the nanowire was measured for 3 different distances of the inner two tips.

The following fine approach of the tips is carried out in STM mode. When the tunneling contact is established, the probe-sample distance is well controlled in the nm range. To establish an electrical contact and to control its resistance, the STM feedback is de-activated and the probe is manually approached by piezo scanner z-offset. However, a permanently connected I/V converter in the signal line prevents transport measurements in four point configuration. Thus, a pA-STM compatible and TTL trigger controlled switching technology is used to reroute signals of the four probes to external BNC connectors and external third party measurement electronics (Source Measurement Unit) for 4-point conductance measurements.

SUMMARY

The new Low Temperature NANOPROBE merges SEM navigated nanoprobing at LHe temperatures with high performance STM imaging, spectroscopy and manipulation. Therefore it represents a "next generation SPM" for creating functional devices by SPM technologies and investigate electrical properties in one experiment. The shown measurements in SEM, STM, and STS at low temperatures represent a first performance proof for its suitability for advanced STM modes such as STS, IETS, SP-STM and atom manipulation.

REFERENCES

1. M. L. Gorzny, A. S. Walton, M. Wnek, P. G. Stockley and S. D. Evans, *Nanotechnology* **19**, 165704-165708 (2008)
2. Z. Wei, D. Wang, S. Kim, S. Y. Kim, Y. Hu, M. K. Yakes, A. R. Laracuente, Z. Dai, S. R. Marder, C. Berger, W. P. King, W. A. de Heer, P. E. Sheehan and E. Riedo, *Science* **328**, 1373-1376 (2010)
3. P. W. Sutter, J. I. Flege and E. A. Sutter, *Nature Materials* **7**, 406-411 (2008)
4. T. Soubiron, R. Stiufiuc, L. Patout, D. Deresmes, B. Grandidier, D. Stievenard, J. Koeble and M. Maier, *Appl. Phys. Lett.* **90**, 102112-102114 (2007)
5. A. Borras, O. Groening, J. Koeble and P. Groening, *Adv. Mater.* **21**, 4816-4819 (2009)
6. Q. Huang, C. M. Lilley and R. Divan, *Nanotechnology* **29**, 075706-075711 (2009)
7. Ch. Joachim, Atomic scale Interconnection Machines, Berlin-Heidelberg, Springer, 2012, pp. 1-8

KEYWORDS

4-probe measurements, 4-point measurements, conductance measurements, conductivity of nanostructures, low temperature 4-probe, STM

TH–09

LOCAL MEASUREMENTS OF GRAPHENE ELECTRONICS USING GATE MAPPING TUNNELING SPECTROSCOPY

Jungseok Chae[1,2], Yue Zhao[1,2], Suyong Jung[1,2,3], Andrea F. Young[4], Cory R. Dean[5,6], Lei Wang[6], Yuanda Gao[6], Kenji Watanabe[7], Takashi Taniguchi[7], James Hone[6], Kenneth L. Shepard[5], Phillip Kim[4], Nikolai B. Zhitenev[1] and Joseph A. Stroscio[1]

1. *Center for Nanoscale Science and Technology, National Institute of Standards and Technology, Gaithersburg, Maryland 20472, USA*
2. *Maryland NanoCenter, University of Maryland, College Park, Maryland 20472, USA*
3. *Korea Research Institute of Standards and Science, Daejeon, 305-340, Korea*
4. *Department of Physics, Columbia University, New York, New York 10027, USA*
5. *Department of Electrical Engineering, Columbia University, New York 10027, USA*
6. *Department of Mechanical Engineering, Columbia University, New York 10027, USA*
7. *Advanced Materials Laboratory, National Institute for Materials Science, Tsukuba, Ibaraki 305-0047, Japan*

INTRODUCTION

We have developed a measurement technique, gate mapping tunneling spectroscopy, to investigate graphene electronics on hexagonal boron nitride substrates with scanning tunneling spectroscopy (STS). Gate map tunneling spectroscopy consists of a series of single STS spectra obtained as a back gate voltage is varied to change the graphene carrier density at the Fermi level. The rich interaction-driven physics in graphene in the presence of magnetic field is successfully resolved with this measurement technique, as described below.

INTERACTIONS IN GRAPHENE

The local electron density of states (LDOS) in semiconductors and semimetals like graphene can be adjusted with respect to the Fermi energy by using an electric field applied by a nearby gate electrode. In this way interaction physics can be turned on and off as the electron density is modulated at the Fermi level in an applied magnetic field. Interaction physics in graphene has been an interesting subject since the first isolation of single layer graphene, due the singular nature of the Dirac point in the graphene spectrum. The electronic density of states at the Dirac point vanishes and the long-range Coulomb interactions are not effectively screened, which gives rise to a rich spectrum of interaction-driven physics in magnetic fields at low temperatures.

EXPERIMENTAL RESULTS WITH GATE MAPPING TUNNELING SPECTROSCOPY

TH–09

Scanning tunneling spectroscopy is a powerful application of scanning tunneling microscope to measure the LDOS of materials at the atomic scale. STS is performed by measuring the differential conductance as a function of voltage between the tip and sample while the tip and sample are held in constant position. Gate map tunneling spectroscopy consists of taking a single spectrum and then incrementally changing the back gate voltage to vary the carrier density at the Fermi level. In this poster, I will present recent experimental results in graphene on boron nitride substrates using gate mapping tunneling spectroscopy [1]. Figure 1 shows a gate map obtained in the presence of a perpendicular magnetic field of 5 T. The gate map shows clear variations of the tunneling spectrum as a function of carrier density. The neutrality point occurs at a gate voltage of ≈-4V, with holes being the majority carriers below this voltage, and electrons above at higher voltages. The formation of Landau levels (LLs) in the magnetic field is observed to form a staircase pattern in the 2-dimensional tunneling bias voltage-gate voltage plane maps of the tunneling conductance in Fig. (1). LLs modulate the LDOS at the Fermi level (zero sample bias) as the carrier density is varied with the gate potential.

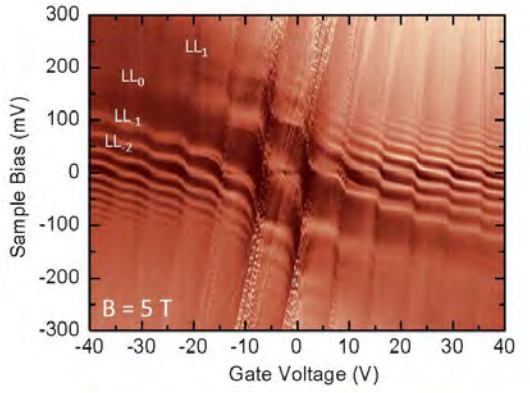


FIGURE 1. Gate mapping tunneling spectroscopy of the Landau level density of states of graphene on hBN. Each map is built of individual tunneling spectra (vertical axis) taken at multiple fixed gate voltages (horizontal axis). The color scale is the differential conductance magnitude.

.

An analysis of the LL peak positions shows that the graphene energy-momentum remains linear at low energies, but that the dispersion velocity is enhanced due to interactions as the density is lowered approaching the Dirac point. Figure 2 shows the Fermi velocity enhancement as a function of carrier density and the experimental data is well-fitted to theoretical predictions [2]. Interaction effects are also strongly seen near zero density by the opening of large Coulomb gaps in the tunneling spectra, which will be presented in the poster.

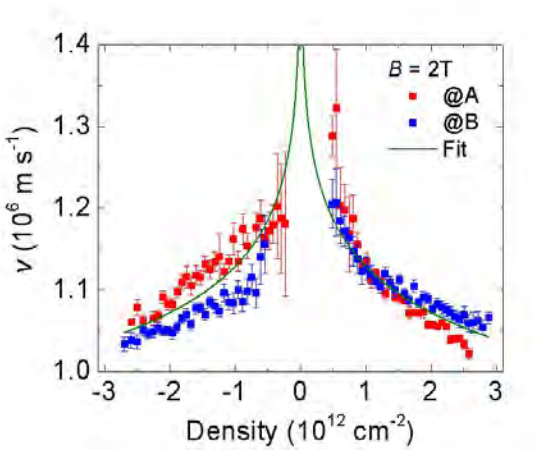


FIGURE 2. Fermi velocity renormalization. A and B represent different spatial positions for the measurements. The solid line is a fit to the theoretical prediction described in reference 2.

REFERENCES

1. J. Chae *et al.*, *Phys. Rev. Lett.*, **197**, 116802 (2012)
2. S. Das Sarma, E.H Hwang and W.-K. Tse, *Phys. Rev. B* **75**, 121406 (2007)

KEYWORDS

Graphene, Scanning Tunneling Microscope, Scanning Tunneling Spectroscopy, Gate Mapping Spectroscopy

TH–10

GRAPHENE AS TRANSPARENT ELECTRODE FOR DIRECT OBSERVATION OF HOLE PHOTOEMISSION FROM SILICON TO OXIDE

Rusen Yan,[1,2] Qin Zhang,[1,2] Oleg A. Kirillov,[1] Wei Li,[1,3] James Basham,[1] Alex Boosalis,[1,4] Xuelei Liang,[3] Debdeep Jena,[2] Curt A. Richter,[1] Alan Seabaugh,[2] David J. Gundlach,[1] Huili G. Xing[2,*] and N. V. Nguyen[1,*]

1. Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, Maryland 20899, USA

2. Department of Electrical Engineering, University of Notre Dame Notre Dame, IN 46556, USA

3. Key Laboratory for the Physics and Chemistry of Nano Devices, Peking University Beijing, China

4. Department of Electrical Engineering and Nebraska Center for Materials and Nanoscience University of Nebraska-Lincoln, Lincoln, Nebraska 68588, USA

INTRODUCTION

Since the 1960s, Internal Photoemission (IPE) Spectroscopy has continually been improved and shown to be a robust technique to characterize the interface properties, determine electronic band alignment [1,2] and extract the material band gap and work function.[3,4] A long-standing issue with in IPE test structure is that, under the bias conditions necessary to observe hole injection from the semiconductor emitter, the current due to hole extraction is usually obscured by the unavoidable electron current from the thin metal contact to the insulator.[5,6] The recent few years have witnessed rapid growth of interest in graphene due to its promise for use in future electronic and optical devices.[7] Specifically, its high optical transmittance and electrical conductivity make graphene an attractive candidate as a transparent electrode.[8, 9] In this report, we propose and demonstrate a novel application of graphene as an elegant solution to this metrology challenge by utilizing graphene as a transparent electrode to collect photo-generated carriers in IPE.

EXPERIMENTS

The high transparency of graphene over a wide spectral range (IR/Visible/UV) enables the direct observation of hole injection, and facilitates the determination of both conduction and valence band offsets at the semiconductor-insulator junction or hetero-junction.

DEVICE STRUCTURE

We employ a graphene/Al_2O_3/Si structure as a technologically important material system to demonstrate the feasibility and utility of our approach. The device structure is schematically depicted in Fig. 1 (a). A 10 nm thick Al_2O_3 layer is deposited by atomic layer deposition (ALD) on a p++ Si substrate. A large-area monolayer graphene sheet grown by chemical vapor deposition (CVD)[10] was transferred onto the already prepared Al_2O_3/Si substrate. A 100 by 200 μm^2 rectangular graphene region was then defined by photolithography and patterned by oxygen plasma etching. A 180 nm thick Al contact is deposited and patterned as a mechanically robust electrical contact to the graphene to complete the test structure fabrication.

TH–10

The top-view optical image of the measured device is shown in Fig. 1 (b).

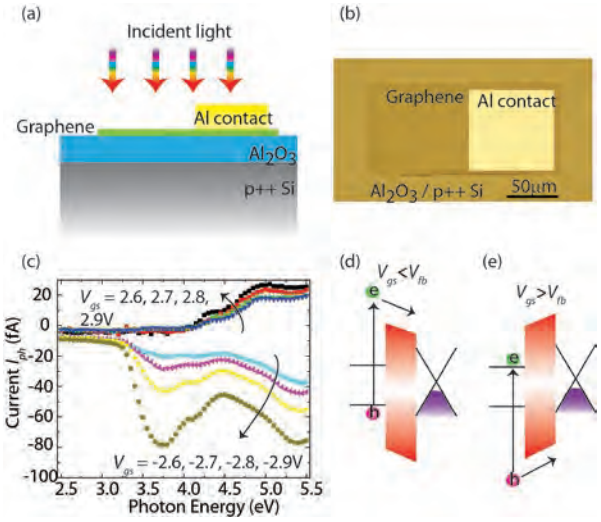


FIGURE 1. (a) Schematic illustration of the graphene-Al_2O_3-Si device structure. (b) The optical image of the measured device. (c) The measured photocurrent as a function of incident photon energy. Different gate voltages are applied to modulate the electric field over the oxide. (d) and (e) The schematic illustration of the electron and hole transitions under two opposite directions of the electric field.

Measured Photocurrent

Shown in Fig. 1(c) are the photocurrents, I_{ph}, consisting of either electron or hole transitions between Si substrate (gate) and graphene (source and grounded) measured as a function of incident photon energy under various applied gate voltage V_{gs}. The oxide flat-band voltage, V_{fb}, occurs when the net electric field in the oxide, thus the current, both reach zero for photon energy larger than the barrier threshold. V_{fb} is found to be about 0.6 V with respect to grounded graphene which is in agreement with a previous band alignment analysis.[6] When V_{gs} = -2.9, -2.8, -2.7, -2.6 V, much smaller than V_{fb}, the spectral photocurrent tends to go negative once the incident photon energy is larger than the electron barrier height, which corresponds to the energy diagram depicted in Fig. 1(d). In this case, the electric field in the oxide drives the electrons from Si into graphene. On the other hand, when V_{gs} = 2.6, 2.7, 2.8, 2.9 V, the reversed electric field drives holes excited in Si into graphene as depicted in the energy diagram in Fig. 1(e). In the latter case, the photo-generated carriers excited in graphene and injected into Si are negligible since the absorption of the incident photons is low for graphene (< 5%) compared to that by Si (> 30%) over the measured spectral range.

Barrier Height Analysis

The electron or hole barrier height is directly determined from the photoemission quantum yield (Y), which is obtained from the measured photocurrent, I_{ph}, normalized by the incident light flux.[7] It is well known that the cubic root of the yield near the barrier threshold (ϕ) is linearly related to photon energy ($h\upsilon$) when the photocurrent is dominated by carriers excited from 3-dimensional semiconductors in an IPE measurement, which follows $Y^{1/3} = A(h\upsilon - \phi)$, where A is a constant dependent on light intensity.[7]

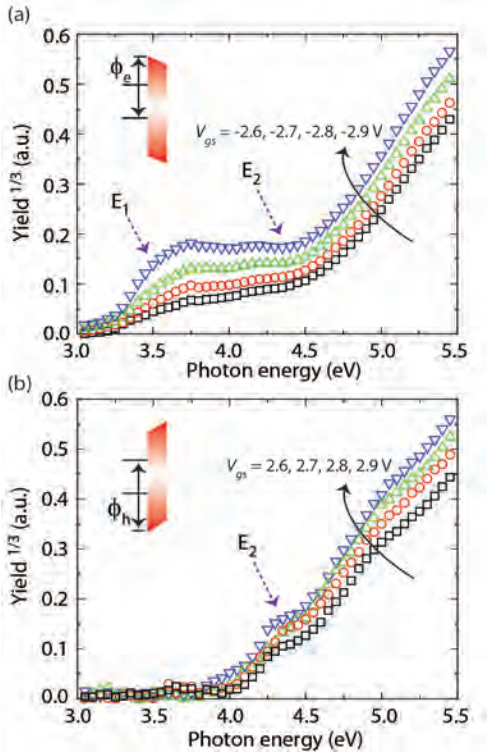


FIGURE 2. Quantum yield for the electron and hole injections. (a) and (b) Cubic root of the quantum yield obtained by the photocurrent normalized to the incident light flux.

TH–10

Observation of Hole Injections

Shown in Fig. 2 (a) and (b) are $Y^{1/3}$ vs. *hv* for the negative (electron) and positive (hole) photocurrents, respectively. It can be seen that, yield starts to increase sharply and linearly at the barrier height threshold. The noticeable features in both injection spectra are the kink at ~ 4.4 eV and the change of slope at ~ 3.5 eV, which will be used to differentiate hole injection from electron injection. In general, the presence of these features is critical to assessing the origin of photocurrent.[3, 5,7] The positions of the 3.5 eV and 4.4 eV features in the yield plot align perfectly with the optical singularities (E_1 and E_2) of crystalline Si, thus clearly indicating that both of the currents are primarily the contribution of carrier injection (electron or hole) from the Si substrate but not from graphene. The positive bias branches in Fig. 2(b) due to hole injection from Si has the appearance of only E_2, and the vanishing of E_1 in the yield plot indicates the barrier height for holes is actually larger than E_1. The transition threshold shifts to lower energy for higher gate voltages following the well-known Schottky barrier lowering effect.[11] This field dependence of barrier height can be well-described by the relation: $\phi = \phi_0 - q(q/4\pi\varepsilon_0\varepsilon_i)^{1/2}F^{1/2}$, where q is the fundamental electron charge, F is the oxide field, ε_0 and ε_i are the vacuum permittivity and the effective permittivity of the oxide. The zero-field barrier heights of electron (ϕ_e^0) and hole (ϕ_h^0) are obtained by a linear fit of ϕ versus $F^{1/2}$ as shown in Fig. 3. As a result, ϕ_e^0 and ϕ_h^0 are found to be 3.5 eV ± 0.1 eV and 4.1 eV ± 0.1 eV, respectively.

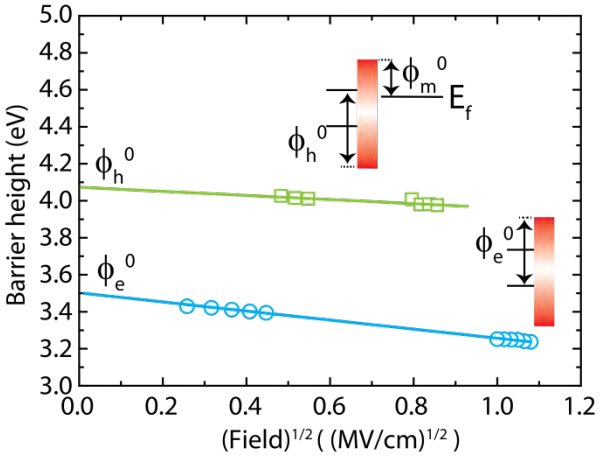


FIGURE 3. Schottky plots of the electron and hole carrier injections as a function of the square root of the electric field. The linear extrapolation to zero field give rise to the zero-field barrier height.

Bandgap Extraction

Our findings, based on the above analysis and made possible by exploiting graphene's unique properties as a semi-transparent electrode, represent a significant advancement in the IPE measurement technique. Unlike prior approaches[7, 12, 13] implemented for IPE measurements that suffer from inherent limitations, our approach enables direct observation of hole transition and provides simultaneous and exclusive information about the conduction and valence band at most critical material interfaces. One additional and beneficial outcome from our approach is that the band gap (E_g) of the insulator can be easily deduced from the electron and hold energy barrier heights by this simple relation: $E_g^{insulator} = \phi_e^0 + \phi_h^0 - E_g^{semiconductor}$ and compared with bandgap calculations derived from purely optical measurements and modeling. In this particular study using ALD Al_2O_3, we find $E_g^{Al2O3} = \phi_e^0$ (3.5 eV) + ϕ_h^0 (4.1 eV) - E_g^{Si} (1.1 eV) = 6.5 eV. This method of determining the bandgap can be preferable for some material systems because it is free from the possible marring influence of excitonic effects.[7] To verify the bandgap value of our ALD Al_2O_3, we also performed vacuum ultraviolet spectroscopic ellipsometry (VUV-SE) measurement on the same Al_2O_3/Si structure. The VUV-SE ranging from 1 to 9 eV is well known to be a reliable and industrial relevant technique to ascertain band gap of high-k gate insulators.[14, 15] Our detailed VUV-SE analysis[14] reveals a band gap of 6.5 eV for Al_2O_3, in an excellent agreement with the value determined by using IPE.

Conclusion

In summary, we have demonstrated a unique and experimentally simple approach to extract a complete energy band alignment using IPE measurements by employing graphene as the

TH–10

semitransparent electrode. Even though the demonstration was performed on a simply structure of Al_2O_3/Si, this technique can be broadly and readily extended to most of structures studied by IPE measurements. The method advanced here is largely free from the experimental complexities and limitations commonly experienced by the past methods, and thus representing a milestone in the advancement of IPE metrology and the field of semiconductor interface studies.

References

1. S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. Ri Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Ozyilmaz, J.-H. Ahn, B. H. Hong and S. Iijima, Nat Nano 5 (8), 574-578 (2010).
2. H. Kim, C. M. Gilmore, A. Pique, J. S. Horwitz, H. Mattoussi, H. Murata, Z. H. Kafafi and D. B. Chrisey, Journal of Applied Physics 86 (11), 6451-6461 (1999).
3. Q. Zhang, G. Zhou, H. G. Xing, A. C. Seabaugh, K. Xu, H. Sio, O. A. Kirillov, C. A. Richter and N. V. Nguyen, Applied Physics Letters 100 (10), 102104-102104 (2012).
4. N. V. Nguyen, M. Xu, O. A. Kirillov, P. D. Ye, C. Wang, K. Cheung and J. S. Suehle, Applied Physics Letters 96 (5), 052107-052103 (2010).
5. V. K. Adamchuk and V. V. Afanas'ev, Progress in Surface Science 41 (2), 111-211 (1992).
6. R. Yan, Q. Zhang, W. Li, I. Calizo, T. Shen, C. A. Richter, A. R. Hight-Walker, X. Liang, A. Seabaugh, D. Jena, H. G. Xing, D. J. Gundlach and N. V. Nguyen, Applied Physics Letters 101 (2), 022105-022104 (2012).
7. V. V. Afanas'ev, Internal Photoemission Spectroscopy: Principles and Applications. (Elsevier Science, 2008).
8. A. K. Geim and K. S. Novoselov, Nat Mater 6 (3), 183-191 (2007).
9. X. Wang, L. Zhi and K. Mullen, Nano Letters 8 (1), 323-327 (2007).
10. X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo and R. S. Ruoff, Science 324 (5932), 1312-1314 (2009).
11. S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3 ed. (Wiley-Interscience, 2006).
12. A. M. Goodman, Journal of Applied Physics 41 (5), 2176-2179 (1970).
13. A. M. Goodman, Applied Physics Letters 13 (8), 275-277 (1968).
14. N. V. Nguyen, S. Sayan, I. Levin, J. R. Ehrstein, I. J. R. Baumvol, C. Driemeier, C. Krug, L. Wielunski, P. Y. Hung and A. Diebold, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films 23 (6), 1706-1713 (2005).
15. S.-G. Lim, S. Kriventsov, T. N. Jackson, J. H. Haeni, D. G. Schlom, A. M. Balbashov, R. Uecker, P. Reiche, J. L. Freeouf and G. Lucovsky, Journal of Applied Physics 91 (7), 4500-4505 (2002).

Keywords

Graphene, transparent electrode, internal photoemission, semiconductor interface, work function

TH–11

DIRECT MEASUREMENT OF THE INTRINSIC DIRAC POINT OF GRAPHENE*

Kun Xu[1,2], Caifu Zeng[3], Qin Zhang[1,4], Rusen Yan[1,4], Peide Ye[2], Kang Wang[3], Alan C. Seabaugh[4], Huili Grace Xing[4], John S. Suehle[1], Curt A. Richter[1], David J. Gundlach[1], and N. V. Nguyen[1]

[1]Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, Maryland 20899, [2]Purdue University, West Lafayette, IN 47907, [3]University of California, Los Angeles, Los Angeles, CA 90095, [4]University of Notre Dame, Notre Dame, IN 46556.

INTRODUCTION

Emerging as a promising and multifaceted material with fascinating electronic properties, graphene has attracted an immense amount of interest from all related disciplines, and fundamental knowledge of the physical properties of graphene and the physical mechanisms governing the electrical operation of graphene-based devices have grown dramatically.[1] In order to advance toward rational designs, fabrication, and implementation of graphene-based electronic and optical devices, the intrinsic barrier height of undoped graphene (Dirac point energy of graphene to the conduction band edge of an insulator), as well as the intrinsic work function of graphene must be accurately determined. We present an internal photoemission (IPE) investigation of a unique semi-transparent metal/high-k/graphene/SiO_2/Si structure, and focus our study on the photoemission phenomena at the graphene/SiO_2 interface. By taking advantage of the optical interference of the optical cavity, the enhanced photoemission from a single layer graphene was observed. As a result, a complete electronic band alignment at the graphene/SiO_2/Si interfaces is established.

DEVICE FABRICATION

Fig. 1 shows the test structure designed and fabricated for this study. The graphene was grown on copper foil by using a chemical vapor deposition (CVD) method and transferred onto a n^{++} doped Si substrate (n_d = 10^{19} ~ 10^{20} cm^{-1}) with 300 nm-thick thermally grown SiO_2 by using a poly(methyl methacrylate) (PMMA) wet transfer method. The PMMA layer was removed with an acetone bath followed by a H_2/Ar forming gas anneal at 350°C for 1 hour. A 3 nm Al sacrificial layer was deposited on top of the graphene by electron-beam (e-beam) evaporation to prevent the contamination from photoresist residues for better contact and cleaner interface.[2] A metal layer of 20 nm-Cr/100 nm-Au, used as the contact for

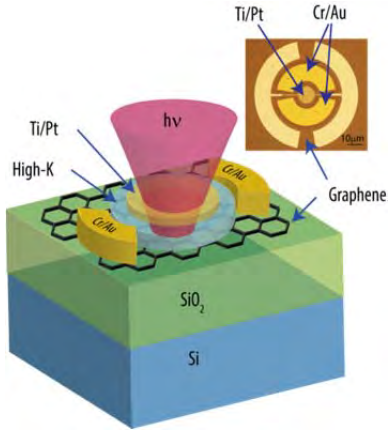


FIGURE 1. Schematic of the test structure with High-*K*/graphene/SiO_2/Si stack. Al_2O_3 and HfO_2 are used at high-K top gate. Top right picture shows the top view of the device under optical microscope.

TH–11

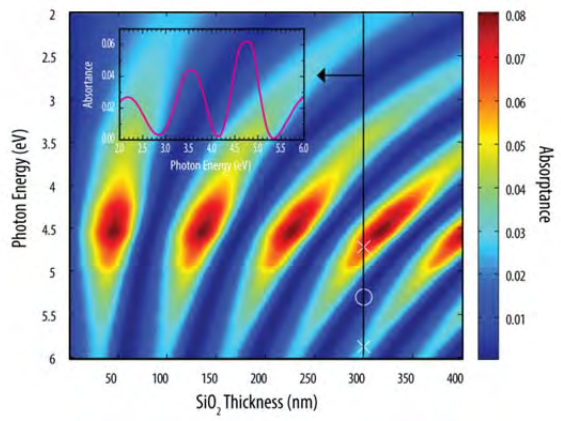


FIGURE 2. Absorptance spectra of in the graphene layer as a function SiO_2 thickness.

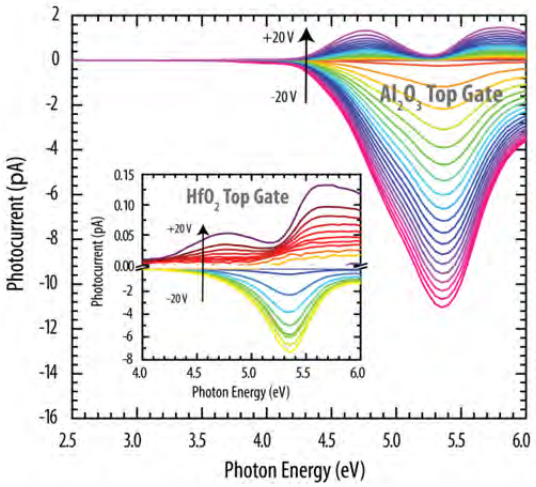


FIGURE 3. Photoelectric current from graphene to 300 nm SiO_2 with Al_2O_3 top gate and HfO_2 top gate measured as a function of incident photon energy and with back gate bias as the parameter.

graphene, was patterned by photolithography and deposited by e-beam evaporation. A 2 nm Al seed layer was deposited by e-beam evaporation and oxidized in atmosphere followed by atomic layer deposition (ALD) of 8 nm Al_2O_3 as the top gate dielectric. Structures with HfO_2 top gate dielectric were fabricated in a similar fashion with 11.5 nm of HfO_2 grown by ALD after 1 nm Ti seed layer. A semi-transparent 1nm-Ti/9nm-Pt layer was used for the top gate metal, through which incident photons were able to reach the desired interfaces. The graphene and the high-*k* oxide outside the active region were etched by reactive-ion-etching (RIE) to isolate each device. A 200 nm thick Al layer, used for the electrodes for the top gate, was patterned by photolithography and deposited by e-beam evaporation.

Results and Discussion

The weak total absorption[3] in a single layer graphene poses a difficult physical challenge to obtain distinguishable IPE signals. Fortunately, the SiO_2 sandwiched between graphene and Si substrate can act as an optical interference cavity that introduces significant modulation to the absorption. To analyze the influence of the SiO_2 thickness on the photocurrent spectra, we compute the absorptance of light in each layer of our device. This is achieved by building a classical optical model of a multi-layer Ti-Pt/Al_2O_3/graphene/SiO_2 /Si, in which the wavelength-dependent complex refractive indices of each material was used. In Fig. 2, the absorptance at the graphene layer is mapped as a function of the SiO_2 thickness and the incident photon energy. The regions with warm colors show a maximum of about 10X higher absorptance than the regions with the lowest absorptance. The constructive interference from SiO_2 cavity causes graphene to more efficiently absorb broader light spectra only at certain thicknesses. The 300 nm SiO_2 thickness is favorable because absorption peaks dispersed at 3.5 eV, 4.8 eV, 5.9 eV, and even at 2.2 eV provide the necessary excited carriers in the graphene layer over multiple spectral ranges.

Fig. 3 shows the IPE photocurrents for samples with an Al_2O_3 top gate and an HfO_2 top gate (shown in the inset). Biased above the flatband condition, the photoexcited electrons come from graphene to SiO_2. The oscillation observed in the photocurrent spectra is attributed to the optical interference effects related to the thickness of the SiO_2. This pronounced oscillation produced by optical interference is essential for enhancing the photoelectric yield that enables the observation of distinct emission of electrons from the Fermi level of graphene to the conduction band of SiO_2.

The spectral threshold Φ_e is extracted by a linear fitting to the cube root of the photoemission. We determine the barrier height (Φ_0) at the flat band

TH–11

condition or zero field in the oxide by employing the Schottky coordinates, $\Phi(F)$ vs. $F^{1/2}$, and plotting the field dependence of the barrier height. The zero-field barrier heights from the Fermi level of graphene to the conduction band edge of SiO_2, Φ_e [$E_{F,Graphene}$-CB_{SiO2}], are 3.25 eV ± 0.05 eV and 3.30 eV ± 0.05 eV for structure with the Al_2O_3 top gate and the HfO_2 top gate, respectively, shown in Fig. 4.

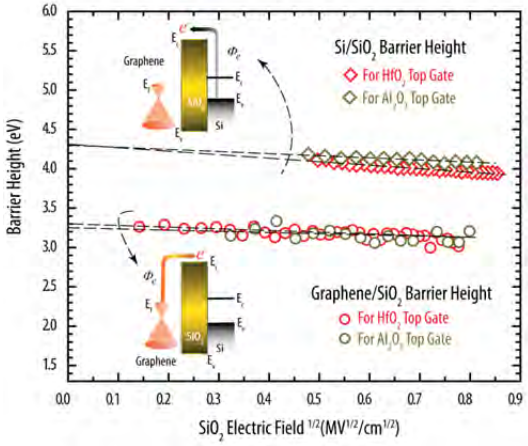


FIGURE 4. Schottky plot of the field dependent IPE threshold measured at graphene/SiO_2 interface for test structures with different top gate high-*k*.

In addition to the barrier heights the position of Fermi level with respect to the Dirac point in graphene need to be determined. They can be extracted by measuring the currents (I_{DS}) between drain (Cr/Au) and source (Cr/Au) (see Fig. 1) when a varying bias (V_{TG}) is applied to the top gate (Ti/Pt). As a result, Fermi level shifts (E_f) are found to be 0.33 eV (Al_2O_3 top gate) and 0.30 eV (HfO_2 top gate) above the Dirac point in graphene when there is no applied gate bias or $V_G = 0$.

The intrinsic barrier height, $\Phi_i = \Phi_e$ [$E_{F,Graphene}$-CB_{SiO2}] + E_f, precisely yields the graphene Dirac point relative to the conduction band of SiO_2. Thus, we are able to construct the complete electronic band diagram as depicted in Fig. 5. We find the intrinsic work function of undoped graphene (the Dirac Point) to be 4.48 eV ± 0.05 eV (Al_2O_3 top gate) and 4.50 eV ± 0.05 eV (HfO_2 top gate).

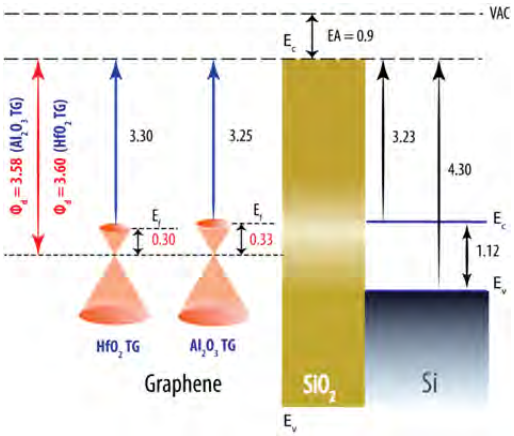


FIGURE 5. Complete electronic band diagram of graphene/SiO_2/Si system, all values are in eV.

CONCLUSION

IPE spectroscopy was used on a uniquely designed optical-cavity graphene/SiO_2/Si test structure to directly measure the barrier height from the Fermi level of graphene to the conduction band edge of SiO_2. An electrical measurement was made on the same test structure from which we obtain the Fermi level position with respect to the Dirac point of graphene. We determined the intrinsic barrier height of graphene (Dirac point of graphene to the conduction band edge of SiO_2), as well as the intrinsic work function of graphene. Such fundamental insights into the band alignment at the graphene-insulator interface are a necessary and important advancement towards the rational design, fabrication, and implementation of graphene-based electronic and optical devices.

REFERENCES

1. Das Sarma, et al., *Rev. Mod. Phys.* **2011**, *83*, 407–470.
2. A. Hsu, et al., *IEEE Electron Device Letters* **2011**, *32*, 1008 –1010.
3. R. Nair, et al., *Science* **2008**, *320*, 1308–1308.

KEYWORDS

graphene, work function, internal photoemission, band alignment, graphene-insulator-semiconductor

TH–12

Revelation of Pattern formation in Single Ferromagnetic CoFeB Film by Using the Giant Spin Hall Spin Torque

Wanjun Jiang*, Pramey Upadhyaya, Li-Te Chang, Kin L. Wong, Jing Zhao, Tianxiao Nie, Murong Lang, Robert N. Schwartz and Kang L. Wang*

Device Research Laboratory, Electrical Engineering Department, University of California, Los Angeles, California, USA, 90095.

INTRODUCTION

Current induced torque enables magnetization switching via a spin transfer torque mechanism, viz., the spin angular momentum of conduction electrons was transferred to the local magnetization. This phenomenon exhibits an important impact on the recording technology, since the opposite (upward/downward) magnetization configurations can be assigned as "0" and "1", respectively, thus leading information to be encoded/decoded electrically [1]. Examples of which can be extensively found, such as magnetic domain wall logics and spin transfer torque random access memory (STT-RAM) in which the magnetization states can be reconfigured via a so called spin transfer torque mechanism [2]. However, the major obstacle is to increase the energy efficiency by lowering the switching current ($10^{10\text{-}12}$ A/m^2) which co-introduces Joule heating, Oersted fields, etc. Exploring novel mechanisms and materials therefore, forms as the dominant trend for which could overcome the above barrier, such as systems with perpendicular magnetization anisotropies, and spin textures (including (anti)vortices, skyrmion). Amongst them, a recent progress have demonstrated the electrical control of magnetic memory and nonvolatile spin logics through in-plane current injection - Spin torque switching with the Giant spin Hall effect in a perpendicularly magnetized Ta/CoFeB/MgO/Ta heterostructure. Owing to the presence of giant spin Hall angle ($\theta_{sh} \approx 0.12$ - 0.15) of the high-resistivity β-tantalum film, the electrical current flows in β -Ta thin film hence produces an abrupt switching of the adjacent ferromagnetic CoFeB layer through the spin Hall spin torque [3].

Device Architectural Demonstration

Here we present the successful fabrication of the above spin Hall spin torque device and demonstrate its great potential as a pattern generator. Our devices are made by utilizing magnetron sputtering in the ultrahigh vacuum with the stack structure: Ta(1 nm)/AlO_x(1 nm)/CoFeB(0.8 nm)/Ta(5 nm)/thermal oxide (500 nm)/Si substrate. Our device is made by electron beam lithography (EBL) and followed by the reactive ion etching. The device is schematically presented in Figure 1 (a). Figure 1 (b) is the corresponding atomic force microscope (AFM) images. The height is confirmed by the presence of step from the AFM measurement, which can also be inferred from the direct transport characterization.

For a single nanodot on top of tantalum Hallbar structure, Figure 2 (a), the related spin Hall spin

TH–12

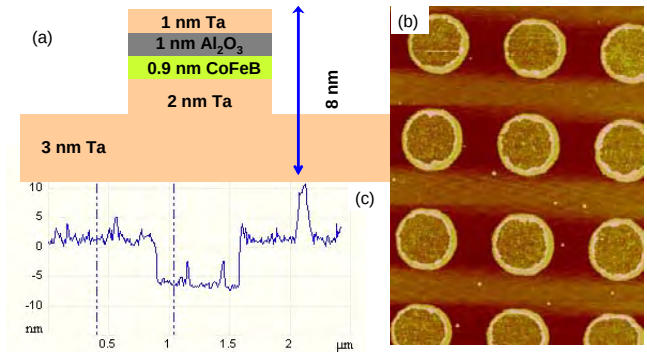


Figure 1. Device concept based on the spin Hall spin torque effect. (a) The cross sectional view. (b) The corresponding device after performing EBL and RIE. The height of these nanopillars is further confirmed by both transport and AFM measurements

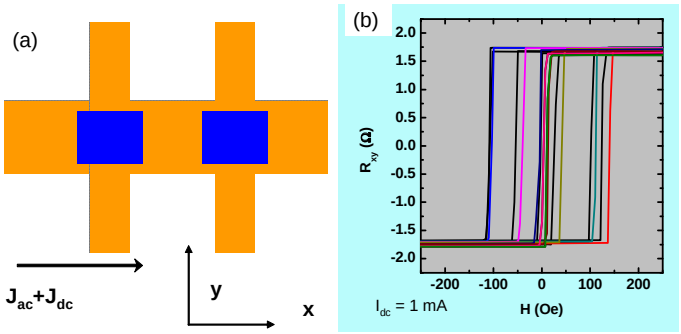
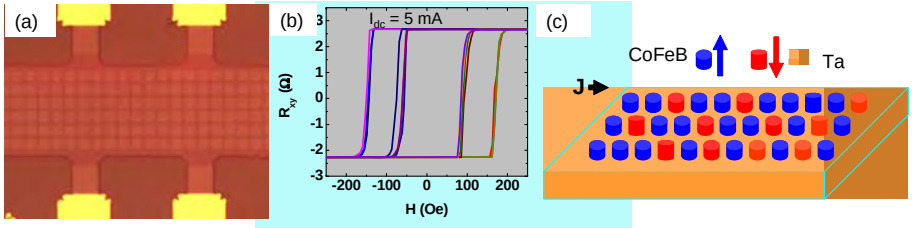


Figure 2. Spin Hall spin torque switching in a single nanodot. Figure (a) is the device layout with CoFeB directly located on top of Ta Hallabr. Transport measurement is given in (b), from which one observes the decreasing of coercivity as a direct consequence of spin Hall spin torque. Noted that H_C = 0 Oe when dc current is 1 mA.



torque switching is given in Figure 2 (b). It is noted that, this measurement is performed under the constant ac current of 20 μA to minimize Joule heating, and a dc offset current is applied simultaneously. When the offset dc current is 0, one realizes that, the corresponding coercivity is approximately 125 Oe. Quite remarkably, such a coercivity is decreasing following an increase dc offset current. This can be understood as follows, when the dc offset current is applied, a spin Hall spin torque is then exerted on the perpendicular magnetization vector, which the alternates magnetization from perpendicular configuration to tilt into the plane. When the dc offset current is approaching 1 mA, the coercivity equals 0 which effectively lower the energy barrier and assist magnetization switching.

Pattern Formation by Using the Spin Hall Spin Torque

For a square lattice located on top of Ta, as shown in Figure 3 (a), however, the above situation is not achieved, Figure 3 (b). It is evident from Figure 3 (b) that, when the dc offset current is increasing between 1 mA and 5 mA, hence both current density and amplitude of spin Hall spin torque is 5 times larger, one realizes that, the coercivity remains approximately as a constant at 75 Oe. This interesting data suggests the pattern formation in the square lattice, Figure 3 (c), viz., the system is in the energy minimum state. The combination of these ferromagnetic and anti-ferromagnetic couplings together, produces a

TH–12

complex magnetization configuration with a perpendicular frustration [4].

Device Architectural Demonstration

In this part, we have offered the device architectural demonstration, as well as the spin Hall spin torque magnetization switching in the single ferromagnetic layer CoFeB with perpendicular magnetization anisotropy. By increasing the dc offset current and hence the amplitude of spin Hall spin torque, the coercivity is decreasing to zero at 1 mA.

Pattern Formation by Using the Spin Hall Spin Torque

In this part, we have observed a finite coercity at 75 Oe under various dc offset current between 1 mA and 5 mA. Such an interesting phenomenon can be related to the pattern formation of the square lattice that located directly on top of Ta. This pattern formation can be understood as a result of system is in the energy minimum state through the combination of ferromagnetic and anti-ferromagnetic couplings.

References

[1] Arne Brataas, Andrew D. Kent and Hideo Ohno, Current-induced torques in magnetic materials, Nature Materials, 11, 372 (2012).

[2] D.C. Ralph and M.D. Stiles, Spin transfer torques, Journal of Magnetism and Magnetic Materials, 320, 1190 (2008)

[3] L. Liu, C.-F. Pai, Y. Li, H.-W. Tseng, D. C. Ralph and R. A. Buhrman, Spin torque switching with the giant spin Hall effect of tantalum, Science 336, 555 (2012).

[4] Sheng Zhang, Jie Li, Ian Gilbert, Jason Bartell, Michael J. Erickson, Yu Pan, Paul E. Lammert, Cristiano Nisoli, K. K. Kohli, Rajiv Misra, Vincent H. Crespi, Nitin Samarth, C. Leighton and Peter Schiffer, Perpendicular Magnetization and Generic Realization of the Ising Model in Artificial Spin Ice. Phys. Rev. Lett. 109, 087201 (2012).

Keywords

Spin Hall spin torque, Pattern generation, Perpendicular frustration

TH–13

MEASURE THE CHARGE STORAGE SPEED AND ENDURANCE OF REDOX-ACTIVE MOLECULES

Hao Zhu [1, 2], Christina A. Hacker [2], Curt A. Richter [2], Hui Yuan [1, 2], Haitao Li [1, 2], Oleg Kirillov [2], Dimitris Ioannou [1] and Qiliang Li [1, 2]

[1] *Dept. of Electrical and Computer Engineering, George Mason University, Fairfax, VA,*

[2] *Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD Contact: qli6@gmu.edu*

INTRODUCTION

Recently, progress in molecular electronics has attracted extensive attention, due to their advantages over the traditional memory or logic devices. [1-3] Redox molecules can be engineered to attach on various surfaces forming self-assembled monolayer (SAM) or multi-layers with simple and low-cost processes. Due to the inherent oxidation and reduction properties of the redox molecules, the device should have distinct charged or discharged states, with very fast program/erase speed and excellent reliability, very attractive for applications in charge-storage memory devices, such as FLASH and DRAM. [4, 5] In this work we fabricated metal/oxide/molecule/oxide/silicon capacitor structure to study the redox molecules. [6] Such a solid-state device structure allows us to use regular electronics characterization metrologies to measure the charge storage of redox molecules, compared to the usual way involving liquid electrolyte. With this capability, we are able to prove that the molecule has fast program/erase (P/E) speed and excellent P/E endurance.

DEVICE FABRICATION

The molecule-attached capacitor memory devices were fabricated by forming a SAM of α-Ferrocenylethanol (Fig. 1a) on SiO_2 surface followed by deposition of blocking insulator and gate electrode. The schematic structure was shown in Fig. 1b. 100 μm × 100 μm effective device size was defined by photolithography. After removing remaining oxide in cell units by hydrofluoric acid dip, a ~ 1.5 nm SiO_2 film was grown by rapid thermal oxidation process. The SAM was prepared by immersing the wafer in a solution of dichloromethane (DCM) with 3-mM Ferrocene. The solution was held at 100 °C in an N_2 environment for 20 min during the attachment process. Attached samples were immediately loaded into the atomic layer deposition (ALD) chamber for 20 nm Al_2O_3 deposition at 100 °C. Finally, the Pd top gate was patterned with photolithographic process, and deposited by using E-beam evaporation with thickness of 80 nm.

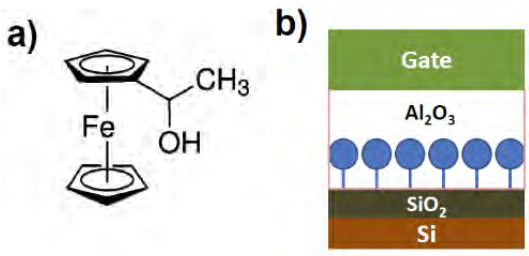


Fig. 1 a) Molecule structure of α-Ferrocenylethanol. b) Schematic of metal-oxide-molecule-oxide-Si capacitor structure.

TH–13

RESULTS AND DISCUSSION

ATTACHMENT CHARACTERIZATION

The cyclic voltammetry (CyV) measurements were performed immediately after the SAM was formed. Fig. 2 shows the CyV curves of the electrolyte-molecule-oxide-Si structure at various scan rates. The inset in Fig. 3 shows the CyV curves of the structure with Ferrocene directly attaching on the H-terminated Si surface. X-ray photoelectron spectroscopy (XPS) measurements were performed on the samples with SAM formed on both SiO_2 and H-Si surfaces. The result proves that the SAM can be formed on both SiO_2 and H-terminated Si surfaces, and the formed SAM can survive in the ALD processing.

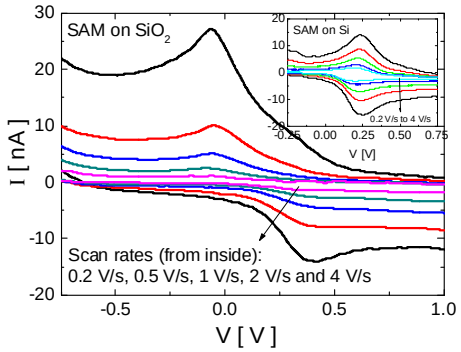


Fig. 2 CyV of the electrolyte-molecule-oxide-Si capacitor at different scan rates. Inset: CyV of electrolyte-molecule-Si capacitor with Ferrocene directly attaching on the H-Si surface

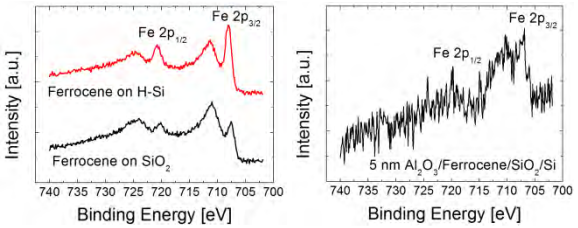


Fig. 3 XPS scans of SAM samples with a) Ferrocene attached on H-terminated Si (red curve) and SiO_2 (black curve) surfaces; b) Ferrocene attached on SiO_2 with 5 nm ALD Al_2O_3 covering on top.

ELECTRICAL CHARACTERIZATION

Fig. 4 shows the 1 MHz C-V hysteresis measurements on Metal/Al_2O_3/Ferrocene/SiO_2/Si (MAFOS) memory devices. Large memory window was observed. The counterclockwise hysteresis loop is due to the charges stored in redox molecules in SAM.

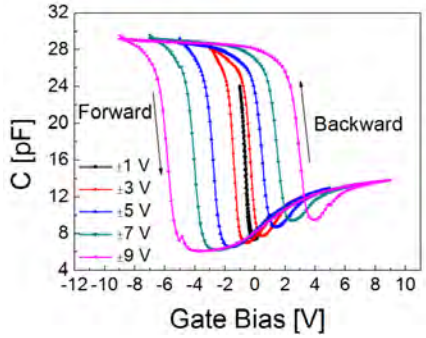


Fig. 4 High frequency (1 MHz) C-V hysteresis curves of MAFOS corresponding to different gate voltage sweep ranges of ±1 V, ±3 V, ±5 V, ±7 V, and ±9 V. The arrows indicate the scan direction.

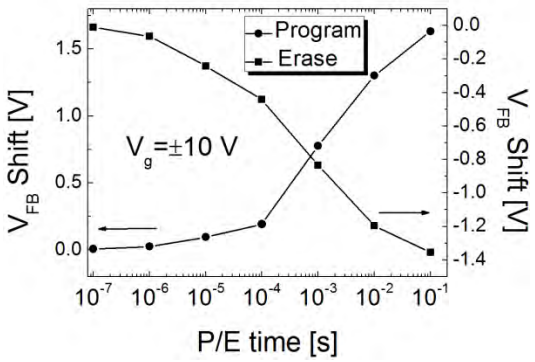


Fig. 5 Programming and erasing speed characterizations of MAFOS device. The P/E voltage is ±10 V.

Fig. 5 shows the device programming and erasing speed. The MAFOS memory device exhibit excellent P/E speed, which arises from the intrinsic fast speed of charging and discharging of the redox molecules. Fig. 6 shows the V_{FB} shift of MAFOS and three control samples as a function of applied P/E voltages by applying 500 µs voltage pulses with increasing positive (negative) height. MAFOS device shows large V_{FB} shift and a clear staircase behavior, while the Metal/Al_2O_3/SiO_2/Si and Metal/Al_2O_3/Si show slight V_{FB} shift, indicating very few charges being stored in the interface and Al_2O_3 traps. The sample with Ferrocene attached on Si surface shows a larger V_{FB} shift during programming

TH–13

process, which is due to the higher molecule coverage density on the Si surface, and thinner tunnel barrier. But for the hole injection in the erasing process, it showed much smaller V_{FB} shift, indicating the fact that the absence of the SiO_2 tunnel oxide resulted in the failure of hole storage in the redox centers of the molecules in SAM. The charging density in the SAM was calculated from the staircase behavior in MAFOS device, and is about 4.41×10^{12} cm^{-2}.

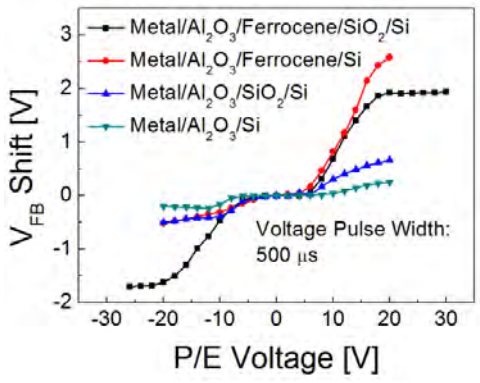


Fig. 6 V_{FB} shift as a function of P/E voltage for MAFOS and three control samples. Voltage pulse width was set at 500 μs.

Fig. 7 shows the room temperature retention and endurance characteristics of the MAFOS device. Referred with the initial memory window of 1.65 V, the ~60% charge loss is mainly due to the thin SiO_2 layer. The endurance characteristic of MAFOS device is shown in Fig. 7(b). Negligible memory window degradation was observed after 10^8 P/E cycles. This good reliability arises from the excellent intrinsic redox behavior of the Ferrocene molecule, and the good interface between the tunnel oxide and Si substrate.

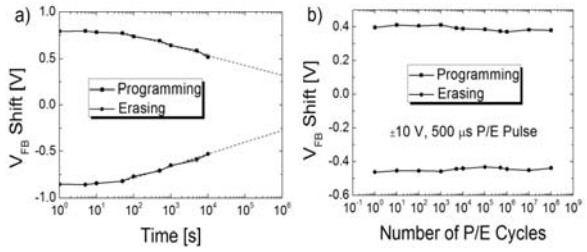


Fig. 8 a) Retention and b) Endurance characteristics of MAFOS device.

Conclusion

The MAFOS device shows fast P/E speed, with sufficiently high charging efficiency. Excellent reliability has been obtained. These excellent characteristics are inherently resulted from both the intrinsic property of redox-active Ferrocene molecules and the protection of good device structure. Such an excellent solid-state molecular memory with enhanced performance is very attractive for future nanoelectronics.

References

1. C. Joachim, J. K. Gimzewski, A. Aviram, *Nature*, **408**, 541 (2000).
2. J. Chen, M. A. Reed, A. M. Rawlett, J. M. Tour, *Science*, **286**, 1550 (1999).
3. G. Atwood, *IEEE Trans. Device Mater. Reliab.* **4**, 301 (2004).
4. K. M. Roth, A. A. Yasseri, Z. Liu, R. B. Dabke, V. Malinovskii, K. Schweikart, L. Yu, H. Tiznado, F. Zaera, J. S. Lindsey, W. G. Kuhr, D. F. Bocian, *J. Am. Chem. Soc.* **125**, 505 (2003).
5. K. M. Roth, N. Dontha, R. B. Dabke, D. T. Gryko, C. Clausen, J. S. Lindsey, D. F. Bocian, W. G. Kuhr, *J. Vac. Sci. Technol. B* **18**, 2359 (2000).
6. Official contributions by the National Institute of Standards and Technology are not subject to copyright.

Keywords

Redox molecule, Non-volatile memory, Reliability, Charging efficiency

TH–14

THE STATISTIC CHARACTERISTICS OF SWITCHING PARAMETERS OF Ta_2O_{5-X} BASED RRAM[1]

Haitao Li[1, 2], Curt A. Richter [2], Oleg Kirillov[2], Hao Zhu[1, 2], Hui Yuan [1, 2], Qiliang Li [1, 2]

1 Dept. of Electrical and Computer Engineering, George Mason University, Fairfax, VA,
2 Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD

INTRODUCTION

The resistive switching (RS) of the TaOx based RRAM has been widely investigated, since the experimental proved extremely high endurance and thermal stability[2,3]. The RS mechanism is generally accepted as the formation and dissolution of nanometer-size conductive filament (CF) respectively formed in set and reset process for most RRAM devices[4]. The mechanism models including the dielectric break down similar process and the modulation of the dielectric gap between electrode and conductive sub oxides, have been introduced to describe the exactly RS process[5,6]; however the exact process is still an open question. Especially the origin of the variation of the RS operation parameters is unknown, which would be an inevitable problem for future ultrascaled RRAM devices. A theoretical model and a few experiments began to work on this variation mechanism and rules[6,7].

We have investigated the statistics of the variation based on nonstoichiometric tantalum pentoxide (Ta_2O_{5-x}) prototype RRAM devices which have the same fabrication processes, but different sizes.

DEVICE FABRICATION

The capacitor structure of Pt/Ta_2O_{5-x}/Ta devices with different size have been fabricated on highly doped 5-10 Ω•cm (100) p-type silicon substrate. First, a layer of 300 nm thermal SiO_2 were grown on the Si substrate by dry oxidation. Then the different effective cell area was defined by photolithography. The devices have five effective sizes, 100×100 μm^2, 50×50 μm^2, 20×20 μm^2, 10×10 μm^2 and pi×6.25 μm^2. After removing remaining oxide in cell units, the 20nm Ta was deposited by RF sputter at room temperature. The Ta_2O_{5-x} layer and top electrode Pt were deposited in a larger pattern defined by the second photolithography. The Ta_2O_{5-x} was RF sputter deposited using stoichiometric Ta_2O_5 target. The deposited film composition was analyzed by XPS. The total thickness of Ta_2O_{5-x} is about 4 nm, 5.2 nm and 6.5 nm respectively.

In our study, all of the ramp voltage was loaded on the top electrode Pt, and the backside bottom electrode is grounded. The schematic and the optic image of the device have been shown in Fig. 1 (a) and (b).

TH–14

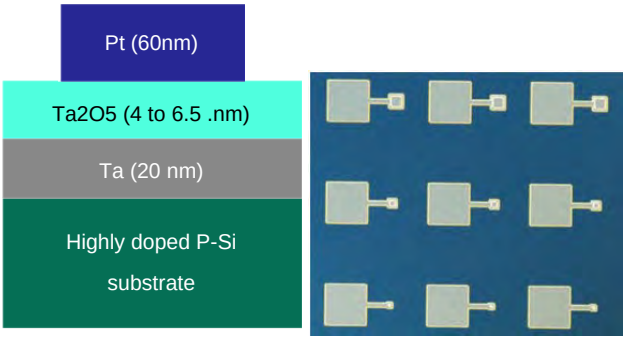


Figure 1. (a) Device schematic, (b) Top view optic image of Devices.

RESULTS AND DISCUSSION

The regular bipolar RS curves of the device under ramp voltage sweep are shown in Fig.2. The operation parameters are named and marked in the graph. All the devices have a larger first set voltage which is called forming voltage ($V_{forming}$).

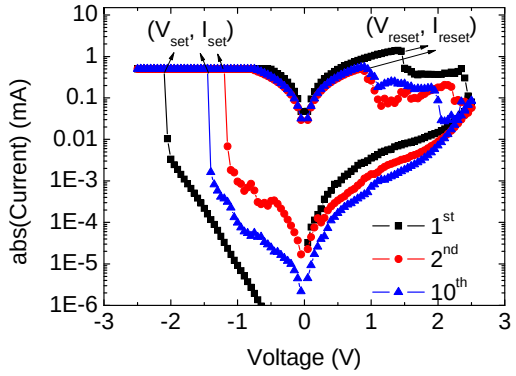


Figure 2. Regular bipolar switching curves. The definition of the operation parameters are marked.

The dependence of $V_{forming}$ on pristine resistance of different devices is shown in Fig. 3 (a). The $V_{forming}$ exponentially depends on the pristine resistance. The devices with thicker oxide layer have larger variation of $V_{forming}$. Figure 3 (b) shows the V_{set} as a function of R_{HRS} before this set process for the five devices with 5.2 nm oxide and different areas. For each device, 11 continuously cycles including the first cycle have been included. The V_{set} shows a clearly exponential dependence on the high resistance (R_{HRS}) before set process for all of the cycles. Therefore, the set process is controlled by voltage stress, and the threshold value V_{set} is decided by the insulation of the device. The relation between V_{set} and R_{LRS} also has been investigated. The R_{LRS} is independent with V_{set}.

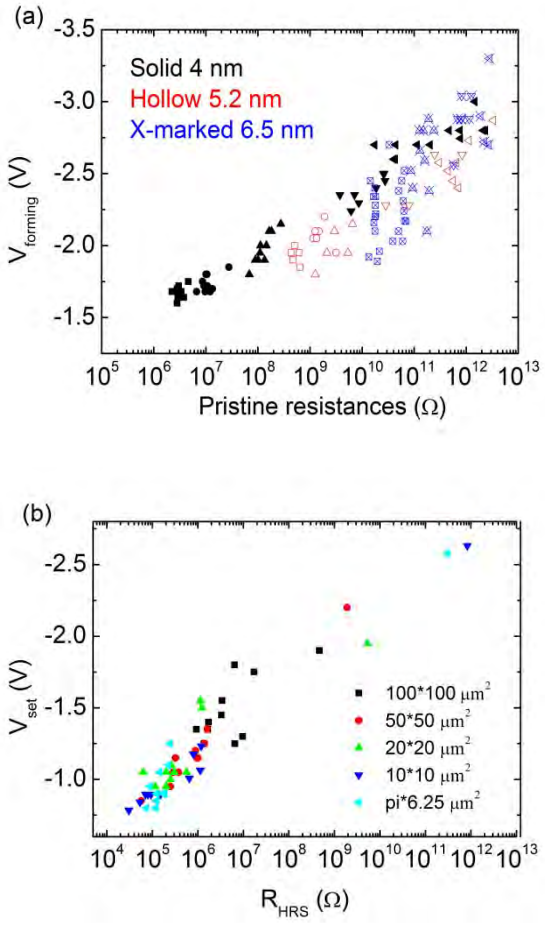


Figure 3. The resistance dependence of the set voltage, (a) $V_{forming}$ as a function of pristine resistance of the devices with different sizes. (b) The V_{set} as a function of R_{HRS}.

The dependences of the I_{reset} and the V_{reset} respectively on R_{LRS} for different devices also have been investigated. All the devices with different sizes have the same rule. Figure 4(a) and (b) shows the dependences obtained

TH–14

from the devices with 5.2 nm oxide layer and 50×50 μm² area. It is obvious that the relations of I_{reset}-R_{LRS} and V_{reset}-R_{LRS} can be separated into two parts according to the values of R_{LRS}. When the resistance is lower, the relation between I_{reset} and R_{LRS} is linear in exponential coordinates, which is similar with the unipolar RRAM which was well explained by the Joule thermal assistance filament annihilate model[8]. With the increase of the R_{LRS}, the I_{reset} decreases to a saturate minimum value which is close to the CC (0.5mA), the average value of V_{reset} increases and seems to play a key role in this part. In this part, the ion migration could contribute more to the dissolution process, in addition to pure diffusion for such range of R_{LRS}.

The relations between V_{reset}-R_{HRS} and I_{reset}-R_{HRS} have also been investigated, but there is no obvious rule in these relations in our study.

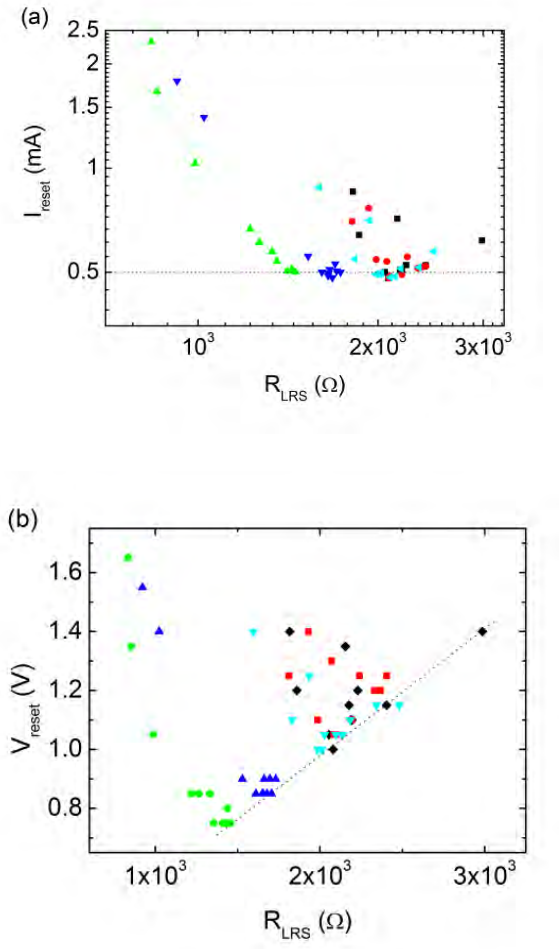


Figure 4. The dependence of I_{reset} and V_{reset} respectively, as a function of R_{LRS} for five different devices with the same size, 5.2 nm oxide layer and 50×50 μm² area.

Conclusion

We have studied the statistics of bipolar resistive switching operation parameters of nonstoichiometric tantalum pentoxide (Ta_2O_{5-x}) based resistive random access memory (RRAM). According to the dependences of operation parameters V_{set}, V_{reset}, and I_{reset} on the resistance of the device, and the statistical analysis of the variation the threshold parameters, we found that the set threshold voltage (V_{set}), the reset voltage (V_{reset}) and reset current (I_{reset}) were mainly dependent on the resistance of the device before SET/RESET operation. The V_{set} is exponentially dependent on the R_{HRS}, and independent with the device size and CC. In the reset process, the Joule thermal assistance filament annihilate and ion migration mechanism coexist, which dominates the reset process is decided by the value of R_{LRS}.

References

1. Official contributions by the National Institute of Standards and Technology are not subject to copyright.
2. Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, I. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, M. Oshima, IEDM, 2008, pp.293.

TH–14

3. M. J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U. I. Chung, I. K. Yoo, and K. Kim, *Nature Materials* **10** (8), 625 (2011).
4. J. J. Yang, I. H. Inoue, T. Mikolajick, and C. S. Hwang, *MRS Bulletin* **37** (2), 131 (2012).
5. X. Wu, K. L. Pey, N. Raghavan, W. H. Liu, X. Li, P. Bai, G. Zhang, and M. Bosman, *Nanotechnology* **22** (45), 455702 (2011).
6. X. M. Guan, S. M. Yu, and H. S. P. Wong, *IEEE TRANSACTIONS ON ELECTRON DEVICES* **59** (4), 1172 (2012).
7. Daniele Ielmini, Federico Nardi, and Carlo Cagli, IEEE *TRANSACTIONS ON ELECTRON DEVICES* **58** (10), 8 (2011).
8. Ugo Russo, Daniele Ielmini, Carlo Cagli, and Andrea L. Lacaita, *IEEE TRANSACTIONS ON ELECTRON DEVICES* **56** (2), 8 (2009).

KEYWORDS

RRAM, Tantalum Pentoxide, Statistic Characteristics

TH–15

INTERACTIONS BETWEEN TWO INDEPENDENTLY CONTACTED AND ROTATIONALLY ALIGNED GRAPHENE LAYERS

Christopher Corbet, Kayoung Lee, Babak Fallahazad, Emanuel Tutuc, Sanjay Banerjee

The Microelectronics Research Center, The University of Texas at Austin
10100 Burnet Road, Building 160, Austin Texas, 78758

INTRODUCTION

Tunneling between two dimensional electron systems can enable beyond CMOS devices thanks to their peculiar current-voltage characteristics [1]. Electrically coupled bilayer graphene systems in close proximity have become a hot bed for this type of electron physics [2]. In this work we discuss efforts working towards the realization of rotational alignment in these graphene systems.

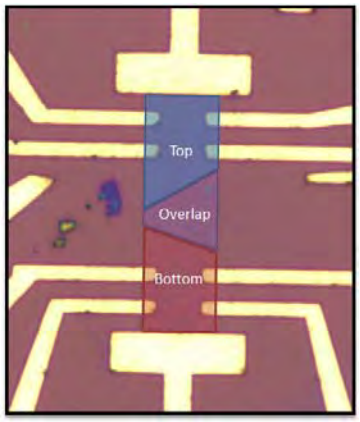


FIGURE 1. Optical micrograph of one of the devices. Top flake is outlined in blue, bottom in red, overlap in purple. Channel width shown is 5μm.

INDEPENDENTLY CONTACTED GRAPHENE LAYERS

We have combined simulations and experiments of two coupled graphene monolayers to study the interlayer tunneling resistance of the system. Using measured data in association with a finite element model of the system we extract an upper limit for the interlayer tunneling resistance of a non-rotationally aligned region.

FABRICATION

To fabricate the overlapped graphene layers used in this work, we begin with two highly doped n-type silicon wafers. 285nm of silicon dioxide is thermally grown and subsequently patterned with alignment marks used for subsequent crystal isolation. Two large single crystal graphene flakes are exfoliated on two separate oxidized substrates using the micromechanical exfoliation technique [3]. One of the graphene monolayers is secured in a sacrificial polymer layer and removed from its substrate via a selective wet etch of silicon dioxide. The captured flake is then transferred on to the second flake and aligned so that the two monolayers overlap by a few micrometers. At this point there is no rotational alignment. Electron beam lithography (EBL) and oxygen plasma (O_2P) are used to isolate and pattern Hall bar structures on each of the two layers and remove excess graphene from the surrounding areas. This

TH–15

geometry allows for the independent extraction of each sheet's carrier mobility and layer density using standard four point measurements.

Independent Layer Characterization

The Hall bar geometry allowed us to independently extract the four-point resistance of each flake in the device: a contact at one end of the device was grounded while the opposite end contact is maintained at 20mV. The substrate was used as a backgate to modulate the carriers in both layers simultaneously. Voltage probes contacting each layer were used to measure a voltage difference on the top (bottom) layer while the backgate was swept from -40V to 40V. Using models [4] we were able to extract a mobility of 7400 (8500) cm^2 / Vs and an impurity concentration of 2E11 (2E11) cm^{-2}.

Device Modeling And Interlayer Resistance Extraction

Using the COMSOL 4.1 Multiphysics simulator, we built a model of two coupled graphene monolayers. The graphene layer resistance was defined as $R_{total} = N_{sq}/(n_{tot}e\mu)$. Where N_{sq} is the number of squares in the device, n_{tot} is the carrier density, and μ is the mobility. Furthermore the carrier density is described as $n_{tot} = \sqrt{(n_0^2 + C_{ox}/e \; [\![V_{BG} - V_{Dirac}]\!] \text{^}2)}$. n_0 is the residual carrier concentration, C_{ox} is the oxide capacitance, and $[V_{BG} - V_{Dirac}]$ is the carrier concentration induced by the applied bias away from the charge neutrality point.

The model introduces the interlayer resistance as a constant resistance placed in between the two layers in the overlap region. Each layer is given its corresponding characteristics extracted from electrical testing. We simulate the current flow between the two layers mimicking the test conditions used during the physical experiment while varying the interlayer resistance. The source to drain bias was 20mV while the backgate was swept from -40V to 40V and the interlayer resistance was varied from 10^{-6} - 10^{-1} Ωcm^2. Electrical screening in the overlapped region was not accounted for.

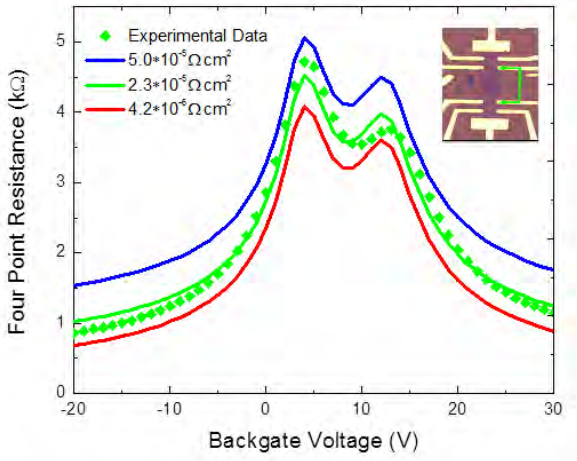


FIGURE 2. A comparison between the experimental and modeled data using several values of the interlayer contact resistance. Inset: voltage probe combination.

Figure 2 shows a comparison between the measured and simulated four-point resistance of one of our devices. In this figure only the comparison of the four-point resistance for the innermost set of probes (shown inset) is given, but all combinations of probes showed similar characteristics. Several devices were fabricated and measured and an interlayer resistance ranging from $2.5 \cdot 10^{-5}\Omega cm^2$ – $7.5 \cdot 10^{-5}\Omega cm^2$ was extracted.

It should be noted that the device pictured has a trapezoidal overlap region, but this shape is not standard from device to device.

TOWARDS ROTATIONAL ALIGNMENT

Recently there has been increased interest in the rotational alignment of two electrically coupled graphene layers to achieve the momentum conservation required for 2D-2D tunneling and negative differential resistance [5].

Fabrication Of Rotationally Aligned Structures

The fabrication of rotationally aligned structures begins with a single large graphene monolayer obtained from micromechanical exfoliation. This

TH–15

large monolayer has a single crystallographic orientation. EBL and O_2P are used to create active areas with the same rotational alignment. Alignment markers are patterned in the excess graphene regions to aid with next level alignment.

The active areas are then separated from one another on distinct PMMA films. One active area is positioned onto a new substrate and electrical contacts are patterned. The second active area, still suspended in its film, is then rotationally aligned and overlapped with the electrically contacted graphene layer using the EBL patterned alignment marks.

The graphene layers shown in Figure 4 are overlapped with rotational alignment of less than one degree. This process flow will also allow the introduction of various dielectrics between the two layers including hexagonal boron nitride and atomic layer deposition (ALD) grown high-k dielectrics. Additionally, this system can be encapsulated with a top dielectric and carrier densities can be additionally modulated with a top gate.

While there have been several devices fabricated, none have provided sufficient electrical characterization for discussion. It is believed that polymer residues left on the surface are significantly disrupting the system. Steps are being taken to develop a cleaner process.

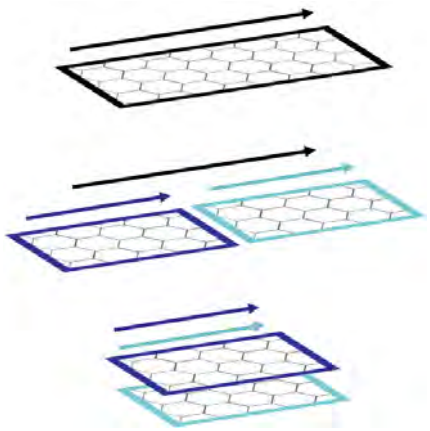


FIGURE 3. A cartoon representing the fabrication process flow for rotational alignment.

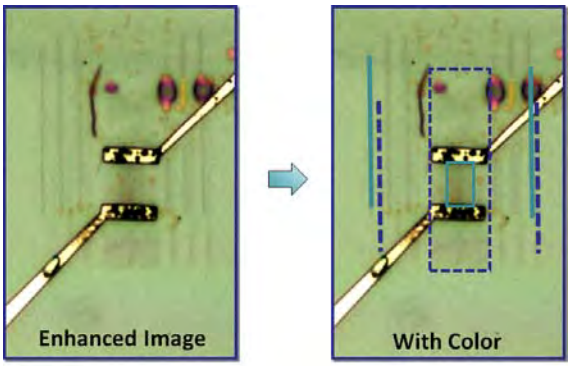


FIGURE 4. Image of an aligned system. Dashed lines are top graphene layer, solid are bottom layer.

References

1. J.P. Eisenstein et al., *Appl. Phys. Letters,* ***58***, 1497-1499 (1991).
2. S. Kim et al., *Phys. Rev. B,* **83**, 161401 (2011).
3. K.S. Novoselov et al., *Science,* ***306****, 666 (2004).*
4. S. Kim et al., *Appl. Phys. Letters*, **94**, 062107-3 (2009).
5. S.K. Banerjee et al., *Dev. Res. Conf.*, **70**, 27-28, (2012).

Keywords

graphene, rotational alignment, 2D-2D tunneling, beyond CMOS

TH–16

FinFET Sidewall Roughness Measurement And Correlation To Device Performance

A. F. Bello[1], Aaron Cordes[2], Abhijeet Paul[1], Shogo Mochizuki[3], Chun-Chen Yeh[4], Huiming Bu[4]

[1]Technology Research Group, GLOBALFOUNDRIES, 257 Fuller Rd., Suite 3100, Albany, NY 12203, [2]Sematech, 257 Fuller Rd., Suite 2100, Albany, NY 12203, [3]Renesas, 257 Fuller Rd., Suite 3100, Albany, NY 12203, [4]IBM Microelectronics, 257 Fuller Rd., Suite 3100, Albany, NY 12203

Introduction

CMOS device performance is directly affected by carrier mobility, which is strongly modulated by surface roughness, especially so in FinFET devices where the current traverses through a thin body of Si that surface effects are more pronounced than a conventional bulk planar or PDSOI device. [1] Fig. 1 shows a schematic of a FinFET device where the gate controls current through three surfaces (the two sidewalls and the top) as a Trigate FinFET or two surfaces (two sidewalls) as a Double-gate FinFET. This is true whether the Si fins are SOI (silicon on insulator) or made out of the bulk Si wafer. The high field carrier mobility depends on fundamental physical characteristics that include surface scattering and hence surface roughness, and is a figure of merit in characterizing device performance.

AFM (atomic force microscopy) is the standard method for the measurement of micro roughness. It is established in failure analysis labs and a mainstay in any fab for its quantitative analysis and ability to measure a variety of surfaces and materials. CD-SEM (critical dimension, scanning electron microscopy) is the standard method in the fab for the measurement of line widths and spaces. It can measure the line edge roughness (LER) and line width roughness (LWR) of small structures. In this paper we measure the sidewall roughness using AFM and the LER using CD-SEM of Fin array structures that have gone through a variety of anneal processing that changes its roughness. A theory is developed on how to correlate this roughness to device transport electrical performance.

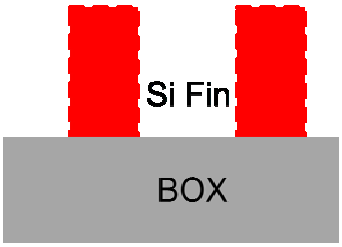


FIGURE 1. SOI (silicon on insulator) fin structure cross section with sidewall roughness.

Experiment

Sample Preparation

Hydrogen annealing is known to improve the electrical performance of FinFET devices [1 - 4] through the smoothing of the fin sidewall. The high field carrier mobility is increased. With such desired effect it is important that the fin sidewall be measured for roughness in order to optimize the best process for device development or to track it during device production.

Fins were produced using the SIT (sidewall image transfer) technique on a SOI (silicon on insulator) wafer. In the SIT process, the deposited sidewall film on a relatively wide feature, the mandrel, is used as the mask on the SOI while a RIE

(reactive ion etch) process etches away the unmasked regions. This RIE process defines the Fin sidewall and it can be rough or damaged depending on the process. Fig. 1 shows the typical structure. Fin formation on ten wafers was followed by hydrogen annealing of various temperature and pressure conditions for each wafer. All were annealed for the same amount of time. After the anneal, an etch process removed some fins in the fine pitch array of fins. The removal of these fins allowed enough space for the AFM probe to measure the sidewall of the remaining ones.

CD-SEM

The two-fin structures were imaged with a CD-SEM (Applied Materials VeritySEM 4i) and the line widths and LER were measured from the top down images. The typical setting was for 800V and using the sum of three detectors – normal and a few degrees on each side from normal. Thirteen die all around the 300 mm wafer were measured for non-uniformity and also for statistics.

AFM

CD-AFM measurements were made using a Bruker InSight 3D-AFM. The InSight is an automated in-line tool used for dimensional process control in semiconductor manufacturing. The measurements were made with Critical Dimension Round (CDR) probes, in this case a 120 nm wide CDR-120. CDR probes have a flared bottom not unlike the head of a nail, giving a projected lateral point that can make contact on the sides of features. The probes are used in Critical Dimension (CD) measurement mode.

Somewhat similar to tapping mode, in CD mode the dither direction and therefore the direction of measurement are dynamically varied by the instrument software to allow contact on the surface regardless of the angle of the feature at the measurement point. Put another way, the instrument will dynamically change from dithering vertically on flat surfaces to dithering horizontally on sidewalls. The instrument also uses a dynamic point distribution instead of a fixed grid, allowing data points to coexist at the same X-Y coordinate. The combination of features allows the instrument to get direct AFM measurement of the slope and roughness of feature sidewalls. It can measure undercut features, to a degree limited by the dimensions of the probe.

To measure sidewall roughness from this data, we select a band of Z values in order to isolate a section of the feature sidewall, then fit a plane to that subset of points. The RMS roughness is then calculated as the root mean square of the deviations of each point in the band from the plane of best fit. This is virtually identical to how roughness is measured in conventional AFM, save that it is being done on a vertical feature.

One problem with this technique is that the apparent width of features is dilated by the width of the tip. Tip dilation is a universal problem in AFM, but it becomes particularly pronounced for measurements with CD tips, where the tip width may well increase the apparent width of features by many times their actual width. To correct for this, we use a Team Nanotec IVPS AFM standard to monitor the tip width, calibrated to a VLSI Standards NanoCD 70. We then use an automated tip shape extraction algorithm developed by Bruker to extract the tip width back out of the feature and reconstruct an approximation of the actual feature dimensions.

RESULTS AND DISCUSSION

Fig. 2 shows typical CD-SEM images from the various process conditions. The figure labeled 1 is the unannealed sample, and the numbers 3, 7, and 8 represent the respective process conditions of the 10 different conditions. From visual inspection slight differences in the line edge roughness can be observed. More evident is the difference in line widths. Previous TEM images tell us that the shape of the fins could be affected. The mid-CD becomes more rounded and thus wider like condition #7 as seen from a top down view. It could get thinner like #3, where the bottom and top of the fins become more square, or the sidewall atoms redistribute themselves towards the top. The LER is obtained by the root-mean-square of the fitted line edge.

TH–16

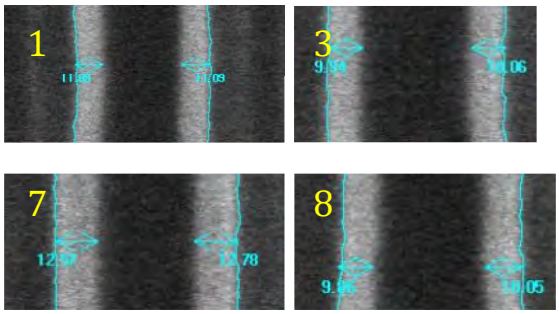


FIGURE 2. Representative top down CD-SEM of the 2-fin structure. The image labeled 1 is the unannealed sample, and the others are labeled with the respective process condition.

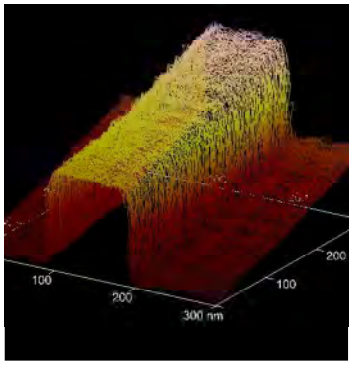


FIGURE 3. AFM of the 2-fin structure. The tip is too wide to measure between fins, so only the outside sidewall data was used for the roughness calculation.

Fig. 3 shows a typical 2-fin AFM measurement. The two fins are not evident because the AFM tip is wider than the space between the fins. Of interest is only the sidewall roughness so distinguishing the top is of no importance.

It must be noted that the sidewall roughness is different from the CD-SEM LER in that the sidewall is fitted to a plane, with the residual defining the RMS. In LER, however, each point on the line is an edge value at that location, and the residual of the fitted line defines the LER RMS. In this work the points on the sidewall that are within the middle 60% from the bottom to top of the fin height were used to calculate the roughness.

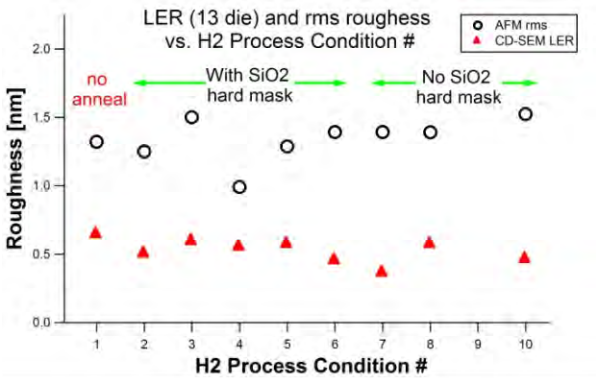


FIGURE 4. The AFM RMS and CD-SEM LER are not directly comparable, although are expected to provide the same trends. The lower LER value has to do with the averaging of points to define the edge. The RMS here was calculated directly from the sidewall.

The RMS from AFM and LER from CD-SEM are shown in Fig. 4, and while not directly comparable, shows the values for comparison and the trend for different annealing conditions. The LER values are relatively smaller because of the averaging done in defining the edge.

The microstructure information in the fin sidewall roughness is typically described using two parameters, namely (i) RMS roughness value (Δ_{RMS}), and (ii) correlation length (λ_r) [5]. The RMS describes the amplitude while the correlation length describes in the lateral direction the amplitude changes. These values are used in either Gaussian or Exponential noise spectrum to describe the roughness information at the semiconductor oxide interface. The surface roughness present at the finFET interface degrades the carrier mobility(μ) under high vertical electric field (high gate bias) when the carriers flow close to the semiconductor oxide interface and feel the potential fluctuation due to the roughness values. Figure 5 shows the impact of Δ_{RMS} and λ_r on the electron mobility at low (5e12/cm2) and high (1e13/cm2) inversion charge density based on the model described by Goodnick et al. [5]. Inversion charge density is directly proportional to the

TH–16

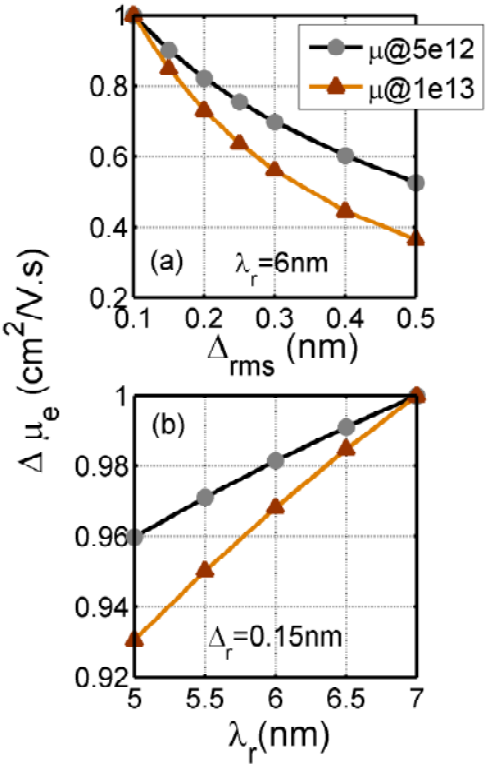


FIGURE 5. Calculations based on a model that uses roughness parameters as inputs. (a) Relative electron mobility reduction with increasing Δ_{RMS} for low (5e12/cm2) and high (1e13/cm2) vertical electric field. (b) Relative electron mobility change with increasing λ_r for low and high vertical electric field. FinFET with width = 10nm and height = 25nm are used for the mobility calculation.

vertical electric field. An increasing of 0.1nm in Δ_{RMS} degrades mobility by ~20%, whereas a reduction in λ_r by 2nm degrades the mobility by only ~4-6%. Thus, improvement in surface roughness is essential in improving the electrical transport in next generation finFETs.

In summary we report the roughness measurements of fin sidewalls using AFM and the line edge using CD-SEM, and show its effect on mobility, a merit of electrical performance. A series of H2 anneal conditions were used to vary the roughness. A model was used to calculate the mobility of finFET devices with roughness parameters of RMS and correlation length as inputs, and it shows that small variations in roughness, especially RMS, has a large effect on the high field electrical mobility. The ability to measure variations (precision) of 0.05 nm in RMS roughness or LER is critical if it because a requirement to track for process control in manufacturing.

Acknowledgement

Adam Ge and Ofer Adan of Applied Materials were influential in analyzing the CD-SEM data. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

References

1. J.-S. Lee, Y.-K. Choi, et al., *IEEE Elec. Dev. Lett.* **24(3)**, 186 (2003).

2. T. Tezuka, N. Hirashita, et al. , *Appl. Phys. Letters* **92**, 191903 (2004).

3. W. Xiong, G. Gebara, et al., *IEEE Elec. Dev. Lett.* **25(8),** 541 (2004).

4. Y-K Choi, et al., EDM 2002, p259 (2002).

5. Goodnick, S. M., Ferry, D. K. et al., Phys. Rev B. 32 (12) 8171-8186, 1985.

Keywords

FinFET, AFM, CD-SEM, sidewall roughness, line edge roughness, H2 anneal

TH–17

OPTICAL SCATTEROMETRY FOR IN-DIE SUB-NANOMETER OVERLAY METROLOGY

Henk-Jan H. Smilde*[a], Martin Jak[a], Arie den Boef[a], Mark van Schijndel[a], Murat Bozkurt[a], Andreas Fuchs[a], Maurits van der Schaar[a], Steffen Meyer[a], Stephen Morgan[a], Jon Wu[a], Vincent Tsai[a], Frida Liang[a], Cathy Wang[a], Kaustuve Bhattacharyya[a], Guo-Tsai Huang[b], Chih-Ming Ke[b], Kai-Hsiung Chen[b]

[a] *ASML Netherlands B.V., De Run 6501, 5504 DR Veldhoven, The Netherlands*
[b] *TSMC Ltd, 8, Li-Hsin Rd. 6. Hsinchu Science Park, Hsinchu, Taiwan 300-77, R.O.C.*

INTRODUCTION

For the semiconductor industrial application of overlay metrology, a trade-off between the measurement precision, the size of the metrology target and the measurement speed is encountered. Significant research and development effort is dedicated to find the optimum balance in sufficient precision with an acceptable target size and with acceptable measurement time. This balance is best achieved by maximizing the detected signal, for example, by increasing the amount of scattering target lines[1] or line edges within the permitted target area.

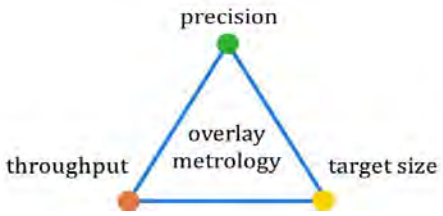


FIGURE 1. Overlay metrology triangle: a trade-off between throughput, precision and target size.

Also the required overlay accuracy and process robustness are increasingly important aspects of the overlay metrology and target design. The emphasis in this contribution will be on the overlay metrology triangle and the in-die application of the optical overlay metrology named micro-diffraction-based-overlay (μDBO) technology.[2]

μDBO TECHNOLOGY

The μDBO technology has recently been introduced to bypass physical limits in optical scatterometry, which are imposed by the diffraction of light, and continue the metrology target size reduction. Such target size reduction is required for the reduction of metrology real-estate consumption on production wafers. More important, the aggressive ITRS roadmap specifications on overlay metrology are not achieved by precise measurements in the scribe lanes around the die and subsequent interpolation into the die area alone. The accuracy at the angstrom level requires local overlay measurements in the die. These in-die overlay targets must be small enough to fit inside the device area, and must match the process requirements of the product structures. In the die, they enable higher order overlay corrections improving local accuracy. Both accuracy and precision at angstrom level are crucial to meet the aggressive ITRS specifications. The following two sub-sections present the measurement technique and metrology targets used in the μDBO technology.

* henk-jan.smilde@asml.com; phone + 31 40 268-7820; fax + 31 40 268-9540; www.asml.com

TH–17

POLARIZED OPTICAL SCATTEROMETRY

The µDBO technology is based on polarized angle-resolved optical scatterometry. This is metrology technique that is sensitive for the asymmetry in the diffraction pattern reflected by a lithographically defined semiconductor stack structure. The µDBO technology employs this asymmetry detection for the overlay metrology. The µDBO-target translates a lateral position-difference between two layers in a stack into an asymmetry in the angle-resolved diffraction pattern. In the sensor, single diffraction orders are optically filtered from this diffraction pattern. Also, the grating-environment contribution to the transmitted pattern is filtered out. As such, the µDBO technology is able to measure each individual grating or other selected area on the semiconductor product wafer for a single diffraction order. The asymmetry between higher orders is then a measure for the overlay.

µDBO METROLOGY TARGET

The layout of the µDBO-target enables optimum use of the metrology target area for a maximum signal-to-noise ratio, as it contains a dense line-space pattern with a typical repeating unit (pitch) of 500 nm. The line-space pattern is present in each layer, resulting in an enhanced compatibility with a product area from processing point of view. An example lay-out, which is used in the simulation section, is given in figure 2. It basically consists of two stacked gratings per direction, with a typical target size of 10 × 10 µm^2. A known overlay-bias serves as an on-wafer calibration of the asymmetry signal.

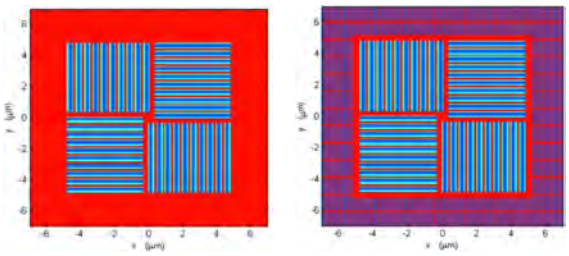


FIGURE 2. Top-view images of (simulated) example 10 × 10 µm^2 µDBO targets with (left) homogeneous reflecting stack, and (right) anchor features at 0.2 µm.

RESULTS

To evaluate the µDBO technology, measurements as well as simulations are performed. First the trade-off between precision, throughput and target size is considered based on measurements varying the grating size and the camera integration time. Thereafter, the product environment's influence on the in-die µDBO accuracy is investigated using a partial coherent optical simulation.

PRECISION-THROUGHPUT TRADE-OFF

Measurement precision is improved by increasing the camera integration time, or e.g. by using a larger irradiance light source. The drawback of an increased acquisition time for the industrial application is a reduced throughput, i.e. less wafers per hour can be measured. This trade-off is studied by varying the camera integration time. Figure 3 presents the result on the overlay precision as function of the total amount of photons acquired per measurement. This is shown for an internal ASML wafer and for a customer wafer. For both, a square root model fit has been applied to the measurements. Stack-related properties such as the diffraction efficiency and the sensitivity to overlay explain the difference between both wafers. An improved precision is clearly observed for extended camera integration time.

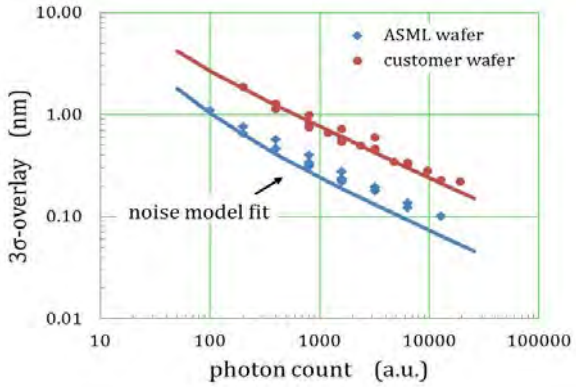


FIGURE 3. Trade-off between measurement precision and measurement time. The photon count is normalized using the reflection intensity of a reference stack.

* henk-jan.smilde@asml.com; phone + 31 40 268-7820; fax + 31 40 268-9540; www.asml.com

TH–17

Precision Versus Grating Size

To investigate the influence of the grating size on the measurement precision, repeated measurements on a set of targets with varying grating dimensions have been performed. They are measured for constant camera integration time. The measured overlay-variation depending on the photon count, is expected to be inverse proportional to the square-root of the grating area that contributes to the detected asymmetry signal. Figure 4 presents this relation between the 3σ-overlay and the grating area. Fits through the origin are added for the x- and y-overlay cases. The absolute 3σ-values depend amongst others on stack properties and sensor settings. A good match to the expected precision behavior is observed.

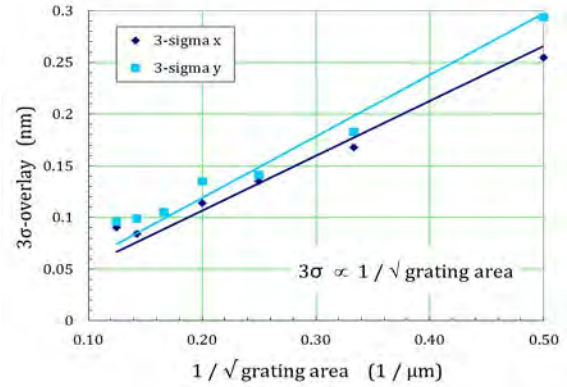


FIGURE 4. Measured inverse proportional relation between overlay precision and the square-root of the grating area.

In-Die Simulation

A partial-coherent simulation model is developed for the physical understanding and risk assessment of the µDBO technology. It includes diffraction effects, sensor properties and the sample interaction. Here, results of the scalar version of the simulation model are presented for the effect on overlay of the in-die positioning of a µDBO-target. Figure 2 presents the schematic top-view lay-out of the simulated 10 × 10 µm² µDBO-target with a homogeneous reflecting stack. Emulating a product environment, the target is also positioned within an anchor features environment at a distance varied from 0 to 2 µm. The anchor features' pitch in horizontal and vertical direction is 80 and 1080 nm, respectively. The 'measured' overlay with anchor features is compared to the one without, as a function of the distance to the µDBO-target. The nominal overlay values in x- and y-direction are 10 and 30 nm, respectively. Figure 5 shows that the expected environment influence on the measured overlay is below 0.1 nm from this simulation. The difference decreases rapidly with distance to the environment, and reduces below 0.01 nm for 1.5 µm with typical proximity-like oscillations.

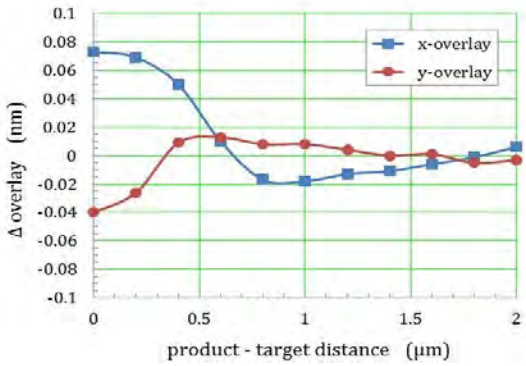


FIGURE 5. Overlay difference between thin-film stack and anchor feature environment as function of distance between the environment and the µDBO-target, for nominal x- and y-overlay of 10 and 30 nm respectively.

Conclusion

Reduction of overlay metrology target size leads to a trade-off between throughput and precision. The µDBO technology offers here an optimum solution, which retains good accuracy in an in-die environment from first simulations.

References

1. N.P. Smith, B.L. Peterson, G.R. Goelzer, Proc. of SPIE 8324, 832418 1-12 (2012).
2. H.J.H. Smilde *et al. Proc. of SPIE* **8324**, 83241A 1-8 (2012).

Keywords

overlay, grating, diffraction, in-die, scatterometer.

* henk-jan.smilde@asml.com; phone + 31 40 268-7820; fax + 31 40 268-9540; www.asml.com

TH–18

CD-SAXS FOR 3D DIMENSIONAL METROLOGY ON 32 NM PITCH LINE PATTERNS

Daniel F. Sunday[1], Wen-li Wu[1], Scott List[2], and R. Joseph Kline[1]

1. *Materials Science and Engineering Division*
National Institute of Standards and Technology
Gaithersburg, MD 20899

2. *Intel Corporation*
Hillsboro, OR 97124

INTRODUCTION

The semiconductor industry continues its path along Moore's Law towards ever smaller and more complex features.[1] These next generation devices will allow higher performance, higher transistor density, and decreased power consumption. The device scaling will also provide intense challenges to dimensional metrology. Currently process monitoring is done using a combination of optical scatterometry (OCD) and critical dimension scanning electron microscopy (CD-SEM) to determine the three dimensional shape and compositions. The key dimensional parameters are the pitch, the feature widths, heights, film thicknesses, and pitch errors due to pitch doubling and quartering methods such as multiple exposures, spacer doubling, and directed self-assembly. As devices get ever smaller and complicated, the current non-destructive metrology methods get more difficult and the destructive and expensive methods such as transmission electron microscopy (TEM) become required more often. We will discuss the use of critical-dimension small angle x-ray scattering (CD-SAXS) as a potential next-generation, non-destructive metrology method.[2] We will show examples of CD-SAXS characterization of 32 nm line gratings fabricated by spacer quartering.[3] CD-SAXS provides the full 3D shape profile and the pitch offset errors from the spacer quartering process. We will also compare measurements with laboratory sources to those done at the synchrotron.

CD-SAXS FOR DIMENSIONAL CHARACTERIZATION

CD-SAXS uses x-ray scattering to determine the dimensions of periodic nanostructures. CD-SAXS is on the ITRS roadmap as a potential next generation non-destructive 3D metrology method.[1] CD-SAXS is a variable angle transmission SAXS method where the sample is rotated along an axis perpendicular to the beam and the direction of periodicity (for a line grating, the rotation axis is parallel to the line pattern). For full 3D structures on a periodic rectangular grid the sample can be rotated along both periodic axes to fully determine the 3D shape. The angular range and step size of the rotation are dependent on the required resolution in the film thickness direction (z) and the film thickness.

The CD-SAXS measurements were conducted at the Advanced Photon Source at Argonne National Laboratory on beam line 5-ID-D. Hard x-rays (E=17 keV) were used to allow transmission through the silicon wafer. The beam size was about 100 μm. The pattern was collected using a CCD camera placed 4 m away from the sample. The incident and diffracted beam paths were under

TH–18

vacuum to minimize air scattering, but the samples were in air. The sample to detector distance was calibrating using a 250 nm SEM calibration bar on the MetroBoost calibration sample.[4] The scattering patterns were fit using a multitrapezoidal model where the Fourier transform of the model is used to simulate the scattering pattern. The model parameters are optimized to match the experimental results. A Monte Carlo Markov chain model is used to determine the sensitivity of the solution to the fit parameters.

Line Profiles for 32 nm Pitch Patterns

The 32 nm line gratings were measured with CD-SAXS and simulated to determine the line profile shape and the periodic pitch offsets due to the spacer quadrupling procedure. Figure 1 shows a representative scattering pattern and the resultant best fit of a 3 trapezoid model. As expected, the lines are rounded on top and have an expanded foot at the bottom. The pitch errors from the spacer quadrupling process were found to be 1 nm to 2 nm.

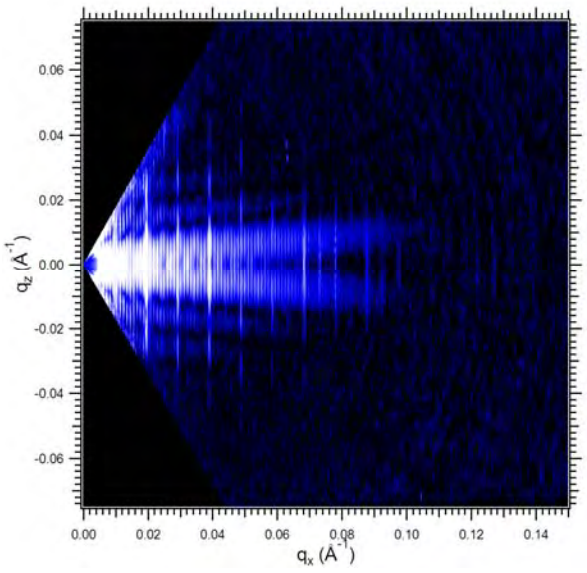


FIGURE 1. Representative CD-SAXS qx-qz scattering pattern for 32 nm pitch line grating.

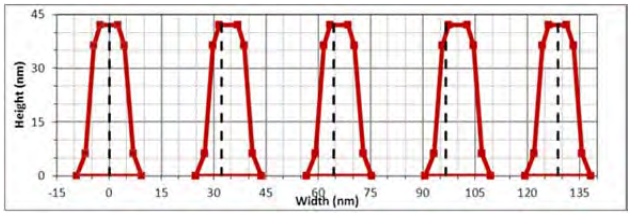


FIGURE 2. Edge line profiles obtained from 3 trapezoid fit model to CD-SAXS experimental data including 3 pitch offset values. The dashed lines show the ideal position for 32 nm pitch.

In conclusion, we have demonstrated that CD-SAXS can determine the line shape of 32 nm pitch line gratings and the periodic offset from the ideal pitch due to the spacer quadrupling process. CD-SAXS is very sensitive to periodic deviations from the pitch.

References

1. The International Technology Roadmap for Semiconductors. (http://www.itrs.net/, 2011).
2. C. Q. Wang, K. W. Choi, W. E. Fu, D. L. Ho, R. L. Jones, C. Soles, E. K. Lin, W. L. Wu, J. S. Clarke, B. Bunday, "CD-SAXS measurements using laboratory-based and synchrotron-based instruments" - art. no. 69222E. Metrology, Inspection, and Process Control for Microlithography Xxii, Pts 1 and 2, 6922 (1-2), E9222-E9222 (2008)
3. van Veenhuizen, M.; Allen, G.; Harmes, M.; Indukuri, T.; Jezewski, C.; Krist, B.; Lang, H.; Myers, A.; Schenker, R.; Singh, K.J.; Turkot, R.; Yoo, H.J.; Interconnect Technology Conference (IITC), 2012 IEEE International , vol., no., pp.1-3, 4-6 June 2012
4. Certain commercial equipment, instruments, or materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose

Keywords

CD-SAXS, 3D metrology

TH–19

On Sub-10 nm 3D CD-SEM Metrology

András E. Vladár, John S. Villarrubia, Bin Ming and Michael T. Postek

National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899-8212, USA

Optical lithography is printing photoresist features that are one tenth or smaller than the wavelength of the ultraviolet light used, and therefore it is indispensable to use various optical correction methods, which model and compensate for various errors in the lithography process down to sub-nanometer, essentially atomic levels. The process has to rely on accurate and highly repeatable dimensional metrology, which is beyond the conventional one-dimensional line width measurements, and it must account for the contours and shapes of sub-10 nm structures. For this the critical dimension measurement scanning electron microscope (CD-SEM) is the key metrology tool. Three-dimensional (3D) metrology is now indispensable for IC technology, but current metrology tools and methods cannot fulfil the requirements. We believe that with the implementation of new methods it will be feasible to develop 3D metrology that will serve well IC production, even on sub-10 nm structures.

Need for Optimized 2D and 3D Metrology

In the past, for a long time, we've been very lucky, because it was enough to measure the critical dimension (CD), the width of the resist line to keep IC production under acceptable control. Nevertheless, CD metrology has never been done really right: by no means were the dimensional measurements fully optimized. For measurements, much less sophisticated methods were used than for crafting of the integrated circuits. This was somewhat understandable, but quite disadvantageous. The use of mostly arbitrary (fudge factor) edge algorithms lead to unpredictable biases, partly due to the neglect of the 3rd dimension, i.e., the shape of the resist structures.(1) There was little regard to and the use of the best principles of metrology and statistics, so likely the industry lost a lot money and time, which it cannot afford anymore; dimensional metrology just sort of drifted through time, there was never a concerted effort to use metrology, which is based on, and fully taking advantage of what physics and statistics can offer.

Production continued rather well, even if the industry kept marking red almost every current and future entry in the ITRS Metrology section.(2) Dimensional metrology of ICs played a vital part of the phenomenal success of this industry, it kept up with the advances in IC production, and likely will continue to do so, but now we have to develop much better measurement methods than before. We have to deal with real 3D structures, which are much smaller than ever before, such that essentially every atom counts (atoms sit ~0.3 nm apart on a Si crystal plane), and we need to take many more measurements.

New SEM Dimensional Metrology Methods

We must measure as quickly as we can, because in the SEM all measurements take place on a moving target, so the effects of drift and vibration must be minimized. Figure 1 illustrates the improvement possible by using a 2D Fourier transform based method that lines up the fast and noisy images with sub-pixel accuracy and retains the image sharpness, which is otherwise lost with the current simple acquisition method.(3) We need a large number of measurements, and have to minimize cost of ownership. CD-SEMs can be faster if we use lasers for navigation, but once we are at the measurement site, we can use the lasers to improve the quality of acquired data to eliminate a large part of stage drift-

---

TH–19

and vibration-related uncertainties. After this step we can use the above-mentioned fast image composition method to minimize beam steering-related uncertainties at the sub-nanometer scale. Laser interferometer-based navigation combined with non-conventional electron beam scanning also allows for measuring only the absolutely necessary sample locations to speed up the measurements and minimize sample damage.

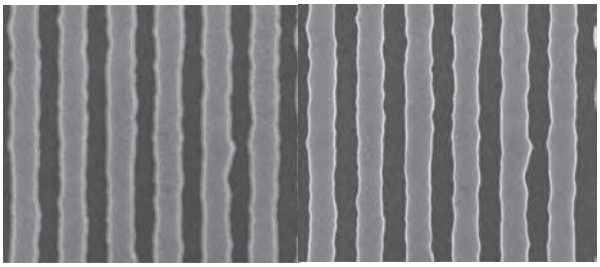


FIGURE 1. Current (left) and new method (right) of adding fast SEM images together. Note the improved image sharpness on the right. The horizontal field of view (HFW) is 1.27 µm for both images.

Once optimized-quality images from different angles are acquired, it is necessary to interpret them correctly and extract useful 3D information. Sound, physics-based, accurate modeling, like the new 3D NIST Monte Carlo method, which now includes sample charging, and the use of model-based (MB) measurement methods can deliver results better than methods that disregard the governing physics of the signal generation. Figure 3 illustrates that 3D simulation can account for all essential characteristics of SEM image generation, including secondary electron enhancement and reduction at the edges and corners, and the full 3D structure. In many cases MB measurement method can determine 3D information from a single top-down view SEM image.

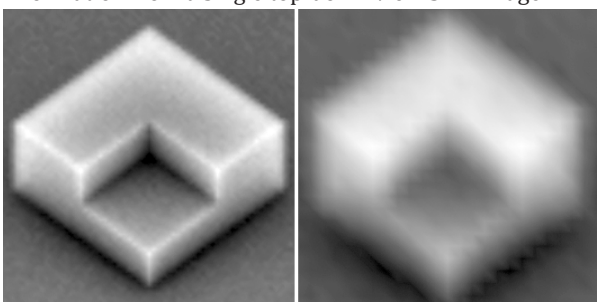


FIGURE 2. On their sides 30 nm (left) and 6 nm wide (right) modeled 3D structures.

As long as we can see the integrated circuit structures in the SEM, we can measure 3D CD on fins and other structures and, with limitations, reconstruct their true 3D shapes. Figure 3 is a top-down view of a resist sample of intentional defect arrays (courtesy of SEMATECH). It illustrates that even top-down images reveal a lot of 3D information. Here delamination, i.e., the top layer is partially peeled away from the underlying one and is clearly visible. So is as some residue on the surfaces. The 5 nm by 10 nm size L-shaped marker helps to assess the size of the various sample features. Some of the smallest ones are less than 5 nm is size, meaning even details of sub-10 nm size features can be imaged and measured. New SEMs achieve a best resolution of a few 100 pm, so superbly detailed images can be acquired, and precise, sub-10 nm 3D measurements will be possible with them.

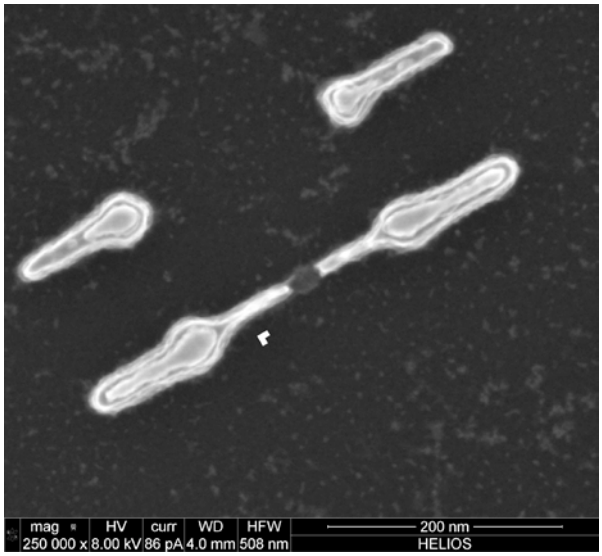


FIGURE 3. A top-down view of a resist sample of intentional defect arrays. Sub-10 nm features are clearly visible. The L shaped marker is 5 by 10 nm, HFW 508 nm

REFERENCES

1. Villarrubia, J. S.; Vladár, A. E.; Postek, M. T., Simulation Study of Repeatability and Bias in the CD-SEM; J. Microlith., Microfab., Microsyst. 4(3) 2005

2. ITRS http://www.itrs.net/home.html

3. Cizmar, P. Vladár, A. E. and Postek, M. T. Real-Time Image Composition with Correction of Drift Distortion 2009 http://wiki.accord.cizmar.org/doku.php

KEYWORDS

SEM, CD, three-dimensional, 3D, metrology, dimensional, nanometer, integrated, circuit

TH–20

CD METROLOGY GAPS ANALYSIS FROM THE 22 NM NODE ONWARDS

Benjamin Bunday[a]

[a]*SEMATECH*
257 Fuller Rd, Albany NY, 12203 USA

ABSTRACT

The 22 nm node marks the beginning of a major transition from conventional scaling-driven planar devices to complex 3D transistor architectures, redefining future needs for lithographic metrology solutions for high volume manufacturing [1][2][3]. Evaluation of critical dimensions (CD), roughness, and other parameters in FinFETs [4] raises new metrology complexities, as the entire 3D structure becomes critical for process control, including fin and gate dimensions, profiles and roughness, and metal gate undercuts (See Fig. 1). Similarly, future 3D memory devices, as in Fig. 2, will include multiple gate-level structures defined by high aspect ratio (HAR) trenches and holes in multilayer stacks—all of which are major known gaps in current metrology technology [5]. No in-line non-destructive metrologies have achieved the sensitivity and resolution to image or measure CD, depth, profile, or contamination of such HAR features [6]. To address these challenges, a robust metrology strategy should encompass the extendibility of conventional techniques that are approaching their fundamental limits, as well as the development of new technologies.

While a variety of CD metrology techniques is available, no single technology solves all CD metrology requirements. Various workhorse metrologies such as CD-scanning electron microscopy (CD-SEM) and optical critical dimension (OCD) scatterometry are in wide use in semiconductor manufacturing, providing complementary information, such as profile and average CD by OCD and discrete CD, CD variation, and roughness by CD-SEM. These technologies are also beginning to directly support each other through hybrid metrology [7]. However in their present forms, they are beginning to reach physical limitations in usefulness for some applications. Likewise, new variants of these conventional techniques and truly disruptive replacement technologies, such as helium ion microscopy (HeIM), small angle ray scattering (CD-SAXS), environmental SEM (E-SEM), and high voltage SEM (HV-SEM), are now being considered to fill gaps in needed capabilities. Also, these metrology techniques come in two distinct types, as they fundamentally function as either imaging tools such as CD-SEM or as spectroscopic tools such as OCD. Moreover, the availability of each broader tool-type for a given application is important for successful metrology.

Here we explore the "big picture" for in-line semiconductor fabrication CD metrology. First we describe the applications for which CD metrology solutions are needed, showing commonalities and differences among them such that broader application families can be defined. We will then report on the expected limits of the various metrology solutions currently being investigated by SEMATECH to address the metrology challenges of future nodes for these application families, including justifications, for conventional CD-SEM and OCD and new potential solutions such as HeIM, CD-AFM, CD-SAXS, HV-SEM, and other variants. A gap analysis matrix will then be presented, as in Table 1, showing current understanding of the future of CD metrology.

TH–20

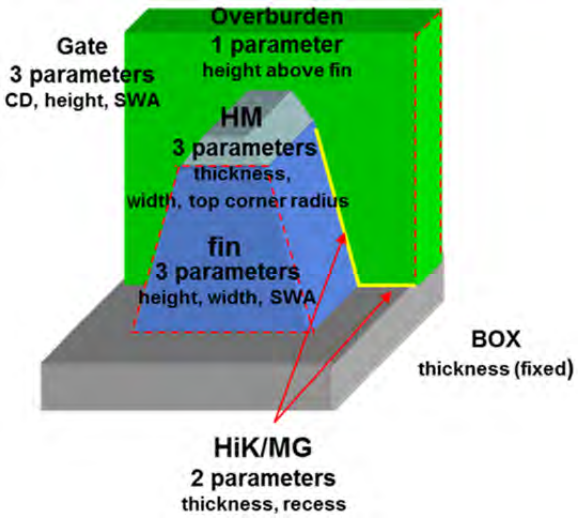


FIGURE 1. Diagram of a basic unit cell of a FinFET, demonstrating twelve important process control parameters. The FinFET is an example of how future devices are truly 3D structures compared to past planar CMOS designs. [1]

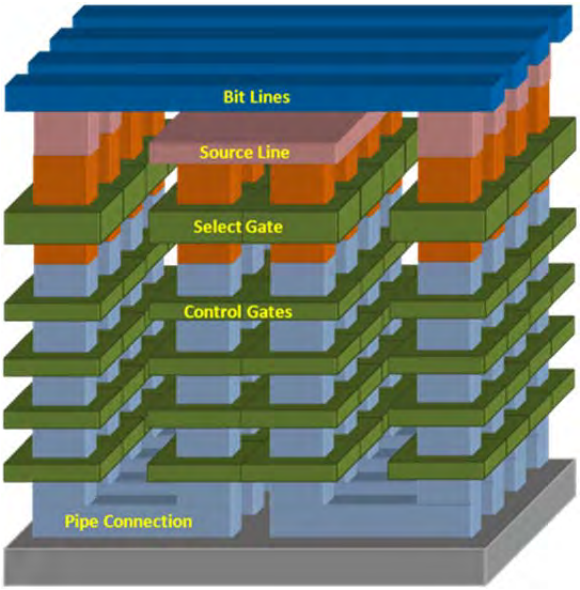


FIGURE 2. Diagram of pipe-shaped bit cost scalable (P-BiCS) flash memory cell, which consists of pipe-shaped NAND strings folded in a U shape; this illustrates how HAR holes and trenches are basic building blocks in future 3D memory devices. [1]

TABLE 1. High level CD Metrology Gaps Analysis. The top section shows the expected outlook of various CD metrology technologies for different application families. From this, possible future roles and areas for improvement for different tool types become more clear. The bottom section rates these techniques for other important characteristics for HVM use.

	<--Imaging Techniques				Spectroscopic Techniques-->					
Application	LV CD-SEM	e/HV CD-SEM	HeIM	CD-AFM	OCD (SE or MM)	OCD (NI / MA)	T-CD-SAXS	GI-CD-SAXS	TSOM	MBIR
2D Litho / hardmask apps									Color Code Key:	
2D Planar Etch apps										limits far away
2D+ Multi-layer planar etch apps									at or near limit, progress needed	cannot cover all important metrics
2D FinFET apps--fin only									maybe--if improved	unknown
3D FinFET apps--gate on fin									maybe--sims predict	
3D HAR apps										

	<--Imaging Techniques				Spectroscopic Techniques-->					
Application	LV CD-SEM	e/HV CD-SEM	HeIM	CD-AFM	OCD (SE or MM)	OCD (NI / MA)	T-CD-SAXS	GI-CD-SAXS	TSOM	MBIR
MAM time									Color Code Key:	
Area of measurement									excellent	high
Destructiveness									okay	very high

TH–20

REFERENCES

1. Bunday, B. "Gaps Analysis for CD Metrology Beyond the 22 nm Node," Metrology, Inspection, and Process Control for Microlithography XXVII. Proceedings of the SPIE, Volume 8681, Invited Oral presentation, paper 8681-57 (2013, publishing pending).
2. The International Technology Roadmap for Semiconductors (San Jose: Semiconductor Industry Association, 2010); available from the Internet: http://member.itrs.net.
3. Bunday, B., Vartanian, V., Arceo, A., & Cordes, A. "Evolution or Revolution: Defining the Path for Metrology Beyond the 22nm Node," Solid State Technology, vol 55, issue 2, March 2012.
4. Doyle, B. et al., "Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout," Symposium on VLSl Technology Digest of Technical Papers, pp. 133-134 (2003).
5. R. Katsumata et al., "Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Operation for Ultra High Density Storage Devices," Symp. on VLSI Tech. Dig., pp136-137, 2009.
6. Aron J. Cepler, Benjamin Bunday, Bradley L. Thiel, and John S. Villarrubia. "Scanning electron microscopy imaging of ultra-high aspect ratio hole features," Proceedings of the SPIE, Vol. 8324, Metrology, Inspection, and Process Control for Microlithography XXVI, 83241N.
7. Vaid, A., et al., "A holistic metrology approach: hybrid metrology utilizing scatterometry, CD-AFM, and CD-SEM," Metrology, Inspection, and Process Control for Microlithography XXV. Proceedings of the SPIE, Volume 7971, pp. 797103-797103-20 (2011).

KEYWORDS

critical dimension, metrology, OCD, CD-SEM, gaps analysis, CD, CD-SAXS, scatterometry

TH–21

FABRICATION AND CHARACTERIZATION OF STANDARDS FOR ATOMIC FORCE MICROSCOPE TIP WIDTH CALIBRATION*

Ronald Dixson[1], Craig McGray[1], Boon Ping Ng[2], Ndubuisi G. Orji[1], Jon Geist[1]

[1]*NIST Semiconductor and Dimensional Metrology Division, 100 Bureau Drive, Gaithersburg, MD 20899*
[2]*Singapore Institute of Manufacturing Technology, 71 Nanyang Drive, Singapore 638075*

INTRODUCTION

The National Institute of Standards and Technology (NIST) has been developing methods and standards for traceable critical dimension atomic force microscopy (CD-AFM). The CD-AFM technique involves flared tips and two-dimensional surface sensing to enable scanning of features with near-vertical sidewalls. [1]

A major source of uncertainty in metrology with CD-AFM is the calibration uncertainty of the tip width. With a new generation of the NIST single crystal critical dimension reference material (SCCDRM) project, we are targeting expanded uncertainties in linewidth (k = 2) below 1 nm.

TIP WIDTH CALIBRATION AND THE SCCDRM PROJECT

The interaction of a CD-AFM tip with the imaged surface is very complex.[2-4] However, for many purposes a simplified, two-dimensional model is useful. In this basic view, the effect of the tip is represented as a simple offset, which must be subtracted from the apparent feature width to obtain an accurate measurement. This offset is referred to as the tip width correction, and there is an uncertainty component that represents the uncertainty in the value of this correction. As a result of the NIST SCCDRM project, which is discussed in the next section, it is possible to calibrate the tip width with a combined expanded uncertainty (k = 2) of less than 2 nm. [2,4] Beyond this correction are the shape-dependent details of the interaction, which are highly specific to each measurement.

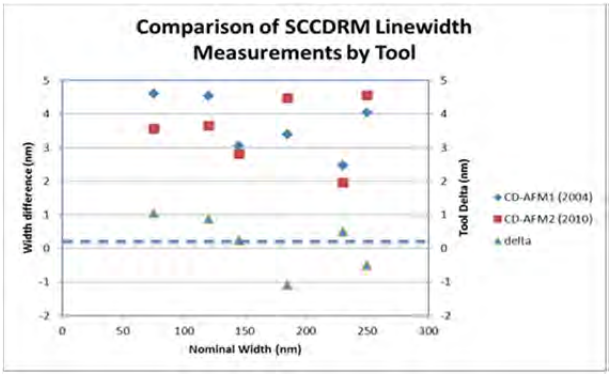


FIGURE 1. Measured line widths of six SCCDRM linewidth features with two generations of CD-AFM.

Figure 1 shows a comparison of linewidth measurements obtained with both our current and prior generation CD-AFM instruments. In both cases, the CD-AFM essentially functions as a width comparator between the target sample and the master/monitor sample – through which the traceability is established.

TH–21

The average difference between measurements of the same features as measured six years apart by two generations of CD-AFM is 0.18 nm. The agreement represented by this average difference is very good, but there were approximately 1 nm deltas for half of the individual features. These were larger than expected, and are not attributable to trivial error sources such as a simple bias in the tip calibration. Our hypothesis is that these differences are due to secondary tip effects (e.g. shape and dither-related contributions). Reducing tip calibration uncertainties below the 1 nm level will require more investigation of such observations.

THE SCCDRM PROJECT

The SCCDRM features have near-vertical sidewalls. This is accomplished using preferential etching on {110} silicon-on-insulator (SOI) substrates.[4] As such, these structures are particularly useful for CD-AFM tip width calibration. The most recent generation has structures with linewidths ranging from 50 nm to 240 nm–and expanded uncertainties (k = 2) of 1.5 nm to 2 nm.

The new SCCDRMs are fabricated using electron beam lithography and a technique for auto-aligning nanostructures to slow-etching crystallographic planes in materials with a diamond cubic structure. A detailed discussion of the fabrication method and AFM evaluation has been published.[5] The method is schematically illustrated in Figure 2. Essentially, the use of offset notches in the drawn feature results in a final etched width that is not affected by small rotational misalignments between the crystal planes and the drawn feature.

In Figure 3 we show a scanning electron microscope (SEM) image of an etched SCCDRM feature with representative CD-AFM profiles in the inset. Note that the CD-AFM profiles are from a different feature and have not been corrected for the tip width.

During a recent fabrication run, we demonstrated line widths as small as 10 nm. Since the uncertainty of a width measurement is significantly affected by the sample non-uniformity, our

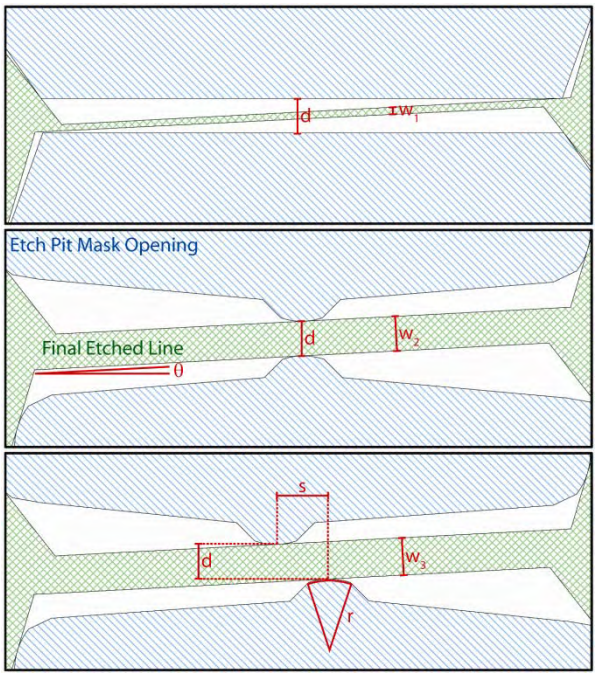


FIGURE 2. Schematic explanation of the auto-alignment method for SCCDRM fabrication. (d represents the drawn width, and w_1 – w_3 represent the final etched widths for different configurations of the as-drawn pattern relative to the crystal planes.)

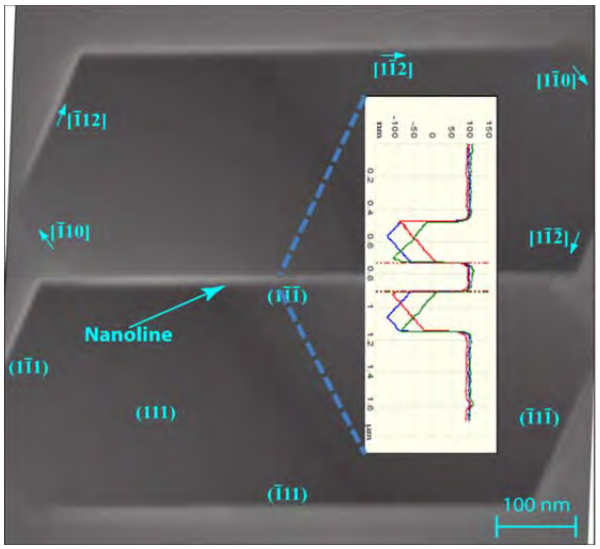


FIGURE 3. Top-down SEM image of a new SCCDRM feature with representative CD-AFM profiles inset.

*Contributions of the National Institute of Standards and Technology are not subject to copyright.

TH–21

priority in screening the SCCDRM features is non-uniformity rather than absolute width.

Figure 4 summarizes AFM line width observations on 29 separate SCCDRM features – indicating both small linewidths and local non-uniformity below 1 nm – as expressed by the standard deviation of width results from 256 linescans taken along the sampled length of each measured feature. A few outliers are present, but the observed non-uniformity is largely independent of feature width.

For feature widths of 10 nm or larger, the new SCCDRM fabrication process works very well and we expect that conventional models of the AFM measurement process, with respect to the tip-sample interaction and behavior, are still valid. However, below the 10 nm level, some conventional assumptions, such as rigidity of the structure during imaging, may have to be refined.

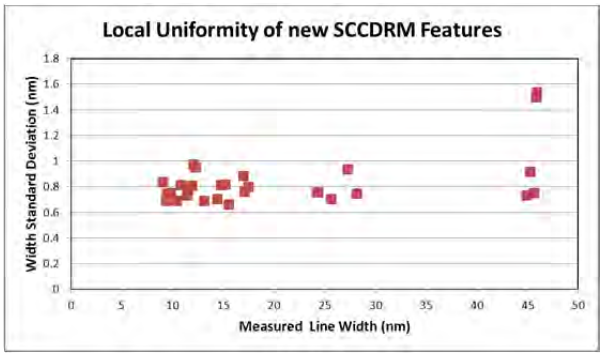


FIGURE 4. CD-AFM results on recent prototype SCCDRMs – showing both very small linewidths and sub-nanometer local non-uniformity.

The first stage of validating the structural integrity and quality of an approximately 10 nm wide feature was performed using high resolution transmission electron microscopy (HRTEM). Details of this work have been published. [2] In this initial evaluation, the feature remained intact during sample preparation, and the observed AFM and TEM linewidths agreed to within 1 nm – less than the combined uncertainty.

In performing such comparisons, a significant complication arises from the line width roughness (LWR) of the features due to uncertainties in the relative positioning of the AFM and TEM measurements.

We have focused considerable effort on improving the etch process to reduce LWR. Since the sidewalls of the SCCDRM structures are Si (111) planes, we are performing an experiment to determine the dependence on etching parameters of the surface roughness in the bottom of etch pits on Si (111).

A recent example is shown in Figure 5. The roughness average Ra in this image is approximately 0.38 nm - about twice the instrument noise floor. This surface is very smooth – and better than most of the sidewalls we have previously etched. We expect to refine the process until the 0.3 nm atomic monolayer steps are clearly observable in our images. Surfaces of such quality have been observed after similar etching techniques. [6]

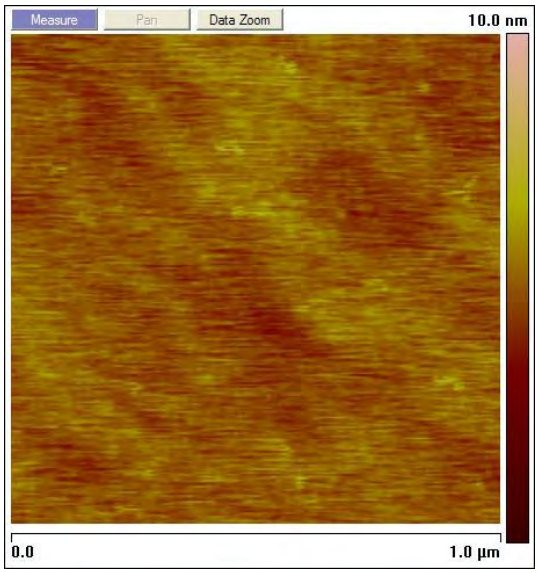


FIGURE 5. Tapping mode AFM image of an etched Si (111) surface. At 0.38 nm, the roughness average Ra is approximately twice the instrument noise floor.

The goal of the SCCDRM effort is to develop a new NIST Standard Reference Material (SRM) for CD-AFM tip calibration. The new SCCDRM features must have width uniformity surpassing the

TH–21

previous generation, and the fabrication process must be consistent enough to yield samples in sufficient quantities for SRM production. These challenges are not trivial, but the current results suggest that our goals are realistic.

REFERENCES

1. Y. Martin, H. K. Wickramasinghe, "Method for imaging sidewalls by atomic force microscopy," *Applied Physics Letters* **64**, 2498-2500 (1994).
2. R. Dixson, N. G. Orji, C. D. McGray, J. Bonevich, J. Geist, "Traceable Calibration of a Critical Dimension Atomic Force Microscope," *J. Micro/Nanolith. MEMS MOEMS* Vol. **11**, 011006 (2012).
3. H.-C Liu, J. R. Osborne, M. Osborn, G. A. Dahlen, "Advanced CD-AFM Probe Tip Shape Characterization for Metrology Accuracy and Throughput," *SPIE Proceedings* Vol. **6518**, 65183K (2007).
4. R. G. Dixson, R. A. Allen, W. F. Guthrie, and M. W. Cresswell, "Traceable Calibration of Critical-Dimension Atomic Force Microscope Linewidth Measurements with Nanometer Uncertainty," *J. Vac. Sci. Technol. B* Vol. **23**, 3028-3032 (2005).
5. C. McGray, R. Kasica, N. G. Orji, R. Dixson, M. Cresswell, R. Allen, and J. Geist, "Robust Auto-Alignment Technique for Orientation-Dependent Etching of Nanostructures," *J. Micro/Nanolith. MEMS MOEMS* Vol. **11**, 023005 (2012).
6. H. Fukidome and M. Matsumura, "A very simple method of flattening Si(111) surface at an atomic level using oxygen-free water," *Jpn. J. Appl. Phys. Vol*. **38**, pp. L1085-L1086 (1999).

KEYWORDS

CD-AFM, tip width, linewidth standard, SCCDRM, lattice-selective etch, traceability

TH–22

SHALLOW PROBE: NON-DESTRUCTIVE COMPOSITIONAL METROLOGY FOR FILMS AND STRUCTURES

Mona P. Moret, Anna Meura, Anne-Sophie Robbes, Michel Schuhmacher

CAMECA, 29 quai des Grésillons, 92 622 Gennevilliers, France

INTRODUCTION

To be able to keep integrating novel functionalities and keep on delivering smarter and higher value products, the nanoelectronics industry is following a path combining the traditional scaling down and an increasing diversification (a.o.: structures, materials, compounds and SoC). In this rich environment there is an increasing need for compositional metrology to: control the element responsible of the key electrical parameters, integrate new active areas, and simply continuously monitor the process.

LEXES has been introduced in logic and memories fabs for more than 10 years and has mainly supported integration of implants for USJ, HKMG and novel oxides, epitaxial layers for p- and n-MOS and is now moving to bring solutions for structures. After reviewing briefly the technique, showing some major applications, we will show detail measurements on recent developments such as enhanced LEXES to measure additional parameters on epitaxial layers stacks.

LEXES

Low energy Electron X-ray emission spectrometry (LEXES) - sometimes called EXES [1] - is a non-destructive characterization technique probing full wafers with a low energy electron beam and analyzing the emitted soft X-rays through wavelength dispersive spectroscopy (WDS). This technique is similar to electron probe micro analysis (EPMA), except for the low energy and high current electron column which has been specifically designed to optimize near-surface instead of bulk analysis. The probing energy can vary from a few hundreds eV to 10keV and the electron beam current can be adjusted from 0.1 to 30µA. The resulting sampling depth ranges typically from top surface down to 800nm. The beam diameter can be adjusted from 15 to 100µm according to the application. The dose of a specific element is measured directly by selecting the corresponding X-ray emission line. For a given energy, the peak minus background (P-B) signal (c/s/µA) is proportional to the dose of the element in at/cm^2 in the probed volume. The P-B quantification is performed from sensitivity factors determined from reference samples. All elements heavier than beryllium can be measured by LEXES. Typical performances will be shown on lanthanum for HKMG and implants in Si.

EPITAXIAL LAYERS METROLOGY

Strong device performances in CMOS are ensured by two different types of stressors at the 22nm node and below.

SiGe B stacks are used for the p-type MOS whereas Si:C P stacks are used for the n-type MOS. These systems are grown by low – temperature

TH–22

CVD processes, therefore a tight metrology is required for these critical steps, as they are the backbone of the final performances of the devices. The control challenges and needs increase as the epitaxial processes intensifies in complexity and as the layer evolve into stacks and are engineered with different dopant concentrations.

In – line metrology techniques are required to measure the dose and concentration of the dopants (P and B) as well as Ge and C in both blanket and patterned (or production wafers). Traditional techniques such as ellipsometry, XRD and scatterometry are used commonly but LEXES is the technique of choice for dopant control and / or Ge in relaxed system or C. LEXES is able to quantify light dopant (C, B, P) as well as major matrice element as Ge. The LEXES can probe the material at different energies and therefore extract depth information from its signal. In the first part we will describe global parameters and the second part the advanced depth information that can be retrieved by LEXES on SiGe:B advanced stacks.

Single Layers or Global Stack Metrology

In this approach, global depth information can be monitored on a single layer. The parameters are the Geat% and the SiGe thickness as well as B concentration and Si(C)P thickness, and C concentration. For a stack the same parameters are measured and corresponds to the whole thickness and the average concentration. Performances on blanket and patterned wafers will be shown. In the figure below a mapping of the C dose in a SiCP wafer is shown.

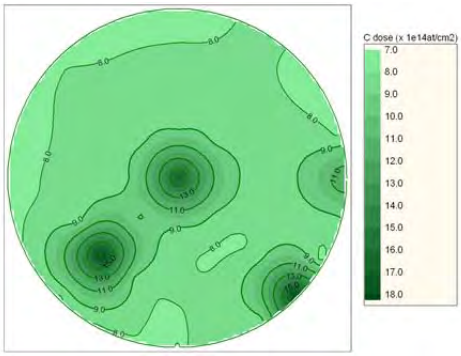


FIGURE 1. Total C dose signature in a SiCP/SiP stack n-MOS on 300 mm wafer. The non-uniformity is 27%

Stacks: Lexes Enhanced Metrology

Recent advances in our LEXES signal interpretation permit us to extract additional in-depth information. This allows LEXES to measure new parameters on stacks, such as top and bottom concentration in graded layers. Examples will be shown on graded SiGe layers. This potential will be investigated experimentally on other stacks.

Measurements on Structures

Up to now, metrology on blanket or pads could be sufficient. Today as the devices shrinks, as the growth / deposition gets more complicated, and due to the presence of loading effect, metrology is required at the device level. Characterization at the single device level such as APT or TEM is destructive. SIMS on an array of devices (or units) is also destructive. LEXES offers an alternative to measurement on an array of units in a non-destructive manner. As the signal is direct, relative compositional comparison across a wafer is always possible. Nevertheless accurate quantification in, non –homogenous laterally and vertically probed materials, is more complicated. Some examples will be shown on simple array.

References

1. P. F. Staub, *Microscopy and Microanalysis* **12** (6), 340 (2006).

Keywords

Compositional Metrology, Non-destructive, LEXES, Implants, Films, Structures

TH–23

DEVICE-LEVEL ELECTRICAL CHARACTERIZATION USING FERROMAGNETIC RESONANCE OF MAGNETIC MULTILAYERS

Eric R. Evarts, Matthew R. Pufall, and William H Rippard

Magnetics Group, Electromagnetics Division
NIST, 325 Broadway, Boulder, CO 80305

INTRODUCTION

Nanometer-scale spintronic devices based on magnetic materials are being explored for applications ranging from memory to logic, driven by the promises of low energy operation, nonvolatility, and novel functionality. Spintronic devices based on the spin-transfer torque effect are a true nanotechnology, in that they show emergent behavior as device dimensions decrease. As a consequence, the function of a device can also depend on the details of the magnetic properties such as magnetization, anisotropy, and defects, at nanometer length scales. Spin transfer torques can cause large-angle, nonlinear magnetization dynamics of amplitudes not readily accessible via applied fields, dynamics that are sensitive to the details of the local magnetic properties. We have developed new electrical metrologies that utilize magnetoresistance and the spin transfer torque effect to quantify the high frequency behavior of fully functional individual devices, and are able to correlate these behaviors with particular magnetic processes.

For MRAM elements, we measure write error rates at 1 part in 10^6 accuracy and correlate these errors with device-level ferromagnetic resonance spectra of magnetic modes. Additionally, we compare device-level ferromagnetic resonance spectra collected using only a DC current excitation to those collected using an AC current excitation.

RESULTS

In the following section we present some of our measurements of spin torque switched MRAM devices patterned at NIST, results that will be expanded upon in the presentation.

WRITE ERROR RATES

Over the past several years, spin torque MRAM (STT-MRAM) has moved from the laboratory to demonstration product,[1-3] with read and write performance testing moving from tens of events to greater than 10^6. New physics has emerged particularly in the infrequent events measured in write error rate (WER) testing, in which the performance of some devices can deviate significantly from the "macrospin" or single magnetic domain model.

Fig. 1a shows the WER of a typical 60 nm x 180nm elliptical magnetic tunnel junction device, with a stack consisting of (thicknesses in nm) bottom/Ta(5)/PtMn(20)/CoFe(2.5)/Ru(0.8)/CoFeB(2.5)/MgO(1.0)/CoFeB(4)/Ta(10)/top. The top layer is called the "free layer" and can switch between two stable states along the long axis of the ellipse, depending on the direction of the current pulse injected into the device. As seen in Fig. 1b, for

TH–23

some devices, the write error rates with increasing voltage for devices with in-plane magnetization can deviate from the single exponential predicted by the single domain, (dual potential well) model.

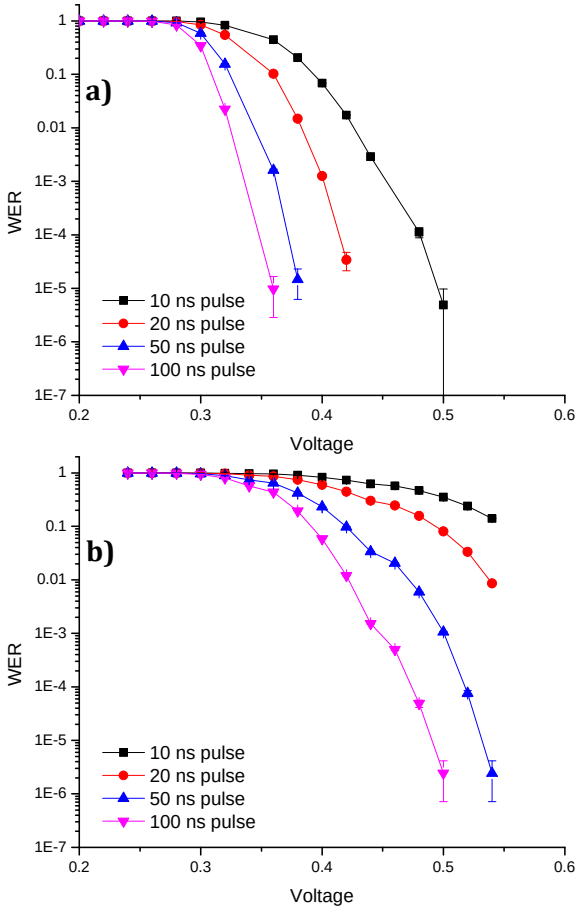


FIGURE 1. a) WER of a typical 60 nm x 180 nm device; b) WER of an anomalous 50 nm x 150 nm device.

Device-Level Ferromagnetic Resonance: Spin Torque

Using spin-torque, we can measure the normal modes of oscillation of a single device using spin-torque induced ferromagnetic resonance (spin torque FMR). An ac current is injected into the device, producing an ac spin torque that induces precession and an ac resistance change, and a rectification voltage is produced by the combined ac resistance and current.

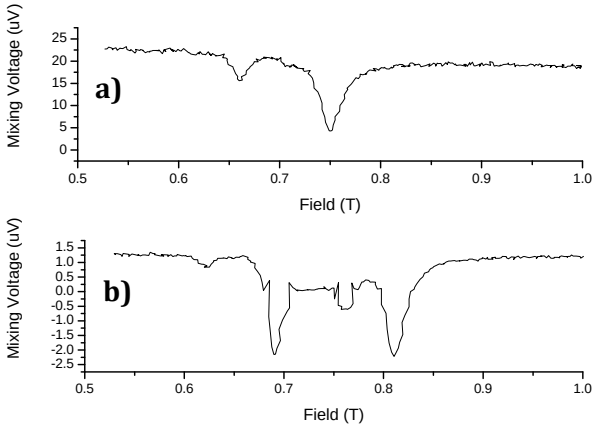


FIGURE 2. a) Spin torque FMR spectrum of the device in Fig. 1a collected at 300 mV DC bias, 15 GHz. The single prominent peak indicates nominally single domain behavior; b) Spin torque FMR spectrum of the device in Fig. 1b collected at 300 mV DC bias, 15 GHz. The two equally prominent peaks indicate that the magnetization is not behaving like a single domain.

As seen in Fig. 2a, multiple resonances are visible as a function of frequency, indicating that the device is not acting as a single domain. Similar spectra are seen for all devices of this size. Nonetheless, in many devices the WER distributions appear as those expected for a single domain. However, we can correlate variations in these spectra with variations in write error rates. In particular, in Fig. 2b, the spin torque FMR spectrum for the anomalous device from Fig. 1b shows two equally prominent resonances, which indicates that the device is strongly deviating from the mostly single domain behavior seen in Fig. 2a. These measurements support the idea that these events result from deviations from single-domain behavior, and that nanostructure in the device is affecting function.

Device-Level Ferromagnetic Resonance: Thermal

In the previous section, we outline measuring the ferromagnetic resonance spectrum by driving the device with a small ac current. Another commonly used method for measuring the ferromagnetic resonance spectrum is to apply a small dc current to the device to add energy to the

TH–23

system and then measure the noise power spectrum. This technique is commonly referred to as thermal ferromagnetic resonance because it is expected that all modes will be uniformly excited by the thermal energy and the small dc current is only for providing a measurable magnetoresistance signal.

We have quantitatively compared the results obtained on devices using both spin torque FMR and thermal FMR. By fitting out the resonance spectra, it is possible to correlate the results from the two techniques as shown in Fig. 3. When both techniques detect a resonance, the resonance frequency and line width agree within experimental error. Surprisingly, there is a resonance peak detected in spin torque FMR that falls between the two resonance peaks detected in the thermal FMR measurements. This resonance peak never appears in the thermal FMR spectrum even at bias currents approaching the dielectric breakdown of the tunnel barrier.

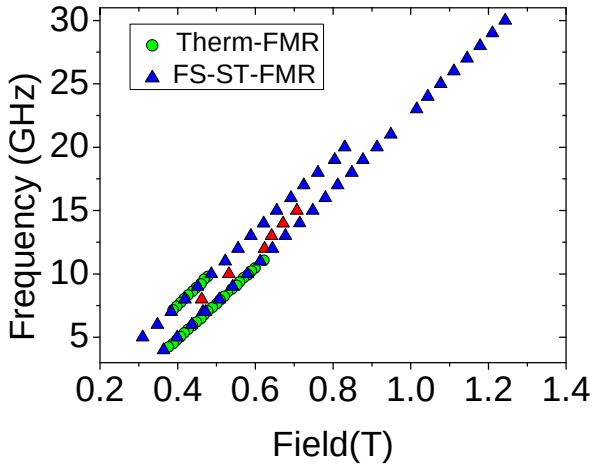


FIGURE 3. Fitted resonance peak position for a single device using both thermal FMR and spin torque FMR. The red triangles indicate a resonance mode only excited by spin torque FMR.

Using micromagnetic simulations, we have determined that the mode only excited in spin torque FMR measurements requires an excitation with an odd symmetry along the long axis of the elliptical device. In spin torque FMR, the ac current produces an alternating circumferential Oersted field with an estimated peak to peak magnitude of 0.2 mT to 0.5 mT for the ac currents used here[4]. This small oscillating field could be enough to break the symmetry and allow the spin torque FMR measurement to couple into this mode, whereas the constant Oersted field produced by the dc current in thermal FMR might not break the symmetry and therefore excludes this mode.

REFERENCES

1. J. Slonczewski and J. Sun, J. Magn. Magn. Mat. **310**, 169–175 (2007).
2. M. Gajek, et al., *Appl. Phys. Lett.* **100**, 132408-132411 (2012);
3. J. Sun, et al., *Phys. Rev. B* **84**, 064413-064422 (2011).
4. V.V. Naletov, et al., *Phys. Rev. B* **84**, 224423 (2011).

KEYWORDS

STT-MRAM; magnetics; spintronics; microwave measurements; ferromagnetic resonance; nonlinear oscillators; NonBoolean;