PTP Power Profile Conformance & Interoperability Assessment

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(UNH-IOL)

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IEEE NIST
Timing Challenges in the Smart Grid Workshop

A brief background

About the speaker

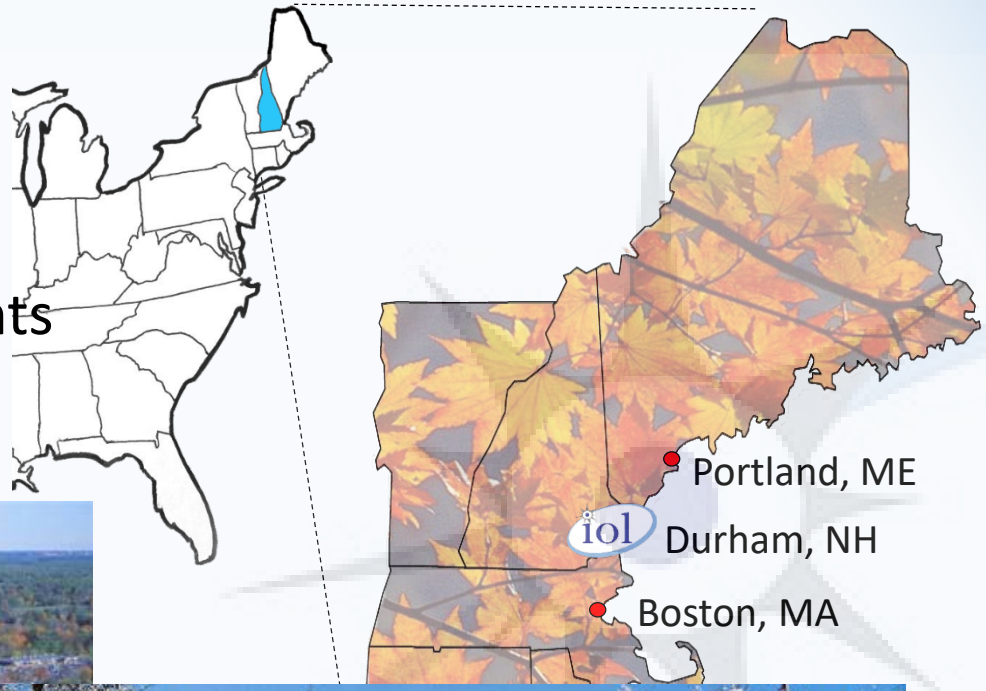
- Chief Engineer at the University of New Hampshire's InterOperability Lab
- Testing conformance & interoperability (C&I) of Ethernet for >20 years
- Developed C&I Test Plans and Tools for 802.1AS (gPTP)
  - To date, **over 80 gPTP devices have been certified**
- Working with NIST and IEEE-SA ICAP to develop test suite specification for the IEEE 1588 Power Profiles
- Supported by NIST grants and industry members to enable validation of 1588 time synchronized devices in the smart grid.

University Of New Hampshire

Founded in 1866

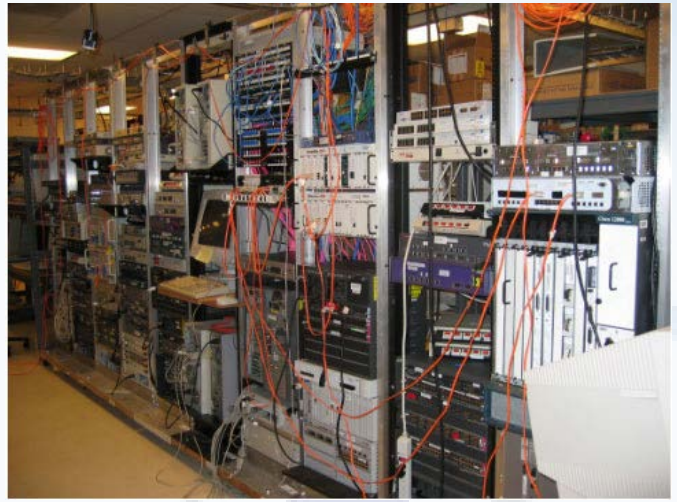
Main campus located in Durham, New Hampshire

12000+ undergraduate students, 2000+ graduate students



InterOperability Laboratory

The UNH-IOL is a non-profit neutral, third-party laboratory dedicated to testing networking technologies through industry collaboration.



Performing Ethernet testing since **1988**

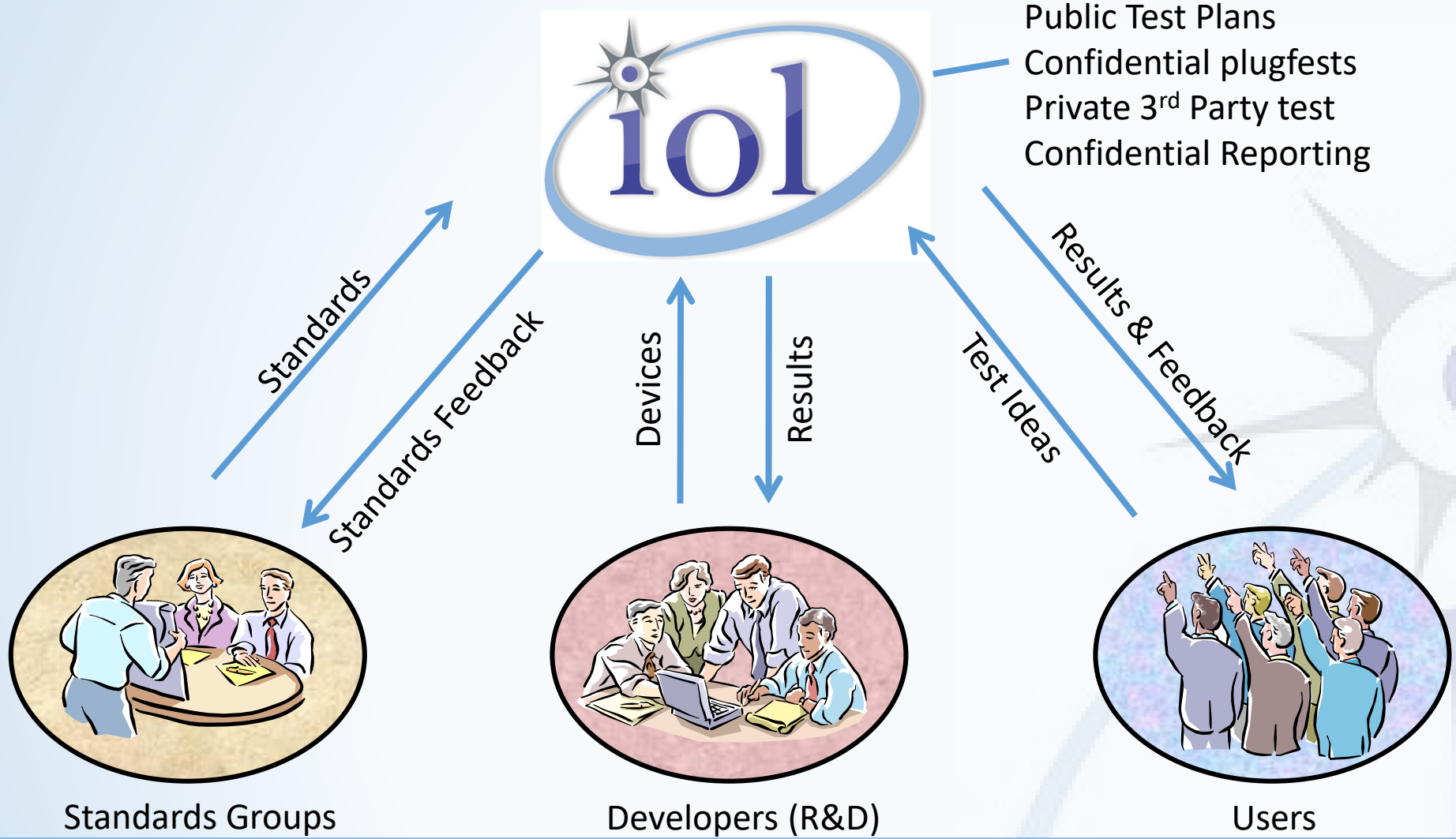
- UNH-IOL Tests are listed on iol.unh.edu for public review
- **100% Industry funded development and test**
  - (+2 NIST grants for power conformity and security work)

Industry leading test facility for data, telecom, storage and time sensitive networking technology & consumer electronics

32,000 sq. ft lab facility

- 5,400 sq. ft pre-wired space dedicated to Plugfests
- >150 Employees, >20 full time staff

UNH-IOL Industry Engagement



Standards / Test Plan / Tools / Testing

Standards:

- IEEE 61850-9-3
- IEEE C37.238-2016
  - Interoperablity requirements
  - Testability requirements

Testing:

- Test execution yields issues
- Issue resolution improves products, tools, test plans, and standards.

Test Plan:

- Details conformance & interoperability test procedures
  - Tool agnostic

Tools:

- Industry standard tools
- Automation Test Harnesses
  - Instantiate Test Plans
  - Multiple solutions
  - Enables 1st & 3rd party common test

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Conformance and Interoperability

- Conformance test **predicts** future interoperability
- Interoperability test **proves** current interoperability

  - Both are essential. Conformance testing is only as good as:
    - The standard's coverage
    - The test plan's coverage
    - The test tools employed
  - Interoperability testing is only as good as the devices, topologies and traffic patterns scrutinized

Why do we need conformity assessment?

The following slides from IEEE-SA ICAP Overview

IEEE Conformity Assessment Program

- IEEE Conformity Assessment Program (ICAP) is a critical component of IEEE SA‟s Standards Implementation services
- ICAP started in 2008 and is wholly operated by IEEE-SA
- ICAP provides an industry support and operational structure that bridges standards development activities with the conformity assessment activities
- ICAP is an important initiative in achieving IEEE SA's strategic objectives and will have ongoing support from SA and IEEE
- ICAP programs **ensure interoperability and accelerate market acceptance** and enable new products and technologies in support of IEEE Standards

Understanding Conformity Assessment

- What is Conformity Assessment?
  - Conformity Assessment is defined as the process or processes that are used to **demonstrate that a product or service meets specified requirements** (set forth in Standards, Test Plans, etc.)
- Conformity assessment
  - Provides assurance and confidence a product or service meets requirements
  - **Empowers the user to make better purchasing decisions**
  - Benefits the supplier as products may gain market acceptance
- Conformity assessment activities include:
  - Conformance, Interoperability, Inspection, Accreditation
  - “Catch-all” term to address range of test-related activities

Benefits of Implementing a Conformity Assessment Program

- Benefits of conformance test before deployment implementation
  - Early identification of non-conformances
  - Exact functionality of the protocol is identified
  - Multi-vendor solutions will have interoperability issues – helps identify such issues
  - New offerings will have bugs – helps to catch them
- **Reduces the vendor's cost**/need for re-tests for different end-users
- Establishes a baseline for performance expectation
  - Eases interoperability
- Transparency based on common implementation/Test Authority

IEEE 1588P CASC Charter

- CASC: **Conformity Assessment Steering Committee**
  - Committee comprised of industry experts from standards, manufacturers and utilities
  - Products used by end users (utilities) should conform to current approved version of IEEE 1588 & C37.238 revision
  - Product conformity should be certified
  - Testing should be performed according to the IEEE 1588 Power Profile Test Suite Specification (TSS) – to be developed by this committee
  - Testing should be assessed by **third party** independent experts

Goals of IEEE 1588P CASC

- Author, review and approve IEEE 1588 Power Profile TSS (Test Suite Specification)
  - Will continue as a standing committee to update and revise TSS as needed
- Advise ICAP about viability of a certification program based on the IEEE 1588 Power Profile TSS

A glance at the IEEE 1588 Power Profile Test Suite Specification

- Coverage includes PTP Attributes; Path Delay Mechanism; Best Master Clock Algorithm; Transport Mechanism; Timescale; TLVs; Time Inaccuracy; VLANs

Generic Test Format

Tests are abstract definitions of test semantics, with **generic** tools

- Purpose
- Device type and Prerequisites
- References
- Resource Requirements
- Modification History
- Discussion
- Test Setup
- Test Procedure
- Observable Results
- Possible Problems

Test PWR.c.2.7 – Restriction on Peer Delay Mechanism

Purpose: To verify that the proper action is taken after the receipt of zero or multiple Pdelay_Resp messages.

Device Type Prerequisites and Certification Classifier:

Part	Applies To Device Type	Prerequisite Conditions
A	All	None
B	OC, BC	None
C	TC	None

References: [1] IEEE Std 1588-2008: sub-clause 11.4.4

Resource Requirements: Two test stations capable of transmitting and receiving arbitrary MAC frames

Modification History: 2012-02-19 Preview release

Discussion: This test will verify that the proper action is taken after the DUT receives a varying number of Pdelay_Resp messages by observing whether the DUT port retransmits a Pdelay_Req message or enters the FAULTY state. Specific actions should be taken after the delay requester, Node-A, receives 0, 1 or multiple Pdelay_Resp messages for a transmitted Pdelay_Req [1]. The receipt of multiple responses can be detected by observing that the sourcePortIdentity fields of the Pdelay_Resp messages differ. When no Pdelay_Resp message is received, Node-A should periodically retransmit a Pdelay_Req message to check for the appearance of Node-B. The standard does not specify a retransmission rate, so this test produces a result of WARN if no retransmitted Pdelay_Req is received within 10 seconds. When a single Pdelay_Resp message is received, the protocol of 11.4 should be executed. When multiple Pdelay_Resp messages are received, ordinary and boundary clock ports should enter the FAULTY state, and peer-to-peer transparent clocks should enter a fault condition. For this case, the device may periodically retransmit a Pdelay_Req message and the port must discard received Sync and Follow_Up messages.

Refer to Appendix C Table 4: Action after Receipt of Pdelay_Resp Message

Test Setup: Refer to Appendix A: DEFAULT TEST SETUP.

Test Procedure:

Part A: 0 Pdelay_Resp Received

A:1. Capture traffic received by TS1 for the duration of this test.
A:2. Wait up to 10 seconds for 3 Pdelay_Req messages to be received from the DUT.
A:3. Respond to five consecutive Pdelay_Req messages from the DUT with Pdelay_Resp and Pdelay_Resp_Follow_Up messages, observing whether the DUT continues to send Pdelay_Req messages.
A:4. Stop responding to the DUT's Pdelay_Resp messages.
A:5. Wait up to 10 seconds for a Pdelay_Req message to be received from the DUT.

Observable Results:

Part:Step	Status	Description
A:2	FAIL	No Pdelay_Req message is received.
A:3	FAIL	The DUT stops sending Pdelay_Req messages.
A:5	WARN	The DUT does not transmit another Pdelay_Req within 10 seconds.
A:5	PASS	The DUT continues to transmit Pdelay_Req messages.

Generic Test Tools

- Abstract test allows focus on standard's requirements, not test implementation
- Non exclusive tools

Part B: Multiple Pdelay_Resp Received

B:1. Capture traffic received by TS1 for the duration of this test.
B:2. With TS2 as grandmaster, send valid Sync and Follow_Up messages from TS2.
B:3. Wait up to 10 seconds for the DUT to forward the Sync and Follow_Up messages received at DUT.TS2 out DUT.TS1.
B:4. Wait up to 10 seconds for 3 Pdelay_Req messages to be received from the DUT.
B:5. From TS1 and within a single Pdelay_Req interval respond to a Pdelay_Req message with two Pdelay_Resp messages, each with differing sourcePortIdentity fields.
B:6. Using SNMP or a vendor-provided method, observe whether DUT.TS1 enters the FAULTY state.
B:7. Observe whether DUT.TS1 discontinues forwarding Sync and Follow_Up messages received from TS2.

Observable Results:

Part:Step	Status	Description
B:3	FAIL	Sync and Follow_Up messages are not forwarded.
B:4	FAIL	No Pdelay_Req message is received.
B:6	FAIL	The device does not enter the FAULTY state.
B:6	FAIL	No FaultyState notification is received indicating the device has entered FAULTY state.
B:7	FAIL	The device continues forwarding Sync and Follow_Up messages.
B:7	PASS	The device enters the FAULTY state and stops forwarding Sync and Follow_Up messages.

Example of a test implementation

- The **correctness of the test should be abstracted from the gory detail** of its implementation

```
32  # 1.b. Ensure that the DUT is sending Pdelay_Reqs.
33  event RcvdFirstPdelayReq create
34  proc  RcvdFirstPdelayReq {} {
35      # Fail if no Pdelay_Reqs arrived.
36      if { [string length [packet firstPdReq get]] == 0 } {
37          log FAIL "$::RED_L FAIL. No Pdelay_Req received within \
38              $::PDELAYREQ_WAIT ms. $::RED_R" GUI-RUN
39          s_shutdown
40      }
41
42      # Log the arrival.
43      set DUT_MAC_PROBED [tm2ws [packet firstPdReq get Ethernet.srcMac] ]
44      log INFO "$::EM_L $::BLU_L received first Pdelay_Req $::BLU_R from \
45          $DUT_MAC_PROBED $::EM_R" GUI-RUN
46
47      # Reply to subsequent Pdelay_Reqs.
48      trigger trigPdReq enable event RcvdPdelayReq repeat
49      log INFO "$::EM_L sending Pdelay_Resps and follow-ups $::EM_R" GUI-RUN
50
51      # Await an Announce message.
52      log COMMENT "A:2 Observe the clockClass member of the grandmasterClockQuality field in the DUT's Announce messages \
53          received at TS1." GUI-RUN
54      trigger trigFirstAnnounce enable event RcvdFirstAnnounce
55      log INFO "$::EM_L expecting first Announce $::EM_R" GUI-RUN
56  }
```

Ongoing and Next Steps: IEEE ICAP; UNH-IOL & NIST

Ongoing and Next Steps

UNH-IOL: Complete TSS with CASC feedback and review

IEEE ICAP: Adopt and Maintain TSS

- NIST and CASC reviewed Test Suite Specification to be adopted as baseline for conformance test

UNH-IOL: Continue Tool Vendor / Solution engagement, complete implementation of TSS for C&I test

Beyond 1588 Conformance

- Interoperability Test Plan in development
  - Interop test plans are not a “straight line” from standard requirements to test procedure.
  - **Input from stakeholders is essential**
    - Define relevant topologies and test cases

Potential Future Items:

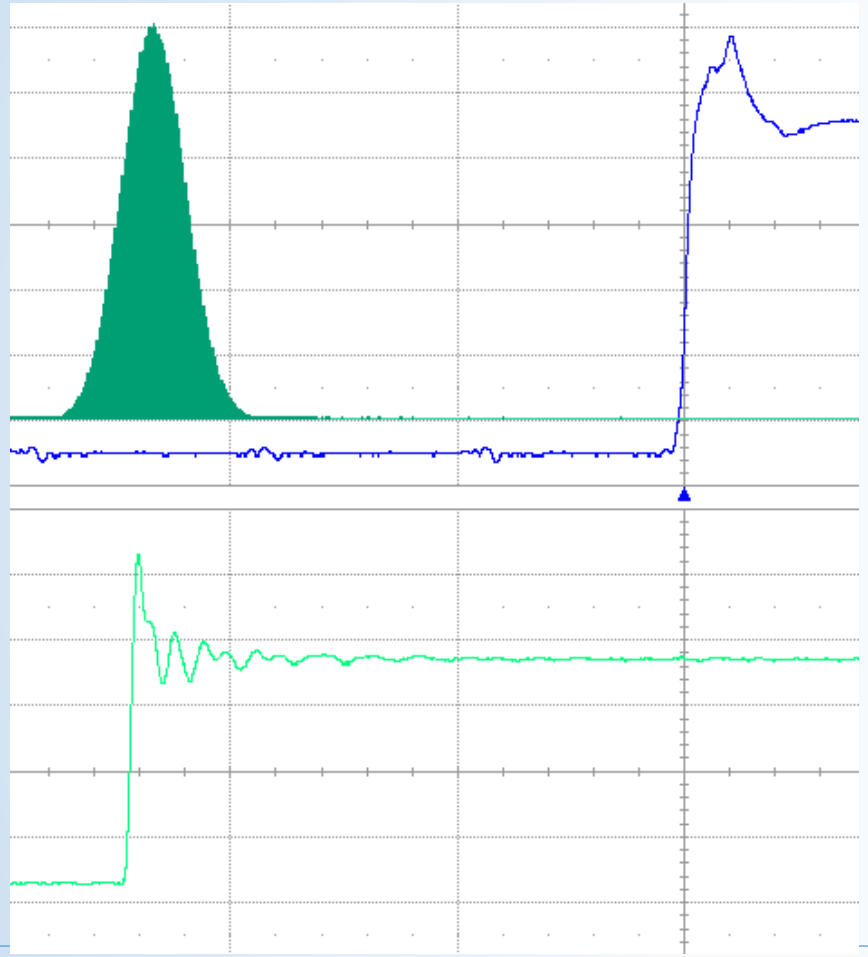
- Conformance test of Timing Redundancy Mechanisms
- Examine Integrated Security mechanisms (Integrity TLV)

Future Steps: 1588 Revision Work

IEEE P1588 Revision

- Revision on track
  - IEEE 1588 Working Group Plenary hosted by UNH-IOL just completed Oct 14
  - Of many improvements:
    - Enhances Performance Monitoring Data Sets
    - Defines Slave Event Monitoring (enables “Digital 1PPS”)
- Updates in the standard (planned 2017)will drive further profile updates
- IEEE 1588 Working Group committed to ongoing role in:
  - Maintenance
  - Errata / Corrigenda publication
  - Continued standardization effort as warranted

Traditional 1PPS monitoring:



- *Scope capture of 1PPS GM (blue) vs Slave (green) with Slave's histogram of timing error over 2 million observations*
  - *Typical Gaussian Jitter around a static offset error*
  - *Real? Or due to unknown/uncalibrated 1PPS delays?*
- ***1PPS itself is not error free***
- *Continuous in-field monitoring of 1PPS signals is simply not practical*
- *Many/most emerging IoT applications utilizing PTP do not expose 1PPS*
  - *Pins/pads are not cheap, and even if available, may not be populated*
  - *(show me the 1PPS output on your phone…)*

A Tool Box for Monitoring

- 1588 Revision includes standardized timing tools to enable network visibility of slave timing error that is verifiable in the lab and actionable in the field.
  - Defined as a “Tool Box” of capability, customizable to specific monitoring needs
  - https://ieee-sa.imeetcentral.com/1588/file/43739452/
  - (for access join the IEEE 1588 WG: https://ieee-sa.imeetcentral.com/1588public/)

- A **network-based mechanism providing application-independent feedback** enables faster, lower-cost evaluation, troubleshooting, and diagnostics. Such a solution also enables novel monitoring aspects useful for safety and security monitoring of a deployed System.
  - Faster – sampling can be greater than once per second
  - Lower-cost – no dedicated pin/pad on silicon required, no need for specialized port to be populated on a box

Need for Monitoring of Timing Error

- "Due to the lack of secured timing sources globally available today, a reasonable approach to securing time is to ensure systems can maintain timing within the tolerance of their application for the duration of a timing compromise**. The future vision of secure time is to ensure timing compromises can be detected sufficiently early** such that systems dependent on accurate and precise timing can seamlessly function under compromised conditions without any performance impact to the CPS."
  - *SOURCE: B.6.4.3, FRAMEWORK FOR CYBER-PHYSICAL SYSTEMS*, RELEASE 1.0

Questions

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Participate in our

UNH-IOL 1588 Consortium

and Test Bed

www.iol.unh.edu/1588