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CRACK EVOLUTION IN Cu/LOW-K STACKS AND CRACK STOP EVALUATION USING IN-SITU MICRO-DCB IN A NANO-XCT TOOL

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MOTIVATION

- Chip-package interaction (CPI) is one of the major reliability concerns in microelectronic products, using low-k and/or ultra-low-k materials in the on-chip interconnect stack, because of the low fracture toughness of these materials.
- To prevent chip damage as cracking, e. g. originated by micro-cracks during dicing, so-called crack-stop structures are integrated.
- Crack pathways have to be imaged nondestructively at high-resolution to estimate reliability risks.
- The study of high resolution microscopy and micro-mechanical experiments of the implemented crack-stop structures allows to understand critical reliability issues as crack propagation in BEoL stacks for advanced´technology nodes.

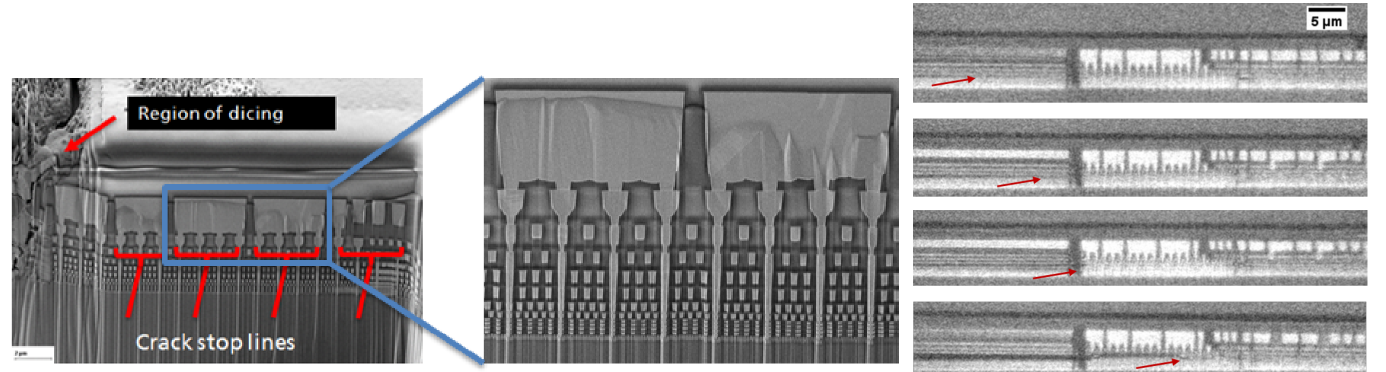

Figure 1
Left) SEM cross-section images with crack-stop structures of an Intel processor with 12 Cu metallization layers.
Right) Series of the virtual cross-sections based on nano-XCT, revealing the crack propagation at the Cu/low-k crack-stop structure.

HIGH-RESOLUTION IN-SITU CRACK PATH STUDY

A miniaturized micro double cantilever beam (µDCB) in-situ test is performed in an x-ray microscope (Xradia nanoXCT-100), which allows sub-100nm resolution with Cu-Kα.

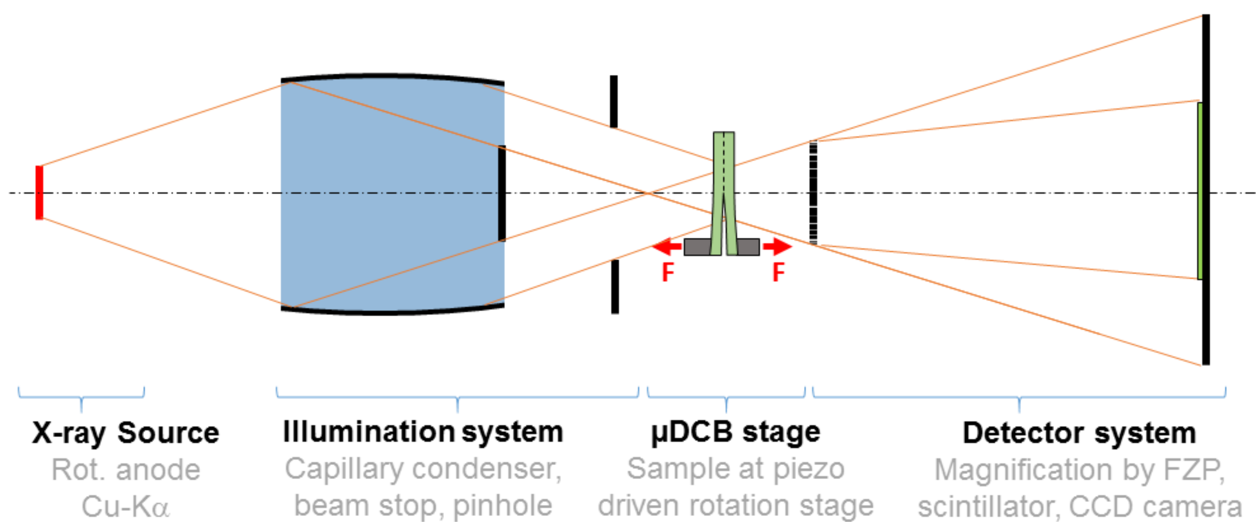

Figure 2
Scheme of µDCB stage inside nano-XCT.

Considering the mass-absorption coefficients of the materials (Cu/low-k stack), samples were prepared mechanically with a thickness of about 50 µm (field of view 65 µm).

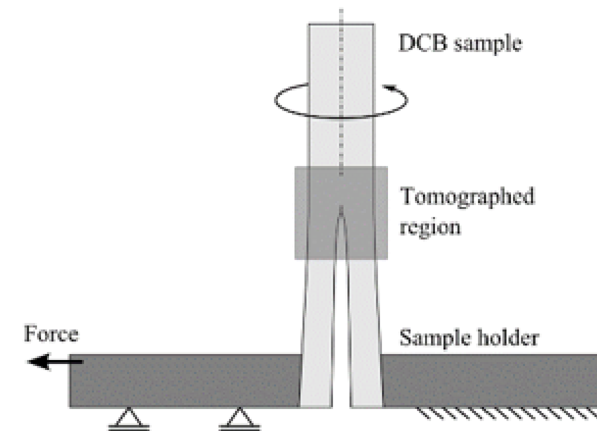

Figure 3
Schematic drawing of the µDCB test.

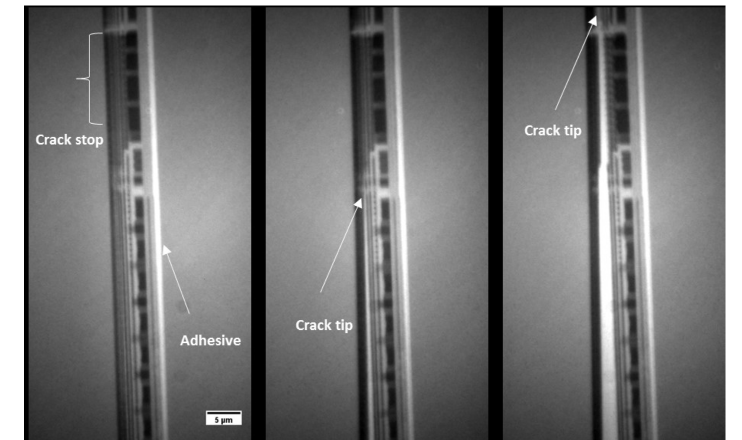

Figure 4
Series of radiographs during µDCB test represent the crack propagation into crack-stop structure.

CRACK PATH STUDY IN Cu/LOW-K STACKS OF INTEL MICROPROCESSOR

The initial crack was mechanically initiated in the BEoL stack.

Sample design allows to study the crack propagation towards the crack-stop structure from both sides: chip interior and scribe line (Figure 5).

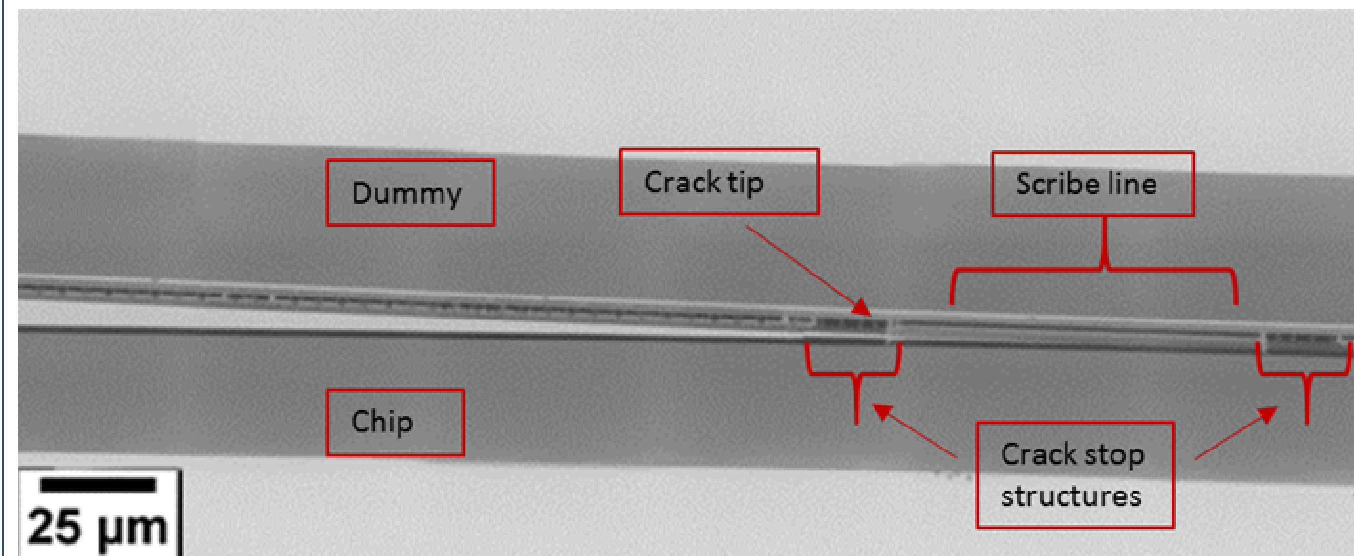

Figure 5
Stitched radiograph of a µDCB sample under load. The crack penetrates the crack-stop structure from chip side. The image is rotated clockwise by 90°.

Delamination occurred typically inside the metallization layer where it was induced until it reached the crack-stop pattern and the crack changed the direction of propagation at the crack-stop structure, in metallization layers 8 to10 in Figure 6.

SEM images (Figure 7) of crack surface after the µDCB test (crack propagated from left to right: Figure 6).

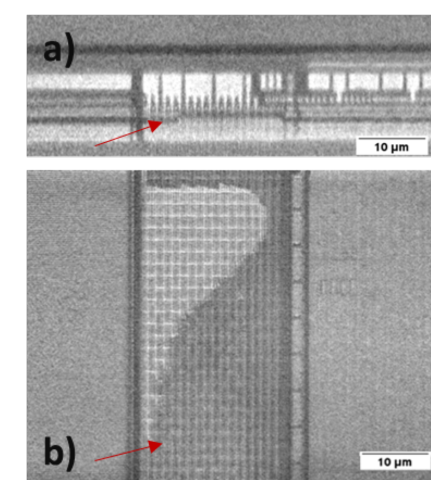

Figure 6
Virtual cross-sections based on nano-XCT:
a) Vertical view: delamination between metallization layers (crack path) and
b) Horizontal view: delaminated area (dark) within the metallization layer (here M8).

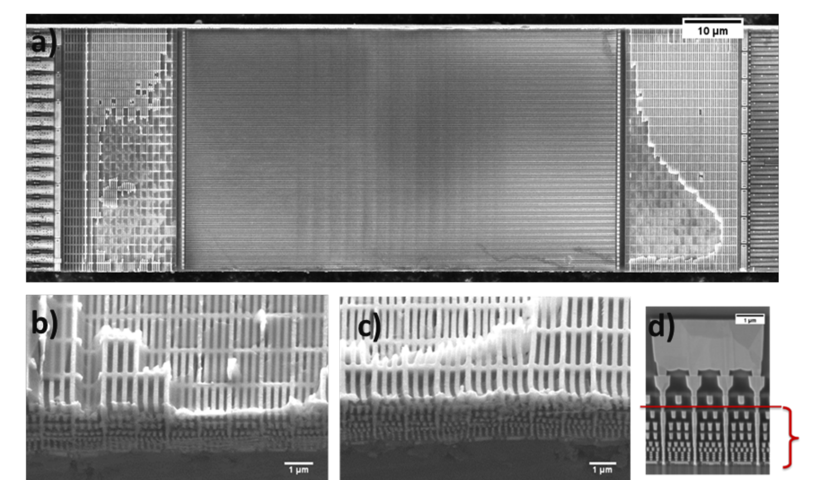

Figure 7
SEM images:
a) Overview of the crack surface with two fractured crack-stop structures and at higher magnification.
b) and c) Comparison of the number of the damaged layers with non-damaged structure.

ACKNOWLEDGEMENTS

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REFERENCES

[1] R. Radojcic, M. Nowak, M. Nakamoto, "TechTuning: Stress management for 3D Through-Si-Via stacking technologies", AIP Conf. Proc. 1378, 5 - 20 (2011)
[2] S. Niese, "Lab-based in-situ X-ray microscopy – Methodical developments and applications in materials science and microelectronics", PhD thesis, BTU Cottbus (2015)
[3] K. Kutukova, J. Gluch, Y. Standke, E. Zschech, Crack path localization in Cu/low-k stacks during micro-DCB tests using nano-XCT", IEEE TDMR, in press (2017)

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