Automatic Detection Of Dislocations In Strained SiGe With HCl Etch And Brightfield Inspection

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INTRODUCTION

The use of strained SiGe as channel material is one method to increase the carrier mobility in 3D transistors (FinFETs). Interfacial defects at the bottom will cause *threading dislocations* that can extend up to the surface, relieving strain and degrading the electrical performance. These defects can be too small to be detected prior to film deposition.

One way to monitor defects has been a *highlighting etch with SECCO or HCl*. The resulting pits can be counted manually under a microscope. This technique can only sample small areas and is not applicable to patterned structures with actual fins.

In this study we improved the method by using *brightfield defect inspection (BFI) to detect and count etch pits* automatically over a larger area across the wafer.

METHOD DEVELOPMENT

We developed a method for highlighting and automatic detection of dislocations. This method was developed on planar pads on every chip of a wafer. Vaporous ***HCl etching was performed to highlight the dislocations*** at the surface in the chamber that is also used for the epitaxial growth of the SiGe and Si films. The same wafer can be etched again and again to investigate how the defects develop over increasing etch times. *A **brightfield inspection tool was used for the detection of the etch pits***. Defect counts were recorded before and after epi growth as well as after each etch step. Several defects were reviewed in a scanning electron microscope (SEM) after each inspection.

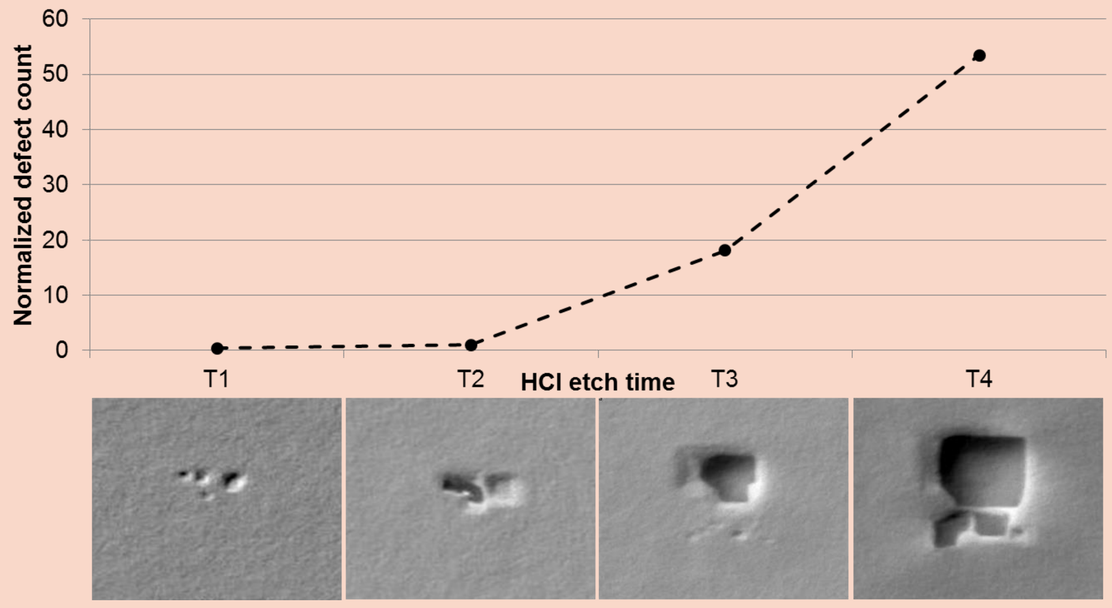

Fig. 1 Defect density and images vs. etch time

Fig. 1 shows how the defect count developed while etching the same wafer several times. T1 means the wafer went through the etch step once, T2 twice, etc. It was expected that the defect count would increase with increasing time as the holes around each defect grew big enough to be detected and then level out once every defect was found.

However, we observed that ***the defect count keeps increasing*** for longer etch times. After T2 the curve bends and counts increase at a faster rate. SEM images show that all initially present defects are highlighted at T2 and new undesired defects appear at longer times. Therefore we set the etch time to be T2 in a single etch step.

RESULTS

Two wafers were etched and inspected after fin patterning: ***One wafer had been processed with a clean process, the other with a process known to create many defects***. A sample of defects from each wafer were reviewed in the SEM and classified. Based on the classified sample the defect density was normalized for defects that look like etch pits; defects caused by other effects were excluded. Fig. 2 shows the defect density for etch pit defects. As expected the ***bad wafer has a higher defect density.*** This confirms that detection and counting works; the BFI provides quantitative results for defect density on full wafers.

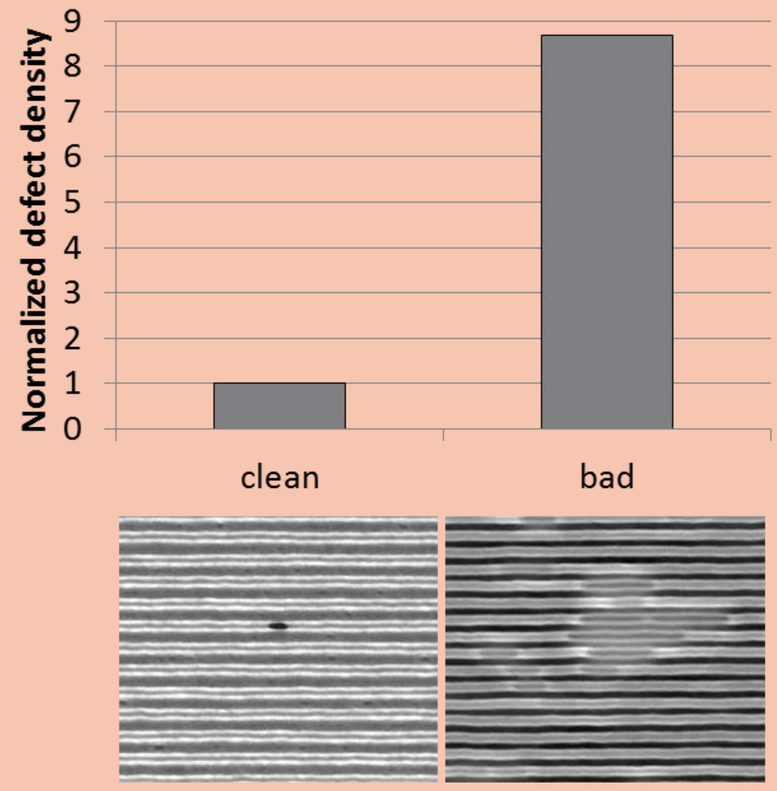

Fig. 2 Defect densities and images of two wafers. On patterned wafers the etch pits can only grow along the fins.

CONCLUSION

A method has been developed to highlight dislocations in strained SiGe and count them using brightfield inspection. The advantages of this method are:

- **Both steps, HCl highlighting and defect inspection can be *run in automation* on tools that are available in the production line. This enables regular monitoring during production.**
- **The automatic detection gives *quantitative results from a large area* of patterned fins.**