NANOFAB FUTURE ELECTRONICS

CNST Center for Nanoscale Science & Technology

Silicon Nanowires for Non-Volatile Memory

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GOAL

To advance fabrication and measurement approaches for silicon nanowire non-volatile memory.

KEY ACCOMPLISHMENTS

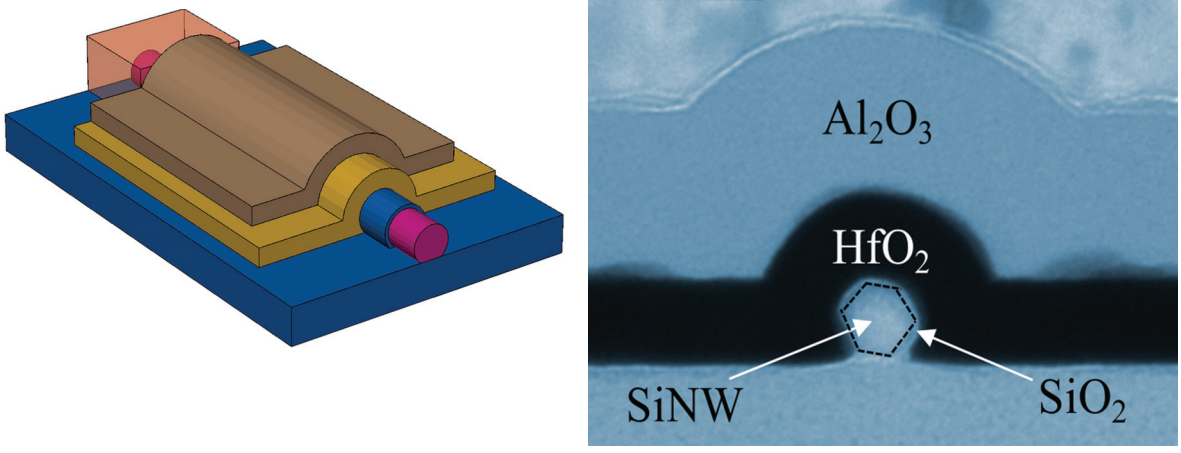
Fabricated novel non-volatile memory cells with silicon nanowire channels and $Al_2O_3/HfO_2/SiO_2$ gate dielectric storage stacks.

Demonstrated that silicon nanowire transistors with charge trapping dielectric stacks show promise for high speed operation.

KEY NANOFAB PROCESS

Growth of silicon nanowires in predefined locations by low pressure chemical vapor deposition.

A schematic and a transmission electron micrograph (TEM) showing a cross-section through a memory device consisting of a silicon nanowire surrounded by a stack of thin layered dielectrics. Schematic by Zhu; TEM by Bonevich.



REFERENCE

Fabrication, characterization and simulation of high performance Si nanowire-based non-volatile memory cells, X. Zhu, Q. Li, D. Ioannou, D. Gu, J. E. Bonevich, H. Baumgart, J. Suehle, and C. A. Richter, *Nanotechnology* **22**, 254020 (2011).