Microfabrication techniques for trapped ion quantum information processing

by

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Microfabrication techniques for trapped ion quantum information processing

Thesis directed by Dr. David Wineland

Quantum-mechanical principles can be used to process information. In one approach, linear arrays of trapped, laser cooled ion qubits (two-level quantum systems) are confined in segmented multi-zone electrode structures. Strong Coulomb coupling between ions is the basis for quantum gates mediated by phonon exchange. Applications of Quantum Information Processing (QIP) include solution of problems believed to be intractable on classical computers. The ion trap approach to QIP requires trapping and control of numerous ions in electrode structures with many trapping zones.

In support of trapped ion QIP, I investigated microfabrication of structures to trap, transport and couple large numbers of ions. Using ²⁴Mg⁺ I demonstrated loading and transport between zones in microtraps made of boron doped silicon. This thesis describes the fundamentals of ion trapping, the characteristics of silicon-based traps amenable to QIP work and apparatus to trap ions and characterize traps. Microfabrication instructions appropriate for nonexperts are included. A key characteristic of ion traps is the rate at which ion motional modes heat. In my traps upper bounds on heating were determined; however, heating due to externally injected noise could not be completely ruled out. Noise on the RF potential responsible for providing confinement was identified as one source of injected noise.

Using the microfabrication technology developed for ion traps, I made a cantilevered micromechanical oscillator and with coworkers demonstrated a method to reduce the kinetic energy of its lowest order mechanical mode via its capacitive coupling to a driven RF resonant circuit. Cooling results from a RF capacitive force, which is phase shifted relative to the cantilever motion. The technique was demonstrated by cooling a

7 kHz fundamental mode from room temperature to 45 K. Ground state cooling of the mechanical modes of motion of harmonically trapped ions is routine; equivalent cooling of a macroscopic harmonic oscillator has not yet been demonstrated. Extension of this method to devices with higher motional frequencies in a cryogenic system, could enable ground state cooling and may prove simpler than related optical experiments.

I also discuss an implementation of the semiclassical quantum Fourier transform (QFT) using three beryllium ion qubits. The QFT is a crucial step in a number of quantum algorithms including Shor's algorithm, a quantum approach to integer factorization which is exponentially faster than the fastest known classical factoring algorithm. This demonstration incorporated the key elements of a scalable ion-trap architecture for QIP.

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Chapter 1

Introduction

Quantum-mechanical principles can be used to process information. In one approach, linear arrays of trapped, laser cooled ion qubits (two-level quantum systems) are confined in segmented multi-zone electrode structures [Cirac 95, Wineland 98, Kielpinski 02, Monroe 08, Blatt 08]. Strong Coulomb coupling between ions is the basis for quantum gates mediated by phonon exchange. Applications of Quantum Information Processing (QIP) include solution of problems believed to be intractable on classical computers. The ion trap approach to QIP requires trapping and control of numerous ions in electrode structures with many trapping zones. In addition to QIP, ion traps are versatile tools found in applications including mass spectroscopy [Paul 90], precision atomic [Schmidt 05] and molecular spectroscopy [Vogelius 04, Schmidt 06], and tests of fundamental physics [Van Dyck Jr 87, Stutz 04].

In this thesis I discuss microfabrication and testing of miniature linear RF Paul traps intended for use in ion QIP experiments. The aim of this effort was demonstration of traps with ion-electrode separation below 50 μ m and investigation of microfabrication technologies amenable to building of large trap arrays. At the outset of my work the state of the art was three-dimensional gold-coated alumina structures resembling 4-rod RF quadrupole traps. In practice, this technology could not be scaled to trap and manipulate large numbers of ions. Moreover, fabrication and testing of trap structures was time-consuming and expensive. To address these shortcomings I investigated microfabricated

structures to trap, transport and couple many ions.

Among several candidate fabrication techniques, I focused on making trap electrodes out of boron doped silicon. With sufficient doping, silicon is an adequate electrical conductor and can be precisely micromachined. Boron doped silicon ion traps have several advantages: tools for processing silicon are ubiquitous in microfabrication facilities; the process uses only silicon, so it is compatible with CMOS foundry processes; surfaces exposed to trapped ions have low surface roughness (< 1 nm RMS); high aspect ratio structures 100's μ m tall are possible; and stray fields from exposed dielectric surfaces are negligible. The doped silicon traps I demonstrated traps included two-layer and surface electrode geometries. The latter geometry is especially amenable to a variety of microfabrication techniques since all trap features lie in a single plane. In my traps single 24 Mg⁺ ions were trapped as near as 40 μ m to the electrodes. All fabrication work was done in-house at the NIST microfabrication facility. It is straightforward to build boron doped traps with electrodes as small as 5 μ m.

A key performance characteristic of ion traps is the rate at which ion motional modes heat. In my traps upper bounds on heating were determined; however, heating due to externally injected noise could not be completely ruled out. Noise on the RF potential responsible for providing confinement was identified as one source of injected noise. Limits on heating from a variety of sources were calculated and the results of several related experiments are presented.

As a result of my work the time required to design, fabricate, and load ions into a new trap structure was reduced from around one year to less than a month. Besides microfabrication, several new techniques were developed to accelerate trap testing. These included streamlined layout and simulation software, a new rapid turn-around vacuum apparatus, plug and play chip carrier technology, the use of ²⁴Mg⁺ (which has a simplified atomic structure relative to ⁹Be⁺, our usual ion qubit) and dedicated laser systems for Doppler cooling and photoionization.

The first Section of this thesis describes the fundamentals of ion trapping, the characteristics of silicon-based traps amenable to QIP work and apparatus to trap ions and characterize traps. In the introductory chapter, the dynamics of ions confined in Paul traps based on the pseudopotential approximation is presented. Subsequent topics include numeric and analytic models for various Paul trap geometries, a list of considerations for practical trap design and an overview of microfabricated trapping structures. The Apparatus chapter discusses in detail the techniques needed to trap and Doppler laser cool ²⁴Mg⁺ ions. It also provides details including specific part numbers for the vacuum apparatus. A lengthy Appendix on microfabrication was written with atomic physicists in mind; it includes step by step instructions appropriate for nonexperts. Throughout, the level of detail is intended to be sufficient so that a physicist with background in atomic physics and access to a fabrication facility should be able to reproduce the traps and experiments I conducted.

Using the microfabrication technology developed for ion traps, I also made a cantilevered micromechanical oscillator and with coworkers demonstrated a method to reduce the kinetic energy of its lowest order mechanical mode via its capacitive coupling to a driven RF resonant circuit. Cooling results from a RF capacitive force, which is phase shifted relative to the cantilever motion. The technique was demonstrated by cooling a 7 kHz mode from room temperature to 45 K. Ground state cooling of the mechanical modes of motion of harmonically trapped ions is routine; equivalent cooling of a macroscopic harmonic oscillator has not yet been demonstrated. Extension of this method to devices with higher motional frequencies in a cryogenic system, could enable ground state cooling and may prove simpler than related optical experiments.

I also discuss an implementation of the semiclassical quantum Fourier transform (QFT) using three beryllium ion qubits. The QFT is one of several QIP algorithms demonstrated in NIST gold-on-alumina ion traps. The QFT is a crucial step in a number of quantum algorithms including Shor's algorithm, a quantum approach to integer

factorization which is exponentially faster than the fastest known classical factoring algorithm. This demonstration incorporated the key elements of a scalable ion-trap architecture for QIP.

Chapter 2

Ion Trapping and Microfabricated Ion Traps

2.1 Introduction

Ion traps are versatile tools found in applications including mass spectroscopy [Paul 90], precision atomic [Schmidt 05] and molecular spectroscopy [Vogelius 04, Schmidt 06], quantum information science [Wineland 98, Steane 97, Kielpinski 02, Blatt 08] and tests of fundamental physics [Van Dyck Jr 87, Stutz 04].

In this chapter¹, I discuss the trapping of atomic ions for quantum information purposes. This is of current interest because individual ions can be the physical representations of qubits for quantum information processing [Cirac 95, Wineland 98, Monroe 08, Blatt 08]. To support this application I investigated microfabricated structures to trap, transport and couple many ions. Microfabrication holds the promise of forming large arrays of traps that would allow the scaling of current quantum information processing efforts to the level needed to implement useful algorithms [Wineland 98, Blatt 08].

There are two primary types of ion traps: Penning traps and Paul traps. In a Penning trap charged particles are trapped by a combination of electrostatic and magnetic fields [Dehmelt 90]. In a Paul trap, a spatially-varying time-dependent electric field, typically in the radio-frequency (RF) domain, confines charged particles in space [Paul 90].

¹ In Summer 2008 I coauthored a book chapter titled Microfabricated Chip Traps for Ions with J. Amini, D. Leibfried and D. J. Wineland. It appears in the book Atom Chips edited by D. Jakob Reichel (MIT) and Prof. Vladan Vuletic (ENS) [Amini 08]. This section of my thesis is a modified version of this chapter and serves as an introduction to microfabricated ion traps and the ion trapping portion of my thesis work.

In this review only Paul traps will be considered.

I will begin this chapter with an introduction to the dynamics of ions confined in Paul traps based on the pseudopotential approximation. Subsequent topics include numeric and analytic models for various Paul trap geometries, a list of considerations for practical trap design and finally an overview of microfabricated trapping structures. The details of microtraps built and tested for this thesis are discussed in Chapter 3 on page 35.

Some readers may be familiar with neutral atom traps. Neutral atoms are trapped by a coupling between external trapping fields and atoms' electric or magnetic moments. As this coupling depends on the atom's internal atomic states, these states can become entangled with the atom's motion (unless special precautions are taken). Trap depths of 1 meV or less (several Kelvin) are achieved. In ion traps an ion is confined by a coupling between external electric trapping fields and the atom's net charge. This coupling does not depend on the ion's internal electronic state, leaving it unperturbed. Typical ion trap depths are 1 eV (many times room temperature).

2.2 Radio-frequency ion traps

In this section I discuss the equations of motion of a charged particle in a spatially inhomogeneous RF field based on the pseudopotential model. Several suitable electrode geometries are discussed.

2.2.1 Motion of ions in a spatially inhomogeneous RF field

Most schemes for quantum information processing with trapped ions are based on the linear RF trap shown schematically in Figure 2.1 on page 8. This trap is essentially a linear quadrupole mass filter with its ends plugged by static potentials. Radial confinement (the x-y plane in Figure 2.1 on page 8) is provided by a radio frequency (RF) potential applied to two of the electrodes (with the other electrodes held at RF ground).

The RF potential alone can not generate full 3D confinement; static potentials V_1 and V_2 applied to "end cap" control electrodes provide weaker axial (z-axis) confinement.

If potential $V_0 \cos(\Omega_{\rm RF} t)$ is applied to the RF electrodes with the others grounded $(V_1 = V_2 = 0)$, the potential near the geometric center of the four rods takes the form

$$\Phi \approx \frac{1}{2}V_0 \cos(\Omega_{\rm RF} t)(1 + \frac{x^2 - y^2}{R^2}),$$
(2.2.1)

where R is a distance scale that is approximately the distance from the trap axis to the nearest surface of the electrodes [Wineland 98, Paul 90]. The resulting electric field is shown in Figure 2.1 on the following page. There is a field null at the trap center and the field magnitude increases linearly with distance from the center in the radial direction [Paul 90].

We can think of the RF electric field as analogous to the electric field from the trapping laser in an optical dipole trap [Grimm 00]. For a neutral atom, the laser's electric field induces a dipole moment, classically a pair of opposite charges bound elastically together with a resonant eigenfrequency ω_0 in the optical range. If the electric field is inhomogeneous, the force on the dipole, averaged over one cycle of the radiation, can give a trapping force. For detunings red of the atom's resonant frequency ω_0 , this potential is a minimum at high fields, while for detunings blue of ω_0 it is a minimum at low fields. An ion, however, is a free particle in the absence of a trapping field and its eigenfrequency is zero. The RF trapping potential is therefore analogous to a blue detuned light field and the ion seeks the position of lowest intensity. In the case of Equation 2.2.1, that corresponds to x = y = 0.

The equation of motion for an ion placed in this field can be treated in two ways: as exact solutions of the Mathieu differential equation or as solutions of a static effective potential called the 'pseudopotential' [Ghosh 95]. The Mathieu solutions provide insights on trap stability and high frequency motion, while the pseudopotential approximation

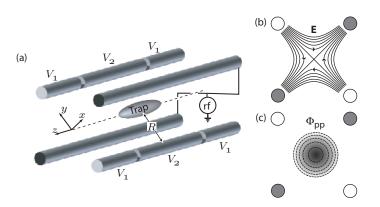


Figure 2.1: Schematic drawing of the electrodes for a linear Paul trap (a). A common RF potential $V_0 \cos(\omega_{RF}t)$ is applied to the two continuous electrodes as indicated. The other electrodes are held at RF ground through capacitors (not shown) connected to ground. In (b) is the radial (x-y) instantaneous electric fields from the applied RF potential. The pseudopotential due to this RF-field is shown in (c). A static trapping potential is created along the z-axis by applying a positive potential $V_1 > V_2$ (for positive ions) to the outer segments relative to the center segments. (Figure by J. Amini)

is more straightforward and is convenient for the analysis of trap designs. The Mathieu solutions will be relegated to Section 8.1 on page 168 and in what follows I will use the pseudopotential [Ghosh 95, Paul 90]².

We define the pseudopotential that governs the secular motion as follows [Dehmelt 67]. The motion of the ion in the RF field is combination of fast 'micromotion' at the RF frequency on top of a slower 'secular' motion. For a particle of charge q and mass m in a uniform electric field $E = E_0 \cos(\Omega_{\rm RF} t)$, the ion motion takes the form

$$x(t) = -\tilde{x}\cos(\Omega_{\rm RF}t) + v_s t, \qquad (2.2.2)$$

where $\tilde{x} = qE_0/(m\Omega_{RF}^2)$ is the amplitude of what we will call micromotion and v_s is the velocity of the secular motion. Along the x direction, if the RF field has a spatial dependence $E_0(x)$, there is a non-zero net force on the ion when we average over an RF

² An alternate derivation of the force on an ion in an inhomogeneous field (aka the pseudopotential) is in Section 8.3.1 on page 174.

cycle

$$F_{\text{net}} = \langle qE(x)\rangle \approx -\frac{1}{2}q \left. \frac{dE_0(x)}{dx} \right|_{x \to x_s} \tilde{x} = -\frac{q^2}{4m\Omega_{\text{RF}}^2} \left. \frac{dE_0^2(x)}{dx} \right|_{x \to x_s} = -\frac{d}{dx} (q\Phi_{\text{pp}})$$

$$(2.2.3)$$

where x was evaluated at position x_s and the pseudopotential $\Phi_{\rm pp}$ is defined by

$$\Phi_{\rm pp}(x_s) \equiv \frac{1}{4} \frac{q E_0^2(x_s)}{m \Omega_{\rm RF}^2}.$$
(2.2.4)

We have made the approximation that the solution in Equation 2.2.2 on the preceding page holds over an RF cycle and have dropped higher order terms in the Taylor expansion of $E_0(x)$ around x_s . For regions near the center of the trapping potential, these approximations hold. In three dimensions, we make the substitution $E_0^2 \to |E|^2 = E_{0,x}^2 + E_{0,y}^2 + E_{0,z}^2$. Note that the pseudopotential is dependent on the magnitude of the electric field, not its direction.

The pseudopotential has another interpretation in terms of conservation of energy.

From Equation 2.2.2 on the previous page, the kinetic energy averaged over a single RF cycle is

$$\mathcal{E}_{\text{total}} = q\Phi_{\text{pp}} + \frac{1}{2}mv_s^2 \tag{2.2.5}$$

where the first term is the average kinetic energy of the micromotion and the second term is the kinetic energy of the secular motion. The pseudopotential therefore represents the average kinetic energy of the micromotion. In the limit where the approximations we made are valid, this total energy remains constant: any increase (decrease) in the secular kinetic energy is accompanied by a corresponding decrease (increase) in the average micromotion kinetic energy.

For the quadrupole field given in Equation 2.2.1 on page 7, the pseudopotential is that of a 2D harmonic potential (see Figure 2.1 on the previous pagec)

$$q\Phi_{\rm pp} = \frac{1}{2}m\omega_r^2(x^2 + y^2) \tag{2.2.6}$$

where $\omega_r \simeq qV_0/(\sqrt{2}m\Omega R^2)$ is the secular frequency. As an example, for $^{24}Mg^+$ in a Paul trap with $V_0 = 50$ V, $\Omega_{\rm RF}/2\pi = 100$ MHz and R = 50 μ m, typical for a microfabricated trap, the secular frequency is $\omega_r/2\pi = 14$ MHz.

The effect of the RF pseudopotential is to confine the ion in the x-y plane. Axial trapping is obtained by the addition of the static "end cap" control potentials V_1 and V_2 in Figure 2.1 on page 8.

When the axial potential is weak compared to the overall radial potential, multiple ions can form a linear crystal along the trap axis due to mutual Coulomb repulsion. The inter-ion spacing is determined by the axial potential curvature (ω_z) . The characteristic length scale of ion-ion spacing is

$$s = \left(\frac{q^2}{4\pi\epsilon_0 m\omega_z^2}\right)^{1/3}. (2.2.7)$$

For a three ion crystal the adjacent separation of the ions is $s_3 = (5/4)^{1/3} s$ [Wineland 98]. For example, $s_3 = 5.3 \ \mu m$ for $^{24}Mg^+$ and $\omega_z/2\pi = 1.0 \ MHz$. For multiple ions in a linear Paul trap, ω_z is the frequency of the lowest vibrational center of mass mode along the trap axis.

A single ion's radial motion in the potential given by Equation 2.2.6 on the previous page can be decomposed into uncoupled harmonic motion in the x and y directions, both with the same trap frequency ω_r . Because the potential is cylindrically symmetric about z, we could choose the decomposition about any two orthogonal directions, called the principle axes. We will see in section 2.3.1 on page 13 when discussing Doppler cooling that we need to break this cylindrical symmetry by the application of static electric fields. In that case, choice of the principle axes becomes fixed and there are now two radial trapping frequencies ω_1 and ω_2 , one for each principle axis.

2.2.2 Electrode geometries for linear quadrupole traps

Designs for miniaturized ion traps conserve the basic features of the Paul trap shown in Figure 2.1 on page 8. Figure 2.2 on the following page shows several microtrap geometries that have been experimentally realized. All these geometries generate a radial quadratic potential near the trap axis, though the extent of deviations from the ideal quadrupole potential away from the axis will depend on the exact design.

In one particular geometry called a surface electrode trap (SET), the electrodes are positioned to lie on a single plane with the ion suspended above the plane as shown in Fig. 2.2 on the next paged. Such SETs were investigated fairly recently [Chiaverini 05a] and trapping of atomic ions in a SET was first demonstrated in 2006 [Seidelin 06]. Trapping in SETs is possible over a wide range of geometries albeit with 1/6 - 1/3 the motional frequencies and 1/30 - 1/200 the trap depth of more conventional quadrupolar traps (e.g. Figure 2.1 on page 8) at comparable RF potentials and ion-electrode distances [Chiaverini 05a]. A comparison between the trapping potentials and geometries for 4-wire traps and SETs is in Figure 2.3 on the next page.

Advantages of surface electrode traps over two-layer traps [Madsen 04, Rowe 02, Stick 06] include easier MEMS fabrication and the possibility of integrating control electronics on the same trap wafer [Kim 05]. A SET at cryogenic temperature was implemented at MIT in 2008 [Labaziewicz 08].

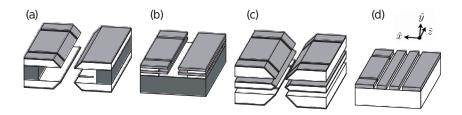


Figure 2.2: Examples of microfabricated trap structures: (a) two wafers mechanically clamped over a spacer, (b) two layers of electrodes fabricated onto a single support wafer, (c) three wafers clamped with spacers (spacers not shown) and (d) surface electrode construction. (Figure by J. Amini)

Research on SET designs is ongoing and holds promise to yield complex geometries that would be difficult to realize in non-surface electrode designs.

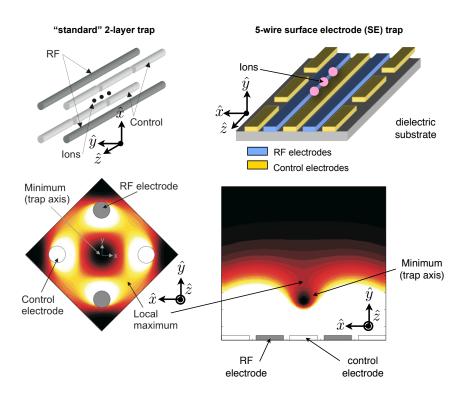


Figure 2.3: Figure illustrating the trapping potential for a standard 2-layer trap and a 5-wire surface electrode trap (SET). In the top row are schematics illustrating the trap geometries. Below each is a false color contour plot of the radial pseudopotential (small: black, large: white).

2.3 Design Considerations for Paul traps

In this section, we will discuss the requirements that need to be addressed when designing a practical ion trap.

2.3.1 Doppler cooling

Ions are loaded into a trap by ionizing neutral atoms passing near the trap center and cooling them with a Doppler laser beam. For Doppler laser cooling, only a single laser beam is needed; trap strengths far exceed the laser beam radiation pressure [Metcalf 99]. However, for motion perpendicular to the laser beam, cooling is offset by heating due to recoil. Therefore, to cool in all directions, the laser beam k-vector must have a component along all three principle axes. This also implies that the trap frequencies are not degenerate, otherwise one principle axis could be chosen normal to the laser beam's k-vector.

Meeting the first condition is usually straightforward for non-SET type traps, where laser beam access is fairly open (see Figure 2.4 on the following page). For SETs, where laser beams are typically confined to running parallel to the chip surface, care has to be taken in designing the trap so that neither radial principle axis is perpendicular to the trap surface. Alternately, for SETs, we could bring the Doppler laser beam at an angle to the surface but the beam would then strike the surface. This can cause problems with scattered light affecting fluorescence detection of the ion and with charging of exposed dielectrics (see Section 2.3.3 on page 17).

If any two trap frequencies are degenerate, then the trap axes in the plane containing these modes are not well defined and the motion in a direction perpendicular to the Doppler laser beam k-vector will not be cooled. The axial trap frequency can be set independently of the radial frequencies and can be selected to prevent a degeneracy with

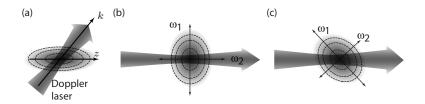


Figure 2.4: Doppler cooling with a single laser beam. The dashed lines are equipotential curves for the pseudopotential. The overlap with the axial direction is fairly straightforward as in (a), but care has to be taken that the orientation of the two radial modes does not place one of the mode axes perpendicular to the laser (b). (c) The radial axes must be at an angle with respect to the laser beam k-vector for efficient cooling. (Figure by J. Amini)

either of the radial modes. There are several ways to break this degeneracy, but usually the axial trapping potential is sufficient. When we apply an axial trapping potential, Laplace's equation forces us to have a radial component to the electric field. In general, this radial field is not cylindrically symmetric about z and will distort the net trapping potential as shown in Figure 2.5, lifting the degeneracy of the radial frequencies. If this is not sufficient, offsetting all the control electrodes by a common potential will result in a static field that has the same spatial dependence (i.e. the same function of x and y) as the field generated by the RF electrodes. This field, shown in Figure 2.1 on page 8b, will further split the radial frequencies. Finally, extra control electrodes can be designed into the trap to generate the necessary static fields to lift the degeneracy. Experimental techniques to measure trap secular frequencies are discussed in Section 8.4.

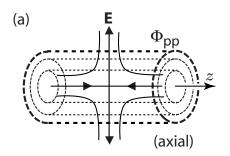


Figure 2.5: The degeneracy in the radial trap modes is lifted by the radial component of the static axial confinement. The RF pseudopotential which provides radial confinement is cylindrically symmetric. A static quadrupole is used to provide axial confinement. This static field is overlaid on radial component; it deforms the net potential seen by the ion, breaking the cylindrical symmetry. (Figure by J. Amini)

2.3.2 Micromotion

If the pseudopotential at the equilibrium position of a trapped ion is non-zero, then the ion motion will include persistent micromotion at frequency Ω_{RF} . This section discusses two mechanisms that can generate a non-zero pseudopotential minimum.

Complex trap structures break the symmetry of the Paul trap in Figure 2.1 on page 8. For such traps there can be a component of the RF field in the axial direction. In this case, the minimum of the pseudopotential well is non-zero. Since this effect is caused by the design of the trap, we refer to the resulting micromotion as **intrinsic** micromotion [Berkeland 98].

Secondly, a static electric field can shift the equilibrium position of an ion away from the pseudopotential minimum. This may be due to 'stray' electric fields as from charging of a dielectric surface near the trap center. Shim potentials applied to the control electrodes can often null these fields. We call this sort of nullable micromotion 'excess' micromotion.

Both intrinsic and excess micromotion can cause problems with the laser-ion interactions such as Doppler cooling, ion fluorescence, and Raman transitions [Wineland 98, Berkeland 98]. An ion with micromotion experiences a frequency modulated laser field due to the Doppler shift. In the rest frame of the ion, this modulation introduces sidebands to the laser frequency (as seen by the ion) at multiples of Ω_{RF} and reduces its intensity at the carrier frequency as shown in Figure 2.6 on the next page. The strength of these sidebands is parametrized by the modulation index β given by

$$\beta = \frac{2\pi}{\lambda} x_{\mu \text{m}} \cos \theta, \tag{2.3.1}$$

where λ is the laser wavelength and θ is the angle the laser makes with micromotion. For laser beams tuned near resonance, ion fluorescence becomes weaker and can disappear entirely. For example, when $\beta = 1.43$, the carrier and first micromotion sideband have equal strength. For $\beta < 1$, the fractional loss of on-resonance fluorescence is approxi-

mately $\beta^2/2$. As a rule of thumb, we aim for $\beta < 0.25$ which corresponds to less than five percent drop in on-resonant fluorescence.

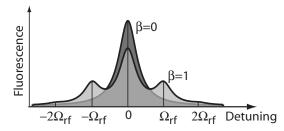


Figure 2.6: In the rest frame of the ion, micromotion induces sidebands on a probing laser. The monochromatic laser spectrum has been convolved with the atomic linewidth. (Figure by J. Amini)

For a given static electric field E_{dc} along the direction of the RF electric field, an ion's displacement x_d from trap center and the resulting excess micromotion amplitude $x_{\mu m}$ are

$$x_d = \frac{qE_{\rm dc}}{m\omega_r^2}, x_{\mu \rm m} = \sqrt{2} \frac{w_r}{\Omega_{\rm RF}} x_d,$$
 (2.3.2)

where ω_r is the radial secular frequency.

Assuming $^{24}Mg^+$, $\Omega_{\rm RF}/2\pi=100$ MHz and $\omega_r/2\pi=10$ MHz, a typical SET with $R\sim 50~\mu{\rm m}$ and an excess potential of 1 V on a control electrode will produce a radial electric field at the ion of ~ 500 V/m. The resulting displacement is $x_d=500$ nm and the corresponding micromotion amplitude is $x_{\mu{\rm m}}=70$ nm. This results in a laser modulation index of $\beta=1.14$.

Stray electric fields can be nulled if the control electrode geometry permits application of independent compensation fields along each radial principle axis. For the Paul trap in Figure 2.1 on page 8, a common potential applied to the control electrodes can only generate a field at the trap center that is along the diagonal connecting the electrodes. Compensation for other directions is possible for example by applying a static offset to one of the time-varying potentials on an RF electrode or by adding extra compensation electrodes.

There are several experimental approaches to detecting and minimizing excess mi-

cromotion [Berkeland 98]. One technique uses the dependence of the fluorescence from a cooling laser beam on the micromotion modulation index. The micromotion can be minimized by maximizing the fluorescence when the laser is near resonance and minimizing the fluorescence when tuned to the RF the sidebands. For more on micromotion detection see Section 8.2.1 on page 171.

Intrinsic micromotion can also be caused by an RF phase difference $\phi_{\rm RF}$ between the two RF electrodes. A phase difference can arise due to a path length difference or differential capacitive coupling to ground for the wires supplying the electrodes with RF potential. We aim for $\beta < 0.25$ (see Section 2.3.2 on page 15) for typical parameters, which requires $\phi_{\rm RF} < 0.5^{\circ}$. This sort of micromotion may have been problematic in a microtrap I built (see Section 3.5 on page 63).

For more on micromotion see Section 8.2 on page 169.

2.3.3 Exposed dielectric

Exposed dielectric surfaces near the trapping region can accumulate stray charge and the resulting stray electric fields can cause problems (see Section 2.3.2 on page 15). Stray charge can be produced by photo-emission from the cooling laser or from electron sources sometimes used to ionize atoms by electron impact (see Section 4.2.1 on page 114). Depending on the resistivity of the dielectric these charges can remain on the surfaces for seconds or longer, requiring time-dependent micromotion nulling or waiting a sufficient time for the charge to dissipate.

SETs are particularly prone to this problem. The metallic trapping electrodes are often supported by an insulating substrate and the spaces between the electrodes expose the substrate. The effect of charging of these regions can be mitigated by increasing the ratio of electrode conductor thickness to the inter-electrode spacing.

Figure 2.7 on the next page illustrates a model for estimating how thick electrodes can suppress the field from a strip of exposed substrate charged to a potential V_s . The

sidewalls are assumed conducting and grounded. Along the midpoint of the trench the potential drops exponentially with height [Jackson 99]. Using this solution to relate V_s to the potential at the top of the trench, and then the techniques described in section 2.6.2 on page 25 to relate the surface potential to a field at the ions, we obtain an approximate expression for the field seen by the ion

$$E_{vert} = (4V_s/\pi^2)(a/R^2)e^{-\pi t/a}, \qquad (2.3.3)$$

where a is the width of the exposed strip of substrate, t is the electrode thickness, and R is the distance from the trap surface to the ion. We have assumed $R \gg a$ and $\pi t \geq a$. Thus, the effect of the stray charges drops off rapidly with the ratio of electrode thickness to gap spacing.

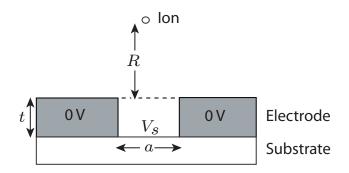


Figure 2.7: Model used for calculating the effect of stray charging. We assume that $R \ll a$ and $t \geq a/\pi$. (Figure by J. Amini)

2.3.4 Loading ions

Ions are loaded into traps by ionizing neutral atoms as they pass through the trapping region. The neutral atoms are usually supplied by a heated oven, but can also come from background vapor in the vacuum or laser ablation of a sample. See Section 4.2 on page 114 for more on ionization techniques and Section 4.1.7 on page 112 for more on ovens.

It is necessary that the neutral atom flux reach the trapping region but not deposit on insulating spacers which might short adjacent trap electrodes. In practice, we do this by careful shielding and, in some SETs, undercutting of electrodes to form a shadow mask (see Figure 2.16 on page 29). Alternately, for SETs, a hole machined through the substrate can direct neutral flux from an oven on the back side of the wafer to a small region of the trap, preventing coating of the surface. This is called backside loading and has been demonstrated in several traps (e.g. dv16m in Section 3.6 on page 70).

2.3.5 Electrical connections

Radio frequency trapping potentials and DC control potentials are delivered to the trap electrodes by wiring that includes traces on the trap substrate. Care is needed to avoid several pitfalls.

The high voltage RF potential is typically by a quarter-wave RF resonator [Jefferts 95] or LC lumped-element resonant circuit. RF losses in a microtrap's insulating substrate can degrade the resonator quality factor (Q_L) and can cause Ohmic heating of the microtrap itself. This can be be mitigated by use of low loss insulators (e.g. quartz or alumina) and decreasing the capacitive coupling of the RF electrodes to ground through the insulators. Typical RF parameters for our traps are $\Omega_{\rm RF}/2\pi=100~{\rm MHz},\,V_{\rm RF}=100~V$ and $Q_L=200$. See also Section 4.6.2 on page 139.

The RF electrodes have a small capacitive coupling to each control electrode (typically $< 0.1 \ pF$) which result in unwanted RF fields at the ion. This RF potential is shunted to ground by a low pass RC filter (typically $R = 1 \ k\Omega$ and $C = 1 \ nF$) on each control electrode (Figure 2.8 on the following page). The impedance of the lines leading to the RC filters should be low or the filtering will be compromised. Proper grounding, shielding and filtering of the electronics supplying the control potentials is also important to suppress pickup and ground loops (which can cause motional heating, Section 2.5 on page 21).

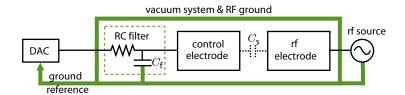


Figure 2.8: Figure showing typical filtering and grounding of a trap control electrode. Inside the vacuum system are low pass RC filters which reduce noise from the control potential source and provide low impedance shorts to ground for the RF coupled to the control electrodes by stray capacitances $C_{\rm s} << C_f$. The RC filters typically lie inside the vacuum system, within 2 cm of the trap electrode. The control potential (assumed in the figure to be derived from a DAC) is referenced to the trap RF ground and is supplied over a properly shielded wire.

2.4 Multiple trapping zones

The emphasis in the recent generation of traps aim to store ions in multiple trapping zones and can transport ions between them.

We can modify the basic Paul trap in Figure 2.1 on page 8 to support multiple zones and ion transport by dividing the control electrodes into a series of segments as shown in Figure 2.9 on the next pagea. By applying appropriate potentials to these segments, an axial harmonic well can be moved along the length of the trap carrying ions along with it (Figure 2.9 on the following pageb). In the adiabatic limit (with respect to ω_z^{-1}), ions have been transported a distance of 1.2 mm in 50 μ s with undetectable heating and undetectable internal-state decoherence [Rowe 02].

For quantum information processing, for example, we need to be able to take pairs of ions in a single zone (e.g. zone 2) and separate them into independent zones (e.g. one ion in zone 1 and a second in zone 3) with minimal heating, as shown in Figure 2.9 on the next pagec. We must likewise be able to combine separated ions with low heating. Separating and combining are more difficult tasks than ion transport; the

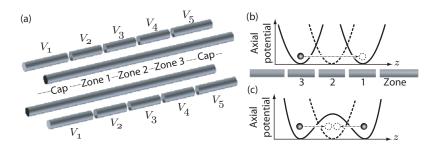


Figure 2.9: Example of a multizone trap (a). By applying appropriate waveforms to the segmented control electrodes, ions can be shuttled from zone to zone (b) or pairs of ions can be merged into a single zone or split into separate zones (c). (Figure by J. Amini)

theory is discussed by Home [Home 06a] and there are several demonstrations [Rowe 02, Barrett 04]. The basis for these potentials is the quadratic and quartic terms of the axial potential. Proper design of the trap electrodes can increase the strength of the quartic term and facilitate faster ion separation and merging with less heating. Groups of two and three ions have been separated while heating the center of mass mode less than 10 quanta and the higher order modes to less than 2 quanta [Barrett 04].

The segmented Paul trap in Figure 2.9 forms a linear series of trapping zones, but other geometries are possible. Of particular interest are junctions with linear trapping regions extending from each leg. Specific junction geometries are discussed in section 2.7 on page 26. The broad goal is to create large interconnected trapping structures that can store, transport and reorder ions so that any two ions can be brought together in a common zone.

2.5 Motional heating

Doppler and Raman cooling can place a trapped ion's harmonic motion into the ground state with >99% probability [Monroe 95, King 98, Wineland 98]. If we are to use the internal electronic states of an ion to store information, we have to turn off the cooling laser beams during that period. Unfortunately, the ions do not remain in the ground state and this heating can reduce the fidelity of operations per-

formed with the ions. One source of heating comes from laser interactions used to manipulate the electronic states [Ozeri 07]. Another source is ambient electric fields that have a frequency component at a secular frequency. We expect such fields from the Johnson noise on the electrodes, but the heating rates observed experimentally are typically several orders of magnitude larger than the Johnson noise can account for [Turchette 00, Deslauriers 06b, Wineland 98]. Currently, this source of anomalous heating is not explained, but recent experiments [Deslauriers 06b, Labaziewicz 08] indicate that it is thermally activated and consistent with patches of fluctuating potentials with size smaller than the ion-electrode spacing [Turchette 00].

The spectral density of electric field fluctuations S_E inferred from ion heating measurement in a number of ions traps are plotted in Figure 2.10 on the following page. The dependence of S_E on the minimum ion-electrode distance R and on the trap frequency ω follows a roughly $R^{-\alpha}\omega^{-\beta}$ scaling, where $\alpha \approx 3.5$ [Deslauriers 06b, Turchette 00] and $\beta \approx 0.8 - 1.4$ [Turchette 00, Seidelin 06, Deslauriers 06b, Epstein 07, Labaziewicz 08]. In addition to being too small to account for these measured heating rates, Johnson noise scales as R^{-2} [Wineland 98, Turchette 00].

In the context of ion quantum information processing, microtraps are advantageous because quantum logic gate speeds and ion packing densities increase as R decreases [Leibfried 03b, Wineland 98, Kielpinski 02]. However, these gains are at odds with the highly unfavorable dependence of motional heating on ion-electrode distance. Extrapolating from current best heating results observed at room temperature, in a trap with $R = 10 \ \mu \text{m}$ the heating rate would exceed 1×10^6 quanta/sec [Seidelin 06]. Heating between gate operations is also problematic because hot ions require more time to recool to the motional ground state [King 98].

I discuss in greater detail motional heating in the context of a microtrap I built

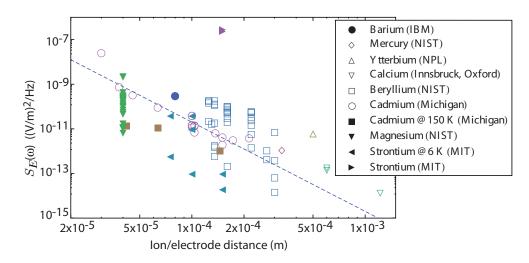


Figure 2.10: Spectral density of electric-field fluctuations inferred from observed ion motional heating rates. Data points show heating measurements in ion traps observed in different ion species by several research groups [Diedrich 89, Monroe 95, Roos 99, Tamm 00, Turchette 00, DeVoe 02, Rowe 02, Home 06b, Stick 06, Deslauriers 06b, Epstein 07, Labaziewicz 08, Britton 08, Blakestad 08]. The several Be^+ measurements between 100 μ m and 400 μ m are for identical traps measured at different times [Turchette 00]. Unless specified, the data was taken with the trap at room temperature. The dashed line shows a R^{-4} trend for ion heating vs ion-electrode separation. (Figure by J. Amini and J. Britton)

in Section 3.6.7 on page 84.

2.6 Trap modeling

Calculation of trap depth, secular frequencies, and transport and separation waveforms requires detailed knowledge of the potential and electric fields near the trap axis.

In the pseudopotential approximation, the general time-dependent problem is simplified to a slowly varying electrostatic one. For simple 4-rod type traps (as in Figure 2.1

on page 8), good trap design is not difficult using numerical simulation owing to their
symmetry. However, SET design is more difficult since the potential may have large
anharmonic terms and highly asymmetric designs are common. Fortunately, for certain
SET geometries analytic solutions exist. These closed form expressions permit efficient
parametric optimization of electrode geometries not practical by numerical methods. In
this section we will first discuss the full 3D calculations and then introduce the analytic
solutions.

2.6.1 Modeling 3D geometries

There are several numerical methods for solving the general electrostatic problem. I used the boundary element method implemented in a commercial software package called Charged Particle Optics (CPO, Ltd). In contrast to the finite element method, the solutions from the boundary element method are in principle differentiable to all orders. A simulation consists of calculating the potential due to each control electrode when that electrode is set to one volt and all others are grounded. The solution for an arbitrary set of potentials on the control electrodes is then a linear combination of these one volt solutions. Similarly, the pseudopotential is obtained from the field calculated for one volt on the RF electrodes and ground on the control electrodes.

2.6.2 Analytic solutions for surface-electrode traps

Numerical calculations work for any electrode geometry, but they are are slow and not well suited to automatic optimization of SET electrode shapes. For the special case of SETs, an analytic solution exists subject to a few realistic geometric constraints. Electrodes are modeled as a collection of gapless plates embedded in an infinite ground plane (see Figure 2.11). The electric field that would be observed from a plate is proportional to the magnetic field produced by a current flowing along its perimeter [Oliveira 01]. The problem is then reduced from solving Laplace's equation to integrating a Biot-Savart type integral around the patch boundary. Furthermore, for patches that have boundaries composed of straight line segments, the integrals have analytic solutions.

Of pedagogical value is the application of this technique to a very simple SET geometry in Reference [Amini 08]. The application of this technique to SETs is in Reference [Wesenberg 08b].

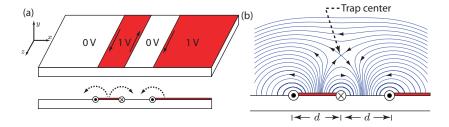


Figure 2.11: Surface-electrode trap composed of two RF electrodes embedded in a ground plane (four-wire trap) (a). All electrodes extend to infinity along the trap (z) axis. The field lines derived from an analytic potential are shown in (b). (Figure by J. Amini)

The main shortcoming of this method is the requirement that there be no gaps between the electrodes. Typical SET fabrication techniques produce $1-5~\mu m$ gaps which can only be accounted for at the level important to ion dynamics by full numerical simulations.

2.7 Trap examples

Having covered the general principles for Paul trap designs, I will now give specific examples of microfabricated ion traps. A number of fabrication techniques have been used for micro-traps, starting with stacking multiple wafers to form a traditional Paul trap type design [Rowe 02, Barrett 04, Wineland 05, Britton 08, Blakestad 08, Huber 08, Hensinger 06, Schulz 08]. Recently, trap fabrication has been extended to single wafer designs using substrate materials such as Si, GaAs, and quartz [Seidelin 06, Britton 06, Stick 06, Pearson 06, Brown 07a, Labaziewicz 08, Britton 08]. The fabrication process flows include such microfabrication standards as photolithography, metallization, and chemical vapor deposition as well as other less used techniques such as laser machining. A detailed discussion of the microfrabrication techniques I used to build microtraps is in Section 8.7 on page 189.

The microfabricated equivalent to the prototypical four-rod Paul trap (Figure 2.1 on page 8) takes two insulating substrates patterned with electrodes and then clamps or bonds the substrates together across an insulating spacer. This approach has been implemented in a number of traps (see [Rowe 02, Barrett 04] and Section 3.2 on page 40) using two substrates as shown in Figure 2.12 on the next pagea. Most recently at NIST this approach culminated in a trap with 18 zones and an 'X' junction [Blakestad 08] shown in Figure 2.13 on the following page. The University of Michigan demonstrated a three wafer trap design like that shown Figure 2.12 on the next pageb incorporating a 'T' shaped junction [Hensinger 06].

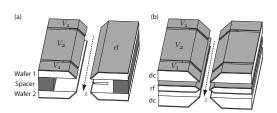


Figure 2.12: Multi-wafer traps mechanically clamp or bond multiple substrates to form a classic Paul trap type structure (a) or a modified three-layer structure (b) [Hensinger 06] Typically, both the top and bottom layers include segmented control electrodes. (Figure by J. Amini)

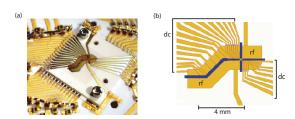


Figure 2.13: Example of a two wafer trap with an 'X' junction. The trap conductors are evaporated and electroplated gold films deposited on alumina substrates. The substrates have been laser machined to form the large slots where the ions reside and to provide the gaps $(20\mu\text{m})$ that separate the control electrodes [Blakestad 08]. (Figure by J. Amini)

Another approach demonstrated recently used two patterned wafers mounted with the conducting layers facing each other and without any slots in the wafers [Debatin 08]. The trapping region was then in the gap between the wafers and laser beam access was in the plane perpendicular to the plane of the wafers.

The direct analog to the four-rod Paul trap can also be realized in single wafer microfabrication by depositing two conducting layers separated by an insulting layer and then etching the electrode profiles [Stick 06].

Surface-electrode traps (SETs) have the benefit of using standard microfabrication methods where layers of metal and insulator are deposited on the surface of the wafer without the need for milling of the substrate itself. There are two general versions of the surface trap electrode geometry as shown in Figure 2.14 on the following page. We looked at the fields from these geometries in Section 2.6.2 on page 25. The four-wire geometry has the trap axis rotated at 45° to the substrate plane, which allows for efficient cooling of the ion (Figure 2.14 on the following pagea). The five-wire geometry has one trap axis

perpendicular to the surface, which makes that axis difficult to Doppler cool because the cooling laser beams propagate parallel to the surface (Figure 2.14 and Section 2.3.1 on page 13).

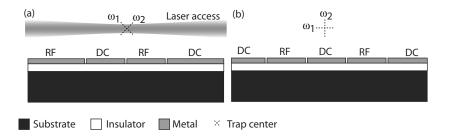


Figure 2.14: Comparison of trap principle axes for two surface electrode geometries. (a) four-wire geometry and (b) five-wire geometry. In practice, the five-wire geometry is not used because of the difficulty of cooling the vertical motion of the trapped ions. (Figure by J. Amini)

Surface-electrode traps (SETs) are fairly new, and only a few designs have been demonstrated [Seidelin 06, Britton 06, Labaziewicz 08]. The first surface-electrode trap for atomic ions was constructed on a fused quartz substrate with electroplated gold electrodes [Seidelin 06]. In addition, meander line resistors were fabricated on the chip as part of the DC filtering. Surface mount capacitors gap welded to the chip provide a low impedance shunt to ground for the RF (see Section 2.3.5 on page 19). The process sequence is shown in Figure 2.16 on the following page (see Section 8.7 on page 189 for more on microfabrication). The bonding pads and the thin meander line resistors were formed by liftoff of evaporated gold. Charging of the exposed substrate between the electrodes was a concern, so the trapping structure was thick 6 μ m electroplated gold with 8 μ m gaps.

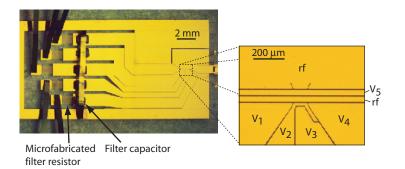


Figure 2.15: An example of a four wire surface electrode trap constructed of electroplated gold on a quartz substrate. (Figure by J. Amini)

A SET for microscopic aminopolystyrene spheres was also demonstrated [Pearson 06].

A similar design was built for low temperature testing using 1 μ m evaporated silver on quartz. They reported a strong dependence of the anomalous heating on temperature (see Section 2.5 on page 21) [Labaziewicz 08].

The construction of these traps was based on adding conducting layers to an insulating substrate. In my thesis work I employed an alternate fabrication method based on removal of material from a conducting substrate. In these traps the conducting electrode surfaces were boron doped silicon; it has a low electrical resistance. This silicon was deep etched to form electrically isolated electrodes. The electrodes were fixed in place by anodic bonding to a glass substrate (see Section 3.2 on page 40 and [Britton 06]) or because it was part of a silicon-on-insulator structure (see Section 3.6 on page 70). The

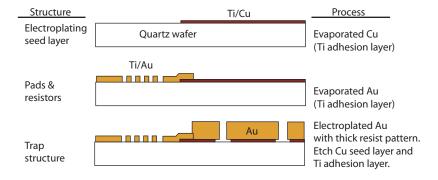


Figure 2.16: Fabrication steps for the example trap in Figure 2.15. The copper seed layer could not extend under the meander line resistors because the final step of etching of the seed layer would fully undercut the narrow meander pattern. (Figure by J. Amini)

SOI design depicted in Figure 2.17 demonstrated multiple trapping zones in a SET linear array and backside loading of ions. These traps are the subject of my thesis work and are discussed in greater detail in Chapter 3 on page 35.

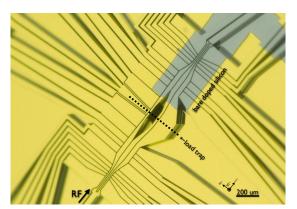


Figure 2.17: Optical micrograph of a SOI SET ion trap. The bright gold regions are gold coated; the dark regions are bare boron doped silicon. The camera is tilted, showing a perspective view of the trap which emphasizes the height of the SOI device layer (100 μ m thick). This trap demonstrated multiple trapping zones in a SET linear array and backside loading ions.

Surface-electrode traps allow for complex arrangements of trapping zones, but making electrical connections to these electrodes quickly becomes intractable as the complexity grows. This problem can be addressed by incorporating multiple conducting layers into the design with only the field from the top layer affecting the ion [Kim 05, Amini 07]. An example of such a multilayer trap was fabricated at NIST on an amorphous quartz substrate is shown in Figure 2.19 on the next page. The metal layers were separated by chemical vapor deposited (CVD) oxide and connections between metal layers were made by vias that are plasma etched through the oxide as shown in Figure 2.18 on the following page. The fabrication process for the surface gold layer was similar to the electroplating shown in Figure 2.16 on the previous page.

Table 2.1 on page 32 is a detailed comparison of the performance of several ion trap fabrication approaches which may meet the needs of future ion trap quantum computing applications. Ion traps developed for other applications like mass spectroscopy are not

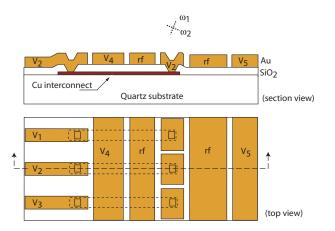


Figure 2.18: Fabrication of a multilayer gold on quartz surface-electrode trap. A CVD oxide insulates the surface electrodes from the second layer of interconnects. Plasma etched holes in the insulated layer connect the two conducting layers. (Figure by J. Amini)

included.

2.8 Future traps

As trapping structures become smaller and trap complexity increases, features such as junctions will expand the capabilities traps. While two of the multiwafer traps we looked at in Section 2.7 on page 26 incorporated a junction, the slots in multilayer traps, the required alignment and assembly steps make it difficult to scale such structures.

Figure 2.20 on page 33 shows an example design of a 'Y' version of an SET junction. The shape of the RF junction is an example of optimization using analytic solutions to the fields (see Section 2.6.2 on page 25). One feature of this geometry is that the pseudopotential does not have large axial micromotion 'bumps' (see Section 2.3.2 on page 15). Components such as this 'Y' can be assembled into larger structures. SETs

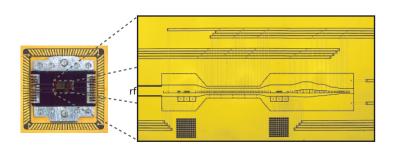


Figure 2.19: Multilayer trap mounted in its carrier and an enlargement of the active region. (Figure by J. Amini)

BL	а	9	c	y d	u	y f	y 9	y h
(eV) ϕ_{eV}						0.1		> 0.15
(\sec)	> 100	> 20		10	0.1	10	30	09
(\min)	> 600	> 60	> 60	> 120	10	> 60	> 60	> 60
$ \left \frac{((V/m)^2/Hz)}{S_E(\omega_z)} \right $	2.22×10^{-13}			7×10^{-12}	2×10^{-8}	5×10^{-11}	5.7×10^{-11}	
(MHz) $\omega_{x,y}/2\pi$						11		
(MHz) $\omega_z/2\pi$	4		0.77	2.83	6.0	1.1	1.9	0.71
Q_L	40-200	372	373			7.5		
$\binom{V}{V_{\mathrm{RF}}}$	500	125	100	103	55	~ 60		99
Z	16	Н	Н	Н	2	6	2	ಸ
$\binom{\mathrm{MHz}}{\Omega_{\mathrm{RE}}}$	80	28	85	28	16	29	50	45
				$^{24}Mg^+$	$^{111}Cd^+$	$^{24}Mg^+$	$^{24/25}Mg^{+}$	$^{24}Mg^+$
	140			42			09	
Materials	alumina/Au	glass/B*Si	m glass/B*Si	quartz/Au	GaAs/AlGaAs	$\mathrm{B*SOI/Au}$	$\mathrm{Si/SiO2/Al}$	Si/SiN/W
Geom.	2-layer	2-layer	$_{ m SET}$	$_{ m SET}$	2-layer	$_{ m SET}$	$_{ m SET}$	SET
Fabricator	LSIN	m NIST~dv10	NIST dv14	ISIN	U. Mich.	NIST dv16m	Lucent	Sandia
Year	2002-8	2004	2006	2006-8	2006	2002	2002	2002

at room temperature. NIST Boulder tested all the traps except for the U. Michigan's trap. SET denotes a surface electrode (ion) trap. B*Si denotes Table 2.1: Table comparing room temperature microtrap technologies designed for ion trap quantum information processing. All traps were tested boron doped silicon.

Year is the year the trap was tested.

Fabricator is the research group that developed a fabrication technology and built the traps.

Geom. is the trap geometry.

Materials are the insulating and conducting materials used.

 ${f R}$ is the characteristic ion-electrode separation.

Ion is the ion species.

 $\Omega_{\rm RF}/2\pi$ is the RF drive frequency.

 ${\bf N}$ is the number of trapping zones demonstrated to work.

V_{RF} is the peak RF drive potential amplitude.

 Q_L is the loaded trap resonator quality factor at $\Omega_{\rm RF}$.

 $\omega_z/2\pi$ is the axial trap frequency.

 $\omega_{x,y}/2\pi$ are the radial trap frequencies. These frequencies are approximately equal; sometimes the splitting was not recorded and so only one frequency is listed for some traps.

 $S_{\rm E}(\omega_z)$ is the electric field noise spectral density at $\tau_{
m Dop}$ is the typical ion lifetime with continuous Doppler laser cooling.

τ_{dark} is the maximum observed ion lifetime without any laser cooling.

 $\phi_{\rm eV}$ is the ion trap depth in electron volts according to simulation. **BL** indicates if the trap demonstrated backside loading (only if it is a SET).

^a See Section 3.1 and [Rowe 02, Blakestad 08]

 b See Section 3.2 and [Wineland 05]

^c This trap suffered from mechanical oscillation of its trapping electrodes. See Section 3.3 and [Britton 06]

 d See [Seidelin 06, Amini 08]

e This trap had problems with breakdown that prevented higher trap frequencies. See [Stick 06]

 f See Section 3.4

^g Exposed SiO2 in this trap made ion transport difficult.

^h Fabrication process was Sandia's SUMMiT V. Ion lifetime was limited by background pressure.

fabricated using standard recipes in a foundry and using standard patterns may eventually make ion traps more accessible to research groups that do not have the considerable time or resources needed to develop their own.

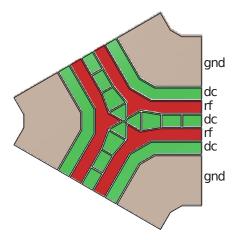


Figure 2.20: Example of a SET 'Y' junction. (Figure by J. Amini)

With increased trap complexity, there are several issues that arise. One of them is the question of how to package traps and provide all the electrical connections needed to operate them. Another issue is that of corresponding complexity of the lasers used in manipulating the ions. Beyond cooling, lasers are needed to manipulate the internal states of the ions and couple pairs or groups of ions. Multiplexing sets of lasers to a number of trapping zones has its difficulties and complicates simultaneous manipulation of several ions. Alternately, instead of laser optical fields magnetic structures, active wire loops and passive magnetic layers could be used [Mintert 01, Leibfried 07, Ospelkaus 08]. If viable, this would switch much of the experimental complexity from large laser systems to electronic packages, which can be reliably engineered and scaled [Kim 05].

The field of microfabricated ion traps is developing rapidly. In this chapter, I looked at the current state-of-the-art ion traps and considerations related to their design. I look forward to continued development of microfabricated ion traps which anticipates expanded single and multi-ion control and, some day, useful ion quantum information

processing. In the chapter that follows I discuss several microfabricated ion traps that I built and the apparatus used to test them.

Chapter 3

Boron Doped Silicon Microtraps

This chapter discusses several microtraps I made as part of my thesis work. The trap geometries were of the two layer and surface electrode trap (SET) types.

introduction In 2001 it was recognized that a fundamental change in ion trap technology was needed to satisfy the needs anticipated by some ion trap quantum information processing (QIP) schemes [Kielpinski 02, Steane 04]. At the time the only ion traps used for QIP were two-layer linear gold-coated laser-machined alumina ion traps [Rowe 01]. These devices were serviceable for demonstration experiments but have no clear path for scaling to the smaller electrode geometries and larger number of traps per chip needed for QIP.

The use of heavily doped silicon in lieu of gold-coated alumina was proposed by Kielpinski in 2001 [Kielpinski 01]. In 2005 Chiaverini, et al. proposed a more fundamental departure: a trap geometry with all electrodes lying in a single plane [Chiaverini 05a]. As part of my thesis work I developed these ideas, and fabricated and trapped ions in several doped silicon structures. The two-layer boron-doped silicon trap I demonstrated in 2004 [Britton 06] was the first in a series of experiments exploring new fabrication technologies at NIST which culminated in a microfabricated surface electrode ion traps with many zones in 2007. Also at NIST, Chiaverini, Seidelin and Amini pursued gold surface electrode ion traps on fused quartz [Seidelin 06]. Other groups also exploring scalable trapping technology include the Monroe group at the Joint Quantum Institute

(JQI) at the University of Maryland and the National Institute of Standards and Technology (NIST) in Gaithersburg, MD., the Slusher group at the Georgia Tech Research Institute, the Kim Group at Duke University. and Sandia National Labs. It is hoped that this these efforts will some day permit very large trap arrays.

This section starts with a description of the tried and true gold-on-alumina trap used at NIST since 2000. Then I describe the boron doped ion traps I made including trap geometry, fabrication steps and trap performance. The section concludes with a comparison of competing microtrap trap technologies.

A variety of microfabrication techniques were used to make my devices. Since many techniques are common to several devices they are separately detailed in Section 8.7 on page 189. Refer to that section for the following topics.

- silicon deep etch by deep reactive ion etching (DRIE) including photolithography
- silicon oxide etch including plasma etching and buffered oxide etch (BOE)
- wafer backside alignment
- metallization and Ohmic contacts in silicon
- anodic and wafer bonding including silicon on insulator (SOI) wafers
- wafer cleaning including Piranha etch
- electrical interconnect using wire bonding, gap welding and resistive welding
- suppliers and specifications for doped silicon wafers, glass wafers, and ultrasonic milling of glass
- shadow masks and wafer dicing saw blades

Section 4 on page 101 discusses the apparatus used to test the boron doped silicon traps.

trap technologies

Table 3.1 on the next page is a chronology of the several ion trap fabrication approaches which may meet the needs of future ion trap quantum computing applications.

Year	Fabrication	Geometry	Materials	Citation
2002-8	NIST	2-layer	$\operatorname{alumina}/\operatorname{Au}$	Sec. 3.1 [Rowe 02, Blakestad 08]
2004	NIST	2-layer	B*Si	Sec. 3.2 [Britton 06]
2006	NIST	SET	B*SOI	Sec. 3.3
2006	NIST	SET	quartz-Au	[Seidelin 06]
2006	U. Mich.	2-layer	${ m GaAs/AlGaAs}$	[Stick 06]
2007	NIST	SET	$\mathrm{B*SOI/Au}$	Sec. 3.4
2007	Lucent	SET	$\mathrm{Si}/SiO_2/\mathrm{Al}$	
2007	Sandia	SET	$\mathrm{Si/SiN/W}$	SUMMiT V

Table 3.1: Table comparing trap technologies exploring scalable ion trap fabrication for quantm information processing. SET is a surface electrode (ion) trap. B*Si is boron doped silicon.

Ion traps developed for other applications like mass spectroscopy are not included.

3.1 2-layer gold coated laser machined alumina ion traps

Gold coated laser machined linear ion traps were used by NIST since the late 1990's [Turchette 00]. As of 2008 only traps made using this technology have been used for quantum information processing experiments at NIST [Turchette 00, Rowe 02, Blakestad 08]. The traps were made by laser machining alumina wafers to define the electrode structure. They were then coated with a 1-3 μ m layer of gold by e-beam deposition, RF sputter deposition or electroplating. Wafers comprising the two trapping electrodes were then aligned by hand and held together with metal screws (see Figure 3.1 on the following page). This technology has several limitations including exposed dielectric surfaces (bare alumina) which can accumulate surface charges that perturb trapped ions, large wafer-wafer alignment errors, and rough surfaces due to the laser machining (see Figure 3.2 on the next page). With currently available laser machining trap electrodes smaller than 25 μ m suffer from large fabrication errors. Alumina traps are also difficult to fabricate and the turn-around time for a new trap is at least a year. This

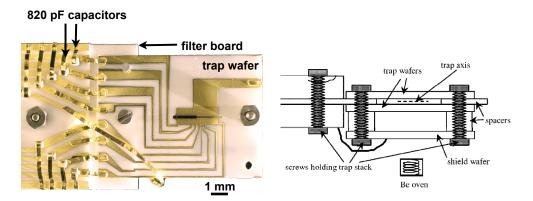


Figure 3.1: Photograph showing assembly of gold coated laser machined alumina wafers. The left hand photograph shows a top view of a trap. Gold traces are visible on the trap wafer, the filter board, 820 pF capacitors and gold ribbon used to make electrical connections (see Section 8.7.7 on page 232). The right hand figure shows a cross section view [Rowe 02]. A pair of trap wafers and ancillary spacer wafers were held together with stainless screws. A NIST trap tested in 2008 using this technology had alignment errors (\sim 1° rotation, \sim 10 μ m horizontal, \sim 40 μ m vertical) which caused ion transport difficulties [Blakestad 08].

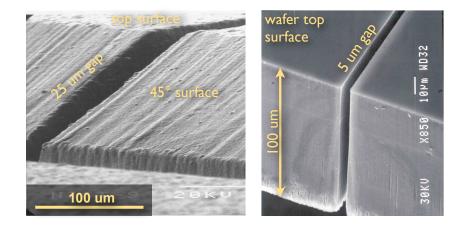


Figure 3.2: Scanning electron micrographs comparing the surface roughness of gold coated laser machined alumina (left) with deep etched silicon (right).

(left) The laser machined wafer is patterned with a vertical trench cut fully through its bulk. The laser machining was done by Resonetics, Inc. The roughness is dominated by the step size of the Excimer laser used to ablate the alumina. The cuts had a 5° sidewall slope. The best available tolerance for 15 μ m wide slits is $\pm 3 \mu$ m.

(right) The deep etched silicon wafer is patterned with a 5 μ m trench (gap) that cuts fully thru the wafer's bulk. The etching was done using the STS DRIE discussed in Section 8.7.1 on page 189. Tolerances are $1-2^{\circ}$ sidewall slope and a pattern resolution of 1 μ m for cuts < 20 μ m deep and 3 μ m for cuts < 200 μ m deep (see Section 8.7.1 on page 189 for more on silicon etch).

technology is difficult to scale beyond several 10's of electrodes.

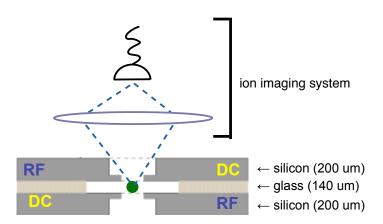


Figure 3.3: Schematic of a 2-layer boron doped silicon trap in cross section. The ion location is marked by a green dot. Due to the L shaped electrode geometry, the trap's numerical aperture is approximately F1 as viewed from above. This matches the numerical aperture of the UV imaging system, maximizing ion fluorescence collection. It also minimizes scattered light from the cooling laser beams. The drawing is not to scale: the glass insulator is at least laterally 5 mm away from the trapping region.

3.2 dv10: 2-layer doped silicon trap

The first doped silicon trap was a variant of previous 2-layer gold coated alumina traps (see Section 3.1 on page 37). The geometry was the same (see Figure 3.3) but the structural material and conductor differed: glass and boron doped silicon were used instead of alumina and gold. Also, instead of screws the wafers were held together by anodic bonding (see Section 8.7.5 on page 220). I call this first incremental design dv10. It was first presented in [Wineland 05].

Advantages of this approach include bonding without screws, smoother trapping surfaces and high resolution photolithographic patterning of trap features. Moreover, because the trap structural material is a conductor there are no insulating surfaces anywhere near the ion. See Figure 3.2 on page 38 for a comparison with laser machined alumina.

3.2.1 Fabrication

The fabrication steps were as follows.

- (1) double sided deep etch defines trap geometry
- (2) dice wafers into chips
- (3) clean the chips
- (4) align and bond
- (5) metallization
- (6) dice the chips to electrically isolate the electrodes
- (7) vacuum processing

The trap structure illustrated in Figure 3.3 on the preceding page was deep etched with the STS DRIE (Section 8.7.1 on page 189) into a 200 μ m double side polished born doped silicon wafer (see Section 8.7.4.3 on page 217 for more on the wafers). The fabrication steps are shown in Figure 3.4 on page 44. Nine trap chips were simultaneously etched into a single 3 inch wafer, each patterned to appear as in Figure 3.5 on page 45. The wafer was etched from both the front and back sides. Care was taken to avoid surface contamination which can cause needles to form during deep etching (see Figure 8.20 on page 201) and may prevent bonding.

double sided deep etch

- (1) Measure the process wafer thickness with a micrometer.
- (2) Attach a sapphire backing wafer with wax (see Section 8.7.1.3 on page 196).
- (3) Spin photoresist on the top side of the process wafer using the 7 μ m recipe. Transfer to the photoresist the trap pattern from a mask using the recipe in Section 8.7.1.1 on page 192.
- (4) Etch using DIRE recipe SPECB to etch the pattern in Figure 3.5 on page 45. Stop etching when there is 40-50 μ m material remaining of the 200 μ m wafer. As a rough estimate assume an etch rate of 3 μ m/min. Use an optical microscope

with a shallow ($< 2~\mu \mathrm{m}$) depth of field and z-axis indicator to measure the etch depth.

- (5) Release the backing wafer as described in Section 8.7.1.3 on page 196.
- (6) Flip the process wafer and reattach the backing wafer.
- (7) Spin photoresist on the top side of the process wafer using the 7 μ m recipe and expose as last time.
- (8) Etch using DRIE recipe SPECB until large apertures fully penetrate the silicon wafer.
- (9) Etch using the DIRE recipe for SOI (see Section 8.7.1.4 on page 197). Inspect narrow trenches on an optical microscope with backlighting. They should be free of silicon (opaque in the visible). If not, continue to etch using the SOI recipe.
- (10) Release the backing wafer as described in Section 8.7.1.3 on page 196.

wafer dicing An automated saw was used to dice the etched 3 inch silicon wafer into 9 chips. A regular silicon-cutting blade was used. See Section 8.7.7.1 on page 234 for details.

glass spacers Glass spacers were made of Corning 7070 glass (see Table 8.5 on page 225). The glass was patterned by ultrasonic milling (see Section 8.7.5.5 on page 229). It was then diced on the automated dicing saw but with a special Resinoid blade (see Section 8.7.7.1 on page 234).

clean the wafers High strength anodic bonding requires clean surfaces. Cleaning steps I, II and IV in Section 8.7.6 on page 230 were followed for both the silicon and glass chips. I used the wafer holders described in Section 8.7.6.1 on page 231. Both the silicon and glass were processed at the same time.

align and bond Anodic bonding was used to adhere the wafers into a stack as in Figure 3.3 on page 40 and Figure 3.4 on page 44. See Section 8.7.5 on page 220 on how anodic bonding works. Follow the advice in Section 8.7.5.1 on page 221 on how to

do wafer bonding.

metallization and electrical interconnect — For electrical contact to the bare silicon electrodes, 1 μ m gold contacts were deposited at the periphery of the bonded chips. As dv10 is a two layer device, pads needed to be deposited on both sides in two deposition steps. Contact to these pads was made using gold ribbon and a resistive welder. I followed the recipe in Section 8.7.4.2 on page 216 with FASTAU. The same recipe was repeated for the back side gold pads. The chip's gold pads were connected to pads on the filter board using resistive welding as in Section 8.7.7 on page 232.

dice to electrically isolate electrodes At this stage in the fabrication process all the doped silicon electrodes are still shorted together. This was necessary for structural support prior to bonding. At this point however they can be safely separated with a second dicing saw cut. See Figure 3.6 on page 46 for a schematic and discussion of this process. Prior to dicing, the delicate structures were protected with wax as in the Wafer Dicing steps above. Again, a Resinoid blade was used since one of the layers was glass.

vacuum processing Prior to insertion into the final ion trap vacuum system, the thermal silicon oxide layer was stripped off the trap. In 2003 this was done with a 15 sec BOE dip (step II in Section 8.7.6 on page 230) within 10 min of insertion into the vacuum. However, this is risky as HF degrades Ti and can damage the bond pads. Success requires thorough rinsing with deionized water. A more conservative approach (as was used in subsequent traps) may have been a plasma etch (see Section 8.7.2 on page 203).

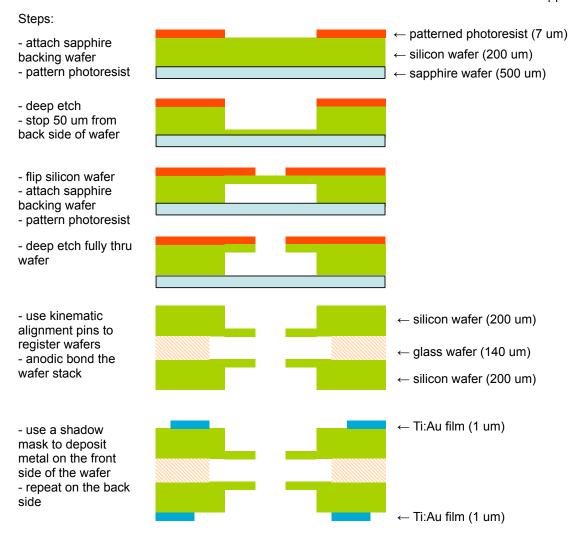


Figure 3.4: Figure outlining the process steps to fabricate trap dv10. The individual steps are discussed in the text. Note that the dimensions are not to scale.

3.2.2 Performance

The trap was installed in a coaxial $\lambda/4$ style vacuum housing (see Section 4.1 on page 101). The endcap voltages were +3.0 V, the middle electrodes were grounded and the RF amplitude was 125 V at 87 MHz. It loaded easily in May 2004. Linear chains of a half dozen ions could be loaded in the trap. Ion lifetime with Doppler cooling was regularly in excess of 1 hour. Ions were loaded from a 24 Mg oven and ionized by electron impact from a hot tungsten filament biased at +50 to +100 V. The trap was successful

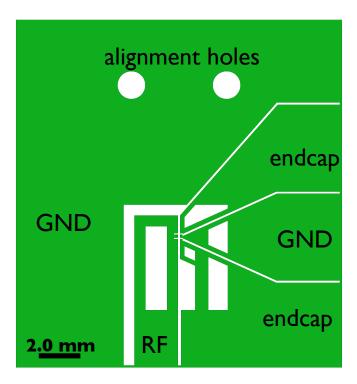


Figure 3.5: Figure showing the deep etch pattern for a dv10 silicon wafer. The white regions are apertures etched fully through the silicon wafer.

but time constraints on the experimental apparatus precluded measurement of the ion oscillation frequencies and motional heating rate. Table 3.2 reviews the characteristics of this trap.

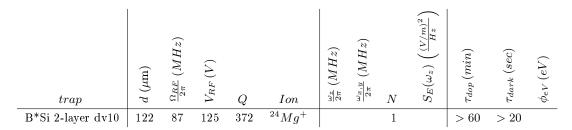


Table 3.2: Trap characteristics of dv10. See Table 2.1 on page 32 for an explanation of the nomenclature. Trap depth $\phi_{\rm ev}$ and $V_{\rm RF}$ were estimated by simulation. Neither the heating rate nor the secular frequencies were measured in this trap.

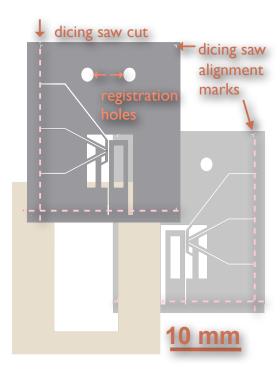


Figure 3.6: Schematic showing the two silicon and one glass layers that comprised trap dv10. The holes in the silicon were formed by deep etching; the glass was ultrasonically milled. The three layers were aligned and anodically bonded on a special stage (see Figure 8.33 on page 223). Alignment was kinematic. The silicon chips were etched with high tolerance ($< 5 \,\mu \rm m$ error) alignment holes. The interior edge of the glass was sized to press against the circumference of these holes. Alumina alignment pins on the bonding stage provided layer-to-layer registration. Under a microscope, the lateral alignment error appeard to be less than 20 $\mu \rm m$. The etched silicon and glass chips were oversized; all the silicon electrodes were initially shorted together. This excess material holds the silicon electrodes in place during bonding. After bonding the electrodes were coated in wax for protection, then electrically isolated by cutting fully thru the wafer stack with a dicing saw. Alignment marks were etched into the silicon indicating where to cut (pink dashed lines in this figure).

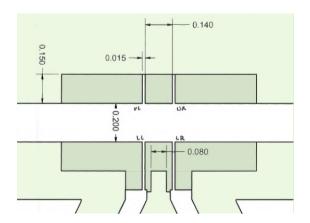


Figure 3.7: Schematic showing trapping region of dv10. The light green surfaces mark the top of the wafer. The dark green surfaces were recessed by about 150 μ m. The white regions were etched fully thru the wafer. Units are in mm.

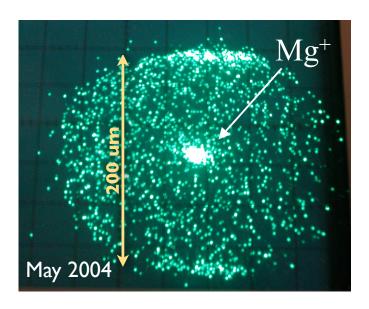


Figure 3.8: Oscilloscope image showing a trapped $^{24}{\rm Mg}^+$ in trap dv10. The image was created from collected ion fluorescence at 280 nm due to the Doppler cooling laser beam. The field of view was 200 $\mu{\rm m}$ wide.

3.3 dv14: surface electrode doped silicon ion trap

The second doped silicon trap I built drew upon the success of dv10 and included a departure from ion trapping convention in its electrode geometry. In 2005 Chiaverini, et al. proposed a trap geometry with all electrodes lying in a single plane [Chiaverini 05a]. My second trap aimed to demonstrate trapping for the first time in such a structure. I succeeded in trapping and Doppler cooling a single ²⁴Mg⁺ ion in March 2006, but was several months too slow. In parallel at NIST, Seidelin led an effort to build a surface electrode ion trap on quartz. In early 2006 we published our results in Physical Review Letters [Seidelin 06]. Later in 2006, Pearson, et al. demonstrated buffer gas cooling of half-micron size aminoploystyrene spheres in a surface electrode trap (PRA [Pearson 06]) and Brown, et al. loaded a ⁸⁸Sr⁺ ion cloud in a surface electrode trap (PRA [Brown 06, Brown 07b]). This section discusses my first surface electrode trap which I call dv14.

Generic advantages of surface electrode traps (SET) over two-layer traps include much easier MEMS fabrication and the possibility of integrating control electronics on the same trap wafer [Kim 05]. My SET fabrication approach has several advantages over other demonstrated SETs. It provides superior shielding of structural dielectric surfaces and addition of large through wafer holes for backside loading is easy. These two features in particular are difficult to obtain in, for instance, gold on fused quartz traps [Seidelin 06]. See Section 2.2.2 on page 11 for more on SET geometry.

3.3.1 Fabrication

dv14 was a 4-wire surface electrode ion trap made of boron doped silicon. The trap structure is illustrated in Figures 3.3.1 on page 50 and 3.9 on the next page. The trap features were deep etched with the STS DRIE (see Section 8.7.1) into a 200 μ m

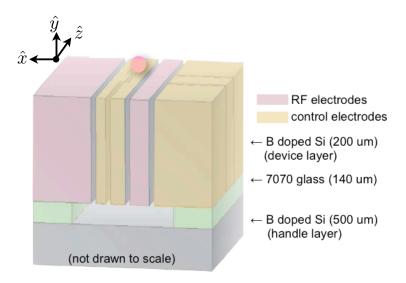


Figure 3.9: Perspective view of the surface electrode ion trap dv14. The conducting surfaces near the ion are bare doped silicon. The trap electrodes are cantilevered over the insulating 7070 glass layer. The ion location is marked by a pink dot. To the left of trap center is an adjacent pair of control electrodes which help null radial micromotion. The drawing is not to scale: the glass insulator is at least 5 mm away from the trapping region.

double side polished boron doped silicon wafer. The trap electrodes were cantilevered over an insulating 7070 glass layer. The conducting surfaces near the ion were bare doped silicon. The fabrication steps were nearly identical to those for dv10, Section 3.2.1 on page 41. Nine trap chips were simultaneously etched into a single 3 inch wafer.

The fabrication steps are as follows.

- (1) double sided deep etch defines trap geometry
- (2) dice wafers into chips
- (3) clean the chips
- (4) align and bond
- (5) metallization
- (6) dice the chips to electrically isolate the electrodes
- (7) vacuum processing

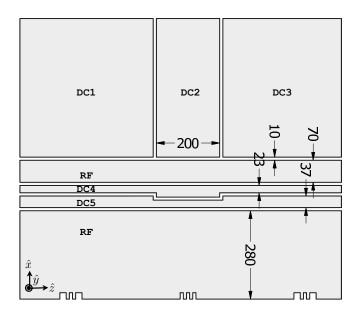


Figure 3.10: Schematic showing the dimensions of the trapping region of dv14. The gray surfaces are the top of the wafer. The white regions are etched fully thru the wafer. Units are in μ m.

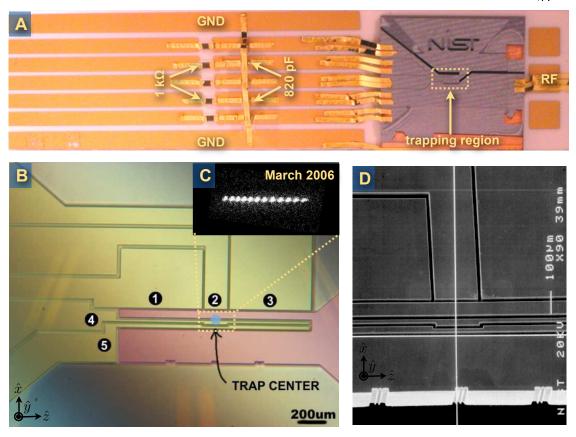


Figure 3.11: Micrographs of a completed dv14 ion trap. (A) Trap chip mounted on a ceramic filter board. Also visible are the RC filter components and traces which provide control and RF potentials to the chip. (B) A false color optical photograph of the trapping region with a blue dot at the trap center. This is the same view that the ion imaging optics has of the trap. The the shape of control electrodes 1-5 was selected to produce a static harmonic electric potential well along the trap z-axis. Electrodes 2, 4 and 5 permit radial micromotion nulling by creating a static radial electric fields at the ion which can compensate for stray electric fields. RF electrodes are in red. Inset (C) shows a linear chain of ions from the same perspective as photo B. (D) A scanning electron micrograph showing details of the trapping region. Alignment marks cut into the edge of the wafer (visible in B and C) assist with laser beam alignment.

	$\frac{\omega_z}{2\pi}$ (1-ion)	$\frac{\omega_x}{2\pi}$	$\frac{\omega_y}{2\pi}$	θ_{axis}
endcap tickle	0.7682			
ion spacing	0.55			
simulation (1-ion)	0.786	3.143	5.257	11.1

Table 3.3: Comparison of observed and simulated characteristics of dv14. The secular frequencies were measured experimentally by the endcap tickle technique (see Section 8.4 on page 179) and by measurement of ion spacing in a linear crystal (see Section 8.4 on page 180 and Figure 3.12 on the following page). The potentials are those reported in the text. See Table 2.1 on page 32 for an explanation of the nomenclature.

3.3.2 Performance

The results for this trap were first presented in [Britton 06]. These results and additional details follow. Table 3.4 on the next page summarizes the characteristics of this trap using the nomenclature of Figure 2.1 on page 32.

Ions were loaded from a 24 Mg oven and photoionized by a 285 nm laser beam. A $\lambda/2$ style vacuum system was used. Initial trap parameters (RF and control electrode potential amplitudes) were determined numerically by simulation. The primary solution constraint was that the ion lie a the pseudopotential zero. An ion was trapped with the following potentials.

$$V_1 = +0.72V; V_2 = +0.32V; V_3 = +0.74V; V_4 = -0.90V; V_5 = +1.00V$$

$$V_{RF} = 125V \text{ at } 87 \text{ } MHz$$

Table 3.3 compares the trap characteristics predicted by simulation with observation.

	I					ı				I		53
trap	d (μm)	$rac{\Omega_{RE}}{2\pi}\left(MHz ight)$	$V_{RF}\left(V ight)$	Q	Ion	$\frac{\omega_z}{2\pi} \left(MHz\right)$	$rac{\omega_{x,y}}{2\pi} \left(MHz ight)$	N	$S_E(\omega_z) \left(\frac{(V/m)^2}{Hz} \right)$	$ au_{dop}\left(min ight)$	$ au_{dark}\left(sec ight)$	$\phi_{eV}\left(eV ight)$
B*Si 1-layer dv14	78	85	100	373	$^{24}Mg^{+}$	0.77	3.1, 4.3	1		> 60		

Table 3.4: Trap characteristics of dv14 in the format of Table 2.1 on page 32. Trap depth $\phi_{\rm ev}$ and $V_{\rm RF}$ were estimated by simulation.

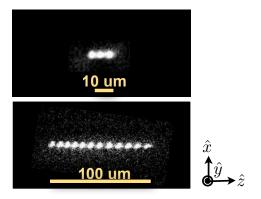


Figure 3.12: Linear ion crystals trapped in dv14. (Top) A linear crystal of three ions along the trap axis confined with the potentials listed in the text. The length of the crystal is about 17 μ m suggesting an axial frequency of ~ 550 kHz. (Bottom) A linear crystal of 12 ions in a very weak trap.

Ions are detected by observing ion fluorescence on a charge-coupled device (CCD) camera or PMT. For QIP applications low background scatter is required [Wineland 98]. The background includes stray light scattered from the cooling laser beam by the trap electrodes and other apparatus. The Doppler cooling beam for dv14 had a waist of 40 μ m trained on the trap center 78 μ m above the surface. The signal-to-background for a single ion was observed to be better than 100:1, even with a beam intensity 40 times the resonance saturation intensity (limited by noise due the CCD chip). The camera used was an Andor, Inc. iXon electron-multiplied charge-coupled device (EMCCD).

In the presence of Doppler laser cooling, single-ion lifetimes greater than one hour

were observed. Loading was reliable.

Ion motional heating measurements were not conducted in this trap because it failed before it was fully characterized. One of the electrodes snapped, shorting an RF electrode to ground. The failure was due to excitation by the RF drive of a mechanical mode in one of the long cantilevered electrodes. This excitation phenomenon is of interest in its own right and is discussed in Chapter 5 on page 145.

In retrospect, the trap would have been robust had I used a continuous sheet of glass and fixed the trap electrodes in place by anodic bonding. This could be done without exposing the ion to the dielectric glass surface, but at the cost of an increase in the capacitance of the RF electrode (to ground thru the glass) which causes RF losses.

3.4 dv16: SOI silicon traps

3.4.1 SOI as a building material

The third and fourth doped silicon traps I built improved upon dv14 by eliminating anodic bonding. Instead of 3 separate silicon and glass wafers, I used a single silicon on oxide wafer (SOI). SOI is monolithic heterostructure (Si:oxide:Si) requiring no assembly (eg anodic bonding) and it is commercially available. The oxide is SiO₂ which has a loss tangent which approaches that of fused silica (0.0002), making it two orders of magnitude lower loss than the 7070 glass used in previous traps (see Table 8.5 on page 225). Use of SOI also reduced the device fabrication time by 2/3 and greatly improved yield. This generation of traps was also the first to use the octagon style vacuum system and UHV compatible chip carrier (see Section 4.1 on page 101). See Figure 3.13 for a schematic and Section 8.7.5.4 on page 226 for more on SOI.

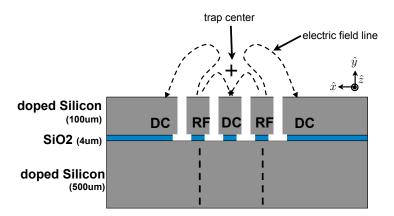


Figure 3.13: Figure showing an SOI ion trap chip in schematic. The dashed lines above the top silicon layer show electric field lines which form an RF quadrupole. The dashed lines on the 500 μ m wafer indicate the location of a backside loading slot.

SOI traps also have advantages over other demonstrated surface electrode traps.

If a thick device layer is used (relative to inter-electrode gap size) the shielding of struc-

tural dielectric surfaces is excellent. Also, fabrication and alignment of holes for backside loading is easy. These features are demonstrated in my traps. In the future, integration with on-chip control electronics is possible using well established microfabrication techniques. One route for this is to put CMOS on an ordinary silicon wafer and wafer or bump bonding it to an SOI trap wafer [Kim 05].

The maximum oxide thickness in SOI wafers is traditionally 4 μ m (for thermally grown oxide). This small gap and its high dielectric constant ($\epsilon_r/\epsilon_0 = 3.9$ for thermal oxide), results in a larger capacitance between RF electrodes and ground than in the anodically bonded traps. The result is that the RF current which must flow to establish the trapping fields may be significant. This can cause Ohmic heating and can degrade the RF resonator quality factor. However, these effects did not appear to be serious problems in my traps which had loaded quality factor of 80 and loaded easily. Thicker oxide can be grown using plasma techniques (see Section 8.7.5.4 on page 226 for more on SOI). The thin oxide layer is also responsible for a larger capacitance between ground and the control electrodes. Under some circumstances this capacitance can act as a shorting capacitor while in others it can cause intrinsic micromotion (see Section 4.6 on page 138 note 6).

I made two SET ion traps in SOI. Outside of demonstrating basic trapping, the devices were designed with features to make possible tests of anomalous ion heating [Turchette 00, Deslauriers 06b]. Both included tapered regions where ion-electrode separation could be continuously varied. They also included regions where the conducting surfaces were either bare doped silicon or evaporated gold, permitting a heating rate comparison. The trap I call dv16k also included a y-junction. It was fabricated and electrically tested but did not make it to the optics table due to concerns about intrinsic micromotion (see Section 2.3.2 on page 15). Another simpler trap, dv16m, successfully loaded ions. A comparison between the gold and silicon traps in this device was not conclusive due to other possible sources of ion heating.

The fabrication steps for SOI traps are discussed first. Then, the geometry and performance of the traps is detailed.

3.4.2 Fabrication

The fabrication steps are as follows. All the fabrication steps were done in the NIST clean room.

- (1) etch loading slot in handle layer
- (2) etch trap features in device layer
- (3) clean in Piranha bath
- (4) etch SiO_2 in BOE bath
- (5) metallization
- (6) dice into chips
- (7) packaging: mount on chip carrier and wire bond
- (8) continuity tests
- (9) vacuum processing

Steps 1-5 are illustrated in Figure 3.14 on page 59. The trap structures were deep etched in doped silicon using an STS DRIE (see Section 8.7.1 on page 189). The wafers are commercially available silicon on insulator (SOI, see Section 8.7.5.4 on page 226). Nine trap chips were simultaneously etched and metalized on a single 3 inch wafer. Each chip included a backside loading slot and required etching from both the front and back sides. Care was taken to avoid surface contamination which can cause needles to form during deep etching (see Figure 8.20 on page 201).

The SOI wafers used in my experiments consisted of the following layers.

layer name	thickness	composition
device layer	$100~\mu\mathrm{m}$	$0.005\text{-}0.020~\Omega\text{-cm}$ B doped silicon
oxide layer	$3~\mu\mathrm{m}$	SiO_2
handle layer	$550~\mu\mathrm{m}$	$0.005\text{-}0.020~\Omega\text{-cm}$ B doped silicon

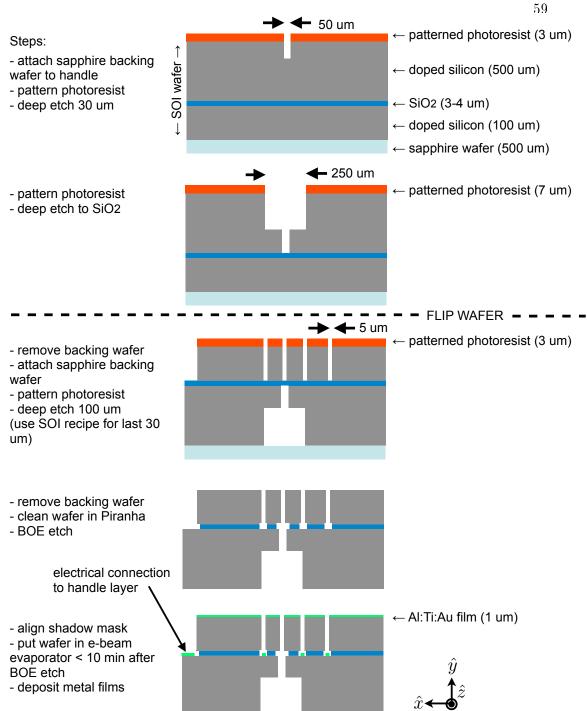


Figure 3.14: Overview of SOI ion trap fabrication steps. Note that drawings are not to scale. The depicted trap is an asymmetric 5-wire trap.

deep etch of loading slot To provide good support for the device layer trap electrodes without causing inconveniently sharp collimation of the neutral beam, the backside loading slot was etched in a two step process. There was a a narrow 50 μ m slot, followed by a wide 250 μ m trench. This etch sequence relied on deep etching being an additive process. The resolution of the wide trench photolithography was reduced due to presence the narrow slot which causes ripples in the photoresist.

- (1) Note SOI handle layer thickness (from the manufacturer's specifications).
- (2) Attach a sapphire backing wafer with wax, handle side up (see Section 8.7.1.3 on page 196).
- (3) Spin on 3 μ m photoresist. Follow the recipe in Section 8.7.1.1 on page 192.
- (4) Expose the photoresist with the mask for the narrow slit pattern.
- (5) Etch using DIRE recipe SPECB. Stop after 30 μ m of material is removed. As a rough estimate, assume an etch rate of 3 μ m/min.
- (6) Spin on 7 μ m photoresist. Follow the recipe in Section 8.7.1.1 on page 192. Don't worry about the slight ripple in photoresist thickness near the already etched features.
- (7) Expose the photoresist with the mask for the wide trench pattern.
- (8) Etch using DIRE recipe SPECB. Stop when 30 μ m of material remains at the base of the wide trench. As a rough estimate, assume an etch rate of 3 μ m/min.
- (9) Etch using the DIRE recipe for SOI (see Section 8.7.1.4 on page 197). Inspect narrow trenches with an optical microscope. They should be free of silicon. If not continue to etch.
- (10) Release the backing wafer as described in Section 8.7.1.3 on page 196.

deep etch of trap features

- (1) Note SOI device layer thickness (from the manufacturer's specifications).
- (2) Flip the SOI wafer and reattach the sapphire backing wafer to the handle side (device side up).

- (3) Spin on 7 μ m photoresist. Follow the recipe in Section 8.7.1.1 on page 192.
- (4) Expose the photoresist with the mask for the trap pattern.
- (5) Etch using DIRE recipe SPECB. Stop when 30 μ m of material remains at the base of the widest features. As a rough estimate, assume an etch rate of 3 μ m/min.
- (6) Etch using the DIRE recipe for SOI (see Section 8.7.1.4 on page 197). Inspect narrow trenches with an optical microscope, they should be free of silicon. If not continue to etch. The thin SiO₂ layer is translucent in the visible.
- (7) The SiO₂ membrane may rupture due to trapped air in the loading slot. This does not seem to damage the trap structure.
- (8) Release the backing wafer as described in Section 8.7.1.3 on page 196.

clean the wafers The long deep etches in the preceding steps may result in baked-on photoresist which can't be removed by solvents. This baked-on resist may appear as in Figure 8.18 on page 199. Remove it and other contaminants as follows.

- (1) Clean the wafer in Piranha for 30-45 minutes as discussed in Step I of the recipe in Section 8.7.6 on page 230. Use the 3 inch wafer holders described in Section 8.7.6.1 on page 231.
- (2) Dry the wafers as in Step IV.
- (3) Etch the SiO₂ exposed at the base of the deep silcon etch¹. The wet etch used in this step requires constant agitation so that fresh etchant is forced into the deep trenches. This is accomplished by agitation with an orbital shaker.
- (4) Place the wafer in a Teflon or PTFE container on top of an orbital shaker.
- (5) Immerse the wafer in buffered oxide etch (BOE) as in Step II of the recipe in Section 8.7.6 on page 230.

¹ This is done for three reasons. First, exposed dielectric is problematic for ion trapping. Second, electrical contact to the handle wafer from the top side requires removal of the insulator. Third, the etched features in the device layer will be used as a shadow mask to prevent shorting of adjacent trap electrodes during the metallization step.

- (6) Etch for about 35 minutes. Fresh BOE at room temperature etches SiO₂ at a rate of about 87 nm/min (see Section 8.7.2 on page 205).
- (7) Inspect the narrow trenches with an optical microscope; the thin SiO₂ layer is translucent in the visible. They should be free of SiO₂. If not continue to etch. Protect the wafer with a clean towel when placing on the optical microscope.

metallization A 1 μ m gold layer was deposited on much of the wafer surface. At the periphery of each trap chip, this layer is used to provide bond pads for connection to external potential sources. The metal layer also lowers the impedance of the path from the bond pads to trap electrodes. During the etch of the device side, a large region of the handle wafer was exposed. Electrical contact to the handle layer is made by contact to bond pads in this region. That is, electrical contact to both the device and handle layers is achieved in a single metallization step. Some regions of the wafer were protected from metallization by a stainless steel shadow mask.

- (1) Follow the FASTAU recipe in Section 8.7.4 on page 210. Use a shadow mask (see Section 8.7.4.2 on page 216). For advice on deposition of thick Au films see Section 8.7.4.1 on page 212.
- (2) If the wafer is placed under vacuum in the e-beam evaporator within 10 minutes of completing the BOE oxide etch, there's no need for the Axic etch step.

wafer dicing An automated saw is used to dice the etched 3 inch silicon wafer into 9 chips. A regular silicon-cutting blade is used. See Section 8.7.7.1 on page 234 for details.

packaging The SOI trap chips were tested in the octagon style vacuum system. They were mounted on special chip carriers. The mounting and wiring methods are discussed in Section 4.1.3 on page 107.

continuity tests Follow the advice in Section 4.1.4 on page 108 prior to insertion into the vacuum system for vacuum processing.

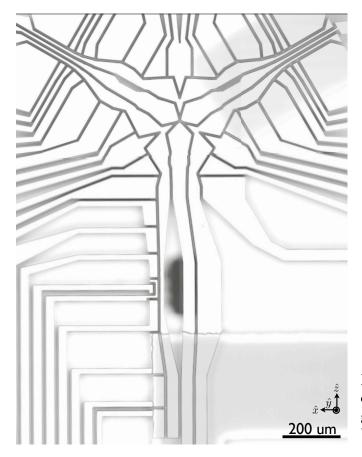


Figure 3.15: Optical micrograph of dv16k. Bright regions are gold coated. Dark regions are bare boron doped silicon.

vacuum processing Prior to insertion into the final ion trap vacuum system the thermal silicon oxide layer is stripped off the trap. A plasma etch was used for this (see Section 8.7.2 on page 203). Be sure to ground all the electrodes to prevent breakdown across the chip in the plasma.

3.5 dv16k: SOI y-trap

My first SOI trap was built to demonstrate a surface electrode y-junction. The electrode geometry was selected to minimize the height of axial pseudopotential bumps along the length of the radial pseudopotential minimum. The electrode shape at the y-junction was dictated by this minimization [Wesenberg 08a]. This trap was named dv16k. See Figure 3.15 for a photo.

dv16k was fabricated and electrically tested, but not loaded with ions due to concerns about a sizable phase difference ϕ_{RF} between the RF electrodes. If $\phi_{RF} \neq 0$, there is intrinsic micromotion which can't be shimmed using control electrode potentials. See Section 8.2 on page 169.

3.5.1 Electrical tests

The loaded Q_L of several trap chips was measured in an octagon style vacuum system (see Section 4.1.2 on page 104). For these tests 10-20 dBm RF was applied to the resonator and all control electrodes were grounded. I observed $Q_L = 50-80$ for $\Omega/2\pi = 30-35$ MHz. Similar results were obtained for the test trap chip in vacuum and in air. See Section 4.6.2 on page 139 to put these measurements in context.

3.5.2 Possible causes of $\phi_{RF} \neq 0$

The underlying problems that contributed to $\phi_{\rm RF} \neq 0$ were that the paths supplying potential to the RF electrodes followed different geometric paths, with different coupling to ground. Consider the two paths $(d_{23} \text{ and } d_1)$ leading to the two RF electrodes at the load zone $(RF_1 \text{ and } RF_2)$. The trap geometry is illustrated in Figure 3.16 on the following page. The path length difference was $\Delta_d = d_{23} - d_1 \sim 1$ cm. For $\Omega_{\rm RF}/2\pi = 35$ MHz, this path length difference would imply a phase difference,

$$\phi_{\rm RF} = 360^{\circ} \times \frac{\Delta_d}{\lambda_{\rm RF}} = 360^{\circ} \times 1 \ {\rm cm/8.6 \ m} = 0.4^{\circ}.$$

The paths leading to the load zone for the two RF electrodes RF₁ and RF₂ had different series resistances and different capacitive couplings to their environment. A crude lumped circuit model is sketched in Figure 3.17 on page 66 that takes into account the resistance of the leads and their capacitive coupling thru vacuum to adjacent electrodes and thru SiO₂ to the SOI handle. The model places distributed capacitances

Figure 3.16: Schematic of SOI ion trap dv16k annotated to explain why it would be expected to have excessive intrinsic micromotion. At the center of the schematic (boxed in red) is the trapping region; an SEM blowup is to the right. At the periphery of the schematic are wire bonding pads which supply the trap electrodes with RF and control potentials. The three RF electrodes (shaded in the SEM) are supplied RF potential by two bond pads (shaded in the schematic). The path length difference between them is $\Delta_d = d_{23} - d_1 \sim 1$ cm. All bond pads and traces are 100 μ m thick doped silicon overcoated by 1 μ m gold, except for the two darker regions in the SEM (boxed in blue) which have no gold overcoating. The series resistance of the electrodes is much higher without the gold. The micromotion analysis discussed in the text requires an estimate of the impedance of the traces (marked with green arrows) leading to the load trap.

at the end of a trace. A simplification to this model is to ignore all the elements with small impedance: keep only R_{1A} , C_{1B} and C_{1A} . This leaves a simple impedance divider.

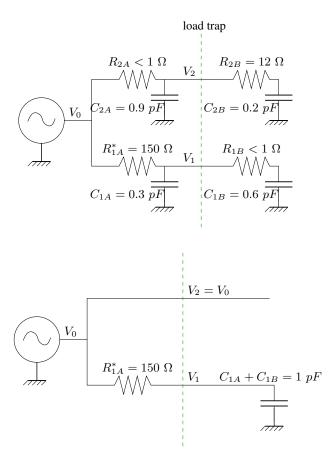


Figure 3.17: Schematic representation of the trap RF impedances. (top) A lumped circuit model for the phase difference between RF voltages at the loading region of trap dv16k. The impedances were calculated assuming: SiO₂ thickness 3 μ m, inter-electrode spacing 10 μ m, SiO₂ dielectric constant $\epsilon_r/\epsilon_0 = 3.9$, $\rho_{\rm Si} = 25,000 \times 10^{-6} \ \Omega$ -cm (experimentally determined as in Figure 3.18 on the next page) and $\rho_{\rm Au} = 2.27 \times 10^{-6} \ \Omega$ -cm. The resistance marked with * was measured experimentally using a pair of tungsten needle probes. (bottom) Simplified model neglecting low resistance elements. This model places an upper bound on ϕ_{RF} .

Suppose the input voltage is $V_0e^{i\omega t}$ and the impedance of the divider is X+iY. Then,

$$V_1 = V_0 e^{i\omega t} (X + iY) = V_0 Z e^{i(\omega t + \phi)}$$

where $Z = \sqrt{X^2 + Y^2}$ and $\phi = \tan^{-1}(Y/X)$.

 R_{1A}^* varied from chip to chip. It was not understood why it was measured to be 6 to 22 times higher than expected from $\rho_{\rm Si}$ (measured independently as in Figure 3.18 on the following page). For the RF phase calculation assume the measured resistance, $R_{1A}=150~\Omega.$

For the values above and the simplified model in Figure 3.17, $\phi_{RF} = 1.8^{\circ} + 0.4^{\circ} = 2.2^{\circ}$. This is an imperfect model for ϕ_{RF} ; C_{1A} and C_{1B} are distributed, not located at

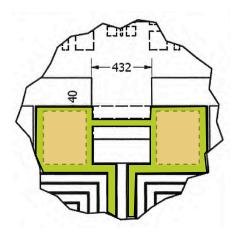


Figure 3.18: Doped silicon bulk resistance measurement test structure. Gold pads (dashed in the Figure) are connected by a 100 μ m tall, 40 μ m wide silicon bridge (shaded green in Figure). The silicon traces leading downward are electrically open. The resistance across this bridge was measured by plotting current vs voltage and confirmed to be Ohmic (see Section 8.7.4.3). From the resistance measurements the restivity was determined to be $\rho_{\rm Si}=25,000\times10^{-6}~\Omega$ cm. This is near the range $(5,000-20,000\times10^{-6}~\Omega$ -cm) specified by the manufacturer (see Section 8.7.5.4 on page 226). The dimension units are μ m.

the tip of electrode RF₁ as the model assumes.

The micromotion amplitude due to ϕ_{RF} is calculated in [Berkeland 98]. An alternate derivation follows. Suppose there is a field E_0 at the location of the ion due to each of the RF electrodes. Normally these fields are in phase and cancel at the center of the quadrupole. If however, there's a phase shift ϕ between them, there is a nonvanishing electric field component at the center of the quadrupole.

$$E_{total} = E_0 \cos(\Omega t) - E_0 \cos(\Omega t + \phi)$$

$$= E_0(\cos(\Omega t) - \cos(\Omega t) \cos(\phi) + \sin(\Omega t) \sin(\phi))$$
assuming $\phi \ll 1$,
$$\approx E_0(\cos(\Omega t)(1-1) + \phi \sin(\Omega t))$$

$$= E_0 \phi \sin(\Omega t)$$

The ion's response to E_{total} can be found by assuming $x = x_0 \sin(\Omega t)$.

$$qE_{\rm total} = m\ddot{x}$$

$$qE_0\phi\sin(\Omega t) = m\left(-\Omega^2\right)x_0\sin(\Omega t)$$

$$\to x_0 = -\frac{qE_0\phi}{m\Omega^2}$$

 $x_0 = x_{0\mu\mathrm{m}}$ is the micromotion amplitude resulting from the dipole term. For the dv16k load zone, 1 V on one of the RF electrodes produces a 2000 V/m radial field at the trap center. Typical trap parameters: $^{24}\mathrm{Mg}^+$, RF potential 80 V (as determined from measurement of secular frequencies and the electrode geometry), $\Omega/2\pi = 35$ MHz. For these parameters the expected micromotion for $\phi_{\mathrm{RF}} = 2.2^{\circ}$ is $x_{0\mu\mathrm{m}} = 500$ nm.

Ion motion can modulate the laser beam phase at the position of the ion. Let β be the modulation depth. It is convenient to express micromotion amplitude in terms of β ,

$$\mathbf{k} \cdot \mathbf{x}_{\mu \mathrm{m}} = \beta \cos(\Omega_{RF}),$$

where $k \cdot x_{\mu m} = k_x x_{0\mu m}$ is the overlap of the micromotion and laser beam k-vector. Typically, the Doppler cooling laser beam propagates at 45° with respect to $\hat{x}_{\mu m}$. So, with $k_x = \frac{1}{\sqrt{2}}k = \frac{1}{\sqrt{2}}\frac{2\pi}{\lambda}$ and $\lambda = 280$ nm, $\beta = \frac{1}{\sqrt{2}}\frac{2\pi}{\lambda}x_{0\mu m} = 8.1$. This micromotion amplitude would seriously affect the usefulness of the recooling method of measuring ion heating and the usefulness of the trap in general. Note that when $\beta = 1.43$, the carrier and first micromotion sideband have equal strength (see Section 8.2.1 on page 171).

3.5.3 Conclusion

These calculations suggest that as fabricated the RF potentials were expected to acquire an intolerable differential phase ϕ_{RF} , leading to considerable intrinsic micromotion. The problem was caused by a higher than expected R_{1A} (see Figure 3.17 on page 66). This could have been fixed by a second deposition of gold across the whole chip. However, this would have removed the possibility of comparing the heating rate

of gold with that of bare doped silicon, an experimental priority. This problem was corrected in this trap's successor, dv16m.

The SOI wafer used in this experiment was obtained from a distributor that resells surplus wafers. SOI with higher conductivity is available by special order. See Section 8.7.5.4 on page 226.

		0										70
trap	d	$\frac{\Omega_{RF}}{2\pi}$	V_{RF}	Q	Ion	$\frac{\omega_z}{2\pi}$	$\frac{\omega_{x,y}}{2\pi}$	N	$S_E(\omega_z)$	$ au_{dop}$	$ au_{dark}$	ϕ_{eV}
	$\mu\mathrm{m}$	MHz	V			MHz	MHz		$\frac{(V/m)^2}{Hz}$	min	sec	eV
B*SOI	41	67	50	90	$^{24}Mg^{+}$	1.125	7.80,	9	1×10^{-10}	60	10	> 60
SET							9.25					
m dv16m												

Table 3.5: Trap characteristics of zone m370 in dv16m in the format of Table 2.1 on page 32. Trap depth $\phi_{\rm ev}$ and $V_{\rm RF}$ were estimated by simulation.

3.6 dv16m: SOI linear trap

introduction A second SOI trap was fabricated with a layout that minimized ϕ_{RF} . This was accomplished by simplifying the trap layout to include just two RF electrodes and by making the path to the RF rails more symmetric. This trap had two multi-zone experimental regions with and without gold overcoating the silicon. Part of these experimental regions were tapered so that the ion-electrode distance R varied from 45 μ m in the load region to 10 μ m. These design features were included to test the dependence of ion motional heating on material type and R. I call this trap dv16m.

Trap dv16m successfully loaded ions. I was able to measure the ion secular frequencies and found they agree reasonably well with simulation. Transport into both the gold and bare doped silicon experimental regions was reproducible over a period of several months. Heating rate measurements were made in the gold and bare silicon experimental zones. However, a comparison of heating from these materials was not conclusive due to other possible sources of ion heating. This section presents the geometry of dv16m and its trapping performance. It then discusses some of the tests done to identify sources of ion heating.

3.6.1 Trap schematics

Figure 3.21 on page 73 is a dimensional schematic of the trapping region which also shows how the 24 DAC channels are shared among the trap electrodes. Figure 3.20 on the following page is a wiring table showing the mapping between the trap chip and the dsub cables leading to the DACs. Table 3.6 on page 74 is a mapping of DAC channel to electrode number.

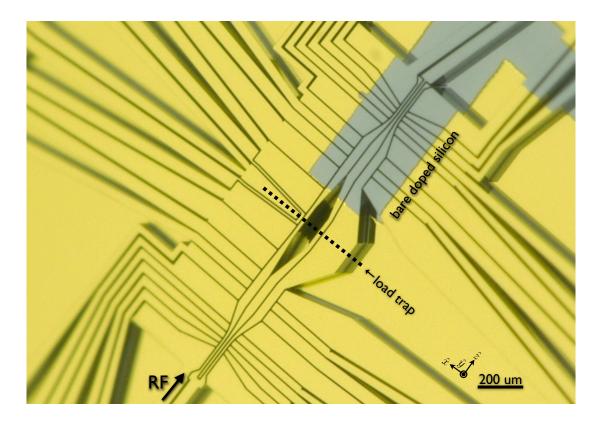


Figure 3.19: Optical micrograph of dv16m. The bright gold regions are gold coated; the darker regions are bare boron doped silicon. The camera is tilted, showing a perspective view of the trap which emphasizes the height of the SOI device layer (100 μ m thick).

updated 8/6/20	007				
function	BGA Pad	BGA Pin	trap side D- CON	DAC side D-CON (map1)	DAC CH
Au L45end	4	C1	T25	T25	1
Au Lstart	6	D1	T11	T11	5
Au LT	7	E2	T10	T10	7
Au LT	8	E1	T12	T12	3
Au L10end	10	F2	T24	T8	11
Au L10mid		F1	T13	T13	2
RF	_	G1	RF		
Au L10end		H1	B1	B1	24
NC		H2	B15	NC	NC
NC		J1	B2	NC	NC
Au R10end		J2	B4	B4	17
Au R10mid	_	K1	B3	B3	20
Au R10end	22		B14	B14	23
Au RT		N3	B16	B16	19
Au RT		N4	B5	B5	16
Au Rstart	-	M5	B17	B17	18
Au R45end		N5	B18	B18	15
Au R45end Au R45mid					
		M6	B19	B2	22
Au R45end		N6	B6	B6	14
Si R45end	_	N8	B8	B13	2
Si R45mid		M8	B20	B20	12
Si R45end		N9	B21	B21	9
Si RTstart		M9	B22	B22	8
Si RT		N10	B9	B9	10
Si RT		N11	B23	B23	6
Si RTend		L13	B25	B25	1
Si R10mid		K13	B11	B11	5
Si R10end		J12	B10	B10	7
NC		J13	B12	NC	NC
middle		H12	B24	B24	4
Si LTend	61	H13	B13	B13	2
Si L10mid	65	F13	T1	T1	24
Si L10end	66	F12	T15	T15	21
Si LT	68	E13	T2	T2	22
Si LT	69	E12	T4	T4	17
Si LTstart	70	D13	T3	T3	20
Si L45end	72	C13	T14	T14	23
Si L45mid	79	A11	T16	T16	19
Si L45end	81	A10	T5	T5	16
Si L		B9	T17	T17	18
Si LloadEnd	-	A9	T18	T18	15
mid near		B8	T19 open	T19 open	NC
mid far		A8	T6 open	T6 open	NC
GND		B7	T7	T7	GND
mid far		A6	T8	T8	11
mid near		B6	T20	T20	12
Au LloadEnd		A5	T21	T21	9
			T22	T22	
Au L		B5			8
Au L45end		A4	T9	T9	10
Au L45mid	97	A3	T23	T3	6

Figure 3.20: Wiring table for dv16m. This table shows details of the signal mapping between each DAC channel and the LTCC CPGA chip carrier. See 4.1.3 on page 107 for more about the chip carrier and its pin numbering.

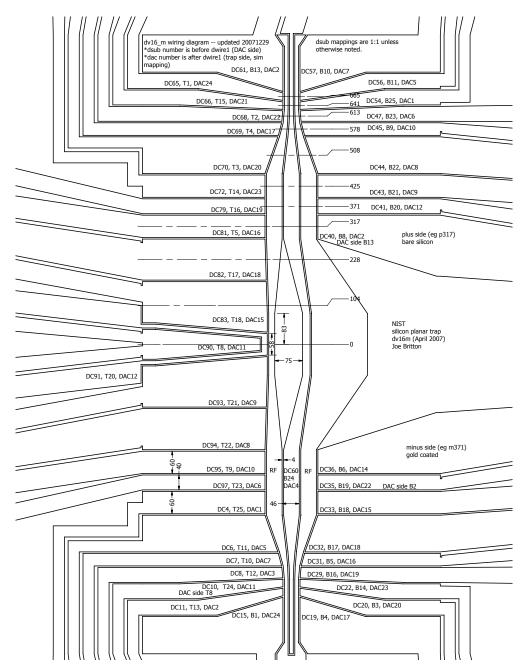


Figure 3.21: Electrode geometry for dv16m. The lengths are reported in μ m. Printed on each electrode is the electrode name (e.g. DC83), it's corresponding pin on the UHV dsub vacuum feedthrough (e.g. T18) and which DAC channel controlled its potential (e.g. DAC15). As there were more electrodes than DAC channels, several of the electrode potentials were connected to the same DAC channel when doing so would not interfere with ion trapping and transport (e.g. DAC15: DC83 and DC33). The nomenclature for particular trapping zones is p/m (plus/minus; the z-axis origin lies at the load zone) followed by the distance of the zone center from the center of the trapping region (e.g. p317). The first bare silicon experimental zone is p317 and the first gold coated experimental zone is m317.

card (line)	channel	electrodes
1 (1)	1	DC54, DC4
1(2)	2	DC40, DC61, DC11
1 (3)	3	DC8
1 (4)	4	DC60
1 (5)	5	DC56, DC6
1 (6)	6	DC47, DC97
1 (7)	7	DC57, DC7
1 (8)	8	DC44, DC94
2 (1)	9	DC43, DC93
2(2)	10	DC45, DC95
2(3)	11	DC90, DC10
2(4)	12	DC41, DC91
2(5)	13	
2(6)	14	DC36
2(7)	15	DC83, DC33
2 (8)	16	DC81, DC31
3 (1)	17	DC69, DC25, DC19
3(2)	18	DC82, DC32
3(3)	19	DC79, DC29
3(4)	20	DC70, DC20
3(5)	21	DC66
3 (6)	22	DC68, DC35
3 (7)	23	DC72, DC22
3 (8)	24	DC65, DC15

Table 3.6: Mapping of DAC channel to electrode number. There are three NI6733 DAC cards in this system each with 8 outputs (lines). The 24 DAC channels are shared among 44 electrodes. For example, electrodes DC54 and DC4 are at the same potential supplied by DAC channel 1.

3.6.2 Simulation

Calculation of the electronic potential and fields from a configuration of trap electrodes is discussed in Section 2.6.1 on page 24. This section presents typical results for these calculations specific to dv16m and gives numerical values for the fields in one of the experiment zones.

Figure 3.22 on the next page shows some plots of the axial component of the electric field along the trap axis. It includes a plot of $\left(E_z(z)\frac{\partial E_z(z)}{\partial z}\right)^2$ which can be a source of ion heating as discussed in Section 8.3.3 on page 177. Ions were not transported successfully into zones with ion to surface distance smaller than 40 μ m. The simulation suggests that trapping would have been difficult due to excessive motion and heating.

Figure 3.22 on the next page shows data generated by numerical simulation. It includes a plot of ion height vs distance along the trap axis; the pseudopotential minimum draws closer to the surface as the electrodes taper.

Figure 3.23 on page 77 is an equipotential plot superposed with electric field vectors near the pseudopotential minimum in zone m370.

Figure 3.24 on page 78 shows equipotential surfaces for the control potentials listed in Table 3.8 on page 80.

dv16m-p371 fields This section gives numerical values for the fields in the bare silicon experiment zone p371.

Let $C_{E_x}\left(\overrightarrow{x}\right)$ be the the x component of the electric field at position \overrightarrow{x} for 1 V on a particular electrode (all other electrodes grounded). For example, for a 1 volt potential on endcap electrode DC72 the electric field strength at the ion position \overrightarrow{x} (x = 371 μ m,

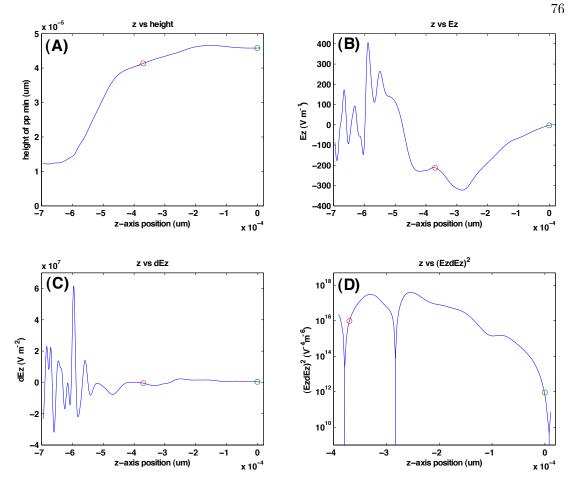


Figure 3.22: In all plots the parameters were evaluated at the local pseudopotential minimum in the x-y plane for each point along the z-axis. The z-axis ranges from the load zone $(z=0 \ \mu \text{m})$ to experiment zone m370 $(z=-370 \ \mu \text{m})$ to the end of the taper $(z=-700~\mu\mathrm{m})$. The location of the load zone and m370 are marked with circles in each plot.

- (A) Ion height above the wafer surface vs distance along the z-axis.
- (B) z-component of the electric field $E_z(z)$ vs distance along the z-axis.
- (C) $\frac{\partial E_z(z)}{\partial z}$ vs distance along the z-axis. (D) $\left(E_z(z)\frac{\partial E_z(z)}{\partial z}\right)^2$ vs distance along the z-axis.

 $y = 0 \mu m, z = 41 \mu m) is,$

$$C_{E_x} = -226 \ V/m \tag{3.6.1}$$

$$C_{E_y} = +476 \ V/m \tag{3.6.2}$$

$$C_{E_z} = -457 \ V/m. \tag{3.6.3}$$

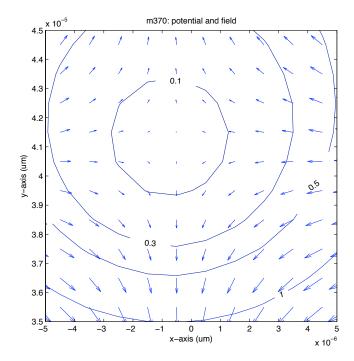


Figure 3.23: Plot of electric potential and fields in zone m370 (an x-y slice at $z=-370~\mu\mathrm{m}$) due to a potential of 1 V on the RF electrodes. The contour plot presents the numerical potential. The arrows are proportional to the electric field.

Let $D_{E_x}(\vec{x})$ be the the x component of the electric field at position \vec{x} for 1 V potential on the RF electrodes. At the same position \vec{x} , the electric field strength at the ion is,

$$D_{E_x} = 0 \ V/m \tag{3.6.4}$$

$$D_{E_y} = 0 \ V/m \tag{3.6.5}$$

$$D_{E_z} = 231 \ V/m \tag{3.6.6}$$

$$\frac{\partial E_z}{\partial z} = 23,500 \ V/m^2. \tag{3.6.7}$$

The axes are the same as those in Figure 3.24 on the next page. These numbers are used to calculate how the potential noise on RF and control electrodes can cause motional heating. Call this case dv16m-p371.

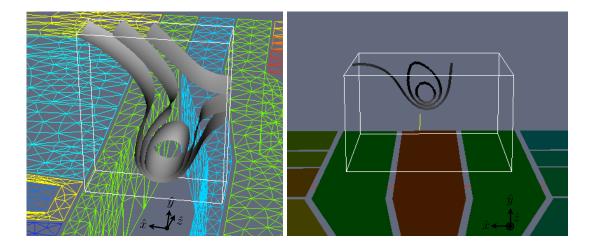


Figure 3.24: Plot of simulated total trapping potentials (pseudopotential plus control potentials) for two zones in dv16m. The white cube in each plot bounds the volume where the potentials were extracted from the simulation. (left) Pseudopotential equipotential surfaces at 50, 70 and 100 meV for the load zone; the minimum lies 45.7 μ m above the electrode surface. Visible in the background of this figure is the mesh grid used in the simulation. Note that the mesh extends downward into the loading slot lying beneath the trapping region. (right) Pseudopotential equipotential surfaces at 10, 25, and 50 meV for the m370 zone; the minimum lies 41.6 μ m above the electrode surface. Visible in the background of this figure are the trap electrodes; the simulation mesh is hidden from view. A comparison with experiment is in Table 3.7 on the next page. The control potentials used for these traps are given in Tables 3.8 on page 80.

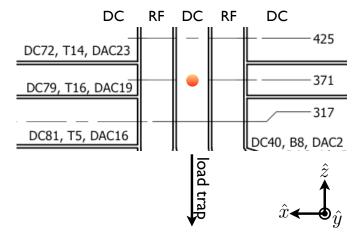


Figure 3.25: Ion trap schematic for first experimental zone of trap dv16m. This zones lies $+371~\mu m$ from the load zone and is 41 μm above the trap surface. The electric fields quoted in the text (Equations (3.6.1) to (3.6.3)) are derived from simulation.

3.6.3 Comparison with simulation

Numerical simulation can be used to optimize trap parameters such as axis rotation and trap depth. This section compares trap parameters measured in the experiment with those predicted by simulation. Figure 3.24 on the preceding page shows equipotential surfaces for the control potentials listed in Table 3.8 on the next page. Table 3.7 compares simulation with experiment.

3.6.4 Transport waveforms

Ion transport from one zone to another was accomplished by applying appropriate potentials to the control electrodes. These waveform potentials translated the axial trapping minimum. This waveform is generated from numerical simulation. For example, an excerpt of the waveform used to transport an ion from the load zone of dv16m to the m370 experiment zone (a distance of 370 μ m) is plotted in Figure 3.26 on page 81. The initial waveform for this transport was produced by solving for the control potentials required to place an ion at the pseudopotential minimum with an axial frequency of

zone		$\Omega_{ m RF}$	$V_{ m RF}$	$\omega_z/2\pi$	$\omega_x/2\pi$	$\omega_y/2\pi$	$\phi_{ m ev}$	$ heta_{ m tilt}$
		(MHz)	(Volts)	(MHz)	(MHz)	(MHz)	(meV)	(degrees)
load	experiment	43.45		2.48	7.15	8.24		
	$_{ m simulation}$	43.45	46.0	2.02	7.15	7.82	67	31°
m370	experiment	67.20		1.125	7.80	9.25		
	$_{ m simulation}$	67.20	50.0	1.082	7.80	8.43	25	2.5°

Table 3.7: Table comparing numerical simulation with experiment for dv16m. In the simulation, $V_{\rm RF}$ was set by the requirement that ω_x match the experiment. The secular frequencies were measured by the endcap tickle technique (see Section 8.4 on page 179). For the load trap the simulation does not match experiment very well. This may be because the loading slot geometry was not accurately specified in the simulation due to its nonuniform geometry. The control potentials for these traps are given in Table 3.8 on the following page.

 $\omega_z = 1.5$ MHz at each of 38 positions along the z-axis. This solution didn't provide useful transport. The final waveform in the Figure was generated by incrementally moving from one point of the simulated waveform to the next and manually tweaking the control potentials to keep the ion's fluorescence a maximum. The same technique was used to generate a waveform for transport from the load zone to p370. A possible reason the simulation alone did not produce successful transport is imperfect representation of the trap geometry in the simulation.

Once a satisfactory waveform was determined, ions could be reliably transported from the load zone to the experimental regions. For example, transport from the load zone to an experimental zone and back could be repeated hundreds of times at a $1\ Hz$ repetition rate without ion loss. For this looping test a pair of Doppler cooling laser beams were positioned in the starting and ending traps.

	$_{ m endcaps}$		middle		center	
	DC83	DC93	DC60	DC91	DC90	
	+4.00	+4.00	+0.53	0.00	-9.38	-
endca	aps A	endca	aps B	\min	ldle	center
	-		aps B DC36			

Table 3.8: This table lists the control potentials used for the experimental data in Table 3.7 on the preceding page. (top) dv16m load zone potentials. (bottom) dv16m m370 zone potentials. The endcaps are asymmetrically biased in order to induce a slight twist to the trap axes.

transport waveform: load zone to m370 DAC 1 1 6 9 10 11 15

Figure 3.26: Transport waveform for moving ions from the load zone to zone m370. To make the plot easier to read, only the potentials for electrodes in the load zone (DAC15, DAC11 and DAC9) zone and one side of the the destination zone (DAC10, DAC6 and DAC1) are plotted. The full waveform specifies potentials for all 24 DAC channels. The waveform step size is 10 μ m and the full transport typically took about 1 ms. At z=0 μ m the load zone ends caps are at ~ 2.0 V. At z>0 the ion is initially pushed along the trap axis in the negative direction by the potential on DAC15. The waveform ends in a weaker trap at m370 with the endcaps at ~ 200 mV.

z (um)

-370 (Au zone) 1

-3

1 0 (load zone)

3.6.5 Electrical tests

The loaded Q_L of several trap chips was measured in an octagon style vacuum system (see Section 4.1.2 on page 104). For these tests 20 dBm RF was applied to the resonator with all control electrodes grounded. I observed $Q_L = 80 - 100$ for $\Omega/2\pi = 43$ MHz. The DC resistance between ground and the control electrodes was >10 M Ω , with typically one low resistance short (10-100 k Ω) between a control electrode and ground per chip. Motional heating tests were done with a chip where $Q_L = 90$ for $\Omega/2\pi = 67 - 74$ MHz and with R(DC22-GND)=40 k Ω (all others >10 M Ω). See Section 4.6.2 on page 139 to put these measurements in context.

3.6.6 Dark lifetime

In well behaved traps, ions will remain trapped even in the absence of cooling laser beams. For example, without laser cooling ${}^{9}Be^{+}$ ions survived in a room temperature trap for several minutes [Rowe 02]. The lifetime of several ions in the dark for the load zone of dv16m is in Table 3.9 on the following page. The longest observed lifetime was 10 seconds.^{2}

² Note that during my first attempt at loading ions in trap dv16m I observed longer dark lifetimes than reported in Table 3.9 on the next page. For example, one ion survived for 60 sec in the dark twice in succession. For this trap $\omega_z/2\pi \cong 500$ kHz and $\omega_{x,y}/2\pi \cong 8$ MHz. Unfortunately, this trap stopped loading after about two days and I installed a new copy of dv16m in the vacuum system. This thesis discusses this second trap which worked reliably for > 6 months.

ion no.	1/2	1	2	3	4	5	10
1	1	3	1	2	1	1	0
2	1	3	1	2	1	1	0
3	1	3	1	2	1	0	
4	1	3	1	2	1	2	0
5	1	3	1	2	1	2	1
6	1	3	1	2	1	1	0

Table 3.9: Table reporting ion lifetime without Doppler cooling in dv16m. The load zone was used for these measurements and the control potentials were supplied by batteries. For this experiment I did not measure the trap frequencies; from previous experiments I estimate that they were $\omega_z/2\pi \cong 2.5$ MHz and $\omega_{x,y}/2\pi \cong 8$ MHz. Each line in the table above corresponds to an ion that was loaded into the trap then Doppler cooled for 3 minutes to permit the vacuum to recover. Then, the cooling laser beam was blocked for durations of 1/2 to 10 seconds. The number in the table is the number of times the beam was blocked for each ion. Ion loss is indicated by an entry of 0. For example, the first ion survived for periods in the dark of 0.5 sec, 1.0 sec, 1.0 sec, 1.0 sec, 2.0 sec, 3.0 sec, 3.0 sec, 4.0 sec, 5.0 sec and was lost when it was put in the dark for 10.0 sec. Note that when the same experiment was done with the DACs instead of batteries (and only the usual 1 $k\Omega$ and 820 pF filtering) the maximum dark lifetime was 1 second.

3.6.7 Motional heating

In addition to trapping and transport, one of the main objectives for this trap was a comparison of the motional heating for two material types: gold and bare boron doped silicon. It was anticipated that the heating for these two surfaces would differ. However, within the sensitivity of my experiments I observed no difference. Moreover, I saw that the electric field spectral density at the ion in dv16m was about ten times higher than the best NIST SET [Seidelin 06] (see Figure 2.10 on page 23) and the heating rate varied by up to an order of magnitude day to day (see Figure 3.27). The large day to day variation is not common for traps tested at NIST, however it is a common occurrence that nearly identical traps have observed to have widely differing heating rates (again, see Figure 2.10 on page 23). It was hypothesized that these observations were due to an external source of electric field noise. This section discusses several possible sources of heating and related experiments.

The following frequencies are known to couple to the motion of a single ion.

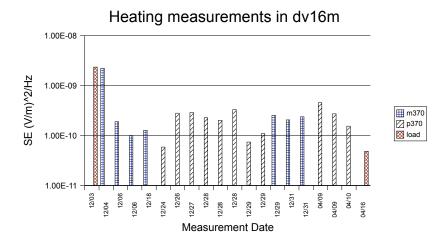


Figure 3.27: Motional heating measured in dv16m over time. For each measurement the control potentials were supplied by batteries and the micromotion was nulled along the cooling laser beam.

- (1) ω_i (direct drive)
- (2) $\Omega_{RF} \pm n \ \omega_i$ for $n \in \{1, 2, ...\}$ (only if micromotion along the i^{th} trap axis)
- (3) $\Omega_{RF} \pm 2 \ n \ \omega_i$ for $n \in 1, 2, ...$ (only if no micromotion along the i^{th} trap axis), where Ω_{RF} is the trap drive frequency and ω_i is the secular frequency along the i^{th} principle axis $i \in \subset \{x, y, z\}$. The third coupling mechanism is called parametric heating. Electric field noise at these frequencies may originate from a variety of sources. There are several sources of noise power at these frequencies in the trap.
 - noise in potentials applied to trap control electrodes (e.g. DAC noise)
 - noise in the RF drive potential (e.g. amplifier and RF oscillator noise)
 - Johnson noise from finite electrode impedance and trap high pass RC filters.
 - Johnson noise from the RF resonator's finite impedance
 - ambient laboratory fields coupled to trap apparatus (e.g. poorly shielded cables)
 - field-emitters (due to sharp points on the electrodes)
 - collisions with background atoms
 - fluctuating patch potentials at the electrode surfaces

The sections that follow discuss some of these noise sources and attempts to mitigate them when possible. They are also discussed in the literature [Turchette 00, Wineland 98, Deslauriers 06b, Labaziewicz 08, Leibrandt 07].

noisy control potentials

One source of electric field noise is potential noise on trap electrodes. The resulting fields directly couple to an ion's motion via its charge and can cause motional heating. One way to characterize the heating is with $\Gamma_{0\to 1}$, the heating rate from the ground state to the first excited motional state in units of quanta/ms. To characterize the noise fields, the electric field noise spectral density $S_E(\omega)$ is usually specified instead of $\Gamma_{0\to 1}$. This is because $S_E(\omega)$ is useful when comparing traps; it normalizes across ion species

	(V/\sqrt{Hz})	(V/\sqrt{Hz})
	Noise at SA	Noise at trap
DAC	125×10^{-9}	523×10^{-12}
DC supply	125×10^{-9}	523×10^{-12}
battery	12×10^{-9}	52×10^{-12}
$50~\Omega$	12×10^{-9}	

Table 3.10: Control potential supply noise at $\omega/2\pi=3$ MHz in a 1 Hz bandwidth. The second column is the expected noise at the trap electrodes after attenuation by the RC filters. 50 Ω termination was used to measure the SA noise floor, which was far larger than the Johnson noise of the resistor.

and trap frequencies. These quantities are connected by [Turchette 00],

$$\Gamma_{0\to 1} = \frac{q^2 S_E(\omega)}{4m\hbar\omega}$$

where q is the ion charge, m is the ion mass, ω is the motional secular frequency, and $S_E(\omega)$ is the electric field noise spectral density at ω .

The potentials applied to trap control electrodes were generated by DC supplies, DACs and batteries (see Table 4.1 on page 134). The noise of these potential sources (at 0 V and 1 V outputs) when they were generating a constant potential was measured at $\omega_z/2\pi=3$ MHz. A spectrum analyzer (SA) with a DC block capacitor and a 50 Ω input impedance was used to measure the potential noise just before the RC filter boxes (see Figure 4.16 on page 130 to see how they are situated with respect to the trap). The SA noise floor was -145 dBm/Hz = $12 \times 10^{-9} V/\sqrt{Hz}$.

The trap RC filters have a 3 dB point of approximately 200 kHz (C=820 pF, R=1000 Ω). The noise potential attenuation factor for the RC at $\omega_z/2\pi=3$ MHz is 240.

Table 3.10 summarizes the observed noise and the calculated noise at the trap electrodes after attenuation by the RC filters.

p371: test case heating For zone p371 (Section 3.6.2 on page 75) calculate ion heating due to potential noise at a trap electrode. For example, for $^{24}Mg^{+}$ an electric

field spectral density $S_E(\omega)$ of $1.23 \times 10^{-11} \left(\frac{V}{m}\right)^2 \frac{1}{\text{Hz}}$ in the z-direction at $\omega_z/2\pi = 3$ MHz in gives rise to a heating rate of 1 quanta/ms. A potential of $7.7 \times 10^{-9} \frac{V}{\sqrt{Hz}}$ at electrode DC72 produces such a field. Note that it is the noise power spectral density that is typically measured on a spectrum analyzer $\frac{S_V(\omega)}{50 \Omega} = -149 \frac{\text{dBm}}{\text{Hz}}$. By way of comparison, the Johnson noise potential of a 50 Ω resistor at room temperature is $0.9 \times 10^{-9}/\sqrt{Hz}$, which as a noise power is $-167.8 \frac{dBm}{Hz}$ (into 50 Ω).

For all heating measurements for dv16m, I used shielded batteries referenced to the trap ground. Control electrode noise is therefore not expected to make a large contribution to motional heating in my experiments.

RC filter Johnson noise

Thermal electronic noise results from finite electrode resistance and from other lossy circuit elements. Since the wavelength of the secular frequencies and RF drive are large compared with the trap geometry, its acceptable to treat the fundamentally microscopic thermal noise with lump-circuit models. In practice, the dominant lossy element is the resistor forming part of the RC low pass filter attached to each control electrode (see Figure 2.8 on page 20) [Wineland 98].

Typically, R=1 $k\Omega$ and C=820 pF. The 1 $k\Omega$ resistor in this filter has an associated room temperature Johnson noise. Its voltage spectral density S_{V_n} is

$$S_{V_n} = 4k_B T R$$

$$= 1.6 \times 10^{-17} V^2 / \text{Hz}$$

$$\sqrt{S_{V_n}} = 4 nV / \sqrt{\text{Hz}}.$$

As a power spectral density (into 50 Ω) this is $-154 \, \mathrm{dBm/Hz}$ which is difficult to measure on many spectrum analyzers.

The noise at the trap electrodes is less than S_{V_n} due to the control electrode RC filter attenuation. The filters can be modeled as a voltage noise source and noise free

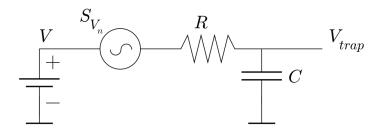


Figure 3.28: Lumped circuit model for the control electrodes' low pass filters. The resistor is modeled as a perfect resistor in series with a Johnson noise source.

resistor. The voltage spectral density attenuation is

$$A_{LP} = \frac{1}{1 + (\omega RC)^2}$$

for the impedance divider. At $\omega/2\pi = 3$ MHz and the RC values above, the attenuation of $S_E(\omega)$ is 240.

It is straightforward to calculate the expected heating rate as

$$\Gamma_{0\to 1} = 4 \times \frac{e^2}{4m\hbar\omega} \times S_{V_n} C_{E_z}^2 \times A_{\rm LP}$$

$$= 0.005 \text{ quanta/ms}$$

where C_{E_z} is as for dv16m-p371 (see Equation 3.6.3 on page 76) and the factor of 4 accounts for the four endcap control electrodes in this trap. This rate is well below that observed experimentally. Therefore, the LP filter Johnson noise doesn't explain the observed ion heating.

RF resonator Johnson noise

The trap RF potential is derived from a voltage step-up transformer fed by an RF

Table 3.11: Noise from RF resonator resistance. For, $\Omega_{\rm RF}/2\pi=71$ MHz, $Q_L=80$, $R=38~k\Omega$ and T=300 K. $\omega_z/2\pi=3$ MHz and $\omega_x/2\pi=10$ MHz are typical axial and radial secular frequencies, respectively.

oscillator. In the lab this takes the form of a $\lambda/4$ RF cavity resonator. See Section 8.5 on page 182 for details on resonant cavity oscillators modeled as lumped circuit RLCs and Section 4.6 on page 138 for details on the experimental apparatus.

On resonance, the cavity's impedance is resistive and is a source of Johnson noise. The parallel resistance R can be calculated and is typically around 38 $k\Omega$ (see Section vrefsec:apparatus:trapQLoss). The resonator line shape filters this and other RF noise sources (e.g. amplifier noise),

$$S_{V_n}(\omega) = 4k_B TR \times \left(1 + 4 Q_L^2 \left(\frac{\omega - \Omega_{RF}}{\Omega_{RF}}\right)^2\right)^{-1},$$

where Ω_{RF} is the RF resonant frequency, Q_L is the resonator loaded quality factor, T is the RF resonator temperature and ω is the observation frequency. Table 3.11 on the previous page summarizes the amplitude of RF power due to Johnson noise at various frequencies which can cause ion motional heating (Section 8.3 on page 174).

This noise power at ω_x and ω_z is far too small to cause noticable heating in my traps (see Section 3.6.2 on page 75). As we will see in Section 8.3 on page 174 noise at secular difference frequencies may however play a role in motional heating.

ambient laboratory fields

Ion heating may also result from electronic noise originating outside the trapping apparatus. These fields could couple to the trap structure via poorly shielded/grounded cables. To check for this, ion heating was measured before and after disconnecting the following apparatus connected to the vacuum system.

- ion gauge controller and cable
- Mg oven current supply and cable
- titanium sublimation pump controller and cable

No change in heating was observed.

Ambient laboratory fields might also couple to the trap structure through optical ports in the vacuum housing. I placed a pickup coil at the trap imaging port, flush with

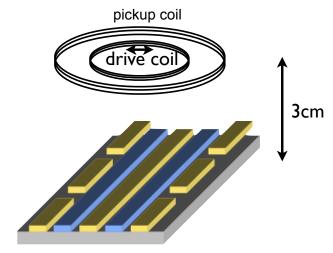


Figure 3.29: Coupling coils for tickle with external fields. Small drive coil (2.75 cm by 11 turn) surrounded by a pickup coil (7 cm diameter by 9 turns). The self resonant frequency of the coils was > 100 MHz.

the quartz window. This port lies 3 cm above the trap. The pickup coil was attached to an operational amplifier (OpAmp) buffer and monitored on a spectrum analyzer (SA). The noise spectrum observed near is in the top half of Figure 3.31 on the next page.

Since the environmental noise had narrow spectral features, it would be hit or miss whether the noise had much power at the ion's axial secular frequency ω_z . It was not experimentally convenient to sweep ω_z . Therefore, I injected broad current noise on a second coupling loop concentric with the pickup loop. I used an amplitude

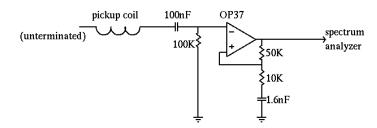


Figure 3.30: OpAmp driver for pickup coil. The voltage gain is 5 times and the low frequency 3 dB point is 10 kHz. The circuit is powered by a battery and is housed in a shielded enclosure.

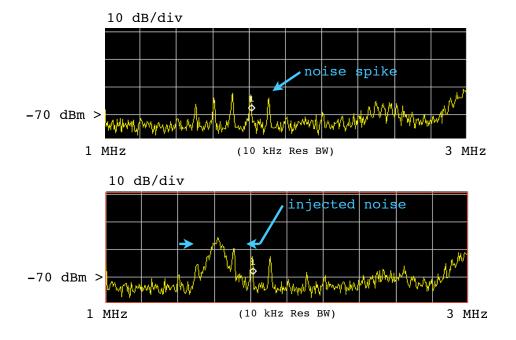


Figure 3.31: Pickup from coupling coil. (top) Spectrum analyzer (SA) trace showing the ambient laboratory noise background. (bottom) SA trace showing ambient noise plus injected noise (20 dB attenuation). The SA resolution bandwidth was 10 kHz.

commensurate with the ambient noise as judged by the pickup loop.

Current noise was generated by frequency modulating a coherent RF source with white noise generated by a SRS DS345. The RF center frequency coincided with the ion axial frequency ω_z . A 100 kHz FM depth was used. With the amplified pickup coil attached to a SA, the field from the drive coil could be detected in addition to environmental noise. Figure 3.31 (bottom) shows injected noise superimposed on laboratory noise spikes extending 10 dB above the noise floor. These spikes were not artifacts of the pickup coil or detector.

Ion heating was measured with various levels of current noise applied to the drive coil. Table 3.12 on the next page shows ion heating and the noise power detected by the pickup coil when the current noise was not attenuated (0 dB), attenuated by 10 dB or

(dB)	$\left(\frac{dBm}{10 \ kHz}\right)$	$({ m quanta/ms})$
Noise Attn.	P	$\Gamma_{0 \to 1}$
∞	-75	< 10
0	-57	790
10	-64	413
∞	-75	< 23
10	-63	467

Table 3.12: Ion heating ($\omega_z=1.6~\mathrm{MHz}$) due to injected noise. A sequence of 300 ms heating measurements were done with varying amounts of attenuation (0 dB, 10 dB, ∞ dB) for the injected noise. P is noise power in a 10 kHz bandwidth observed at 1.6 MHz using the pickup coil on a spectrum analyzer (SA). The SA resolution bandwidth was 10 kHz.

disconnected (∞ dB) from the drive coil.

With 10 dB attenuation, the current noise caused considerable ion heating and the signal from the pickup coil was difficult to discern from background noise on the spectrum analyzer. This experiment suggests that environmental noise could cause considerable heating if it were to overlap with the ion's motional frequencies.

These observations suggests that ambient laboratory fields which may be difficult to detect with laboratory electronic sensors may couple to ion motion and cause heating. When striving to minimize ion motional heating it is advisable to try several axial frequencies as there may be environmental noise.

micromotion compensation For quantum information applications it highly desirable that an ion have no micromotion at the several experimental zones along the trap z-axis (e.g. at $z = +370 \mu \text{m}$). See Section 8.2 on page 170 for why micromotion is problematic. If the ion is constrained to lie at a particular point along the z-axis where an axial RF electric field exists, micromotion results which can't be nulled. Conventional 2-layer ion traps (see Figure 2.1 on page 8) by symmetry have no axial electric field. In this kind of trap there is no intrinsic axial micromotion and we need only to be concerned with nulling micromotion in the radial directions. In contrast, surface electrode ion traps (SETs) do not have this symmetry and gradients in the RF potential along the trap axis

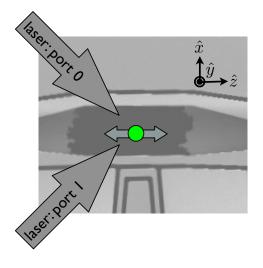


Figure 3.32: Two Doppler cooling laser beams in the plane of the surface electrode trap. They are equally sensitive to the micromotion component along the trap axis (gray arrow). The ion location in this picture is the load trap (0 μ m along the z-axis).

are possible. Some SET electrode geometries result in significant axial RF electric field and micromotion occurs that can't be nulled with control potentials.

When I designed the dv16m electrode geometry I did not take any measures to minimize the axial RF electric field. Numerical simulations show that the dv16m geometry had significant axial fields in all trapping zones except the load zone. The tapered region was especially problematic in this respect. See for example Figure 3.22 on page 76 which shows $\partial E_z^2(z)/\partial z \propto \phi_{pp}$ along the trap axis.

load zone Simulations predicted a pseudopotential zero in the load zone (see Figure 3.22 on page 76). To check this I applied a pair of orthogonal Doppler cooling laser beams to an ion in the load zone (illustrated in Figure 3.32). Micromotion in a plane parallel to the trap surface can be measured using this pair of beams which propagate along the surface and have a large inclination with respect to the trap z-axis. Motion along the z-direction gives a Doppler shift to both beams. z-axis micromotion was minimized by minimizing the fluorescence on the n = 1, 2, ... RF sidebands on both beams. If sideband amplitude remains and is symmetric for the two beams, then it is due to axial micromotion.

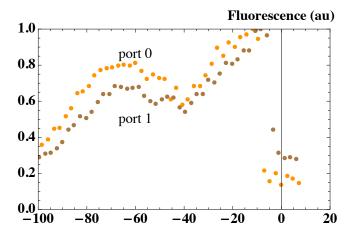


Figure 3.33: Fluorescence for the laser beams at port 0 and port 1 after following the micromotion nulling recipe. The residual axial micromotion corresponds to a modulation index of $\beta \sim 1.3$.

This experiment was carried out in the load zone with all the endcaps shorted to ground. In this configuration it is expected that the ion will sit at the axial field minimum barring displacement due to stray electric fields; I saw no evidence of sizable stray fields. From simulation, this is the only place in the trap structure where there is zero axial micromotion. However, even at this location I could not simultaneously null the micromotion sidebands for the pair of beams. That is, there was significant intrinsic axial micromotion. The plots in Figure 3.33 show symmetric sidebands that couldn't be further minimized using control potentials. This could indicate a nonzero phase difference between the RF potentials on the RF electrodes as discussed in Section 3.5.2 on page 64.

ion heating due to noisy RF potentials and micromotion

The RF pseudopotential which provides ion confinement can also cause motional heating $\dot{\bar{n}}$ if the RF source is noisy and the ion has micromotion. See Section 8.3 on page 174 for details on this mechanism.

Micromotion in the radial direction arises due to uncompensated stray electric fields; this micromotion can be nulled using control potentials if it can be detected. For a particular trap zone along the z-axis, micromotion in the axial direction arises due

to an axial RF electric field; this micromotion can't be nulled. Figure 3.22 on page 76 shows $E_z(z)$ (the electric field along along the trap axis). Small micromotion amplitude does not adversely impact the recooling heating measurement technique (discussed in Section 4.7 on page 141). However, in both cases noise on the RF potential can cause heating of the axial and radial modes.

The importance of minimizing $E_z(z)\frac{\partial E_z(z)}{\partial z} > 0$ in Equation 8.3.26 on page 177 was not fully appreciated until after the trap was built. In this section I calculate the heating due RF noise and micromotion in dv16m zones m370 and p370.

I denote the noise power at frequency ω_n relative to the power at the carrier frequency $\Omega_{\rm RF}$ as $\alpha^2 \equiv P_{noise}/P = 2S_{E_n}/E_0^2 = 2S_{V_n}/V_0^2$. According to the manufacturer's specification for the oscillator I used, an HP 8640B, $\alpha_{8640B}^2 \cong -147$ dBc for noise at $(\Omega_{\rm RF} - \omega_n)/2\pi = 1$ MHz (see Figure 4.17 on page 138). There may also be additional noise added by the RF amplifier, a Amplifier Research, Inc. 1 W AR 1W1000A. However, a noise figure is not available for this amplifier.

axial heating If $\left|E_z(z)\frac{\partial E_z(z)}{\partial z}\right| > 0$ and there is noise on the RF potential at the axial trap frequency ω_z , as in Equation 8.3.17 on page 176, ion heating \dot{n} results.

Section 8.3.3 on page 177 derives the following expression for the axial heating rate,

$$\dot{\bar{n}}(\omega_z) = \frac{1}{4m\hbar\omega_z} \times \left[\frac{q^2}{m\Omega_{\rm BE}^2} E_0(z) \frac{\partial E_0(z)}{\partial z} \right]^2 \frac{S_{E_n}(\omega_n)}{E_0^2(\omega_n)},\tag{3.6.8}$$

in units of quanta per second.

Consider zone p371 ($z=+371~\mu\mathrm{m}$), discussed in Section 3.6.2 on page 75. Typical trap parameters are $^{24}Mg^+$, $\Omega_{\mathrm{RF}}/2\pi=70~\mathrm{MHz}$, $\omega_z/2\pi=3~\mathrm{MHz}$ and $V_{\mathrm{RF}}=50~\mathrm{V}$. Numerical simulation gives $E_z(z)=213~V/m$ and $\frac{\partial E_z(z)}{\partial z}=23,500~V/m^2$ (Equations 3.6.6 on page 77 and 3.6.7 on page 77). Accounting for 17 dB of attenuation due to the $\lambda/4$ resonator (see Table 4.2 on page 139),

$$\frac{\dot{\bar{n}}(\omega_z)}{\alpha^2} = 1.3 \times 10^{11} \ quanta/ms. \tag{3.6.9}$$

If $\alpha^2 = \alpha_{8640B}^2 \cong -147$ dBc, then $\dot{\bar{n}}(\omega_z) = 27 \times 10^{-6}$ quanta/ms.

This heating rate could be four orders of magnitude greater for locations just several 10's μ m away from position p370 (see Figure 3.22 on page 76) or if α^2 were larger.

radial heating If an ion's mean position is displaced radially from the pseudopotential minimum by a distance x, as from a stray static electric field, the ion undergoes micromotion. If the RF electric field is noisy, as in Equation 8.3.17 on page 176, ion heating results.

Section 8.3.3 on page 177 derives the following expression for the the radial heating rate,

$$\dot{\bar{n}}(\omega_x) = \frac{1}{4m\hbar\omega_x} \times \left[2m\omega_x^2 x\right]^2 \frac{S_{E_n}(\omega_x)}{E_0^2(x)} \tag{3.6.10}$$

in quanta per second and where ω_x is the frequency of radial motion.

Consider zone p371 ($z=+371~\mu\mathrm{m}$), discussed in Section 3.6.2 on page 75. Typical trap parameters are $^{24}Mg^+$, $\Omega_{\mathrm{RF}}/2\pi=70~\mathrm{MHz}$ and $\omega_x/2\pi=10~\mathrm{MHz}$. Assume $\beta=1.43$, which gives a micromotion amplitude of 64 nm and a displacement of $x=1.05~\mu\mathrm{m}$ (see Section 2.3.2 on page 15). Accounting for 27 dB of attenuation due to the $\lambda/4$ resonator (see Table 4.2 on page 139),

$$\frac{\dot{\bar{n}}(\omega_z)}{\alpha^2} = 2 \times 10^{17} \ quanta/ms. \tag{3.6.11}$$

If $\alpha^2 = \alpha_{8640B}^2 \cong -147$ dBc, then $\dot{\bar{n}}(\omega_z) = 0.4$ quanta/ms.

This heating rate could greater if β or α^2 were larger.

3.6.8 Trap environment and motional heating

There are several key difference between the vacuum apparatus used in my experiments and in Seidelin's at NIST where an order of magnitude lower motional heating rate was observed. I used an octagon style vacuum system discussed in Section 4.1.2 on

page 104 for tests of dv16m. Seidelin used a $\lambda/4$ style vacuum discussed in Section 4.1.1 on page 102 [Seidelin 06]. Some of the differences between these systems could contribute to the difference in motional heating. Further evidence for this possibility is suggested by results found in an ion trap (Amini, NIST) very similar to the Seidelin design which had excellent heating. This trap was tested in an octagon style vacuum system and also exhibited an approximately order of magnitude higher heating rate (see Figure 2.10 on page 23) than Seidelin's.

Following is a list of several differences between the octagon and $\lambda/2$ style vacuum systems which could be related to the electronic environment at the ion.

RF lead length The RF lead length in the vacuum systems differ. In both it is a Kapton wrapped wire. It's length should be a minimum to prevent radiative losses, inductive impedance and capacitive coupling to ground.

- octagon: The RF lead length in the vacuum system is typically 5 cm.
- λ/4: The RF lead length beyond the end of the λ/4 center conductor is typically short, < 2 cm. Moreover, the entire trap chip including the lead lie within the bore of the λ/4 resonator.

UHV RF FT The location of RF UHV feedthrough differs.

- octagon: The UHV RF feedthrough lies at the tip of the resonator, near it's highest voltage point. It has a large (8-15 pF) capacitance to ground.
- λ/4: The UHV RF feedthrough lies inside the λ/4 resonator at about its midpoint. It has a smaller (4.5 pF) capacitance to ground.

Resonator geometry The geometry of the RF resonators differ.

- octagon: The resonator is a helical cavity resonator [Macalpine 59].
- $\lambda/4$: The resonator is a coaxial cavity resonator [Jefferts 95].

Loaded Q_L The loaded Q_L of the RF resonators differs with no trap chip attached.

• octagon: With the resonator attached to the vacuum system, with the RF routed

to a pin on the chip carrier but with no trap chip installed, I observed $Q_L=225$ at $\Omega_{\rm RF}=45$ MHz.

• $\lambda/4$: With the resonator attached to the vacuum system but no trap chip attached to the center conductor of the resonator, typical values are $Q_L = 800$ at $\Omega_{\rm RF} = 100$ MHz.

Delivery of RF and control potentials to trap chip

- octagon: A cofired ceramic chip carrier was used (see Section 4.1.3 on page 107)
 to supply the trap chip with both control and RF potentials. These potentials
 were communicated to the chip carrier by spring-loaded socket-pin connectors.
 Also, cofired ceramic is a new material for ion trapping applications.
- λ/4: An alumina or quartz substrate was used to route the control and RF
 potentials to the trap. Wires supplying these potentials were attached directly
 to traces on the substrate by resistive welding.

Shielding The degree of shielding from ambient laboratory noise.

- octagon: It's geometry is open with many view ports with line of sight to the trap chip.
- $\lambda/4$: The entire trap chip including the lead lie within the bore of the $\lambda/4$ resonator. Openings for the lasers and imaging system are smaller than for the octagon.

RC filter location The location of the RC filters differ for the two systems. These filters short to ground RF potential coupled to the control electrodes from the RF electrodes by a small inter-electrode capacitance C_T . In my traps $C_T \leq 0.1$ pF. I used C = 820 pF and R = 1 k Ω . A low impedance path between control electrodes and trap ground at the trap RF frequency $\Omega_{\rm RF}$ is desired.

• octagon: The RC filters lie outside the vacuum system. The lead length from control electrode to RF shorting capacitor is 7-10 cm. Along this length there are many metal-metal connections. Specifically, from control electrode to RC

filter: 1 wire bond, 1 BeCu chip carrier spring connector, 2 crimps, 1 UHV D-Sub feedthrough, 1 socket connection and several solder joints (on the RC filter PCB).

The impedance of this lead at $\Omega_{\rm RF}/2\pi=100$ MHz can be significant. A lumped circuit model (vs transmission line model) is reasonable since $\lambda_{RF}>>10$ cm. A crude estimate of the lead's inductance may be calculated assuming it is a length (l=10 cm) of thin (a=0.5 mm) wire, near (d=1 cm) a conducting plane [Terman 55].

$$L = \mu_0 l(\ln(2d/a) + 1/4) = 495$$
 nH
 $Z_L = i~2\pi~\Omega_{\rm RF} L$
 $= i~2\pi~100$ MHz × 495nH
 $= i~311~\Omega$

In some traps there is a relatively large capacitance to ground C' at each control electrode. This capacitance coupled to L can be problematic. For example, if L=100 nH and $C'=30 \mathrm{pF}$ the resonant frequency of the resulting LC oscillator is

$$f_{\rm LC'} = \omega_{\rm LC'}/2\pi = (2\pi\sqrt{\rm LC'})^{-1} = 92~MHz$$

This frequency may lie near the trap drive frequency Ω_{RF} . If this is the case resonant effects can suppress the shunting effect of the RC filters if the resonant Q is high. The result is a larger RF potential on the control electrodes. This potential may moreover acquire a phase shift (due to the LC's reactance) with respect to the RF on the RF electrodes, a situation which can cause intrinsic micromotion [Berkeland 98].

λ/4: So far, only simple traps have been used in λ/4 systems and the RC filters
 were located < 1 cm from the trap chip inside the vacuum system.

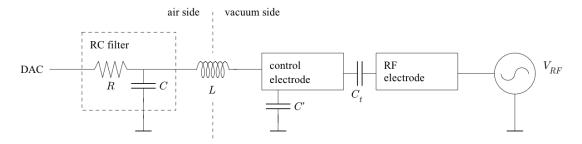


Figure 3.34: Schematic illustrating why it is desirable to put RC filters near the ion trap (see text).

3.6.9 Conclusion

The basic features of ion loading and transport between zones worked. And, predicted secular frequencies were verified by experiment. A heating comparison between gold and bared doped silicon surfaces was inconclusive because ion heating from externally injected noise could not be completely ruled out.

It may be that the difficulty I had nulling micromotion in this trap is due to a phase difference between the RF electrodes (see Section 8.2 on page 169). Possible causes were discussed in the context of trap dv16k in Section 3.5.2 on page 64.

The SOI wafer used in this experiment was obtained from a distributer that resells surplus wafers. SOI with higher conductivity is available by special order. See Section 8.7.5.4 on page 226.

Chapter 4

Microtrap Testing Apparatus

The chapter provides an introduction to the apparatus used to house and test surface electrode ion traps. Throughout this section dv16m, dv16k and dv10 refer to specific ion trap geometries discussed in Chapter 3 on page 35.

4.1 Vacuum apparatus

An ultra high vacuum (UHV) environment ($\sim 1 \times 10^{-11}$ Torr) is required for QIP with ion traps. At higher pressures background collisions can cause ion heating and qubit decoherence. Additionally, during some collisions there may be a chemical reaction with the trapped ion, creating a different and undesired ion species. This is especially problematic for ${}^9Be^+$ where ion lifetime is fundamentally limited by collisions with H_2 [Mølhave 00, Wineland 98]. I did not observe such problematic chemistry with ${}^{24}\text{Mg}^+$. However, the importance of good vacuum can't be underestimated since ${}^9\text{Be}^+$ is emerging as a good candidate for QIP [Ozeri 07].

Obtaining UHV quality vacuum requires careful choice of trap materials, meticulous cleaning and a long bake at high temperature. An excellent guide to UHV processing is the 27 page appendix to Birnbaum's doctoral thesis in the Kimble group at Caltech [Birnbaum 05].

This section details distinguishing features of the two vacuum systems I used in my experiments.

4.1.1 Quarter-wave style vacuum system

The ion trap vacuum system design used in all the QIP experiments at NIST to date is identifiable by the integration of a prominent $\lambda/4$ coaxial RF resonator (see [Jefferts 95] for details). Such a system was used for testing of early boron doped silicon ion traps (see trap "dv10" in Section 3.2 on page 40 and trap "dv14" in Section 3.3 on page 48). It consists of a $\lambda/4$ copper coaxial RF resonator surrounded by a quartz vacuum envelope with optical quality quartz windows for laser beams and imaging. The boundary conditions for the RF cavity produce a voltage maximum at the tip of the resonator. The trap RF electrodes are attached to this tip. The trap control electrodes are referenced to the RF ground at the resonator sheath. See Figure 4.1 on page 104 for a labeled photograph.

Many of the $\lambda/4$ vacuum system components were available off the shelf from the following manufacturers. The stainless steel conflat flange components were purchased from (Kurt J. Lesker, Inc.) and (MDC Inc.). The two vacuum pumps visible in the photo were used to maintain vacuum following the bake. They are a Varian, Inc. titanium sublimation pump (TSP, p/n 916-0061) and 20 L/s StarCell VacIon Plus ion pump (p/n 9191144) purchased from Kurt J. Lesker, Inc. The pumps were controlled by a Varian MiniVac controller (p/n 9290191) and a Varian TSP controller (p/n 9290022). The ion gauge is a Granville-Phillips, Inc. nude ion gauge (p/n 274022) and is controlled by a SRS, Inc. IGC100. A turbo pump backed by a diaphragm pump, a large ion pump and a SRS RGA100 residual gas analyzer were used during the bake. The multi-pin connector is made by Insulator Seal, Inc.. The remaining components were custom made.

Two-thirds of the $\lambda/4$ coaxial microwave resonator resides in vacuum (shown in Figure 4.1 on page 104), while the remainder is in air (removed in the photo in the Figure, represented by dashed lines). It is surrounded by a quartz envelope made by

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Allen Scientific Glass, Inc. The optical quality quartz windows (CVI Laser Optics,

Inc.) and quartz to metal seal (Larson Electronic Glass, Inc.) were attached to the

envelope. The UHV microwave feedthrough is designed with a small capacitance to

ground and to minimize the impedance mismatch between the vacuum-side and air-side

of the $\lambda/4$ resonator. It was manufactured to my specifications by Ceramaseal a division

of CeramTec, Inc. Omley Industries, Inc. was unsuccessful at building the feedthrough.

The vacuum-side copper resonator and air side aluminum resonator (not shown) were

made by the University of Colorado CIRES Integrated Instrument Development Facility.

The copper is OFHC grade (oxygen free).

The trap chips were mounted on a ceramic filter board. Traces were RC Filters

put on the filter board by silk screening with gold paste (see Section 8.7.7 on page 232).

Trap RF may be capacitively coupled to the control electrodes and must be shunted

to ground. This was done using an RC filter for each control electrode mounted in the

vacuum system on the filter board. The capacitors and resistors were surface mount

devices (820 pF, 1000 Ω) with a high breakdown voltage (> 100 V). It is crucial to use

devices without any solder tinning which can spoil the UHV vacuum.

The 830 pF capacitors were made by Novacap, Inc. with the following character-

istics.

• size: 1.27 mm x 1.02 mm x 1.12 mm

• precision: +/-5%

• maximum voltage: 300 V

• termination: palladium silver

• part number: 0504B821J301P

The 1 $k\Omega$ resistors were made by Amitron (formerly of North Andover, MA). Amitron

was purchased by Anaren, Inc.

• size: 1.52 mm x 0.76 mm

• style: top contact

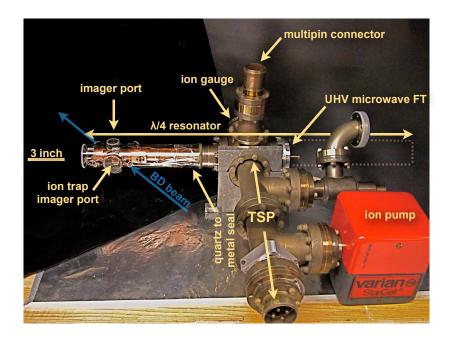


Figure 4.1: $\lambda/4$ style vacuum system.

• base material: 0.010 inch alumina

• tolerance: $\pm 5\%$

• termination: gold

• part number: R1A1508-100J5A0

4.1.2 Octagon vacuum system

The vacuum system design used for recent NIST surface electrode (SE) ion trap experiments has a prominent stainless steel conflat flange (CF) enclosure with eight 3.75 inch CF ports. See Figure 4.2 on page 106. It is an extension of the technology used in the $\lambda/4$ style system (see Section 4.1.1), designed especially for many electrode SE ion traps. Its octagonal vacuum system was favored for SE traps because it can be made of commercially available components (see below) while meeting many SE trap needs. My SOI SET was tested in this vacuum system (see trap "dv16m" in Section 3.6

on page 70).

- 5 optical ports accommodate cooling and photoionization beams that pass above the trap electrode surface.
- Large top and bottom ports support F1 light collection optics and accommodate high density UHV multi-pin electrical feedthroughs.
- An open geometry and plug-and-play chip carrier make systematic testing of multiple traps faster and less error prone (see 4.1.3).
- Since it is modular, electrical interconnect and vacuum processing for a new ion trap chip can be completed in one week, at least a factor of four improvement over the λ/4 system.

I used this system because one of the surface electrode (SE) traps I tested had 43 control electrodes each with an independent control potential. This necessitated an equal number of feedthroughs, a difficult proposition with the $\lambda/4$ style vacuum system due to geometric and wiring constraints. Routing of 43 (or more) wires to the trap electrodes inside the vacuum system and outside to the DACs was a significant engineering challenge. NIST collaborated with the University of Michigan to develop a UHV compatible 100-pin socket for a chip carrier like those used in the microelectronics industry [Stick 07]. A similar vacuum system was use to test traps produced by the Lucent Inc. and Sandia National Labs ion trap foundries. See Figure 4.2 on the next page for a labeled photograph.

Many of the octagon vacuum system components are available off the shelf from the same manufactures as the $\lambda/4$ style trap (see Section 4.1.1). The RF feedthrough is a standard Insulator Seal, Inc. part. The five quartz laser beam access windows are mounted on 2.75 inch CF. They were made by MPF Products, Inc. (p/n A0651-A-CF). The stainless parts were baked at 400° c in air overnight to outgas adsorbed hydrogen [Bernardini 98]. The remaining components were custom made.

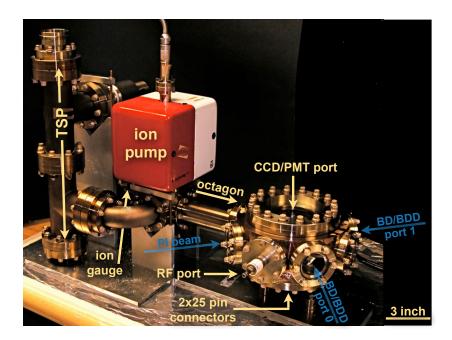


Figure 4.2: Octagon style vacuum system.

The RF resonator was of a helical variety and lies completely outside the vacuum system [Cohen 65]. Two 25-pin connectors (not visible in the photo in Figure 4.2) were made by Insulator Seal, Inc. and were welded to a CF by Accu-Glass Products, Inc. The CCD/PMT port is a large quartz window attached to a a CF by a quartz to metal seal made by Larson Electronic Glass, Inc. It uses a solder which melts at 300° c; we follow Larson's advice to bake at temperatures no higher than 200° c.

RC Filters As in the $\lambda/4$ system RC filters were used for each control electrode (see Section 4.1.1). Due to the large number of control electrodes it was convenient to put the RC filters outside the vacuum system. However, it is better to put them as close as possible to the trap chip (inside the vacuum system). This avoids the inductive impedance of the connecting wires and doesn't rely on the control electrode UHV feedthroughs to be low impedance at RF. Possible ramifications of putting the RC filters outside the vacuum system are discussed in Section 3.6.8.

4.1.3 Chip carrier and socket

NIST collaborated with Dan Stick at the University of Michigan to develop a UHV compatible-100 pin socket for a chip carrier like those used in the microelectronics industry. The chip carrier is a two-layer design made of Vespel and machined with a grid of holes to house 50 gold-plated spring-loaded sockets which interface with pins on a chip carrier. Each socket was connected by a Kapton wrapped wire to a pin on one of the 25-pin UHV vacuum feedthroughs. Both ends of the wire were crimped with a special crimp tool.

Kapton is a DuPont, Inc. UHV compatible polyamide film. Vespel is a DuPont, Inc. UHV compatible plastic that is easily machinable. The Kapton wrapped wire is 22 AWG silver plated copper made by Accu-Glass Products, Inc. (p/n 100680). See Stick's thesis for details including other part numbers [Stick 07].

The chip carrier was a UHV compatible 100-pin low-temperature co-fired ceramic (LTCC) pin grid array (CPGA) package make by Kyocera, Inc.. It can be purchased from Global chip Materials, Inc. (p/n PGA10047002). Extraction of the chip carrier from the socket required care to avoid bent pins. I used a chip extractor made by Emulation Technologies, Inc. (p/n TW2063, S-PGA-13-101-A). It is helpful to conduct electrical tests on traps mounted on chip carriers outside of the vacuum system. A breakout printed circuit board (PCB) was built for this purpose with a 169-pin zero insertion force (ZIF) PGA socket (Digi-Key, Inc. p/n 169-PRS13001-12). See Figure 4.4 on the following page for the electrode numbering scheme I used.

A ceramic paste was used to attach silicon trap chips to the cPGA chip carriers. It is made by Aremco, Inc. with part number Ceramabond 569. The bulk of the paste is alumina. It is a very poor adhesive in layers thicker than 3 mil. It was cured overnight at 200° c. Be cautious to avoid application to surfaces near the wafer front surface as it was once observed to shed small alumina flakes. Before installing the trap chip a hole

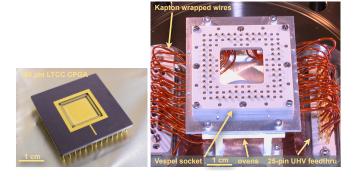


Figure 4.3: Photographs of 100pin chip carrier and Vespel chip carrier socket.

was machined in the back of the chip carrier to permit back side loading.

Wire bonding with 0.001 inch diameter gold was used to interconnect the ion trap chip to the chip carrier. See Section 8.7.7 on page 232. Before wire bonding the chip was attached with the ceramic paste.

4.1.4 Prebake checklist

Here's a list of some things to check when installing an ion trap in a vacuum system prior to the bake.

• Don't let the imager have a direct line of sight to the electron filament because it will be blinded (and possible damaged) during loading.

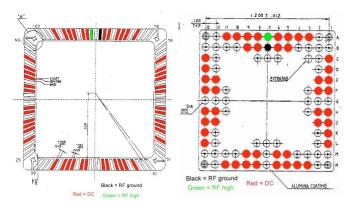


Figure 4.4: 100 pin cPGA pin numbering.

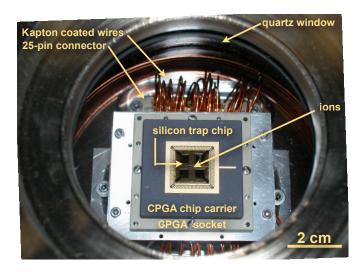


Figure 4.5: Trap chip in octagon vacuum system.

- Have a direct view of ovens from outside vacuum system so you can look for it's glow. This is helpful to approximate their temperature.
- Have baffles for the ovens which can be viewed from outside the vacuum system.
 It's helpful to have an indicator of oven plating. Plating is difficult to observe with a flashlight; turn on the room lights.
- Don't operate Mg ovens in advance of bake. Magnesium oxide is helpful in that it will help the oven withstand higher temperature bakes.
- Check that the oven openings do not have a view of their own wiring, that of their neighbors, any trap traces, the imager window or the laser beam ports.
 Shorts or inconvenient obscuration may result.
- Make sure there is a direct line of sight from the electron filaments and ovens to the trap center.
- Test electron filaments prior to bake at low pressure ($< 1 \times 10^{-6}$ Torr). Ramp up the current slowly. As the filaments are baked their emission current steadily improves. Don't walk away!
- Check for the presence of the RC filter for each electrode. Do this by looking on a scope for the filter response to a current limited square wave.
- Look for finite resistance paths (< 1 $M\Omega$) between adjacent control electrodes

(and to ground).

- Look for finite resistance paths (< 1 $M\Omega$) between each control electrode and the RF electrodes.
- Laser beams should not clip any wires or trap features inside the vacuum system.

 check for clearance before and after bake.
- During the first half of the bake, run all the TSP filaments at 30 A for 2-3 hours each. These filaments outgas a great deal and it is better if contaminants are pumped away and not deposited on the vacuum system walls. Note that the usual TSP operation cycle is 3 min at 47 A once per week (or as needed).
- Confirm that the RC filter ground is tied to the trap RF ground inside the vacuum system. It should be a good RF quality ground.

4.1.5 Bake procedure

The vacuum systems were baked at 200° C for about 5 days. The bake was ended when at constant temperature the observed pressure plateaued around 1×10^{-7} Torr. For advice on UHV baking see [Birnbaum 05].

4.1.6 Post bake checklist

Here's a list of tests to do (and not do) to an ion trap after it's been baked but before you try to load it.

- Do not use HCl to clean the copper oxide off tarnished RF feedthroughs. HCl attacks the braze joints. Use a Scotch-Brite pad instead.
- Check for the presence of the RC filter for each electrode. Do this by looking on a scope for the filter response to a current limited square wave.
- Look for finite resistance paths (< 1 $M\Omega$) between adjacent control electrodes (and to ground).
- Look for finite resistance paths (< 1 $M\Omega$) between each control electrode and

the RF electrodes.

- Apply a little power to the RF resonator and tweak the coupling to > 90 %. Slowly ramp up the power over several hours. Breakdown may happen if there are field emitters present. In some cases they can be burned off. Do this by applying > $\Gamma_{RF}/2$ frequency modulation to the RF source while ramping up the power. Γ_{RF} is the RF resonator linewidth, $\Gamma_{RF} = \Omega_{RF}/Q$. If breakdown is observed (as a sharp discontinuity in reflected power) wait until it goes away before applying more power. The trap temperature may change due to dissipation of RF in the trap structure. In this case the RF capacitance of the trap to ground may change causing a shift RF cavity resonant frequency and coupling.
- Check for continuity between each trap electrode and external wiring. It's possible that a wire has broken between the RC filter and the trap electrode. There are several tricks of decreasing specificity.
 - (1) Shine a UV laser beam on a trap electrode and look for the resulting photocurrent. One observation in a functional trap with gold coated boron doped silicon electrodes: $\sim 500~\mu\mathrm{W}$, 280 nm, grazing incidence on a control electrode produced $\times 10^{-9}$ A to 0.1×10^{-9} A induced current.
 - (2) Turn on an electron filament with an emission current of 100 μA and a bias of minus 50 100 V. There should be several μA collected on each of the trap electrodes that have a line of sight of the filament (and perhaps some others if the trap RF is turned on). One observation in a functioning trap: filament 1.2V 830 mA, 100 μA emission, -80 V bias; 1 5 mV on a Fluke 79III multimeter (10 MΩ input impedance, 100 500 nA); trap RF off.
 - (3) Turn on the trap RF. Look for RF on the control electrodes (from capacitive pickup). Note that it may be difficult to determine the RF coupling path.
- Install a copper pinch-off on the vacuum system valve cF after the bake is complete. This is a stopgap in the event of a valve failure. A Varian, Inc. adapter

is needed to connect the turbo pump to the pinch-off tube (p/n FCP03750275).

• Prior to loading with an electron gun, permit it to outgas for several hours with an emission current of $\sim 100~\mu\text{A}$, 50-100~V bias. The RGA indicates that tungsten filaments are a source of hydrogen.

4.1.7 Mg ovens

A vapor of Mg is produced by a metal sample in a miniature oven with an aperture directed toward the trap center. The tubes were heated by running current thru their bulk. The current was supplied by thin wires with low thermal conductivity.

The ovens were thin walled stainless steel tubes packed with Mg fragments and sealed at the ends by crimping. A small hole along the length of the tube permitted Mg vapor to escape in a beam pointed at the trap. The tubes were 5-8 mm long by 1 mm diameter with a wall thickness of 100 μ m. They were made of 304 stainless steel. The stainless was baked at 400° c in air overnight to outgas adsorbed hydrogen [Bernardini 98]. The hole was made at the middle of the tube by nicking it's circumference with a 150 μ m wide saw blade. Mg fragments were inserted in the tub and the ends crimped with pliers. Electrical connection to each end of the stainless oven was made by gap welding a pair of thin (75 μ m diameter) tantalum wires. The tantalum was in turn gap welded to thick stainless wires using Advance metal (see Section 8.7.7 on page 232). The resistive losses in the stainless dominated so most of the power was dissipated in the oven, not the leads, care must be taken to prevent the metal vapor from contacting functional surfaces in the vacuum system including electrical traces on the trap wafers and laser/imaging ports. In the octagon trap this is accomplished with a glass tube surrounding the ovens which abutted the back side of the ceramic chip carrier.

The natural abundance of Mg is 79% for 24 Mg, 10% for 25 Mg and 11% for 26 Mg [Lide 08]. The isotopically enriched 24 Mg used in my experiments was obtained from Oak Ridge National Lab (ORNL 54 - 0134).

As the current to the Mg oven is increased its temperature rises. An indication of the presence of a Mg vapor is metallization (plating) of exposed trap surfaces. However, the onset of metallization is extremely nonlinear in current. It is believed this is due to the natural oxide (MgO) on the surface of Mg which forms in air. MgO has a substantially higher vaporization temperature (2830° C) than Mg (650° C) (www.webelements.com). It is observed that there is little vapor released by the oven until the oxide layer is broken, then there is a lot of vapor. The abrupt increase in deposition was accompanied by an sharp increase in vacuum system pressure (e.g. from 1×10^{-10} Torr to $> 1 \times 10^{-9}$ Torr). It is advised to watch for this pressure burst and quickly reduce the oven current by 50% to prevent exhaustion of the oven Mg supply. Then, slowly ramp back up the oven current.

In one of my ovens I observed the onset of plating at 380 mW (0.76 A, 0.50 V). At this point the oven glow was barely visible on an IR viewer with the lab lights off and the ion gage filament off. In another similar oven, plating was observed at 633 mW (1.02 A, 0.65 V). Subsequent loading occurred at lower oven current. Note that some ion trappers at NIST have consistently loaded Mg ions with oven currents low enough that a pressure burst was not observed.

Note that the leads to the trap ovens are current loops which may couple external electric fields into the vacuum system (and cause ion heating). This can be minimized by sinking oven current to the vacuum housing and using a stiff low pass filter on the oven current supply.

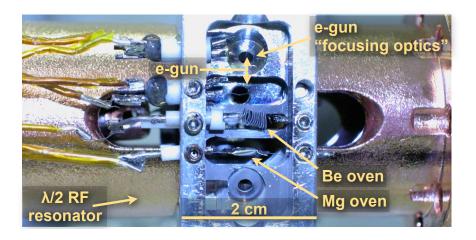


Figure 4.6: Photograph of electron filaments and a Mg oven attached to a $\lambda/4$ resonator. They are mounted on an aluminum jig which orients the electron/neutral flux toward the ion trap center. The jig is attached to a quarter wave microwave resonator used to generate the trap RF potential. The ion trap is located at the center of the resonator. It is not visible since it lies behind the ovens in this picture. A Be oven is visible in this photograph but was not used in my experiments.

4.2 Ionization techniques

4.2.1 Electron impact ionization

Electron impact ionization is a standard technique for generating single and multiple ionization states of atoms. It is used at NIST for a variety of atomic species (Mg,

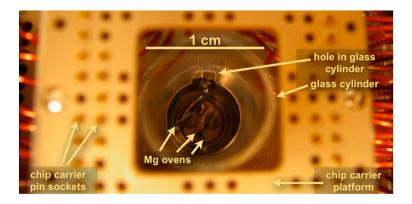


Figure 4.7: Photograph of three Mg ovens (for redundancy) installed in the octagon vacuum system. The Mg vapor flux is upward, out of the page. The ion trap chip is plugged into the pin sockets mounted in an array on the chip carrier platform. There is a slit in the trap wafer permitting Mg vapor to reach the trapping region (on the front side of the wafer). Surrounding the ovens is a glass cylinder which prevents deposition of Mg on the back side of the chip carrier platform and on the laser beam ports. A hole in the glass provides conductance of the cylinder to the ion pump (not visible).

Be, Hg, Al). In 2005 a laser photoionization system was built for Mg (see Section 4.2.2 on the next page). This section discusses electron impact ionization as used in my early ion trap work.

Electrons were produced by thermionic emission from a hot ($\sim 1200^{\circ}$ C) 75 μ m diameter tungsten filament. They were directed to the trap center by crude electron optics biased to about -100 V with respect to the trap RF. The electron energy is sufficient to overcome the 7.65 eV ionization threshold in Mg. Multiple ionization states of Mg may have formed but were not trapped ([Jha 02]).

Tungsten filaments work fine but are unpleasant in that they must be very hot (causing pollution of the vacuum system), they burn out immediately if exposed to air and become extremely fragile (brittle) after first use. After my first trap I switched to 1% thoriated tungsten which operates at lower temperatures and is less fragile after first use. Yb-oxide and Th-oxide are also options. For a thoriated filament, a -80 V bias and a filament current of 830 mA, a 1.2 V drop across the ~ 5 mm long filament and $100~\mu A$ emission was observed.

Note that the (thermionic) work function for tungsten is 4.54 eV while for thoriated tungsten it can be as low as 2.96 eV [Mason 90].

While a stalwart in ion trapping, electron impact ionization is problematic for microtraps. The electron beam is poorly directed and is further deflected by the high RF potentials on the trap electrodes (~100 V, ~100 MHz). A low electron density at the trap center and charging of dielectric surfaces may have contributed to early unsuccessful attempts at loading my first surface electrode trap in summer 2005 (see Section 3.3 on page 48). Loading of this trap was ultimately successful in 3/2006 using photoionization. The Seidelin trap was initially loaded several times using electron impact ionization, but the loading efficiency was low and ion lifetime extremely short due presumably to surface charging [Seidelin 06]. To my knowledge no surface electrode microtrap has been routinely loaded by electron impact.

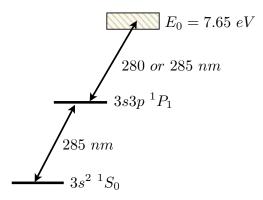


Figure 4.8: Two photon photoionization of 24 Mg. Two-photon ionization takes place thru the $3s^2\,^1S_0 \rightarrow 3s3p\,^1P_1$ transition. The first photon is resonant with the strong transition to the lowest lying P state. A second photon of the same frequency goes to the continuum. The second photon can also be a 280 nm photon.

4.2.2 ²⁴Mg photoionization

Neutral Mg can be photoionized (PI) with 1-10 mW CW 285 nm laser light (focused to a 40 μ m waist). Photoionization of Mg was first demonstrated experimentally by Madsen, Drewsen, *et al.* in 2000 [Madsen 00].¹

There are several advantages of PI over electron impact ionization. With the PI laser there is no need for a hot electron filament and loading is possible with lower Mg oven currents. The result is less contamination of the vacuum system during loading. The 285 nm laser beam's power is focused on the trap center on a trajectory which avoids the trap electrodes. As as result there is less charging of trap dielectrics near the ion.

The 285 nm system is shown in Figure 4.9 on the next page. The pump is a Spectra Physics, Inc. Ar^+ laser lasing multimode with 5 W output power. This light pumps a Coherent, Inc. 699 ring dye laser stabilized with a Hansch-Couillaud lock to a reference cavity [Hansch 80]. The dye is Exciton, Inc. Rhodamine 560 in ethylene glycol (1.6 g per 400 mL). The green light pumps a Wavetrain resonant doubling cavity made by Laser Analytical Systems, GmbH. (Berlin). Second harmonic generation occurs in an angle phase matched BBO crystal. The cavity is stabilized by the Pound-Drever-

¹ Our labs also photoionize 9 Be using a frequency quadrupled pulsed Ti: Sa [Deslauriers 06a].

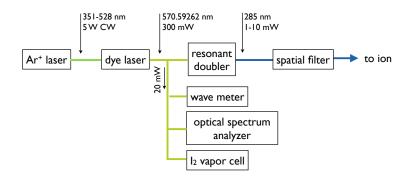


Figure 4.9: Schematic of laser setup for the 285 nm cW laser light used to photoionize ²⁴Mg.

Hall method [Drever 83]. The UV light beam had numerous lobes perpendicular to the cavity plane.² The center lobe was highly astigmatic and required correction by a pair of cylindrical lenses. A spatial filter was used to select the highest power mode and produce a clean beam.

For 24 Mg photoionization the dye laser was tuned near the $3s^2\,^1S_0 \rightarrow 3s3p\,^1P_1$ transition at 285.59262 nm using a traveling cart wave meter [Hall 76, Fox 99]. A Doppler broadened transition in an I_2 vapor cell was used as a crude absolute frequency reference at 570.6 nm. I tuned approximately 300 MHz to the red side of the 1.2 GHz Doppler broadened (at 300 K) feature set at 17,525.632 cm^{-1} (scan number 1749006 in Volume 3 of the JSPS iodine atlas [Katô 00]. Note that 1 cm^{-1} is approximately 30 GHz. There were no AOM's used in this setup. The laser stability and Doppler broadening of the hot ($\sim 400^{\circ}$ C) 24 Mg vapor permitted efficient photoionization with the laser system running open loop for hours at a time. Single mode operation was confirmed with a Tropel L240 optical spectrum analyzer with a 1.5 GHz free spectral range in the visible (3.0 GHz in the UV).

² These lobes lie along the matching axis of the BBO and are due to beam walk off. They are an intrinsic feature of angle phase matched doublers.

4.3 $^{24}Mg^+$ laser cooling

The electronic structure of ²⁴Mg⁺ is simple. Like an alkali neutral atoms it has only a single valence electron. And, since its nuclear spin is zero it has no hyperfine structure. Laser cooling is possible on the D1 and D2 transitions at 280 nm. Laser cooling of ²⁴Mg⁺was first demonstrated by Wineland, *et al.* in a Penning trap [Wineland 78].

Ordinarily, laser cooling of many atomic ion species requires wavelengths that can only be produced by dye lasers and frequency doubling. Recently, however, commercial solid state fiber lasers have become available at 1120 nm, the fourth subharmonic of 280 nm [Friedenauer 06]. I used a Koheras, Inc. CW Boostik Y10 fiber laser system is available in the range 1030 - 1121 nm with 0.5 nm tuning, a 70 kHz line width and 1-2 W coherent emission (\sim 1 W amplified spontaneous emission).

The choice of ²⁴Mg⁺ for ion trap testing has several motives. Beyond successful trapping, a critical measure of a trap's promise for ion QIP is its electric field noise which can heat the ions. Historically, this has been measured in ions with hyperfine structure cooled to the motional ground state, an expensive and technically challenging undertaking [Wineland 98, Monroe 95]. In 2007 a measurement technique relying on only a single Doppler cooling was demonstrated for ²⁴Mg⁺ (see Section 4.7 on page 141 and [Wesenberg 07, Epstein 07]). The absence of hyperfine structure also obviates the need for a quantizing magnetic field, a repump laser and careful laser beam polarization control. Also, Mg thermal ovens are straightforward to build and operate (see Section 4.1.7 on page 112) and Mg can be photoionized (see Section 4.2.2 on page 116).

To be conservative, the blue most $3s^2 \, ^2S_{1/2} \to 3p \, ^2P_{3/2}$ transition in $^{24}{\rm Mg}^+{\rm at}$ $\lambda_0=279.636$ nm was selected for laser cooling [Drullinger 80]. This transition has a linewidth of $\Gamma_0\simeq 40{\rm MHz}$. Note that the fine-structure splitting between the $P_{1/2}$ and $P_{3/2}$ states is about 0.7 nm (2.75 THz) [Ozeri 07]. See also the NIST atomic spectra

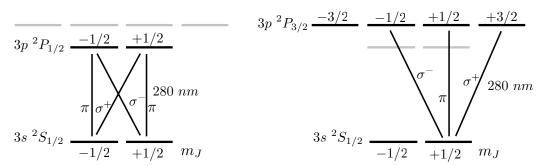


Figure 4.10: Atomic level diagram for $^{24}\text{Mg}^+$ showing the low lying P states and two cooling transitions: (left) D1 $3s^2\,^2S_{1/2} \to 3p\,^2P_{1/2}$ and (right) D2 $3s^2\,^2S_{1/2} \to 3p\,^2P_{3/2}$. In my experiments I used circularly polarized light (σ^+ or σ^-) on the D2 transition for laser cooling. In the ~ 10 Gauss ambient magnetic field the m_J levels were degenerate at the sensitivity of my experiments.

database.

The Boostik Y10 fiber laser I used had a factory set center frequency of 1118.54 nm. It did not meet many of the factory specifications but worked well enough for my purposes. It could be slowly temperature tuned over a 0.5 nm range centered at about 41.7° c in several minutes. Tuning is also possible with a piezoelectric element over a bandwidth of several GHz at a rate of < 1 kHz, considerably less than the 0.4 nm and 100 kHz, respectively, specified by Koheras. The laser's output polarization was often stable, but some days drifted at up to 1/2 radian per hour. Over the course of a typical day its frequency drifted by < 1 GHz. Between power cycles the frequency varied by < 10 GHz. The fiber laser is frequency stabilized by locking it's frequency with a piezo tuning element to a saturated absorption hyperfine feature in an I_2 vapor cell whose frequency is nearly twice that of the cooling transition [Wieman 76, Preston 96]. Piezo tuning has considerable hysteresis but not enough to prevent locking. The laser reliably produced 1.8 W of coherent laser light since 2006.

The fiber laser light is doubled four-fold to 280 nm by a pair of resonant doubling cavities, crudely approximating the setup of the Schätz group [Friedenauer 06].

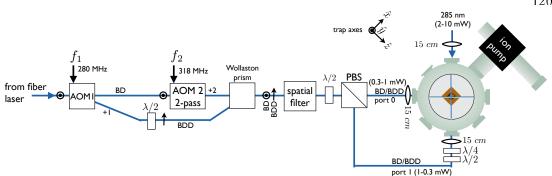


Figure 4.11: Schematic of ²⁴Mg⁺ Doppler cooling laser.

In the first cavity, visible light at 560 nm is generated by second harmonic generation in a noncritical phase matched LBO crystal at 95.0° C [D 68]. The cavity is a folded ring cavity and is stabilized by the Hansch-Couillard method [Hansch 80]. Its output is largely TEM₀₀mode. In the second cavity, UV light is produced by a Wavetrain resonant doubling cavity made by Laser Analytical Systems, GmbH. Second harmonic generation occurs in a two-mirror Delta cavity with a a critically phase matched BBO crystal (see LAS website for details). The cavity is stabilized by the Pound-Drever method [Drever 83]. The UV light beam was highly astigmatic and had numerous lobes perpendicular to the cavity plane.³ A spatial filter was used to select the middle most mode and produce a clean beam. This light was then sent to a pair of acoustooptic modulators (AOMs) before being directed to the ion trap.

A pair of acoustooptic modulators provides frequency shifts to the Doppler laser setup which assist with cooling, micromotion compensation and heating measurements. The first, AOM 1 in Figure 4.12 on page 123, splits the incoming light into two beams: a Doppler cooling laser (BD) and a detuned Doppler cooling laser (BDD). AOM 2 varies the BD detuning $\Delta_{\rm BD}$ with respect to resonance at f_0 , $\Delta_{\rm BD} = f_{\rm BD} - f_0$. It is

³ These lobes lie along the matching axis of the BBO and are due to beam walk off. They are an intrinsic feature of angle phase matched doublers.

setup in a double pass configuration making its deflection angle first order insensitive to the RF drive frequency f_2 . This AOM is used to measure the atomic transition line shape and determine the transition's frequency ω_0 and linewidth Γ_0 . These numbers are needed because Doppler cooling efficiency varies with detuning $\Delta_{\rm BD}$ and is an important parameter for estimating ion heating (see Section 4.7 on page 141).

Ion fluorescence is sensitive to micromotion along the laser beam direction at $\Delta = \omega_0 - n \Omega_T$, where $n \in \{1, 2, ...\}$ and Ω_T is the trap RF drive frequency (see Section 8.2.1 on page 171). When $f_2 = 318$ MHz, BD is on resonance $\Delta_{\rm BD} = 0$. Typically, $f_2 = 313$ MHz giving $\Delta_{\rm BD} = -\Gamma/4 = -10$ MHz.

Frequency f_1 is applied to AOM 1 which puts power into a secondary, detuned Doppler laser beam, BDD. When an ion's temperature is well above the Doppler cooling limit, the near resonant BD beam has little cooling power due to the Doppler broadening of hot ions. Additional cooling from BDD also prevents ion loss. Typically, $f_1 = 280 \text{ MHz}$ giving $\Delta_{\text{BDD}} = -356 \text{ MHz}$.

The AOMs are IntraAction, Inc. ASD-3102LA62-1 wide band modulators with a center frequency of 310 MHz and an efficiency of > 60% over a range of 100 MHz. The frequencies f_1 and f_2 are generated by computer controlled direct digital synthesizers (DDS). The same computer collects ion fluorescence with a PMT (see Section 4.5 on page 128).

It is desired that BD and BDD recombine after the AOM's and copropagate. Combining beams on a 50/50 beam splitter is straightforward but wastes half the power in each beam. Instead, the BDD beam's polarization was rotated by 90° with a wave plate and combined with the BD beam on a Wollaston prism. While there is little power loss with this approach, the copropagating beams have orthogonal polarizations. This is exploited to permit continuous variation of the ratio of BD to BDD light incident on two ports of the vacuum system using a wave plate. Note that the UV mirrors I used attenuate horizontally polarized light more than vertically polarized light (for

propagation in the plane of the optics table). In some experiments the BDD beam was extinguished completely by switching off power to AOM 1.

The vacuum system has several quartz optical ports (see Figure 4.12 on the next page). The beam at Port 0 was directed to the trap's load zone by a 15 cm singlet lens. This beam was used principally for ion loading. The ratio of BDD to BD power was 2-4. The beam at Port 1 was used to cool ions in various experimental trap zones. Its polarization was controlled (see below) and the ratio of BD to BDD power was 2-4. A 15 cm singlet was also used for Port 1. The photoionization laser entered the vacuum system thru a port counterpropagating with respect to the the Port 1 cooling beams. It was focused to the position of the load trap by a 15 cm singlet lens. For $\lambda = 280$ nm, an initial beam diameter of w = 1mm and f = 15 cm, the beam waist at the trap is $\frac{\lambda f}{\pi w} \sim 14~\mu\text{m}$.

The polarization of the BD and BDD beams for port 1 is set by a pair of adjustable wave plates ($\lambda/2$ followed by $\lambda/4$, see Figure 4.12 on the following page). They were set to maximize ion fluorescence from the BD laser beam in Port 1. This operation compensates for birefringence in the quartz window mounted on the vacuum system. Note that this compensation may not be complete in the case of a spatial gradient to the birefringence across the laser beam due for example to mechanical stress in the window. The window is mounted on a vacuum conflat flange (CF). The range of fluorescence observed for various laser beam polarizations was at most a factor of two. Note that the ambient lab magnetic field was ~ 10 Gauss so the m_J levels were degenerate at the sensitivity of my experiments.

It is important that the Doppler cooling laser overlap ($\geq 10^{\circ}$) with all trap principle axes. Otherwise, photon recoil can cause heating. Meeting this requirement in surface electrode ion traps requires proper choice of trap electrode geometry [Chiaverini 05a].

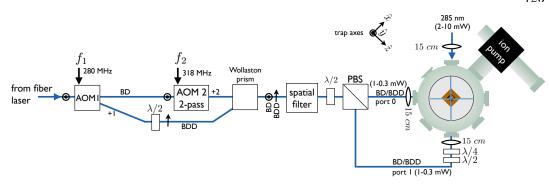


Figure 4.12: Schematic of AOMs and beam geometry.

See Section 2.3.1 on page 13.

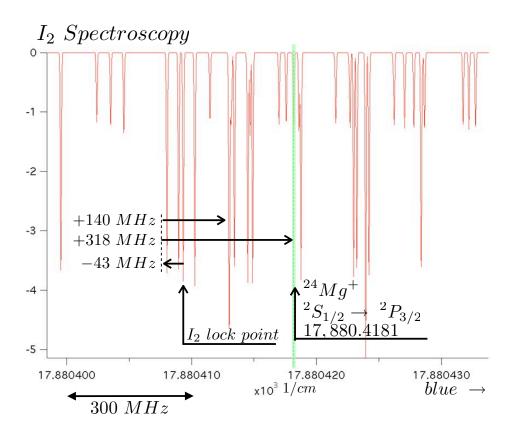


Figure 4.13: Iodine spectroscopy for the Doppler cooling transition in $^{24}\text{Mg}^+$. Absorption features in iodine span much of the visible spectrum. In the figure is an absorption spectrum corresponding to the hyperfine spectra of a certain rho-vibrational transition. The same features are visible in my Doppler free spectroscopy setup and serve as an excellent absolute frequency reference. The green line marks the location in the iodine spectrum for the $^2S_{1/2} \rightarrow ^2P_{3/2}$ transition in $^{24}\text{Mg}^+$ in the visible at 17,880.4181/cm (559.271039 nm) [Schaetz 06]. See also [Herrmann 08]. The fiber laser is locked to the marked spectral feature using Doppler free spectroscopy which adds a -43 MHz shift. Laser light resonant at the atomic transition is obtained by doubling the 599 nm light and shifting it by 2×318 MHz in the UV with a double pass AOM. Nonresonant laser light detuned from resonance by -356 MHz is obtained with a 280 MHz AOM in the UV. See Figure 4.12 on the preceding page. This I_2 spectrum was generated by the Toptica, GmbH. Iodine Spec software [Bodermann 02, Knöckel 04]. The actual signal in my setup has a dispersive line shape for easy locking (see Figure 4.14 on the next page).

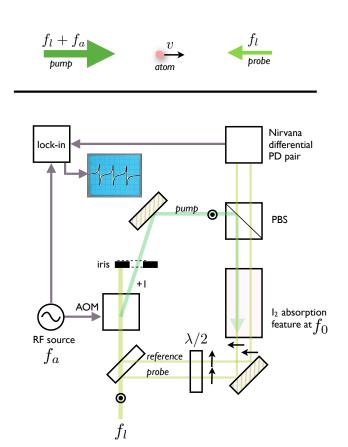


Figure 4.14: Schematic of saturated absorption spectroscopy setup for I_2 using a single AOM.

I_2 spectroscopy

At room temperature the hyperfine spectra plotted in Figure 4.13 on the preceding page are each Doppler broadened (at room temperature) to about 1 GHz. Saturated absorption spectroscopy is a technique which uses spectral hole burning to resolve these features. The components I used to do this are shown in Figure 4.14. A good pedagogical discussion is by D. Preston [Preston 96].

The 560 nm laser beam at frequency f_l has a linewidth ($\sim 70 \text{ kHz}$) that is narrow relative to the I_2 hyperfine feature spacing (several MHz). The lock signal is offset from f_l by $-f_a/2$. This can be seen as follows. Suppose we wish to resolve an I_2 HF feature

at f_0 . Let v be the velocity of atoms resonant with the pump at $f_l + f_a$,

$$f_0 = (f_l + f_a)(1 - v/c).$$

These atoms are pumped into the excited state, leaving a spectral hole. Let v' be the velocity of atoms resonant with the probe at f_l ,

$$f_0 = f_l(1 + v'/c).$$

Note that the plus sign in this expression is due to counter propagation of the pump and probe beams (as compared to the previous expression where there is a minus sign and the beams copropagate). The probe is minimally absorbed when it is resonant with the population of pumped atoms moving at velocity v. That is, when v = v'. This happens when $f_l = f_0 - f_a/2$.

A signal appropriate for the lock-in technique is generated by applying a 100 kHz dither to f_a and using a differential photodiode pair (New Focus, Inc. Nirvana Detector). The signal from of the lock-in has a dispersive line shape symmetric about zero which can be easily used in a PID servo loop. In my setup $f_a = 86.065$ MHz. The iodine cell was purchased from Triad Technology, Inc. (p/n TT-I2-100-V-P).

4.4 Ion imaging optics

The ion imaging system collects ion fluorescence and directs it to an imaging camera or a photomultiplier tube. It was designed for good collection efficiency and resolving power at both 280 nm (for Mg⁺) and 313 nm (for Be⁺). In particular it was desired that the system clearly resolve individual ions in a linear crystal. For example, 5.5 μ m is the inter-ion spacing for a ²⁴Mg⁺ three ion crystal when $\omega_z/2\pi = 1.0$ MHz. ω_z is the frequency of the lowest (COM) vibrational mode along the trap axis. The geometry is illustrated in Figure 4.15 on page 129.

The imaging system discussed below was designed for the ion trap testing setup. It resides outside the vacuum system, oriented normal to the trap surface. A full system simulation using ZEMAX was done by Pei Huang in 2006. For the geometry in Figure 4.15 on page 129 he found the resolution to be 4.5 μ m at 280 nm for rays near the optical axis and 6.5 μ m for rays at the edge of the lens.

The objective was a custom F/1.43, 4.7x, 4-element system made by Karl-Lambrecht, Inc. On the way to the detectors the ion's fluorescence passed thru a 0.25 inch (6.35 mm) thick quartz UHV window. This window caused significant spherical aberration for far off axis rays. The light then propagated in air to the objective. The objective was designed to correct spherical aberration, but for a 2 mm window not a 6.35 mm one. An additional refractive element could increase the lens's resolution (to 3.3 μ m on axis) by correcting this aberration. An adjustable iris was occasionally used to clip these rays when resolution was valued above collection efficiency. Laser beam light may be scattered into the objective from trap structures, a background that degrades signal to noise. This stray light was reduced by placing a pinhole at the primary's focus which clips rays not originating from the ion's focal depth. A commercially available F/6.7, 13x UV microscope objective imaged the pinhole and relayed light to the detectors (Newport Corporation Inc. p/n U-13X). The system's design magnification was 30x but in practice was operated at around 50x.

A flipper mirror directed the light to either a charge-coupled device (CCD) camera or a photomultiplier tube (PMT). The entire optical train from the objective to the detectors was in a light tight box (not illustrated in Figure 4.15 on page 129). Micrometers translated the objective permitting the 50 μ m field of view to be panned across the trap surface. The focus was set by a third micrometer.

The PMT was a Hamamatsu H7732P-11 designed for photon counting. The radiant sensitivity of its cathode was $R_{\lambda} = \sim 55$ mA/W at 280 nm, giving a QE of 24%. Note that 100% quantum efficiency at 280 nm is $\left(\frac{\hbar\omega}{e}\right)^{-1} = \left(\frac{hc}{\lambda e}\right)^{-1} = (4.43 \ W/A)^{-1} = 0.23 \ A/W$. It's dark count at room temperature was specified to be 80 s^{-1} . The PMT signal was processed by a discriminator and converted to TTL for recording by an FPGA

in the experiment control computer.

The camera was an Andor, Inc. iXon DV887 electron multiplying CCD (EMCCD). Its 512x512 pixel array was readout serially at 10 MHz, 26 ms/frame. In practice we used a longer integration time (300ms/frame) to improve signal to noise. The CCD pixel size was 16x16 μ m and its quantum efficiency at 280 nm was ~35%. The electron multiplication gain factor was variable: 1-1000x. The CCD saturated at 174,000 electrons/pixel/sec and could be exposed to room light. With minimum gain, the total dark count rate was about 1 kHz when the CCD was cooled (thermomelectrically) to -90° C.

The Andor replaced the imaging photon detector used in previous NIST ion trap experiments, the Photek, Inc. IPD3 multichannel plate (MCP) detector. Advantages of the EMCCD over the MCP include higher pixel count, much higher saturation level, lower cost, higher quantum efficiency at 280 nm and more fully featured software. The MCP is superior for single photon counting due to its lower dark count rate (64 Hz at 20° C) and when excellent timing resolution (20 ns) is required.

4.5 Experiment control electronics

4.5.1 Introduction

A custom software/hardware platform was developed at NIST to control the experiment apparatus used in quantum logic and trap testing experiments. It's primary functions are the following.

- define a syntax to specify controlled interactions between ions and trapping fields and modulated laser/RF source; the evolution of a particular experiment is specified in a digital control .dc file
- deterministically control experiment evolution
- measure and record ion qubit states by resonance fluorescence

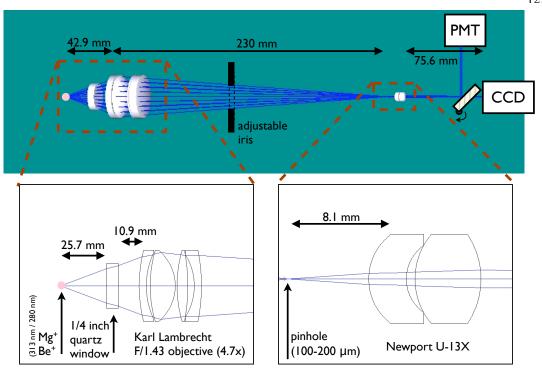


Figure 4.15: Schematic of ion imaging optics. The ray trace diagrams are due to Pei Huang.

- deterministically branch experiment evolution in minimal time based on measurement outcomes
- support calibration and diagnostic routines

The architecture for this system was designed by Chris Langer and is discussed in detail in his thesis [Langer 06]. Since 2006 the system was extended by many people at NIST. For example, the .dc file syntax was extended to control DACs and optics micropositioners. The trap testing experiment utilized a subset of these capabilities. Prior to Langer's platform, other tools were used. See for example Section 4.5.3 on page 135.

Figure 4.16 on the following page shows the experiment control apparatus used for trap testing with ²⁴Mg⁺. The sequence of operations comprising an experiment is written in a special language and stored in a .dc file. This file is interpreted by software on the PC which fills a table in a field programmable gate array (FPGA) with the

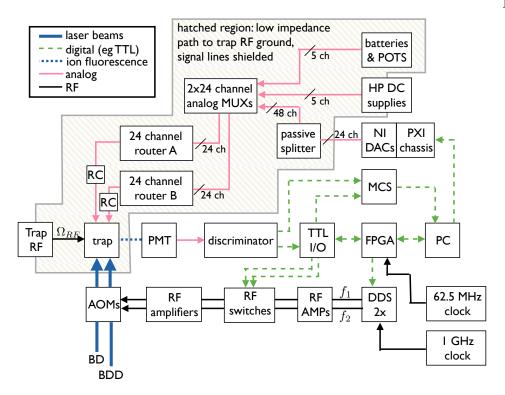


Figure 4.16: Functional schematic of the electronics controlling the trap testing experiment

experiment steps. It also prepares control electrode potential waveforms for issuance by the DACs. Our qubit evolves at a characteristic frequency ω_0 (\sim 2 GHz) and some operations (eg laser beam pulses) must be synchronous with its evolution. Such coherent operations are are completely governed by the FPGA.

The heart of the system is an FPGA. An FPGA is a microelectronics chip which implements a user defined logic. Traditionally this logic was implemented using individual logic components (chips) like AND gates, shift registers and memory interconnected on a printed circuit board. An FPGA however accomplishes the same logic using a very large (200,000) array of elementary logic elements whose interconnection is determined by a reconfigurable bank of switches. Unlike microprocessors which typically respond to external stimulus via interrupt requests (IRQs) with μ s delays, an FPGA is a state

machine and responds deterministically (with ns delay) to multiple simultaneous stimuli. The logic it performs is specified in a language called VHDL and compiled (and optionally simulated) for a specific FPGA chip. The FPGA logic for ion trapping experiments provides a structure (a table) which holds a sequence of operations (e.g. apply laser S to an ion or collect photons from PMT X) and executes appropriate steps to implement each operation in experiment hardware (e.g. turn on RF switch S or record pulses from PMT X) at the right time.

The RF driving the acoustooptic modulators (AOMs) is generated by direct digital synthesizers (DDS). Direct digital synthesis is a means of generating arbitrary frequencies from a fixed frequency reference. The RF is turned on and off by TTL controlled RF switches and amplified by RF instrumentation amplifiers. The RF electronics responsible for confining the ions is discussed in Section 4.6.1 on page 138.

4.5.2 Control systems built for this thesis work

The remainder of this section discusses my contributions to the experiment control system.

The FPGA communicates with the DDS modules and the TTL IO board over a low voltage differential signal (LVDS) bus. LVDS is a digital signaling standard for transmitting high speed data in noisy environments over cheap twisted-pair cables. Multiple devices can tap the bus along its length and all devices can transmit and receive. The ends of the bus are terminated in 110 Ω . The performance of this bus (lower bus error rate) was improved in recent years by reducing its total length and using a custom rigid backplane instead of twisted-pair cables.

Light scattered by the ion (and stray light) is detected by a photomultiplier tube (PMT) (see Section 4.4 on page 126). A discriminator rejects low amplitude PMT pulses associated with dark noise and produces TTL pulses for signals above a threshold. Two signal processing systems exist which generate histograms of observations spanning

many identical experiments. In one system, the .dc file specifies the interval during an experiment when the FPGA responds to PMT pulses. During this interval the FPGA counts the number of PMT pulses it receives and adds the count to a histogram on the FPGA (number of experiments vs. photon count). Multiple distinct detection intervals (and resulting histograms) can be defined within a single experiment. In the second system, PMT pulses are sent to a multichannel scalar (MCS). The .dc file defines a specific starting time when the MCS should begin to record PMT pulses. Then for some period the MCS is programmed to record the arrival time of each pulse it sees. These arrival times are recorded in histograms on the MCS with a fixed bin duration (number of experiments vs. photon arrival time).

control potentials Static control potentials applied to endcap electrodes provide axial (\hat{z} – direction) confinement. In ion traps with a single trapping zone these potentials are sometimes derived from voltage limited power supplies. The potentials are adjusted to null micromotion in that single zone. Multiple zone (multi-zone) traps require many more potential sources. Ion transport from zone to zone and separation of ions requires time-varying potentials. Nulling micromotion in multiple zones simultaneously requires position dependent shims to the trapping potentials. In trap tests with a single ion, potential sources can be shared by multiple electrodes in widely-separated zones of the trap. However, in real QIP experiments with multiple ions in different zones, source sharing may be less practical. This is because ions' trajectory thru the trap structure are expected to differ, hence requiring independent potentials for many of the control electrodes.

The control electrode potentials in my experiments were supplied by several sources. DC supplies ($\pm 10 \text{ V}$) were used for initial trap loading for convenience, DACs were used to test ion transport and batteries ($\pm 18 \text{ V}$) were used for ion heating measurements (owing to their low intrinsic noise). All supplies were located within 2 meters of the trap and used shielded wiring schemes to bring the potentials to the vacuum system port.

A pair of 24-channel analog multiplexers could switch between the supplies without ion loss.

The DC supplies and battery box included a shielded routing box for applying potentials to any of the 24 channels. The battery box contained voltage dividers to permit continuous manual variation of its potentials.

The DACs were 8 channel, 16 bit, 750 kHz National Instruments 6733 DACs residing in a PXI bus. DAC waveform data was held in PC memory and streamed real-time over a MXI-express bus (up to 100 MB/sec). These 24 channels were shared by up to 48 trap electrodes as determined by a pair of routing boxes (printed circuit boards with jumpers). Different routing boxes were used for different trap layouts to accommodate their specific wiring requirements. The cables were doubly shielded 24 pin D-Sub (parallel port) cables which mated to the vacuum feedthroughs.

Proper grounding and shielding of the apparatus supplying the control electrode potentials is important to suppress injected noise which can cause ion heating (see Section 2.5 on page 21). A star-grounding scheme referenced to the trap vacuum housing (continuous with the RF ground) was used to suppress ground loops and pickup. A glaring exception was the DACs. The 6733s' ground reference was hard wired by National Instruments to the PXI chassis, continuous with PC ground. That is, the DACs are single-ended and floating on the noisy PC ground, a poor design choice. Better is a double-ended configuration where each DAC output is referenced to a user supplied potential. Cost constraints and a dearth of high channel count DAC options resigned me to using this DAC product. See Figure 2.8 on page 20 for how it should be done.

Ground loops were avoided by using the trap vacuum housing as a ground reference (DC supply and battery) or by breaking the ground shield near the source (DACs). Note that the choice of breaking the DAC ground reference is not ideal as it leaves the DACs

DAC	National Instruments PCI-6733 card.
DC supply	Hewlett Packard 3620A (operated as a voltage source)
battery	alkali batteries (in shielded box with a voltage divider)

Table 4.1: Supplies used for the control electrodes.

floating on the PC ground. However, this was done because the alternative results in a very large ground loop through the ac line ground via the PC.

apparatus list Following is a list of apparatus mentioned in this section.

- **FPGA** Xilinx, Inc Xtreme DSP kit with Virtex IV FPGA and the Nallatech, Inc. FUSE library
- PCI bus interface Nallatech, Inc. BenADDA V4-XC4VSX35-FF668
- DDS Analog Devices, Inc. AD9858 PCB evaluation board with parallel interface
- LVDS Texas Instruments, Inc. SN65LVDM1676 (no termination) and SN65LVDM1677 (110 Ω termination)
- TTL driver Texas Instruments, Inc. SN64BCT25244
- DC supplies Agilent, Inc. #3610A and 3620A
- mechanical shutters Uniblitz, Inc. D122 and VCM-D1 (not shown in schematics)
- PMT discriminator PRA, Inc. 1762 (NIM module, 100 MHz)
- RF amplifiers Mini-Circuits, Inc. ZHL-1000-3W, ZHL-03-05WF, ZFL-500HLN and Motorola, Inc. CA2832C
- RF switches Mini-Circuits, Inc.
- 1 GHz clock Stanford Research Systems, Inc. CG635
- RF counter MFJ, Inc. MFJ-888 (10 Hz 3 GHz) (not shown in schematics)
- RF power meter Spectra Dynamics, Inc. RFPWR (-25 25 dBm, 1 MHz 1 GHz) (not shown in schematics)
- DACS National Instruments, Inc. PXI-6733 and PCI-6733; NI-DAQmx API
- MXI-express National Instruments, Inc. PXI-8360 and NI PCIe-8361
- PXI chassis National Instruments, Inc. PXI-1042Q
- MCS EG&G Ortec, Inc. Turbo-MCS
- 24-channel analog multiplexer parallel port 4-way switch box

4.5.3 Early experiment control

I developed part of the software and hardware platform used to control the quantum logic experiments conducted between 2002-2005. These packages addressed a practical need to automate and simplify parts of our increasingly complex experiments. From 2005 onward a superior and extensible FPGA platform developed by Chris Langer was

used. His platform largely superseded many of these packages though some were used thru 2007.

rdye.exe is an application which permits remote control of an laser servo lock over the internet. It was written in LabWindows CVI and interfaced with National Instruments, Inc. (NI) analog input/output hardware. The software included a signal processing algorithm which could identify and lock to particular absorption features in an iodine saturated absorption spectroscopy setup. rdye.exe was used in a sympathetic cooling experiment [Barrett 03].

pmtreadout.dll is a library which integrates with counter hardware to permit multiple distinct measurement periods within a single experiment, each with its own histogram. The counter hardware is a National Instruments NI-6602 and is limited to a count rate of 5 MHz. The library was written in C. The pmtreadout.dll platform was used in a number of experiments [Chiaverini 05b, Schaetz 05, Chiaverini 04, Barrett 04, Schaetz 04].

zaberc.exe is an application which integrates PMT readings with 2-axis computer control of lenses to quickly locate and maximally overlap Raman laser beams with ions. Lens motion was controlled by Zaber, Inc. linear actuators (T-LA28-S). In addition to computer controlled position scans, it is helpful to walk beams manually. However, using a computer mouse/keyboard to do this is not intuitive. Instead, a natural, haptic control system was implemented using a pair of Griffin Technology, Inc. PowerMate USB digital encoders. The software was written in NI LabWindows cVI. zaberc.exe was used in several experiments [Leibfried 05, Reichle 06, Knill 08].

6733wvf.exe is a software and hardware system for applying potentials to ion trap electrodes for ion transport, separation and logic gates. It met a variety of complex needs including waveform modification on the fly using experimental feedback (open loop), externally triggered waveform production (eg for changing trap potentials synchronized with laser pulses during phase gates) and features to diagnose ion transport

problems. The arbitrary waveform hardware was the National Instruments 6733 and it was coded in Lab Windows CVI. The system was developed over many years and was integral to several experiments [Langer 06, Reichle 06, Leibfried 05, Langer 05, Ozeri 05, Chiaverini 05b, Schaetz 05, Chiaverini 04, Barrett 04, Schaetz 04].

The source code for these applications is available on the NIST Ion Storage intranet.

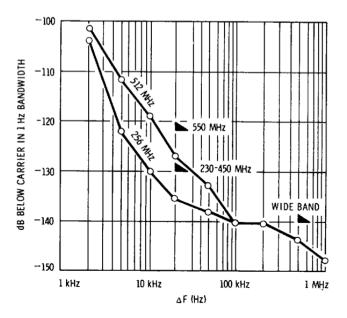


Figure 4.17: Measured single sideband noise vs offset from carrier for HP 8640B RF oscillator. The data was collected for two carrier frequencies 256 MHz and 512 MHz. The power is stated in a 1 Hz bandwidth. Figure provided by the manufacturer.

4.6 Trap RF

4.6.1 RF electronics

The trap RF is derived from a Hewlett Packard 8640B RF cavity oscillator stabilized to its internal temperature controlled crystal oscillator (drift $< 5 \times 10^{-8}$ /hr). According to the manufacturer's manual an 8640's phase noise at 1 MHz from the carrier is -147 dBc (dB below the carrier) (see Figure 4.17). Note that this specification is important as noise can cause ion heating (see Section 8.3 on page 174). The oscillator has amplitude and phase modulation inputs and can be locked to an external 5 MHz reference. This source is amplified by an Amplifier Research, Inc. 1 W AR 1W1000A amplifier. A Mini-Circuits, Inc. XFDC-20-1H directional coupler sends power reflected from the $\lambda/4$ resonator to a Agilent 8471D power detector (diode rectifier, www.agilent.com). This reflected power is used to measure coupling and loaded quality factor Q_L for the $\lambda/4$ resonator (see Section 8.5 on page 182). Typical trap RF drive frequencies for surface electrode traps are $\Omega_{\rm RF}/2\pi = 50 - 100$ MHz, coupling > 95%, $Q_L = 50 - 100$. A

Table 4.2: Attenuation of the $\lambda/4$ RF resonator for typical parameters: $Q_L=80$, $\Omega_0/2\pi=70$ MHz, $\omega_x/2\pi=10$ MHz, $\omega_z/2\pi=3$ MHz.

Minicircuits SHP-25 high pass filter attenuates RF at 10 MHz by 67 dBm (in addition to attenuation by the $\lambda/4$ resonator line shape).

A high Q RF cavity also rejects noise from the RF source. That is, its Lorentzian line shape attenuates off-resonant RF.

$$P/P_{max} \propto (V/V_{max})^2 \propto \left(1 + 4Q_L^2 \left(\frac{\Omega - \Omega_0}{\Omega_0}\right)^2\right)^{-1}$$

The power attenuation for several typical detunings is given in Table 4.2.

4.6.2 Q_L and ion trap chip losses

The loaded quality factor Q_L of the RF resonator can be a good indicator of losses at the ion trap chip. In the octagon style vacuum housing RF is brought to the chip via

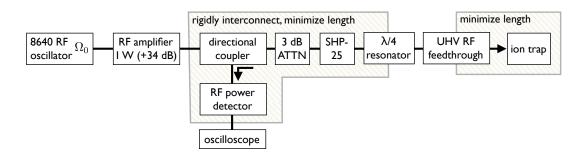


Figure 4.18: Schematic of trap RF electronics for the octagon style vacuum system. The left hatched region marks components which are rigidly interconnected with minimum length connectors. This and the 3 dB attenuator minimize RF line resonances. The right hatched region marks where the length of the RF wiring (a Kapton wrapped wire) should be a minimum to prevent radiative losses and capacitive coupling to ground and other trap features.

a RF vacuum feedthrough (RF FT) which has a large capacitance to ground, unshielded wires, a chip carrier socket and a chip carrier.

Q_L	$\Omega_{ m RF}/2\pi$	RF components
~300	156 MHz	resonator
~ 270	63 MHz	$^{\circ}$ + RF FT
\sim 290	45 MHz	$"+ { m bare\ wire} + { m chip\ carrier\ socket}$
~ 170	38 MHz	" + empty Kyocera chip carrier
~80	43 MHz	$^{\circ}$ + dv16m trap chip (see
		Sec. 3.6.5)

The lowering of the resonator frequency as RF components are added is due to their capacitance to ground. Degradation in Q_L can arise due to losses in the trap chip.

It is instructive to estimate what the losses might be in the trap chip. A resonator can be modeled as a parallel RLC where,

$$\Omega_{\rm RF}^2 = 1/(LC)$$
 and $Q_L = R/|Z_C| = RC \ \Omega_{\rm RF}.$

Note that this ignores the fact that L and C are distributed and not lumped elements. As an example of approximate experimental parameters, let $\Omega_{\rm RF}/2\pi=40$ MHz, $Q_L=170$ and $L=1~\mu{\rm H}$ then we have C=16~pF and $R=43~k\Omega$. The resonator's inductance was modeled as a 1.9 meter long vacuum coax with a ratio of outer to inner conductor of 12. Suppose that a trap chip is added to the circuit and the quality factor drops to $Q_{Lt}=80$ (with no change in $\Omega_{\rm RF}$) as in Figure 4.19 on the next page. Then the new parallel resistance of R and R_t is $R_p=20~k\Omega$. And,

$$R_t = \frac{RR_p}{R + R_p} = 38 \ k\Omega.$$

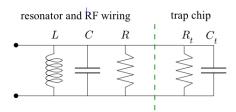


Figure 4.19: Parallel RLC model for ion trap chip losses. R is due to the intrinsic losses in the bare resonator and other wiring. R_t (C_t) accounts for the additional loss (capacitance) due to the trap chip.

If the RF potential at the trap is V = 50 volts, then the power dissipated by the trap is $\frac{1}{2}V^2/R_t = 32$ mW.

4.7 Time-resolved Doppler cooling

A critical measure of an ion trap's utility in QIP is its electric field noise which can heat the ions. Historically, this has been measured in ions with hyperfine structure cooled to the motional ground state, an expensive and technically challenging undertaking [Caves 80, Diedrich 89, Monroe 95, King 98, Turchette 00, Wineland 98]. In 2007 a measurement technique relying on only a single Doppler cooling laser beam was demonstrated experimentally for ²⁴Mg⁺ [Epstein 07] and was explained theoretically [Wesenberg 07]. ²⁴Mg⁺ has no hyperfine structure; there is no need for a quantizing magnetic field, a repump laser or careful laser beam polarization control [Seidelin 06, Epstein 07]. The key physics for this method is that near resonance, an atom's fluorescence rate is influenced by its motion due to the Doppler effect. Experimentally, this can be exploited as follows.

- (1) Cool a trapped ion to its Doppler limit.
- (2) Let it remain in the dark for some time. Ambient electric fields couple to the ion's motion and heat it.
- (3) Turn on the Doppler cooling laser. Measure the ion's time-resolved fluorescence.
- (4) A fit from a theoretical model to ion fluorescence rate vs time (during recooling) gives an estimate of the ion's temperature at the end of step 2 [Wesenberg 07].

recooling of hot ions The theory by Wesenberg, et al. explored cooling of hot ions where the Doppler shift is on the order of the cooling transition line width Γ . The model is a one-dimensional semiclassical theory of Doppler cooling in the weak binding limit where $\omega_z \ll \Gamma$. It is assumed that hot ions undergo harmonic oscillations with amplitudes corresponding to the Maxwell-Boltzman energy distribution when averaged over many experiments [Wesenberg 07].

As a one-dimensional (1D) model, only a single motional mode is assumed to be hot. Since the electric field spectral density S_E at the ion is observed to scale approximately as $S_E \propto \omega^{-\alpha}$ where $\alpha = 1$ to 1.5, the heating is effectively 1D if $\omega_z \ll \omega_x, \omega_y$ [Deslauriers 06b, Turchette 00]. This is also important experimentally because efficient Doppler cooling requires laser beam overlap with all modes simultaneously: a change in ion fluorescence can arise from heating of any mode.

Note that ion heating may result from effects unrelated to electric field fluctuations, for example collisions with ions or neutrals. Also, the model only applies to single trapped ions. Other heating mechanisms are possible with multiple ions [Walther 93]. It also requires that the 3D micromotion be nulled as this opens the door for other sources of heating (see Section 8.3 on page 174).

The model accuracy is related to three experimental parameters. They should be optimized to the extent permitted by experimental constraints like trap depth and the background collision rate.

- (1) Doppler cooling laser detuning δ from resonance ω_0 should be small. While $\delta = -\Gamma/2$ is optimal for laser cooling of atoms near the Doppler limit, I used $\delta = \omega_{\text{laser}} \omega_0 = -\Gamma/4.4$
- (2) The cooling laser beam intensity should be as low as is practical. I operated at a small saturation parameter: $s \sim 1$. ⁵

⁴ This choice was made because $-\Gamma/4$ was better for the micromotion minimization experiment that frequently preceded heating experiments. It was experimentally convenient to not change the detuning.

⁵ In the optical Bloch equation model for 2-level atomic systems, the saturation parameter s relates

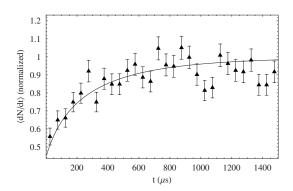


Figure 4.20: Plot showing normalized fluorescence rate dN/dt during Doppler cooling of a hot ion vs ion dark time. The experimental data is fit to the 1D model discussed in the text. The fit has a single free parameter: the ion's temperature at the outset of cooling (averaged over many experiments). The error bars are based on counting statistics.

(3) The ion's initial temperature should be high enough so that its fluorescence is reduced considerably due to Doppler broadening. For my trap parameters this corresponded to about 1000 quanta.

The saturation parameter for a particular laser beam intensity can be estimated by recording ion fluorescence as a function of intensity and doing a fit to this expression.

Measurement of an ion's temperature by time-resolved fluorescence was first reported by Seidelin, et al. [Seidelin 06]. The technique was later confirmed experimentally by comparison with Raman resolved sideband cooling (an established method, [Monroe 95]. It was also confirmed that ion heating rates measured at the > 1000 quanta level can be extrapolated to the single quantum level [Epstein 07]. This is important in the context of ion QIP where gate fidelity is impacted by very few motional quanta.

Experimental steps

The apparatus used to control the Doppler cooling laser beam and collect timeresolved fluorescence is discussed in Section 4.5 on page 128. The experiment proceeded as follows.

laser intensity to the steady state excited population ρ_{ee} ,

$$\rho_{\rm ee} = \frac{s/2}{1 + s + (2\delta/\Gamma)^2}.$$

Assuming, $\delta = 0$, for s = 1, $\rho_{ee} = 1/4$ and for $s \to \infty$, $\rho_{ee} = 1/2$.

- (1) Null ion micromotion.
- (2) Measure the axial trap frequency ω_z .
- (3) Measure the ion saturation parameter s.
- (4) Doppler cool the ion.
- (5) Turn off the Doppler cooling laser beam for time τ .
- (6) Turn on the Doppler cooling laser. Measure the ion's time-resolved fluorescence.
- (7) Repeat steps 4-6 and build up a histogram of fluorescence vs time.
- (8) Repeat steps 4-7 for several periods τ .

Care must be taken owing to duty cycle related thermal effects in AOMs. Some of the RF power delivered to an AOM is absorbed and causes it to heat up. The deflection angle in the AOMs I used depends weakly on temperature. During heating measurements, the RF to AOM 2 was switched on/off in order to turn on/off the BD Doppler laser beam (see Figure 4.12 on page 123). The AOM temperature change during these on/off cycles was sufficient to cause BD laser beam overlap with the ion to change. This is observed as a change in ion fluorescence over several seconds after RF is applied to a cool AOM 2. This effect was accounted for when measuring the saturation parameter; saturation was measured with the AOMs operated on same duty cycle as used in ion heating experiments.

Section 8.6 on page 185 lists the .dc file used in this experiment.

Chapter 5

RF Cooling of a Micro Cantilever

In this chapter I discuss the demonstration of a method to cool a fundamantal motional mode of a miniature cantilever by its capacitive coupling to a driven RF resonant circuit. Cooling results from the RF capacitive force, which is phase shifted relative to the cantilever motion. The technique was demonstrated by cooling a 7 kHz cantilever from room temperature to 45 K, obtaining reasonable agreement with a model for the cooling, damping, and frequency shift. Extending the method to higher frequencies in a cryogenic system could enable ground state cooling and may prove simpler than related optical experiments in a low temperature apparatus.

Precise control of quantum systems occupies the efforts of many laboratories; an important recent application of such control is in quantum information processing. Some of this work is devoted to quantum-limited measurement and control of the motion of mechanical oscillators. This has already been accomplished in a "bottom-up" approach where a single atom is confined in a harmonic well and cooled to the ground state of its quantum mechanical motion [Diedrich 89]. From this starting point physicists have made nonclassical mechanical oscillator states such as squeezed, Fock and Schrodinger-cat states [Meekhof 96, Monroe 96, Leibfried 05, Ben-Kish 03]. Quantum control of motional states has also emerged as powerful tool for spectroscopy and coupling of quantum systems [Leibfried 05, Haffner 05, Schmidt 05, Blatt 08].

For various applications, there is also interest in a "top-down" strategy, which has

approached the quantum limit by using ever smaller mechanical resonators [Braginskii 70, Braginskii 77]. In this case, small ($\sim 1~\mu m$) mechanical resonators, having fundamental motional frequencies of 10-100 MHz, can approach the quantum regime at low temperature ($< 1~\mathrm{K}$); mean thermal occupation numbers of 25 have been achieved [Naik 06]. For a review of this approach see [Schwab 05].

Cooling of macroscopic mechanical oscillators also has been achieved with optical forces and active external electronics to control the applied force [Cohadon 99, Arcizet 06, Weld 06, Kleckner 06, Poggio 07]. Passive feedback optical cooling has also been realized in which a mirror attached to a mechanical oscillator forms an optical cavity with another stationary mirror. For appropriate tuning of radiation incident on the cavity, a delay in the optical force on the oscillator as it moves gives cooling. This delay can result from a photothermal effect [Metzger 04, Harris 07] or from the stored energy response time of the cavity [Arcizet 06, Gigan 06, Corbitt 07]. Closely related passive cooling has been reported in [Naik 06, Schliesser 06].

We demonstrate a passive cooling mechanism where the damping force is the electric force between capacitor plates that here contribute to a resonant RF circuit [Braginskii 77, Wineland 06]. This approach has potential practical advantages over optical schemes; the elimination of optical components simplifies fabrication and integration into a cryogenic system, and the RF circuit could be incorporated on-chip with the mechanical oscillator.

This work was reported in Physical Review Letters in 2007 in an article titled "Passive cooling of a micromechanical oscillator with a resonant electric circuit" [Brown 07a]. The theory describing the cantilever-resonator coupling and cooling mechanism appeared in a 2006 Archive paper titled "Cantilever cooling with radio frequency circuits" [Wineland 06].

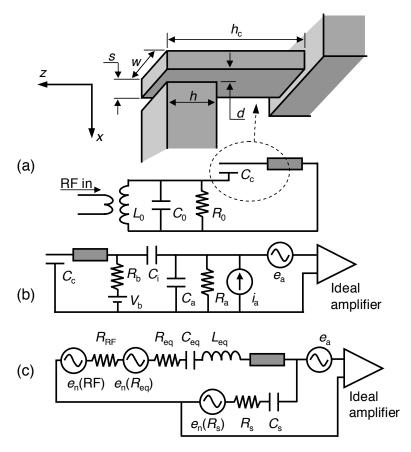


Figure 5.1: Schematics of the cantilever cooling and detection electronics. (a) Cantilever and associated RF circuitry. (b) Motional detection electronics. Near ω_c the RF circuit looks like a short to ground as shown. (c) Equivalent circuit for the cantilever and detection electronics near $\omega \approx \omega_c$.

A conducting cantilever of mass density ρ is fixed at one end (Fig. 5.1(a)). One face is placed a distance d from a rigidly mounted plate of area $w \times h$, forming a parallel-plate capacitor $C_c = \epsilon_0 w h/d$, where ϵ_0 is the vacuum dielectric constant. An inductor L_0 and capacitor C_0 in parallel with C_c form a resonant RF circuit with frequency $\Omega_0 = 1/\sqrt{L_0(C_0 + C_c)}$ and with losses represented by resistance R_0 . We assume $Q_{\rm RF} \gg 1$, where $Q_{\rm RF} = \Omega_0 L_0/R_0 = \Omega_0/\gamma$ and γ is the damping rate.

We consider the lowest-order flexural mode of the cantilever, where the free end oscillates in the \hat{x} direction (vertical in Fig. 5.1(a)) with angular frequency $\omega_c \ll \gamma$. We take x to be the displacement at the end of the cantilever, so the displacement as a function of (horizontal) position z along the length of the cantilever is given by x(z) = f(z)x, where f(z) is the mode function (see, e.g., [Butt 95]). Small displacements

due to a force F can be described by the equation of motion,

$$m\ddot{x} + m\Gamma\dot{x} + m\omega_c^2 x = F, (5.0.1)$$

where Γ is the cantilever damping rate and m its effective mass, given by $\rho \xi_{\rm c}'' w h_{\rm c} s$, where $\xi_{\rm c}'' \equiv \frac{1}{h_{\rm c}} \int_{h_{\rm c}} f(z)^2 dz = 0.250$ for a rectangular beam.

For simplicity, first assume $h \ll h_{\rm c}$, so that the force is concentrated at the end of the cantilever. If a potential V is applied across $C_{\rm c}$, the capacitor plates experience a mutual attractive force $F = \epsilon_0 w h V^2/(2d^2) = C_{\rm c} V^2/(2d)$. Consider that V is an applied RF potential $V_{\rm RF} \cos(\Omega_{\rm RF} t)$ with $\Omega_{\rm RF} \approx \Omega_0$. Because $\omega_{\rm c} \ll \Omega_0$, the force for frequencies near $\omega_{\rm c}$ can be approximated by the time-averaged RF force

$$F_{\rm RF} = \frac{C_{\rm c} \langle V^2 \rangle}{2d} = \frac{C_{\rm c} V_{\rm RF}^2}{4d} = \frac{\epsilon_0 w h V_{\rm RF}^2}{4d^2},$$
 (5.0.2)

where, for a fixed input RF power, $V_{\rm RF}$ will depend on $\Delta\Omega \equiv \Omega_0 - \Omega_{\rm RF}$, according to

$$\frac{V_{\rm RF}^2}{V_{\rm max}^2} = \frac{1}{1 + \left[2Q_{\rm RF}\Delta\Omega/\Omega_0\right]^2} \equiv \mathcal{L}(\Delta\Omega) \ . \tag{5.0.3}$$

As the cantilever oscillates, its motion modulates the capacitance of the RF circuit thereby modulating Ω_0 . As Ω_0 is modulated relative to Ω_{RF} , so too is the RF potential across the capacitance, according to Eq. (5.0.3). The associated modulated force shifts the cantilever's resonant frequency. Due to the finite response time of the RF circuit, there is a phase lag in the force relative to the motion. For $\Delta\Omega > 0$ the phase lag leads to a force component that opposes the cantilever velocity, leading to damping. If this damping is achieved without adding too much force noise then it cools the cantilever.

The average force due to applied potentials displaces the equilibrium position d_0 of the cantilever. We assume this displacement is small and is absorbed into the definition of d_0 , writing $d \equiv d_0 - x$, where $x \ll d_0^{-1}$. Following [Braginskii 77] or [Wineland 06] we find $\omega_c^2 \to \omega_c^2 (1 - \kappa)$ and $\Gamma \to \Gamma + \Gamma'$, with

$$\kappa \equiv \frac{C_{\rm c} V_{\rm max}^2 \mathcal{L}(\Delta \Omega)}{2m\omega_{\rm c}^2 d_0^2} \left[\xi'' + \frac{2(\xi')^2 Q_{\rm RF} \Delta \Omega \mathcal{L}(\Delta \Omega)}{\gamma} \frac{C_{\rm c}}{C_{\rm c} + C_0} \right], \tag{5.0.4}$$

¹ This expression for d neglects the curvature of the flexural mode and is strictly true only for $h \ll h_c$ and $d_0 \ll w$, h.

$$\Gamma' \equiv \frac{Q_{\rm RF} V_{\rm max}^2 C_{\rm c}^2}{m\omega_{\rm c} d_0^2 (C_{\rm c} + C_0)} \frac{(\xi')^2 \Delta \Omega \mathcal{L}(\Delta \Omega)^2}{\gamma} \sin \phi, \tag{5.0.5}$$

where $\xi' \equiv \frac{1}{h} \int_h f(z) dz$ and $\xi'' \equiv \frac{1}{h} \int_h f(z)^2 dz$ are geometrical factors required when $h \ll h_c$ is not satisfied. The phase ϕ is equal to $\omega_c \tau$, where $\tau = 4\mathcal{L}(\Delta\Omega)/\gamma$ is the response time of the RF circuit [Marquardt 07]. For $\Delta\Omega > 0$, Γ' gives increased damping. For $\Delta\Omega = \gamma/2$ and $h \ll h_c$ ($\xi' \approx \xi'' \approx 1$), we obtain the expressions of [Wineland 06]. For our experiment, $h \approx h_c$, $\xi' = 0.392$, and $\xi'' = \xi''_c = 0.250$.

We detect the cantilever's motion by biasing it with a static potential $V_{\rm b}$ through resistor $R_{\rm b}$ as shown in Fig. 5.1(b), where $R_{\rm a}$, $C_{\rm a}$, $i_{\rm a}$, and $e_{\rm a}$ represent the equivalent input resistance, capacitance, current noise, and voltage noise, respectively, of the detection amplifier. We make $R_{\rm a}$ and $R_{\rm b}$ large to minimize their contribution to the current noise $i_{\rm a}$. We assume $C_{\rm i} \gg (C_{\rm c} + C_{\rm a})$ and $\omega_{\rm c} R(C_{\rm c} + C_{\rm a}) \gg 1$, where $1/R \equiv 1/R_{\rm b} + 1/R_{\rm a}$. As the cantilever moves, thereby changing $C_{\rm c}$, it creates a varying potential that is detected by the amplifier.

The (charged) cantilever can be represented by the series electrical circuit in Fig. 5.1(c). From Eq. (5.0.2) and following [Wineland 75], the equivalent inductance is given by $L_{\rm eq} = m d_0^2/(q_c \xi')^2$, where q_c is the average charge on the cantilever. From $L_{\rm eq}$, $\omega_{\rm c}$, and Γ , we can then determine $C_{\rm eq} = 1/(\omega_{\rm c}^2 L_{\rm eq})$ and $R_{\rm eq} = L_{\rm eq}\Gamma$. Additional damping due to the RF force is represented by $R_{\rm RF} = L_{\rm eq}\Gamma'$. For frequencies $\omega \approx \omega_{\rm c}$, the parallel combination of $R_{\rm b}$, $C_{\rm a}$, and $R_{\rm a}$ can also be expressed instead as the Thévenin equivalent $R_{\rm s}$ - $C_{\rm s}$ circuit in Fig. 5.1(c). The amplifier's current noise $i_{\rm a}$ is now represented as $e_{\rm n}(R_{\rm s})$. The intrinsic thermal noise of the cantilever is characterized by a noise voltage $e_{\rm n}(R_{\rm eq})$ having spectral density $4k_{\rm B}T_{\rm c}R_{\rm eq}$, where $k_{\rm B}$ is Boltzmann's constant and $T_{\rm c}$ is the cantilever temperature.

We must also consider noise from the RF circuit. In Eq. (5.0.2), we replace $V_{\rm RF}$ with $V_{\rm RF} + v_{\rm n}({\rm RF})$, where $v_{\rm n}({\rm RF})$ is the noise across the cantilever capacitance $C_{\rm c}$ due to resistance in the RF circuit and noise injected from the RF source. The

cantilever is affected by amplitude noise $v_{\rm n}({\rm RF})$ at frequencies near $\Omega_{\rm RF} \pm \omega_{\rm c}$, because cross terms in Eq. (5.0.2) give rise to random forces at the cantilever frequency. This force noise can be represented by $e_{\rm n}({\rm RF})$ in the equivalent circuit. The noise terms sum to $e_{\rm n}^2 = e_{\rm n}^2(R_{\rm eq}) + e_{\rm n}^2(R_{\rm s}) + e_{\rm n}^2({\rm RF})$ ($e_{\rm a}$ does not drive the cantilever), which gives a cantilever effective temperature

$$T_{\text{eff}} = \frac{e_{\text{n}}^2}{4k_{\text{B}}(R_{\text{eq}} + R_{\text{RF}} + R_{\text{s}})}.$$
 (5.0.6)

Our cantilever has nominal dimensions $h_{\rm c}\approx 1.5$ mm, $s\approx 14~\mu{\rm m}$, and $w\approx 200~\mu{\rm m}$, created by etching through a p++-doped ($\sim 0.001~\Omega~{\rm cm}$), 200 $\mu{\rm m}$ thick silicon wafer with a standard Bosch reactive-ion-etching process. Its resonant frequency and quality factor are $\omega_{\rm c}/(2\pi)\approx 7$ kHz and $Q\approx 20,000$. The cantilever is separated by $d_0\approx 16~\mu{\rm m}$ from a nearby doped silicon RF electrode, forming capacitance $C_{\rm c}^2$. The sample is enclosed in a vacuum chamber with pressure less than 10^{-5} Pa. The RF electrode is connected via a vacuum feedthrough to a quarter-wave resonant cavity with $L_0=330(30)$ nH and with loaded quality factor $Q_{\rm RF}=234(8)$ at $\Omega_{\rm RF}/(2\pi)=100$ MHz when impedance matched to the source. The cantilever is connected by a short length of coaxial cable and blocking capacitor $C_{\rm i}=4$ nF to a low-noise JFET amplifier (see Fig. 5.1(b)). We have $C_{\rm a}=48(1)$ pF, with $R_{\rm a}=R_{\rm b}=1$ G Ω . We use $V_{\rm b}=-50$ V, which gives a measured 2.5 $\mu{\rm m}$ static deflection at the cantilever end.

We temporarily lowered $R_{\rm a}$ to 600 k $\Omega \approx 1/(\omega_{\rm c}C_{\rm a})$, in which case the cantilever noise spectrum strongly distorts from a Lorentzian lineshape (not shown), and it becomes straightforward to extract the equivalent circuit parameters of Fig. 5.1(c). We find $L_{\rm eq} = 27,000(600)$ H. To lowest order in RF power this equivalent inductance remains constant, so we assume this value for $L_{\rm eq}$ in subsequent fits to the thermal spectra, while $R_{\rm RF}$ is allowed to vary to account for RF power induced changes in the cantilever damping.

² The uncertainties for these numbers are a few micrometers, stemming from spatial nonuniformity in our etch process.

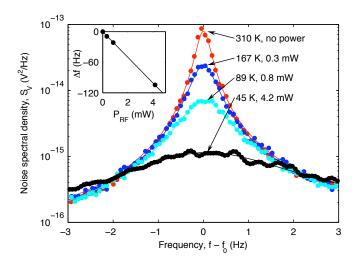


Figure 5.2: Cantilever thermal spectra for four values of RF power. The x-axis for each spectrum has been shifted to align the maxima of the three datasets. $S_{\rm v}$ is the measured noise referred to the input of the amplifier. Solid lines are fits to the model in Fig. 5.1(c), giving the temperatures indicated by arrows. (Inset) Cantilever frequency shift Δf versus RF power.

For $R_{\rm a}=1~{\rm G}\Omega$ we measure $e_{\rm a}=1.5~{\rm nV/\sqrt{Hz}}$ and $i_{\rm a}=16~{\rm fA/\sqrt{Hz}}$. Figure 5.2 shows a series of thermal spectra acquired with this value of $R_{\rm a}$ at different values of RF power $P_{\rm RF}$ but at constant detuning $\Delta\Omega=2\pi\times90~{\rm kHz}=0.21\gamma$. Both the lowering and the broadening of the spectra with increasing $P_{\rm RF}$ are evident, in accordance with Eq. (5.0.5). Here, the effective temperature is very nearly proportional to the area under the curves, although there is a slight asymmetric distortion from a Lorentzian lineshape, fully accounted for by the equivalent circuit model. The center frequency of each spectrum also shifts to lower frequencies for increasing $P_{\rm RF}$, as predicted by Eq. (5.0.4) and the definition of κ in terms of $\omega_{\rm c}$. After calibrating the gain of the amplifier, we extract $e_{\rm n}^2$ for each spectrum from a fit to the model of Fig. 5.1(c). The absolute effective temperature is then given by Eq. (5.0.6).

Equations (5.0.5) and (5.0.6) predict that the cantilever's effective temperature should fall with increasing $P_{\rm RF}$, as demonstrated by the data in Fig. 5.3 for low power. With no RF applied we find $T_{\rm eff}=310(20)$ K. The coldest spectrum corresponds to a temperature of 45(2) K, a factor of 6.9 reduction. The minimum temperature appears to be limited by AM noise from our RF source. This noise power at $\Omega_{\rm RF}\pm\omega_{\rm c}$ is constant

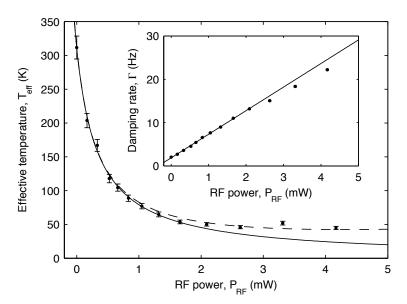


Figure 5.3: $T_{\rm eff}$ as a function of RF power. The solid line is the temperature predicted by Eq. (5.0.6) using Γ from the fit in the inset and $e_{\rm n}=e_{\rm n}(R_{\rm eq})$, while the dashed line takes into account additional noise due to the RF source. (Inset) Damping rate versus RF power. The solid line is a linear fit to the first ten points.

relative to the carrier, leading to a noise power at ω_c given by $e_n(RF)^2 \propto P_{RF}^2$. We fit the residual noise $e_n(RF)^2$ to a quadratic in P_{RF} , giving the dashed line temperature prediction in Fig. 5.3. From this fit we determine that the AM noise of our source is -170 dBc/Hz, reasonably consistent with the value (-167 dBc/Hz) measured by spectrum analysis.

The inset shows the cantilever damping rate Γ versus $P_{\rm RF}$. The slope is $\Gamma'/P_{\rm RF}=5,450(70)~{\rm Hz/W}$, slightly higher than the value 3,970 Hz/W calculated from Eq. (5.0.5) and the nominal cantilever dimensions. The nonlinearity in $\Gamma'/P_{\rm RF}$ at higher powers is consistent with the cantilever being pulled toward the RF electrode. We have numerically simulated this effect and find reasonable agreement. The variation of κ with $P_{\rm RF}$ (not shown) is also linear, with a slope $\kappa/P_{\rm RF}=7.64(8)~{\rm W}^{-1}$, compared with the value $3.45~{\rm W}^{-1}$ calculated from Eq. (5.0.4).

Although $\Gamma'/P_{\rm RF}$ and $\kappa/P_{\rm RF}$ differ from their predicted values, this disagreement is not unexpected considering the relatively large variations in dimensions d_0 and s^3 . Another indication of these uncertainties is that optical measurements of the static deflection of the cantilever along its length disagree with predictions based on a constant

³ The uncertainties for these numbers are a few micrometers, stemming from spatial nonuniformity in our etch process.

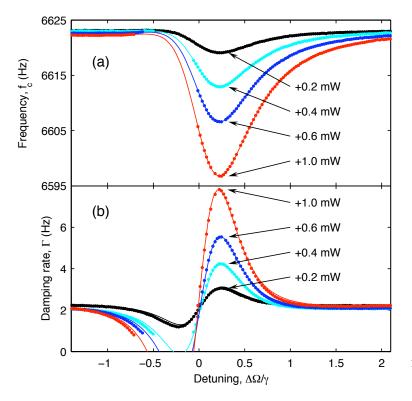


Figure 5.4: Variation of the cantilever resonance with respect to RF frequency. (a) Cantilever frequency $f_{\rm c}$ and (b) damping rate Γ versus normalized RF detuning $\Delta\Omega/\gamma$ for several values of P_{RF} . The missing points between -0.7 MHz and 0 MHz correspond to a region of instability where Γ becomes negative. Solid lines are fits to Eqs. (5.0.4) and (5.0.5).

cantilever cross section. This will lead to deviations from our calculated values of ξ' , ξ'' , and ξ''_{c} . However, we stress that these deviations should not give significant errors in our measured values of L_{eq} , R_{eq} , and therefore our determination of T_{eff} .

To further test the model, we examine Γ and ω_c as a function of $\Delta\Omega$ (Fig. 5.4). For large detunings $\Delta\Omega$, Γ asymptotically approaches the value obtained in Fig. 5.3 for $P_{\rm RF}=0$. Near $\Delta\Omega=0$, $f_{\rm c}$ is generally shifted to a lower value, while Γ is either enhanced or suppressed, according to the sign of $\Delta\Omega$. Data cannot be obtained for $\Delta\Omega<0$ when the RF power level is sufficient to drive the cantilever into instability ($\Gamma<0$). The solid line fits show good agreement with the predicted behavior. From these fits we extract $C_{\rm c}=0.09~{\rm pF}$, lower than the value 0.17 pF obtained from the physical dimensions. This disagreement is not surprising for the reasons mentioned above.

Some experiments using optical forces have observed strong effects from the laser power absorbed in the cantilever mirror. A conservative estimate of the RF power

dissipated in our cantilever gives a temperature rise of less than 1 K at the highest power, so these effects should not be significant.

Although rather modest cooling is obtained here, the basic method could eventually provide ground state cooling. For this we must achieve the resolved sideband limit, where $\omega_{\rm c} > \gamma$ [Marquardt 07, Wilson-Rae 07], and the cooling would be very similar to the atomic case [Diedrich 89, Monroe 95]. To insure a mean quantum number n less than one, the heating rate from the ground state $\dot{n}_{\rm heat} = \Gamma k_{\rm B} T_{\rm c}/(\hbar\omega_{\rm c})$ must be less than the cooling rate for $n=1\to 0$. The cooling rate $\dot{n}_{\rm cool}$ can be estimated by noting that each absorbed photon on the lower sideband (at the applied RF frequency $\Omega_0 - \omega_{\rm c}$) is accompanied by re-radiation on the RF "carrier" at Ω_0 . If we assume the lower sideband is saturated for $n\approx 1$, $\dot{n}_{\rm cool}\approx \gamma/2$. Hence we require $R\equiv \dot{n}_{\rm heat}/\dot{n}_{\rm cool}\approx 2k_{\rm B}T_{\rm c}Q_{\rm RF}/(\hbar\Omega_0Q_{\rm c})\ll 1$. For example, if $T_{\rm c}=0.1$ K, $\Omega_0/(2\pi)=20$ GHz, $Q_{\rm RF}=5,000$ (e.g., a stripline), and $Q_{\rm c}=20,000$ we have $R\approx 0.05$. For resolved sidebands, we require $\omega_{\rm c}/(2\pi)>4$ MHz.

Chapter 6

Semiclassical Quantum Fourier Transform

In this chapter I summarize an implementation of the semiclassical quantum Fourier transform (QFT) in a system of three beryllium ion qubits (two-level quantum systems) confined in a segmented multi-zone trap. The quantum Fourier transform is a crucial step in Shor's algorithm, a quantum algorithm for integer factorization which is superpolynomially faster than the fastest known classical factoring algorithm. The QFT acts on a register of qubits to determine the periodicity of the input states' amplitudes. With coworkers at NIST I applied the transform to several input states of different periodicities; the results enable the location of peaks corresponding to the original periods.

Among quantum algorithms discovered up to this time, Shor's method for factoring large composite numbers [Shor 94] is arguably large-scale quantum information processing's most prominent application; efficient factoring would render current cryptographic techniques based on large composite-number keys vulnerable to attack. The key component of this algorithm is an order-finding subroutine that requires application of the quantum discrete Fourier transform to determine the period of a set of quantum amplitudes [Shor 94, Coppersmith 94, Ekert 96, Nielsen 00]. In addition to this application, the QFT is also an essential part of quantum algorithms for phase estimation and the discrete logarithm [Nielsen 00]. In fact, the polynomial-time QFT is responsible for most of the known instances of exponential speedup over classical algorithms.

Relative phase information of the output state from the QFT is not required

when applied in any of the algorithms mentioned above; only the measured probability amplitudes of each state are used. This allows the replacement of the fully coherent QFT with the semiclassical, or "measured" QFT [Griffiths 96], in which each qubit is measured in turn, and the prescribed controlled phase rotations on the other qubits are conditioned on the classical measurement outcomes. This eliminates the need for entangling gates in the QFT protocol, which for an ion implementation considerably relaxes the required control of the ions' motional states. In addition, the semiclassical version is quadratically more efficient in the number of quantum gates when compared with the fully coherent version. That is, for n qubits the required number of quantum gates is O(n) instead of $O(n^2)$.

Prior implementations of the QFT were in nuclear magnetic resonance (NMR) systems and used the coherent version of the protocol [Vandersypen 00, Weinstein 01, Vandersypen 01, Lee 02, Weinstein 04]. This implementation was distinguished in that it used the more efficient measured-QFT and that ions are a scalable system for quantum information processing, while NMR is not [Cory 00]. Extension of our implementation to larger quantum registers requires a linear increase in the number of qubits and qubit operations [Wineland 98, Kielpinski 02].

The details of the QFT as realized in the lab were published in a paper which appeared in Science in 2005 titled "Implementation of the semiclassical quantum Fourier transform in a scalable system" [Chiaverini 05b]. Details on the apparatus, experimental techniques and principles of quantum control of beryllium ion qubits are discussed in the literature [Wineland 98, Kielpinski 01, Barrett 04, Langer 06].

The QFT is a basis transformation in an N-state space that transforms the state $|k\rangle$ (k is an integer ranging from 0 to N-1) according to

$$|k\rangle \to \frac{1}{\sqrt{N}} \sum_{j=0}^{N-1} e^{i2\pi jk/N} |j\rangle.$$
 (6.0.1)

The action on an arbitrary superposition of states may be written as

$$\sum_{k=0}^{N-1} x_k |k\rangle \to \sum_{j=0}^{N-1} y_j |j\rangle, \tag{6.0.2}$$

where the complex amplitudes y_j are the discrete Fourier transform [Arfken 85] of the complex amplitudes x_k . For three qubits, switching to binary notation, where k_1 , k_2 , and k_3 are the most to least significant bits, respectively, in the label for the state $|k_1k_2k_3\rangle = |k_1\rangle \otimes |k_2\rangle \otimes |k_3\rangle$ ($k_i \in \{0,1\}$), the transform can be written as [Nielsen 00]

$$|k_1k_2k_3\rangle \to \frac{1}{\sqrt{8}} \left(|0\rangle + e^{i2\pi[0.k_3]}|1\rangle \right) \otimes \left(|0\rangle + e^{i2\pi[0.k_2k_3]}|1\rangle \right) \otimes \left(|0\rangle + e^{i2\pi[0.k_1k_2k_3]}|1\rangle \right), \tag{6.0.3}$$

where $[0.q_1q_2\cdots q_n]$ denotes the binary fraction $q_1/2+q_2/4+\cdots+q_n/2^n$. When written in this form, it can be seen that the QFT is the application to each qubit of a Hadamard transformation $\left[|0\rangle \to \frac{1}{\sqrt{2}}\left(|0\rangle + |1\rangle\right)$ and $|1\rangle \to \frac{1}{\sqrt{2}}\left(|0\rangle - |1\rangle\right)\right]$ and a z rotation conditioned on each of the less significant qubits, with a phase of decreasing binary significance due to each subsequent qubit, all followed by a bit-order reversal [Nielsen 00]. The three-qubit quantum circuit, without the bit-order reversal, is shown in Fig. 1a. The simplified circuit for the measured QFT is shown in Fig. 1b.

In the experiment, z rotations are transformed into x rotations, which are more straightforward to implement in our system, and rotations are redistributed to accommodate required spin-echo refocussing pulses (π rotations) which reduce dephasing due to fluctuating magnetic fields [Hahn 50, Allen 75, Rowe 02], but this does not change the basic protocol. Because of the substitution of $\pi/2$ rotations for Hadamard operations and our choice of conditional-rotation direction, the coherent QFT corresponding to our measured QFT is described by

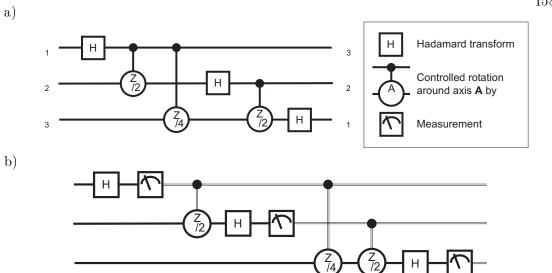


Figure 6.1: Circuits for the quantum Fourier transform (QFT) of three qubits. (a) The QFT as composed of Hadamard transforms and two-qubit conditional phase gates [Nielsen 00]. The gate labeling scheme denotes the axis about which the conditional rotation takes place and, below the axis label, the angle of that rotation. The $|\varphi_i\rangle$ and $|\chi_i\rangle$ are the input and output states, respectively, of qubit i. The most-significant qubit corresponds to i=1. This circuit produces the QFT in reverse bit order, so in practice, the qubits are simply read out in reverse order [Nielsen 00]. (b) The semiclassical (or "measured") QFT [Griffiths 96]. The double lines denote classical information. This circuit can be implemented by means of a single classically-controlled quantum operation on each qubit. The protocol is preceded by state preparation (not shown in figure) of the quantum state to be transformed.

$$|k_1 k_2 k_3\rangle \to \frac{1}{\sqrt{8}} \left(|0\rangle - e^{-i2\pi[0.k_3]} |1\rangle \right) \otimes \left(|0\rangle - e^{-i2\pi[0.k_2 k_3]} |1\rangle \right) \otimes \left(|0\rangle - e^{-i2\pi[0.k_1 k_2 k_3]} |1\rangle \right).$$
(6.0.4)

The sign differences from Eq. 3 are unimportant, because only the probability amplitudes of the output state are measured; the relative phases of the output basis states are arbitrary. We have applied this three-qubit QFT to input states of several different periodicities.

The qubits comprise two states of the ground-state hyperfine manifold of ${}^{9}\text{Be}^{+}$: the state $|F=1,m_F=-1\rangle$, labeled $|0\rangle$, and the state $|F=2,m_F=-2\rangle$, labeled $|1\rangle$.

These states are separated in frequency by 1.28 GHz. Rotations

$$R(\theta, \phi) = \cos \frac{\theta}{2} I - i \sin \frac{\theta}{2} \cos \phi \, \sigma_x - i \sin \frac{\theta}{2} \sin \phi \, \sigma_y \tag{6.0.5}$$

are performed by means of two-photon stimulated-Raman transitions [Monroe 95, Wineland 03]. Here θ is the rotation angle, ϕ is the angle of the rotation axis from the x axis in the xy plane of the Bloch sphere [Allen 75], I is the identity operator, and σ_x and σ_y are the usual Pauli spin operators. The beryllium ions are confined in a linear radio-frequency Paul trap [Barrett 04] similar to that described in [Rowe 02]. This trap contains six zones, and the ions can be moved between these zones, together or separately, by means of synchronized variation of the potentials applied to the trap's control electrodes. State determination is made by projection of the qubit state with the use of resonance fluorescence [Monroe 95] (an ion in the $|1\rangle$ state fluoresces, whereas an ion in the $|0\rangle$ state does not). Measurement results were recorded, and laser pulses were applied by means of classical logic to implement conditional operations. The QFT protocol proceeded as depicted in Fig. 2a, with ions located in the multizone trap as shown in Fig. 2b.

Five different states were prepared to test the QFT protocol (Table 1). These states have periods of 1, 2, 4, 8, and approximately 3. The three-qubit state space consists of eight states, labeled $|000\rangle$, $|001\rangle$, ..., $|111\rangle$ in binary notation and ordered lexicographically. The periodicity is derived from the recurrence of the quantum amplitudes in a superposition of these eight states.

The period 1 state was generated by applying the rotation $R(\pi/2, -\pi/2)$ to all three ions in the initial state $|111\rangle$. The period 2 state was generated from $|111\rangle$ by physically separating ion 3 from ions 1 and 2, applying a rotation $R(\pi/2, -\pi/2)$ to ions 1 and 2, and then bringing all three ions back together. Similarly, the period 4 state was created by applying the rotation $R(\pi/2, -\pi/2)$ to only the first ion after

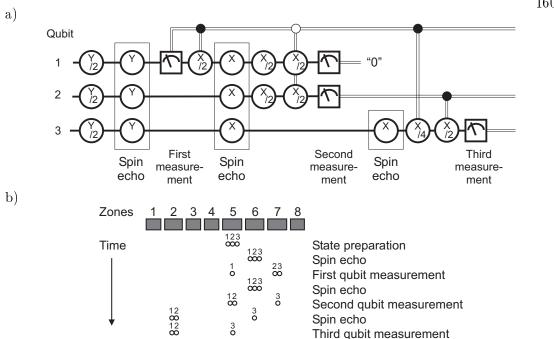


Figure 6.2: Circuit for the QFT and locations of the ions in the multizone trap during protocol execution. (a) The semiclassical QFT [Griffiths 96] as implemented in this Report. The double lines denote classical information. The closed circles on control lines denote rotation conditional on "1;" the open circles denote rotation conditional on "0." The initial conditional rotation of qubit 1 ensures that it is in the non-fluorescing state when the second ion is measured (the second ion is measured in the presence of the first ion, which contributes negligibly to the fluorescence signal during the second measurement [Schaetz 04]; refer to "Second qubit measurement" (b)). This circuit, up to some irrelevant phases, can be obtained from that in Fig. 1b through conjugation of rotations and reordering of some operations. (b) The locations of the ions in the multizone trap structure during the QFT protocol as a function of time. Separation of ions and refocussing operations are performed in zone 6, and all other qubit operations are performed in zone 5.

separating it from ions 2 and 3. The period 8 state was simply the state of the ions after initialization, $|111\rangle$.

The most obvious (approximate) period 3 state in this eight-state space is $|000\rangle +$ $|011\rangle + |110\rangle$ (here and in the following, we omit normalization factors). Becasue this state's periodicity is not commensurate with the state space, the addition of the next (in a sequence of three) basis state $|001\rangle$ to this superposition also results in an approximate period 3 state, $|\psi_3'\rangle = |000\rangle + |011\rangle + |110\rangle + |001\rangle$. We used a cyclic permutation of $|\psi_3'\rangle$;

Table 6.1: Periodic states	prepared to test the	semiclassical QFT protocol
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Periodicity	State (normalization omitted)	Preparation fidelity
1	$ \psi_1\rangle = 000\rangle + 001\rangle + 010\rangle + \dots + 111\rangle$	0.98(1)
2	$ \psi_2\rangle = 001\rangle + 011\rangle + 101\rangle + 111\rangle$	0.98(1)
~ 3	$ \psi_3\rangle = 001\rangle + 011\rangle + 100\rangle + 110\rangle$	0.90(2)
4	$ \psi_4\rangle = 011\rangle + 111\rangle$	0.98(1)
8	$ \psi_8\rangle = 111\rangle$	> 0.99(1)

in particular, adding 3 (mod 8) to each state produces $|\psi_3\rangle = |011\rangle + |110\rangle + |001\rangle + |100\rangle$. This state is the tensor product of $|01\rangle_{1,3} + |10\rangle_{1,3}$ (ions 1 and 3) with $|0\rangle_2 + |1\rangle_2$ (ion 2). Starting from $|111\rangle$, this state can be prepared by entangling the outer two ions (ions 1 and 3) with a geometric phase gate embedded between two rotations— $R(\pi/2, \pi/4)$ and $R(3\pi/2, \pi/4)$ —applied to all three ions [Leibfried 03b, Barrett 04]. This was followed by a rotation $R(\pi/2, -\pi/2)$ to all three ions. This state was produced with a fidelity of approximately 0.90 (resulting from the reduced fidelity inherent in multi-qubit entangling operations compared with single-qubit rotations).

Each experiment began with Doppler cooling and Raman-sideband cooling to bring the ions to the ground state of all three axial vibrational modes of the trapping potential and optical pumping to prepare the three ions in the internal state |111⟩ [Wineland 98, King 98]. The aforementioned input states were then prepared as described above. For each input state, several thousand implementations of the QFT were performed, each involving: (i) rotation of ion 1, (ii) measurement of ion 1, (iii) rotation of ion 2 conditional on the measurement of ion 1, (iv) measurement of ion 2, (v) rotation of ion 3 conditional on the first two measurements, and (vi) measurement of ion 3. Each experiment required approximately 4 ms after initial cooling, optical pumping, and state preparation.

The measured output state probabilities after application of the QFT algorithm

are shown in Fig. 3 along with the theoretically expected probabilities for the five different input states. The data generally agree with the theoretical predictions, although the deviations from the predicted values are larger than can be explained statistically, and are due to systematic errors in the experiment. These systematic errors are associated with the state preparation (not associated with the QFT protocol) as well as with the separate detections and conditional rotations of the three ions (intrinsic to the QFT protocol). The first, second, and third ions were measured approximately 1.2 ms, 2.4 ms, and 3.5 ms after the beginning of the algorithm. Dephasing due to slow local magnetic-field fluctuations, though mitigated by the refocussing (spin-echo) operations, grows as a function of time during each experiment; the chance that an error occurs because of dephasing grows from approximately 5% for the first ion to approximately 13% for the third ion.

Even with these systematic errors, the results compare well with theory, as can be shown by examining the squared statistical overlap (SSO) (derived from the statistical overlap of [Fuchs 96]) of each set of data with the associated predictions. Here, we define the SSO as $\gamma = \left(\sum_{j=0}^{7} m_j^{\frac{1}{2}} e_j^{\frac{1}{2}}\right)^2$, where m_j and e_j are the measured and expected output-state probabilities of state $|j\rangle$, respectively. This is an effective measure of fidelity without regard for relative output phases. The lowest measured SSO for the five prepared states is 0.87, suggesting that peaks can be reliably located to determine periodicities as required for Shor's factorization algorithm. To verify the reliability of the protocol for this task, one should compare the experimental and theoretical values of the measurement probabilities of the output states where peaks are located. For the period 2 state, the measured probability for the output state $|4\rangle = |100\rangle$ (the measurement outcome sufficient to determine the periodicity as 2), was 0.538, an 8% difference from the expected value of 0.5. For the period 3 state, the sum of the measured proba-

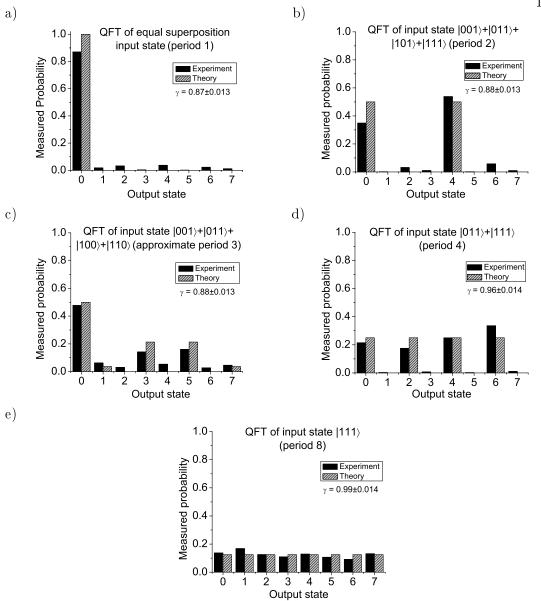


Figure 6.3: Results of the semiclassical QFT. Measured probability of each output state occurring after the application of the protocol is shown along with the expected transform output. Each plot contains data from 5000 experiments. The SSO γ is a measure of transform accuracy. Uncertainties quoted for the SSO are statistical and do not include systematic errors. (a) to (e) are the QFTs for $|\psi_1\rangle$, $|\psi_2\rangle$, $|\psi_3\rangle$, $|\psi_4\rangle$, and $|\psi_8\rangle$, respectively.

bilities for output state $|3\rangle = |011\rangle$ and state $|5\rangle = |101\rangle$ (the states corresponding to the most correct periodicity) was 0.301, a 29% difference from the expected value of 0.426. Notably, the preparation fidelity of this state was not as high as for the others.



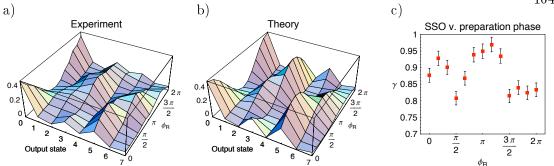


Figure 6.4: Semiclassical QFT of nominal period 3 state as a function of preparation phase ϕ_R (Eq. 6). (a) The measured probabilities are plotted as a function of the output state and the phase of the state preparation after application of the QFT protocol. The QFT at each phase is based on 2000 experiments. (b) The expected probability plotted in the same manner. (c) The SSO γ as a function of preparation phase. Error bars represent 1σ statistical uncertainties only.

One other set of input states was created to demonstrate that the semiclassical QFT protocol is sensitive to relative input phases. All the states of Table 1 had amplitudes (of the basis states in the superpositions) with the same phase. We also prepared a period 3 state with a relative phase between some states in the superposition. By incrementing the phase of the three uniform rotations used in the creation of the period 3 state with respect to the operations in the QFT protocol by a phase ϕ_R (that is, $R(\theta, \phi) \to R(\theta, \phi + \phi_R)$), we can create the state

$$|\psi_3(\phi_R)\rangle = |001\rangle + e^{i\phi_R}|011\rangle + |100\rangle + e^{i\phi_R}|110\rangle.$$
 (6.0.6)

The relative phase between pairs of basis states in this superposition leads to a Fourier transform that depends on ϕ_R . The measured probabilities of the eight output states are plotted in Fig. 4a along with the theoretical values in Fig. 4b. The level of agreement can be seen in Fig. 4c, a plot of the SSO as a function of preparation phase.

These results demonstrate that for small state-spaces, the QFT can be performed

semiclassically with a signal-to-noise level sufficient for period-finding in quantum algorithms by means of a system of trapped-ion qubits. Even with input state infidelities as large as 0.10, as in the period 3 state created here, the measured QFT had substantial SSO with the theoretical prediction for the correct input state. Furthermore, the effect of the incommensurability of state periodicity with state space is diminished as the size of the state space increases. Peaks due to similar incommensurate periodicities will be easier to locate in larger state spaces (compared to the case of a period 3 state in an eight-state space). Extension of the technique described here to larger quantum registers [Wineland 98, Kielpinski 02] is a function only of trap-array size and involves a linear overhead in ion separation and movement. The main source of intrinsic error in our implementation was qubit dephasing resulting from magnetic-field fluctuations. Use of first-order magnetic-field-independent qubit transitions [Wineland 98] can mitigate this problem and lead to a high-fidelity method for implementation of the QFT, a necessary step toward large-number-factorization applications of quantum computing.

Chapter 7

Conclusion

This thesis work investigated new ways of building ion traps for use in quantum information applications. Several traps made of boron doped silicon were demonstrated with ion-electrode separations down to 40 μ m. Improvements in trap fabrication and testing reduced the time from concept to trapping by an order of magnitude compared to previous demonstrations. In my traps upper bounds on ion heating rates were determined; however, heating due to externally injected noise could not be completely ruled out. Noise on the RF potential responsible for providing confinement was identified as one source of injected noise.

Future directions for this work include further studies of the sources of ion heating. A next step for boron doped traps is to positively identify sources of injected noise, with special attention to the possible role of sideband noise on the trap RF potential source. In addition, systematic investigation of ion heating as a function of trap temperature [Labaziewicz 08], electrode metal type and electrode surface preparation is needed. Trapping with ion-electrode separations as small as 10 μ m is interesting not just for QIP purposes, but also because ions are sensitive probes of near near field electric and magnetic fields [Maiwald 08]. In several surface electrode traps it is observed that in the absence of laser cooling ions depart from the trap more quickly than can be accounted for by background collisions. This may be due to parametric heating or inelastic collisions with the trap ponderomotive confining potential. For scaling to the number of

trapping zones needed for large-scale QIP, integration with CMOS electronics, MEMS optics and optical fibers may be fruitful.

Using the microfabrication technology developed for ion traps, I made a cantilevered micromechanical oscillator and with coworkers demonstrated a method to reduce the kinetic energy of its lowest order mechanical mode via its capacitive coupling to a driven RF resonant circuit. Cooling results from a RF capacitive force, which is phase shifted relative to the cantilever motion. The technique was demonstrated by cooling a 7 kHz fundamental mode from room temperature to 45 K. Ground state cooling of the mechanical modes of motion of harmonically trapped ions is routine; equivalent cooling of a macroscopic harmonic oscillator has not yet been demonstrated. Extension of this method to devices with higher motional frequencies in a cryogenic system, could enable ground state cooling and may prove simpler than related optical experiments.

I discussed an implementation of the semiclassical quantum Fourier transform (QFT) using three beryllium ion qubits. The QFT is a crucial step in a number of quantum algorithms including Shor's algorithm, a quantum approach to integer factorization which is exponentially faster than the fastest known classical factoring algorithm. This demonstration incorporated the key elements of a scalable ion-trap architecture for QIP. Future work could improve the fidelity of the QFT, by for example using magnetic field independent qubit transitions [Langer 05], and incorporate it as a subroutine in more complex algorithms. In order for it to be considered a true subroutine experimental control apparatus is needed which automates the many calibration steps involved in operating the QFT.

Chapter 8

Appendix

8.1 Mathieu equation of motion

If potential $V_0 \cos(\Omega_{RF}t) + V_{DC}$ is applied to the RF electrodes with the others grounded ($V_1 = V_2 = 0$), as in Figure 2.1 on page 8, the potential near the geometric center of the trap takes the form

$$\Phi \approx \frac{1}{2} \left(V_0 \cos(\Omega_{RF} t) + V_{DC} \right) \left(1 + \frac{x^2 - y^2}{R^2} \right),$$
(8.1.1)

where R is a distance scale that is approximately the distance from the trap center to the surface of the electrodes [Wineland 98].

The classical solutions to the equations of motion for a particle of mass m and charge q for the potential in Equation 8.1.1 were first solved by Paul, Osbergahaus, and Fischer [Paul 58]. Here, only the x-direction will be solved since the solutions are decoupled in the spatial coordinates. The x coordinate equation of motion is

$$\ddot{x} = -\frac{q}{m}\frac{\partial\Phi}{\partial x} = -\frac{q}{m}\left(V_0\cos(\Omega_{\rm RF}t) + V_{\rm DC}\right)\frac{x}{R^2}.$$
(8.1.2)

With the following substitutions,

$$\xi = \frac{\Omega_{RF}t}{2}, a_x = \frac{4qV_{DC}}{m\Omega_{RF}^2R^2}, q_x = \frac{2qV_0}{m\Omega_{RF}^2R^2}, \tag{8.1.3}$$

the equation of motion can be cast in the form of the Mathieu differential equation,

$$\ddot{x} + [a_x - 2q_x \cos(2\xi)] x = 0. \tag{8.1.4}$$

The solution to this equation to first order in a_x and second order in q_x is [Ghosh 95],

$$u_x(t) = A_x \{\cos(\omega_x + \phi_x) \left[1 + \frac{q_x}{2} \cos(\Omega_{RF}t) + \frac{q_x^2}{32} \cos(2\Omega_{RF}) \right]$$
 (8.1.5)

$$+ \beta_x \frac{q_x}{2} \sin(\omega_x t + \phi_x) \sin(\Omega_{RF} t) \}, \qquad (8.1.6)$$

where A_x depends on initial conditions, $\omega_x = \beta_x \frac{\Omega_{\text{RF}}}{2}$ and $\beta_x \sim \sqrt{a_x + q_x^2/2}$. The oscillation at ω_x is called **secular motion** while that at Ω_{RF} and $2\Omega_{\text{RF}}$ is called **micromotion**. When $a_x << q_x^2 << 1$ we can ignore the micromotion terms and the ion behaves as if it were trapped radially by a harmonic potential Φ_{pp} called the **pseudopotential**,

$$q\Phi_{pp} = \frac{1}{2}m\omega_x^2 x^2 \tag{8.1.7}$$

where $\omega_x = \frac{qV_0}{\sqrt{2}\Omega_{\rm RF}mR^2} = \frac{q_x\Omega_{\rm RF}}{2\sqrt{2}}$ is the radial secular frequency.

A quantum-mechanical solution to the problem is possible [Glauber 92, Leibfried 03a] and it is found to match the classical one for the range of parameters commonly encountered in my experiments.

Books on ion trapping include those by Gosh [Ghosh 95] and Major, et al. [Major 05]. There is a review by Paul [Paul 90] and a study of the effects of higher order terms in the trapping potential by Home and Steane [Home 06a].

8.2 Micromotion

This section discusses in more detail micromotion, which was introduced in Section 2.3.2 on page 15.

The first-order solution to the Mathieu equation (see Section 8.1 on the previous page) in the limit of small trap parameters ($|q_i| \ll 1$ and $|a_i| \ll 1$) is

$$u_i(t) \approx u_{1i} \cos(\omega_i t) \left(1 + \frac{q_i}{2} \cos(\Omega_{RF} t)\right)$$

where $\omega_i \cong \frac{1}{2}\Omega_{RF}\sqrt{a_i + \frac{1}{2}q_i^2}$, $i \in \{x,y,z\}$. The secular harmonic motion $u_i(t)$ is at frequency ω_i with amplitude u_{1i} . This motion carries the ion back and forth thru the RF

pseudopotential minimum. The coherently driven motion at Ω_{RF} is called **micromotion**. It can't be cooled since it's driven motion but it's amplitude can be minimized by reducing the secular amplitude u_{1i} , that is cooling the i^{th} mode at ω_i . Intrinsic micromotion also arises from a nonzero phase difference ϕ_{RF} between the potentials applied to the RF trap electrodes. This can happen due to a path length difference leading to the electrodes or differential coupling to their environment.

Additional micromotion can arise if the ion's mean position doesn't lie at a zero in the pseudopotential. This can happen if a static electric field E_{DC} pushes the ion radially off axis. The resulting motion is called excess micromotion can can be nulled by applying a compensating field. The ion position along the x (or y) radial direction may be calculated [Berkeland 98],

$$u_x(t) \cong (u_{0x} + u_{1x}\cos(\omega_x t)) \left(1 + \frac{1}{2}q_x\cos(\Omega_T)\right) - \frac{1}{4}q_x R\alpha\phi_{ac}\sin(\Omega_T t).$$

The x motion due to $m{E}_{\mathrm{DC}}$ is has amplitude

$$u_{0x} \cong \frac{4Q\mathbf{E}_{\mathrm{DC}} \cdot \hat{u_x}}{m\omega_x^2}.$$

Excess micromotion disappears when $\mathbf{E}_{DC} = 0$. $\mathbf{E}_{DC} = 0$ can achieved by applying feedback to the trap control electrode potentials, pushing the ion back to the pseudopotential minimum. Axial RF fields can result from asymmetric trap geometries like tapers or gaps between electrodes. Careful simulation can minimize these fields in trap regions where it may be problematic.

Micromotion can also result when there is a phase difference between the RF potentials applied to the trap RF electrodes. This is discussed in Section 3.5.2 on page 64.

effects of micromotion Micromotion causes a first-order Doppler shift which can alter the fluorescence spectrum of an ion. This can result in suppressed fluores-

cence during state readout, decressed Doppler cooling efficiency and ion heating from the Doppler cooling laser beam. Micromotion may lead to ion heating if there is noise on the RF potential at a motional difference frequency (see 8.3 on page 174) [DeVoe 89]. Other effects include a second-order Doppler shift and an AC Stark shift. Micromotion energy can be parametrically exchanged between secular modes (see [Wineland 98] [Hunt 08] 4.1.5). Minimization of excess micromotion is therefore desirable.

8.2.1 Micromotion detection

There are a variety of approaches to detect the presence of micromotion. One technique is amplitude modulation of the trap RF drive at a secular difference frequency $\Omega_{\rm RF} \pm \omega_i$, see Section 8.3 on page 174. This approach can be used to null the 3D micromotion. Another approach is measurement of the ion fluorescence spectrum vs the detuning of the Doppler cooling laser. Finally, a time-resolved fluorescence measurement correlated with the ac drive produces a signal indicative of micromotion [Berkeland 98]. The latter two approaches only provide information about micromotion along the direction of the cooling laser.

micromotion detection by Doppler fluorescence

A straight forward means of measuring ion micromotion is observing the fluorescence spectrum from the ion as the frequency of the Doppler cooling laser is varied. An ion with excess micromotion of amplitude u' experiences a modulated laser field. For a laser of frequency ω_{laser} , amplitude E_0 and wave vector k,

$$E(t) = E_0 \exp^{i\mathbf{k}\cdot\mathbf{u} - i\omega_{laser}t}$$

$$\cong E_0 \exp^{i\mathbf{k}\cdot(\mathbf{u_0} + \mathbf{u'}) - i\omega_{laser}t}.$$

It is assumed that the micromotion amplitude is small relative to the secular amplitude. The modulation amplitude is

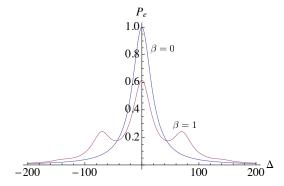


Figure 8.1: Plot of normalized ion fluorescence vs cooling laser detuning. $\Omega_{\rm RF}/2\pi=71\,$ MHz, $\gamma=40\,$ MHz and $\beta=0,1.$ Note that for $\beta=1$ there is a drop in carrier fluorescence and sidebands appear at $\Delta=\pm n\,\Omega_{\rm RF}$ for $n\in 0,1,2,\ldots$ If $\beta>0$ there is micromotion along the direction of the beam.

$$\mathbf{k} \cdot \mathbf{u}' = \beta \cos \left(\Omega_{\mathrm{RF}} t\right)$$

where the modulation index β is

$$\beta = \frac{1}{2} \sum_{i=x,y} k_i u_{0i} q_i.$$

Let ρ_{22} be the excited state population of the cooling transition. Let E_0 be the amplitude of the micromotion modulated laser electric field at the ion. ρ_{22} can be calculated the low intensity limit using the steady-state solutions of the optical Bloch equation

$$\rho_{22} = \left(\frac{\mu E_0}{2\hbar}\right)^2 \sum_{n=-\infty}^{\infty} \frac{J_n^2(\beta)}{(\Delta + n\Omega_T)^2 + \left(\frac{1}{2}\gamma\right)^2},$$

where $\Delta = \omega_{atom} - \omega_{laser}$, γ is the transition line width and $J_n^2(\beta)$ are n^{th} order Bessel functions and μ is the transition electric dipole moment. γ ρ_{22} is the ion fluorescence rate [Allen 75, DeVoe 89].

Micromotion is considered significant when it impacts ion fluorescence. Consider for example the case where the amplitude of the carrier and first micromotion sideband are equal. That is, $\frac{J_0^2(\beta)}{J_1^2(\beta)} = 1$ which happens at $\beta = 1.43$.

In practice ion micromotion is minimized by tuning the cooling laser so that $\Delta = -n\Omega_{RF}$ for $n \in \{1, 2, 3, ...\}$ and minimizing the observed ion fluorescence.

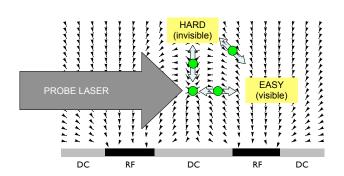


Figure 8.2: Drawing showing electric field vectors for a symmetric 5-wire surface-electrode trap. The ion's micromotion motion lies along the field lines at the ion's position. The probe laser propagating parallel to the surface is sensitive only to the micromotion resulting from horizontal displacements of the ion from the RF null.

In a 3D Paul trap with an open geometry it is possible to direct three laser beams at an ion at large relative angles thereby spanning 3-space. Each laser is then sensitive to motion along it's direction of propagation and full 3D nulling is possible.

Surface electrode traps pose special challenges for micromotion nulling due to their planar geometry. In demonstrated microscale surface electrode ion traps the ion lies about 40 μ m above the surface and photons are collected from overhead. In such traps it is not practical to use a vertical beam because light scattered off the surface can enter the camera. Vertical micromotion therefore can't be detected in this fashion and other techniques must be used [Berkeland 98].

8.3 Ion heating due to noisy RF potentials

This section discusses a way in which noise on the trap RF potential can couple to ion motion and cause heating \dot{n} [Wineland 98]. The heating rate for a secular mode of frequency ω_z due to force noise at $\omega_n = \omega_z$ is related to the force noise spectral density $S_{F_n}(\omega)$ by,

$$\dot{\bar{n}}(\omega_z) = \frac{S_{F_n}(\omega_z)}{4m\hbar\omega_z},\tag{8.3.1}$$

in quanta/second [Turchette 00] 1 .

8.3.1 Ion motion in an oscillating electric field

This section starts with a derivation of the equation of motion for a charged particle in a sinusoidally oscillating electric field. For simplicity, all calculations are one-dimensional.

First, consider the motion of an ion of mass m and charge q in a homogeneous RF electric field. Such a field is found inside a parallel plate capacitor of separation d as in Figure 8.3 on the next page. Let \bar{z} be the initial position of the ion. The ion's equation of motion is,

$$m\ddot{z} = F_z = qE_0(\bar{z})\cos(\Omega_{\rm RF}t),\tag{8.3.3}$$

where $E_0(\bar{z}) = V_0/d$.

The resulting ion motion is,

$$z(t) = \bar{z} + \xi(t) \tag{8.3.4}$$

$$\xi(t) = \xi_0 \cos(\Omega_{\rm RF} t)$$
, where $\xi_0 = -\frac{q E_0(\bar{z})}{m \Omega_{\rm RF}^2}$, (8.3.5)

$$S_{F_n}(\omega) \equiv 2 \int_{-\infty}^{\infty} \exp^{i\omega\tau} \langle F(t)F(t+\tau) \rangle d\tau$$
 (8.3.2)

is the spectral density of force fluctuations in units of N^2Hz^{-1} .

1

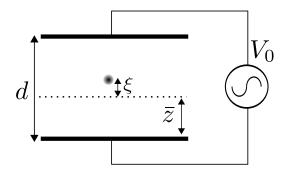


Figure 8.3: Ion in a homogeneous RF electric field of amplitude V_0/d from a parallel plate capacitor. The guiding center for the ion's motion is \bar{z} with micromotion excursions of amplitude ξ . Homogeneity of the electric field requires that the capacitor lateral dimensions be much larger than d.

where the ion's initial position \bar{z} is assumed to be constant about which there is small micromotion $\xi(t)$ (of amplitude ξ_0) at frequency Ω_{RF} . The time average of the force on the ion due to the homogeneous electric field is,

$$\langle F_z(t) \rangle = 0. \tag{8.3.6}$$

Suppose the electric field acquires a spatial dependence $E_0'(z)$, but with the same value at \bar{z} : $E_0'(\bar{z}) = E_0(\bar{z})$ [Dehmelt 67]. I will show that this inhomogeneity in the electric field gives a finite time-average force in the direction of weaker RF field. This new field perturbs ion motion (now $z(t) = \bar{z} + \xi'(t)$) and the force acting on it (now $F_z'(t)$),

$$m\ddot{z} = F_z' = qE_0'(z)\cos(\Omega_{\rm RF}t) \tag{8.3.7}$$

$$\xi'(t) = \xi_0 \cos(\Omega_{\rm RF} t)$$
, where $\xi_0 = -\frac{q E_0'(\bar{z})}{m \Omega_{\rm RF}^2}$. (8.3.8)

Expanding the field about position \bar{z} ,

$$E'_{0}(z) = E'_{0}(\bar{z}) + \frac{\partial E'_{0}(\bar{z})}{\partial z}(z - \bar{z}) + \dots, \tag{8.3.9}$$

where $z - \bar{z} = \xi'$. Assume that the inhomogeneity is small,

$$\left| E_0'(\bar{z}) \right| >> \left| \frac{\partial E_0'(\bar{z})}{\partial z} \right| \xi_0.$$
 (8.3.10)

The time average of the new force F'(z) is,

$$\langle F'(z) \rangle = \langle q E'_0(\bar{z}) \cos(\Omega_{RF} t) \rangle + \langle q \frac{\partial E'_0(\bar{z})}{\partial z} \xi' \cos(\Omega_{RF} t) \rangle$$
 (8.3.11)

(to good approximation, assume
$$\xi' = \xi$$
 [Dehmelt 67]) (8.3.12)

$$\cong -\left\langle q \frac{\partial E_0'(\bar{z})}{\partial z} \xi_0 \cos^2(\Omega_{RF} t) \right\rangle \tag{8.3.13}$$

$$= -\frac{q}{2}\xi_0 \frac{\partial E_0'(\bar{z})}{\partial z} \tag{8.3.14}$$

$$= -\frac{q^2}{2m\Omega_{\rm RF}^2} E_0'(\bar{z}) \frac{\partial}{\partial z} E_0'(\bar{z})$$
(8.3.15)

$$= -\frac{q^2}{4m\Omega_{\rm RF}^2} \frac{\partial}{\partial z} E_0^{\prime 2}(\bar{z}). \tag{8.3.16}$$

The force always points in the direction of weaker RF fields independent of the sign of the ion charge.

8.3.2 RF electric field noise and associated force noise

Suppose the electric field has a small noise term at $\Omega_{RF} + \omega_n$. The noise is a perturbation to the drive at Ω_{RF} ,

$$E(z,t) = E_0(z) \left[\cos(\Omega_{RF}t) + \alpha \cos(\Omega_{RF} + \omega_n) t \right], \qquad (8.3.17)$$

where $\Omega_{RF} >> \omega_n$ and $\alpha << 1$. Following similar steps as those leading to Equation 8.3.16 for the resulting force noise,

$$\langle F(z) \rangle = -\frac{q^2}{4m\Omega_{\rm DE}^2} \frac{\partial}{\partial z} \left\langle E^2(z,t) \right\rangle. \tag{8.3.18}$$

Calculating $\langle E^2(z,t) \rangle$ over period $\tau = 2\pi/\Omega_{\rm RF},$

$$\langle E(z,t)^2 \rangle = E_0^2(z) \left\langle \left[\cos(\Omega_{RF}t) + \alpha \cos(\Omega_{RF} + \omega_n) t \right]^2 \right\rangle$$
 (8.3.19)

$$= E_0^2(z) \left\langle \cos^2(\Omega_{RF} t) \right\rangle + E_0^2(z) \alpha^2 \left\langle \cos^2(\Omega_{RF} + \omega_n) t \right\rangle$$
 (8.3.20)

$$+2E_0^2(z)\alpha \left\langle \cos(\Omega_{\rm RF} + \omega_n)t \times \cos(\Omega_{\rm RF}t) \right\rangle] \tag{8.3.21}$$

$$\cong \frac{1}{2} E_0^2(z) \left[1 + 2\alpha \left\langle \cos(2\Omega_{RF} + \omega_n) t \right\rangle + 2\alpha \left\langle \cos(\omega_n t) \right\rangle \right] \tag{8.3.22}$$

$$= \frac{1}{2} E_0^2(z) \left[1 + 2\alpha \cos(\omega_n t) \right], \tag{8.3.23}$$

where a noise term in the force equation at ω_n has emerged from the cross term. The time-average force (Equation 8.3.16 on the previous page) over period τ depends on $\langle E_0(z,t)^2 \rangle$. The force noise is then

$$F_z(z) = \frac{q^2}{m\Omega_{RF}^2} E_0(z) \frac{\partial E_0(z)}{\partial z} \times \frac{E_n(\omega_n)}{E_0(z)}, \qquad (8.3.24)$$

where $E_n = \alpha E_0(z) \cos(\omega_n t)$. Noise is often expressed in terms of a spectral density function.

$$S_{F_n}(\omega_n) = \left[\frac{q^2}{m\Omega_{RF}^2} E_0(z) \frac{\partial E_0(z)}{\partial z}\right]^2 \times \frac{S_{E_n}(\omega_n)}{E_0^2(z)}.$$
 (8.3.25)

Note that $S_{V_n}/V_0^2 = S_{E_n}/E_0^2$ can be measured on a spectrum analyzer.

8.3.3 Motional heating due to RF electric field noise

axial heating Consider an ion trapped in a potential with an axial trapping frequency of ω_z . Suppose there is a time-varying RF field at $\Omega_{\rm RF}$ along the axial direction with noise at $\Omega_{\rm RF} + \omega_n$ as in Equation 8.3.17 on the preceding page. This gives rise to force noise which causes ion heating. Using Equation 8.3.1 on page 174, [Turchette 00],

$$\dot{\bar{n}}(\omega_z) = \frac{1}{4m\hbar\omega_z} \times \left[\frac{q^2}{m\Omega_{\rm DE}^2} E_0(z) \frac{\partial E_0(z)}{\partial z} \right]^2 \frac{S_{E_n}(\omega_z)}{E_0^2(z)},\tag{8.3.26}$$

in quanta/second.

Therefore, noise at $\Omega_{RF} + \omega_z$ can cause axial heating if there is a nonzero gradient to the RF electric field along the trap axis.

radial heating Consider now a specific spatial dependence of the electric field. In the radial direction near the trap axis, the electric potential is given by

$$\phi(x, y, t) \cong \frac{1}{2} V_0 \cos(\Omega_{RF} t) \left(1 + \frac{x^2 - y^2}{R^2} \right),$$
 (8.3.27)

where R is determined by the electrode geometry. The electric field in the x direction

due to ϕ is,

$$E(x,t) = -\frac{\partial}{\partial_x}\phi(x,t) \tag{8.3.28}$$

$$= E_0(x) \times \cos(\Omega_{RF}t), \text{ where } E_0(x) = -V_0 \frac{x}{R^2}.$$
 (8.3.29)

Assume that the time variation of $E_0(x)$ is small over $\tau = 2\pi/\Omega_{\rm RF}$. That is, $E_0(x,t) \cong E_0(x,t+\tau)$. Noticing that the force on an ion from this field is harmonic with frequency ω_x , $E_0(x)$ can be rewritten as follows ²,

$$E_0(x) = -\sqrt{2} \frac{m\Omega_{\rm RF}\omega_x}{q} x. \tag{8.3.33}$$

Suppose there is noise on the RF at $\Omega_{RF} + \omega_n$ as in Equation 8.3.17 on page 176. This gives rise to force noise which causes ion heating. Using Equations 8.3.1 on page 174 and 8.3.25 on the preceding page,

$$\dot{\bar{n}}(\omega_x) = \frac{1}{4m\hbar\omega_x} \times \left[2m\omega_x^2 x\right]^2 \frac{S_{E_n}(\omega_x)}{E_0^2(x)} \tag{8.3.34}$$

in quanta/second.

Therefore, noise at $\Omega_{RF} + \omega_x$ can cause radial heating if there is a stray electric field displaces the mean position of the ion to position x. If the ion lies at x = 0 there is no heating due to this mechanism.

8.4 Secular frequency measurement

I used several techniques to measure the axial and radial potential curvatures in my traps. The corresponding experimental parameter is the secular oscillation frequencies

$$\langle F_x(x) \rangle = -\frac{q^2}{4m\Omega_{RF}^2} \frac{\partial}{\partial x} \langle E_0(x)^2 \rangle$$
(8.3.30)

$$= -\frac{q^2 V_0^2}{2m\Omega_{\rm RF}^2 R^4} \times x \tag{8.3.31}$$

$$= -m\omega_x^2 \times x,\tag{8.3.32}$$

the equation of motion for harmonic motion of mass at frequency $\omega_x = \frac{qV_0}{\sqrt{2}m\Omega_{\rm RF}R^2}$. For this potential there is slow harmonic motion at ω_x with superimposed, low amplitude harmonic motion at $\Omega_{\rm RF}$ (see Mathieu equation solution, Section 8.1 on page 168). This holds only when $\omega_x << \Omega_{\rm RF}$.

² Equation 8.3.29 is of the form of 8.3.7 on page 175 and so the time-average force is given by 8.3.16 on page 176. For this potential, over period τ ,

of an ion.

endcap tickle Due to the Doppler effect, an ion's fluorescence can change if a secular mode is heated. An electric field oscillating at an ion's secular mode frequency (and with a component along that principle axis) causes heating. This causes a Doppler shift of the Doppler cooling laser beam and can cause a change in ion fluorescence. This resonance effect can be used to measure an ion's secular frequencies.

For example, the axial oscillation frequency $\omega_z/2\pi$ was measured experimentally by adding an oscillating potential at frequency ω to an endcap electrode's static potential (e.g. any one of the electrodes marked V_1 in Figure 2.1 on page 8).

$$V_{\rm endcap} = V_{\rm dc}(1 + \epsilon \cos(\omega t))$$

Ion fluorescence was observed while sweeping ω . When $\omega = \omega_z$, the ion(s)'s motion is excited and the observed fluorescence decreases (see Section 8.2.1 on page 171). Radial secular modes can be measured by tickling using an electrode at the center of a trap zone.

Sample data are in Figure 8.4 on the next page for a sweep of ω in search of the radial secular frequencies in trap dv16m.

RF amplitude modulation

Due to the Doppler effect, an ion's fluoresence can change if a secular mode is heated. In this case intentional heating can be caused if the ion has excess micromotion and the RF drive is amplitude modulated (RF AM) at a secular difference frequencies $\Omega_{\rm RF} \pm n\omega$. This can be used to measure the frequency of the secular modes. This phenomena is discussed in more detail in Section 8.3 on page 174.

The experimental apparatus used to apply RF AM is drawn in Figure 8.5 on page 181. The trap drive RF at Ω_{RF} was amplitude modulated by a spectrally broadened, dense noise source centered at ω . The AM was accomplished using an RF mixer fed

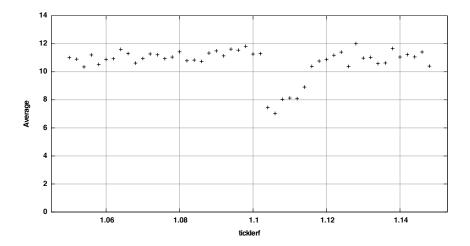


Figure 8.4: Plot showing the axial secular mode identified by the control electrode tickle technique. Each point in the plot is an average of about 100 experiments. Each experiment consisted of applying an oscillating potential to an endcap control electrode and counting the number of photons observed on the PMT in a 400 μ s interval. The laser beam was continuously applied to the ion for these experiments. The vertical axis is the average photon number. A drop in ion fluorescence is observed at the secular frequency $\omega_z/2\pi \cong 1.11$ MHz.

by a DC biased noise source. The noise source started as a continuous wave source centered at ω_{motion} which was then frequency modulated by white noise generated by a SRS DS345. A 100 kHz FM modulation depth was used. The DC bias was a heavily filtered ($\tau_{RC} \sim 100$ ms) power supply.

Sample data are in Figure 8.6 on the following page for a sweep of ω in search of the axial secular frequency for a single ion in trap dv16m.

Another, simpler appratus that also worked was use of a directional coupler to add noise power directly at $\Omega_{\rm RF} \pm n\omega$.

ion spacing The axial secular frequency $\omega_z/2\pi$ can be estimated by observing the inter ion spacing for a linear crystal. The frequency follows assuming equilibrium

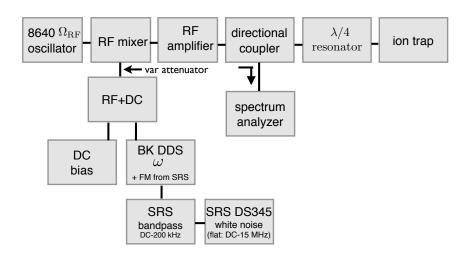


Figure 8.5: Schematic of RF electronics used for the RF AM tickle. The 8640 is a Hewlett Packard cavity oscillator. The BK DDS is a BK Precision direct digital synthesizer. SRS is Stanford Research Systems.

between the ions' mutual Coulomb repulsion and the restoring force of the axial trapping field. This follows assuming equilibrium between the ions' mutual Coulomb repulsion

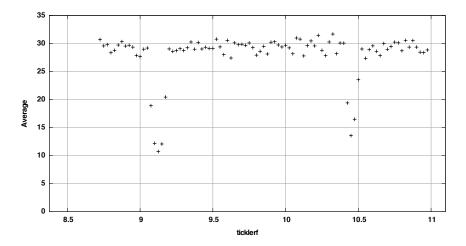


Figure 8.6: Plot showing radial secular modes identified by RF AM. Each point in the plot is an average of about 100 experiments. Each experiment consisted of applying AM to the trap drive RF and counting the number of photons observed on the PMT in a 400 μ s interval. The laser beam was continuously applied to the ion for these experiments. The vertical axis is the average photon number. A drop in ion fluorescence is observed at the two secular frequencies $\omega_x/2\pi \cong 9.2$ MHz and $\omega_y/2\pi \cong 10.45$ MHz.

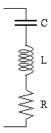


Figure 8.7: Series RLC circuit.

and the restoring force of the axial trapping field. For a three ion crystal with inter-ion spacing s_3 , $\omega_z = \frac{q}{2} \left(\pi \epsilon_0 m s^3\right)^{-1/2}$ where $s_3 = (5/4)^{1/3} s$ [Wineland 98]. In some traps this measurement was made for a three-ion crystal to determine $\omega_z/2\pi$.

8.5 RF cavity coupling

In ion trap systems we want to communicate maximum power to the $\lambda/4$ resonator which generates the RF trapping potential. Under what condition does this happen?

coupling to a series RLC load. Consider the case where the load is a series RLC oscillator. Such a model can represent the distributed resistance, inductance and capacitance of a transmission line or tank resonator.

When the RLC is not coupled to an external circuit it's said to be **unloaded** and its resonant frequency ω_0 and unloaded Q_0 are related as

$$\omega_0 = 1/\sqrt{LC}$$

$$Q_0 = Z_L/R = \omega_0 \ L/R$$

$$Q_0 = Z_C/R = \frac{1}{\omega_0 C \ R}$$

In practice it may not be possible to directly measure these circuit parameters if they are distributed as in a transmission line. Also, we must be aware of how the measurement apparatus couples to the circuit and modifies its quality factor and resonant frequency. Such an apparatus is said to **load** the resonator.

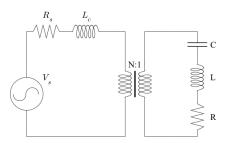


Figure 8.8: Lumped circuit representation of cavity impedance matching. The cavity is modeled as a series RLC oscillator inductively coupled to a source with resistance R_s by an ideal N-turn transformer with a series inductance L_c .

To couple maximum power to the resonator, its on resonance impedance R must equal the transformed source impedance. Figure 8.8 is circuit showing a RLC inductively coupled to a source with output impedance R_s by a N-turn ideal transformer with series inductance L_c .

Following Liao, a simplified equivalent circuit is drawn in Figure 8.9 [Liao 80]. As seen by the RLC, the transformed source impedance is now reactive N^2 ($i\omega L_c + R_s$) and its voltage is NV_s , where N is the transformer turns ratio. When the coupling impedance N^2L_c is small compared to L, the Q factor is shifted.

$$Q_0 = Z_L / R$$
$$= \omega_0 L / R$$

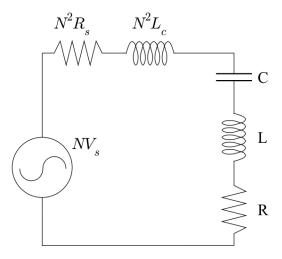


Figure 8.9: Simplified lumped circuit representation of cavity impedance matching.

to

$$Q_L = \frac{\omega_0 L}{R + N^2 R_s}$$
$$= \frac{1}{1 + N^2 R_s / R},$$

where Q_L is called the **loaded Q**. It is assume that the resonant frequency shift due to the coupling is negligible. As in the coupled resistors example a coupling coefficient may be defined.

$$\kappa = \frac{N^2 R_s}{R}.$$

In terms of κ the loaded Q_L becomes

$$Q_L = \frac{Q_0}{1 + \kappa}.$$

how to measure Q_L When the source and load impedances in an RF circuit are perfectly matched ($\kappa = 1$), no power is reflected by the load and $Q_0 = 2 \ Q_L$.

The loaded Q_L may be determined by measuring the power reflected from the cavity with a directional coupler,

$$Q_L = \frac{\omega_0}{\Delta \omega},$$

where $\Delta\omega$ is the full width at half max. That is, $\Delta\omega = |\omega_1 - \omega_2|$ where ω_1 and ω_2 are the frequencies where the reflected power is half the maximum reflected power.

For more on microwave electronics see [Liao 80, Montgomery 48, Kajfez 99, Terman 43, Purington 30].

8.6 Time-resolved Doppler laser cooling .dc file

The detailed experiment evolution for the ion heating rate measurement technique discussed in Section 4.7is specified in the computer file below. The syntax is defined in Chris Langer's thesis [Langer 06].

```
- cool to Doppler limit
- reheat for heattime_in_ms in the dark
- trigger multichannel scaler to integrate
- detect ion for 50 us to see whether it is still around
MCS: pass length: 200
MCS: dwell time: 50us
*/
uvar interpn=10;
name det_pmt1_bd = pmt(1),bd;
name det_pmt2_bd = pmt(2),bd;
tvar heattime_in_ms = 11 dlb:11 dub:2000; //never below 3
fvar null=0 dlb:0 dub:1;
//// START PULSES /////
pulse bdd 10; //first pulse
//block to reset DDS 0 to 3 because they tend to conk out at random times
pulse wait minsetselt setsel(dds0);
pulse wait 10;
pulse wait minsetrft setfreq(313.0);
pulse wait 10;
pulse wait minsetselt setsel(dds1);
pulse wait 10;
pulse wait minsetrft setfreq(280);
pulse wait 10;
//initial cool of ion
pulse bdd 30e3;
//measurement into PMT 1 for monitoring ion. */
pulse det_pmt1_bd 400;
if(pmt(1) >= 3)
lbrace
//time delay for reheating (in ms)
pulse shutter_bd on;
```

```
pulse wait heattime_in_ms*1000-10001;
pulse shutter_bd off;
pulse wait 10000;
//trigger pulse for multichannel device
pulse exptrig 2.0; //Trigger, for programs/hardware that require it.
pulse mult_ch 2;
//extra multch_delay waittime after trigger
pulse wait 250;
//pulse with BD and RD to observe change in fluorescence on multichannel scaler
//dwell time = 50us; pass length=
pulse bd 20e3; //equal to MCS passlength*dwelltime
rbrace
if(pmt(1)<3)
lbrace
pulse bdd 100e3;
rbrace
pulse bdd 10;
The following file is prepended to the .dc file above. We use a graphical user interface to
adjust experiment parameters like the potential on control electrodes (as when nulling
micromotion). This file specifies the relationship between an experimental parameter
and a computer user interface element.
//Below are some macros for simplifying the waveform
//syntax. In particular it compartmentalizes explicitly
//defined waveforms listed in series in a .dc file and
//the automatic interpolation (if any) between them.
@include initial_defs.dch //type definitions
@include stdnames.dch //eg name shutter =5;
@include IonProperties_inc.dc
//NOTE: Files that include this file need to be passed thru GNU cpp
//c:\cygwin\bin\cpp.exe -x c -P -CC filename.dc filename_cpp.dc
//define a two point waveform for joining
wvfdef(interp) // Exactly two points only!
wvfend
//define some macros that properly implement waveforms
//AO should be the first in a series of waveforms
```

```
//B for subsquent waveforms
//A1 should be the last in a series of waveforms
//PWVF is the waveform name
//PINTERPPTS is the number of points to use to interpolate
//PARGS are whatever other arguments should be passed in the body of wvf()
//POFFSETS is a list of offsets to append
//Variables to control from pulser_ui
pvar dwell=500e3 dlb:500e3 dub:1e7;
pvar load_cennear=ip_load_cennear dlb:-5 dub:5;
pvar load_cenfar=ip_load_cenfar dlb:-2 dub:2;
pvar load_middle=ip_load_middle dlb:-1 dub:1;
pvar load_endcaps=ip_load_endcaps dlb:-1 dub:1;
pvar load_endcapsd=ip_load_endcapsd dlb:-1 dub:1;
pvar load_shimAll=ip_load_shimAll dlb:-1 dub:1;
pvar load_shimRadial=0 dlb:-1 dub:1;
//include as Ion Properties
pvar m370_97=ip_m370_97 dlb:-1 dub:1;
pvar m370_35=ip_m370_35 dlb:-1 dub:1; //-0.9
pvar m370_middle=ip_m370_middle dlb:-1 dub:1;
pvar m370_endcaps=ip_m370_endcaps dlb:-2 dub:2;
pvar m370B_97=ip_m370B_97 dlb:-1 dub:1;
pvar m370B_35=ip_m370B_35 dlb:-1 dub:1; //-0.9
pvar m370B_middle=ip_m370B_middle dlb:-1 dub:1;
pvar m370B_endcaps=ip_m370B_endcaps dlb:-2 dub:2;
pvar m370B_95=0 dlb:-1 dub:1;
pvar m370B_4=0 dlb:-1 dub:1;
pvar m370B_36=0 dlb:-1 dub:1;
pvar m370B_33=0 dlb:-1 dub:1;
pvar m370C_97=ip_m370C_97 dlb:-1 dub:1;
pvar m370C_35=ip_m370C_35 dlb:-1 dub:1; //-0.9
pvar m370C_middle=ip_m370C_middle dlb:-1 dub:1;
pvar m370C_endcaps=ip_m370C_endcaps dlb:-2 dub:2;
pvar p370_79=ip_p370_79 dlb:-1 dub:1;
pvar p370_41=ip_p370_41 dlb:-1 dub:1; //-0.9
pvar p370_p79m41=0 dlb:-1 dub:1;
pvar p370_middle=ip_p370_middle dlb:-1 dub:1;
pvar p370_endcaps=ip_p370_endcaps dlb:-2 dub:2;
pvar p370_endLnear=0 dlb:-1 dub:1;
pvar p370_endLfar=0 dlb:-1 dub:1;
pvar p370_endRnear=0 dlb:-1 dub:1;
pvar p370_endRfar=0 dlb:-1 dub:1;
pvar p370_vertPush=0 dlb:-1 dub:1;
pvar p370_twist=0 dlb:-2 dub:2;
//differential shim on endcaps to translate ion axially
```

pvar p370_endcapsDif=0 dlb:-1 dub:1; pvar shim_dac1=0 dlb:-5 dub:5;

8.7 Microfabrication Techniques

A variety of microfabrication tools were used to build the ion traps and cantilevers discussed in this thesis. The techniques of patterning and machining micro scale devices in materials like silicon fall under the umbrella of micro-electromechanical systems (MEMS). The NIST cleanroom is operated by the NIST Cryoelectronics Division which focuses on Josephson junction devices. Therefore, many common MEMS techniques were not routine in our facility (circa 2002) and had to be developed. They are discussed in this section. Techniques commonly exercised in the NIST cleanroom (and many other facilities) like photolithography are not discussed. The NIST Cryoelectronics and Ion Storage wikis are good resources for such details for NIST staff.

This section is written with the physics AMO community as the target audience but it is not meant to be comprehensive introduction to MEMS. For a good introduction to MEMS see Liu's Foundations of MEMS [Liu 06]. A handy reference on a wide variety of MEMS topics is Mandous Fundamentals of Microfabrication [Madou 02].

8.7.1 Silicon deep etch

Plasma etching of silicon permits high aspect ratio features with good repeatability and excellent mask selectivity. The NIST etcher utilizes a variant of the BOSCH etch process optimized for silicon deep etch (> $50\mu m$) [Larmer 92]. This process forms high aspect ratio features in silicon by interleaving etch and surface passivation steps. The etch step is a chemically active RF plasma (SF_6 and O_2) inductively coupled to the wafer surface. The charged component of the plasma is accelerated normal to the surface, enhancing its etch rate in the vertical direction. The passivation step (C_4F_8) coats all exposed surfaces including sidewalls with fluorocarbon polymer. Etch and passivation cycles (typically 12 and 8 seconds respectively) are balanced so that sidewalls are protected from over/under etching as material is removed thru the full wafer thickness.

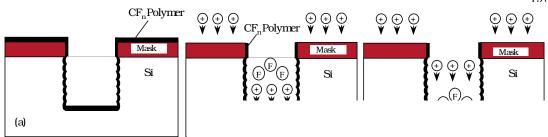


Figure 8.10: An illustration of the Bosch silicon deep etch mechanism. a) During passivation a fluorocarbon polymer uniformly coats all exposed surfaces. b) During etch the surfaces oriented normal to the plasma flux (vertical) degrade fastest. c) The sidewalls are protected. The figure is from [McAuley 01].

The cycled etching causes the sidewalls to have a microscopic scalloped appearance with an amplitude of 100-500 nm and a period of 200-1000 nm.

The details of the etch chemistry for the STS etcher are proprietary. However, the general topic of fluorine reactive ion etch is discussed in the literature [Flamm 90, Madou 02]. For anisotropic processes common etch gas combinations include CF_4/O_2 and SF_6/O_2 . Other chemistries are possible but these are popular in commercial systems due to the convenience and safety of the reactants and their selectivity of silicon over photoresist and silicon oxide.

Low pressure (<10 mTorr)³ and high ion density ($>10^{11} \text{ cm}^{-3}$) are best for silicon deep etch. In the STS the plasma is confined by an ac axial magnetic field at $\Omega=13.56$ MHz that causes an azimuthal electric field (from $dB/dt=\nabla\times B$), confining the plasma current (see Figure 8.13 on page 193 and [Bhardwaj 95]). Phase locked to axial field source is an ac bias voltage at Ω applied to the platen (wafer chuck) which independently controls the ion energy. A frequency of 13.56 MHz selected because of sanction as an industrial, scientific, and medical band by the FCC [Madou 02].

 $^{^3}$ 1 Torr is 133 Pa

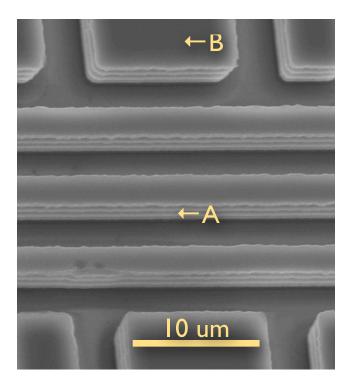


Figure 8.11: Micrograph showing scalloping along the edges of a 3 μm deep silicon etch performed on the NIST STS etcher. Arrow A points to sidewall scalloping due to process cycling. Arrow B points to the top wafer surface that was protected during etching by photoresist (removed for this micrograph). This etch was performed using recipe SPECB which is optimized for etches $> 200 \mu m$ deep. Somewhat smoother sidewalls can be obtained using recipe SPECA at the price of a slower etch rate.

See the National Telecommunications and Information Administration's United States Frequency Allocation Chart.

The primary etch mechanism for SF_6/O_2 is due to chemical reactions between

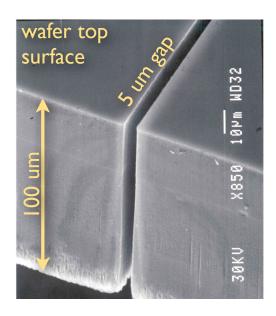


Figure 8.12: Micrograph of silicon etched by the NIST STS DRIE.

neutral atomic fluorine formed in the plasma and silicon at the surface. The fluorine is adsorbed by the surface before or during the chemical reaction. Ion bombardment can assist with the adsorption, reaction and ultimate evolution of SiF_4 as a gaseous product. The details are complex but occur roughly stepwise as follows.

etchant formation
$$e + F_2 \text{to} 2F + e$$
 (in plasma)
chemical reaction $Si + 4F$ to SiF_4 (at surface)

Oxygen acts to degrade the fluorocarbon polymer CF_x to form gaseous products.

$$O_2, O + CF_x$$
 to $COF_2, CO, CO_2 + F$

The gaseous products are pumped away and do not redeposit on the process wafer. Following a deep etch there may be residual fluorocarbon polymer on the wafer surface. Use of a short oxygen plasma cycle (DESCUM recipe, see below) appears to remove it.

As one of the first NIST users of the STS etcher (2002) I developed several nonstandard techniques that were new at NIST. These are documented in the following sections.

8.7.1.1 deep etch $(>50\mu m)$

STS etch patterns are defined by photolithography of a mask layer. Typically, this mask is 1 μm thick Shipley 510L-A photoresist. The selectivity of a mask is the rate at which it is degraded relative to the desired etch process. For the 3 $\mu m/\text{min}$ silicon etch recipe SPECB, 510L-A has a selectivity of 1:35. Very deep etches require higher selectivity and a thicker mask. Alternatives include silicon oxide (1:100) and silicon nitride (1:75-125), but using standard growth techniques low pressure chemical vapor

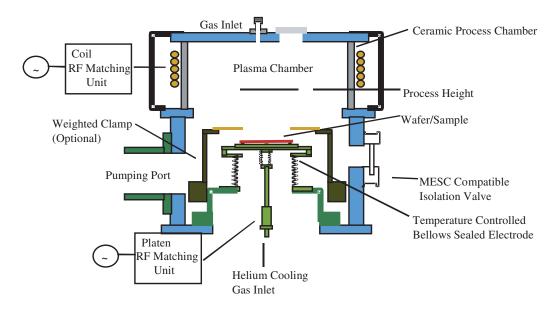


Figure 8.13: STS silicon deep etch tool schematic. The figure is from [McAuley 01].

deposition (LPCVD⁴) and thermal oxidation ([wiki 08, Tystar 08]) films thicker than 2 μm are impractical. Moreover, dielectric mask patterning requires additional etch steps.

⁴ LPCVD: low pressure chemical vapor deposition

	a se	Gas Clork	Coil Power	Platen Power
\mathbf{Recipe}	exer	Cyde	Cox	G. Jos
SPECA	etch	$130 \text{ sccm } SF_6$	600 W	600 W
		and 13 sccm O_2		
	passivation	$120 \text{ sccm } C_4 F_8$	12 W	0W
SPECB	etch	$130 \text{ sccm } SF_6$	600 W	$12 \mathrm{W}$
		and 13 sccm O_2		
	passivation	$85 \text{ sccm } F_4F_8$	600 W	0 W
DESCUM	etch	$6 \text{ sccm } SF_6$	0 W	0 W

Table 8.1: STS etcher recipe details. In all several dozen parameters fully specify this recipe. They are proprietary to STS but provided to owners of STS etch systems. SPECA: This recipe produces smoother sidewalls than SPECB and is appropriate for etches $<50~\mu m$ in depth. The etch rate is about 1.5 $\mu m/\text{min}$. SPECB: This recipe is appropriate for etches $>200~\mu m$ in depth. The etch rate is about 3 $\mu m/\text{min}$. sccm: standard cubic centimeter per minute, but there is little agreement as to what constitutes standard temperature and pressure (STP) (see Wikipedia)

It was found that for deep etches (> $50\mu m$) Shipley SPR-220 photoresist applied in $3\mu m$ or $7\mu m$ films and cured at elevated temperatures provides greater selectivity to the STS etch (1:75).

$3 \mu m$ SPR-220 recipe ($< 200 \mu m$ deep etches)

- (1) clean: on spinner rinse with acetone then isopropanol
- (2) prime with HMDS then spin (4 krpm, 35 sec) ⁵
- (3) apply photoresist: SPR-220 3.0 μm on wafer with dropper
- (4) spin (3.0 krpm 40 sec, yields 3 μm)
- (5) prebake: 90° C 60 sec, 115° C 60 sec (hot plate)
- (6) expose photoresist: 2:00 min
- (7) NIST Karl Suss exposure tool parameters: no UV300, soda lime mask, CH2, 300 mW
- (8) hold wafer in air for 10 min
- (9) post exposure bake: 90 sec on 115° C hot plate
- (10) develop with Solitec: 40-60 sec, 45 rpm (also use low rpm for spin dry)
- (11) inspect
- (12) harden: 110° C 30 min (Blue M oven)

7 μm SPR-220 recipe (<500 μm deep etches)

- (1) clean: on spinner rinse with acetone then isopropanol
- (2) prime with HMDS then spin (4 krpm, 35 sec)
- (3) apply photoresist: SPR-220 7.0 μm on wafer with dropper
- (4) spin (3.5 krpm 35sec -> yields 7.0 μm)
- (5) prebake: 90° C 100 sec, 110° C 100 sec (hot plate)
- (6) expose photoresist: 2:30 min
- (7) NIST Karl Suss exposure tool parameters: no UV300, soda lime mask, CH2, 300 mW

⁵ Hexamethyldisilazane (HMDS) is a photoresist-silicon adhesion promoter [Wikipedia 08].

- (8) hold wafer in air for 30 min
- (9) develop with Solitec: 120-180 sec, 45 rpm (also use low rpm for spin dry)
- (10) inspect
- (11) bake: 90 min at $80^{\circ} 90^{\circ}$ C (BlueM oven)
- (12) bake: 30 min at 110° C (BlueM oven; skip if not doing deep etch or if rounded edges are not desired)

Process tips for SPR-220.

- Store unused photoresist in a refrigerator.
- Only spin photoresist that has warmed to room temperature.
- Note that in SPR-200 the chemical process initiated by exposure to UV light requires water to come to completion (see product data sheet). This is the reason to leave the wafer exposed to air at room temperature prior to the post exposure bake.

8.7.1.2 thin wafer etching

Etching a wafer $< 500 \ \mu m$ thick requires care. Inside the STS etcher the process wafer sits atop a pedestal in the plasma stream (see Figure 8.13 on page 193). Chilled helium gas flowed across the backside of the wafer to control its temperature during etching. The helium gas is excluded from the process environment by a Viton o-ring seal on a stage beneath the wafer. The seal integrity is enhanced by application of force to the wafer circumference. The force is communicated by several thin ceramic fingers situated around the wafers circumference (the Weighted Plate in Figure 8.13 on page 193). The fingers are attached to a 5 kg weight. The spatial nonuniformity of this force atop the elastic o-ring can cause the wafer to flex and crack.

A special wafer carrier was built to more uniformly distribute the fingers force around the wafer circumference. Use of this carrier prevents wafer cracking. The carrier is made of aluminum, the only metal compatible with the silicon STS etch process. It

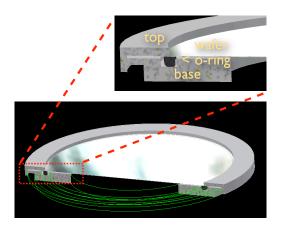


Figure 8.14: STS wafer carrier schematic. This aluminum wafer carrier housed the silicon wafer during processing. An o-ring between the top and base sealed the wafer to the carrier. The STS stage o-ring sealed to the carrier base to the STS etchers chilled stage. See Figure 8.13 on page 193.

consists of three parts: a top aluminum retaining ring, a Viton o-ring, and a sturdy aluminum base. See Figure 8.14 for a schematic of the carrier.

8.7.1.3 thru wafer etching

Etches that penetrate the full wafer thickness require use of a backing wafer to prevent helium leakage, process contamination and loss of wafer backside chilling. The backing wafer is thermally contacted to the process wafer by a thin adhesion layer of Crystalbond 509 wax (Structure Probe Inc., www.2spi.com). It flows easily at 125° C and is soluble in acetone. Sapphire was used as a backing wafer because it is transparent in the visible and permits inspection of the wafer back side to check for proper etch termination. With a sapphire backing wafer and a thin layer of wax thermal conductivity is reduced. Therefore decrease the helium backside chiller temperature to around 10° C to keep the process wafer cool enough.

STS suggests use of Cool Grease (AI Technology, www.aitechnology.com) as a thermal contacting layer to backing wafers. Cool Grease is a suspension of alumina powder. I had trouble completely removing it after processing and do not recommend it.

If using a transparent backing wafer like sapphire the STS load lock may not see

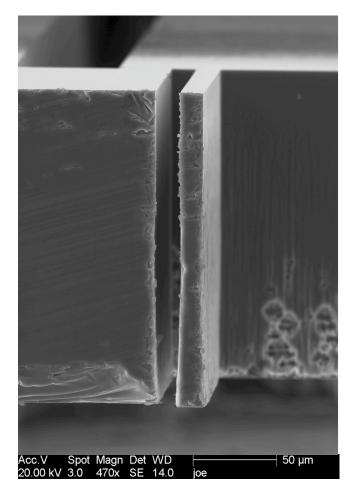


Figure 8.15: Scanning electron micrograph showing the etch profile for a 10 μm wide, $200 \ \mu m$ deep trench cut using recipe SPECB. The foreground surfaces were exposed by a dicing saw cut and are not representative of the deep etching process surface quality. Observe that the 10 μm wide trench tapers to about 8 μm wide near the back side. In the photograph the photoresist (removed for the micrograph) protected the top surface from etch. A backing wafer (also removed) was used for this thru-wafer etch.

your wafer. It detects wafers using a LED mounted beneath the wafer loading arm. Attach opaque tape to the wafer backside opposite the wafer flat. Take care to not compromise the o-ring seal region. Remove the tape before use of a solvent which can transport adhesive to the process surface.

8.7.1.4 etch termination on dielectric

Special care is required when an etch is terminated by a dielectric layer. The problem is that charges from the plasma stick to the dielectric and cause vertical or lateral deflection of the plasma depending on the geometry of the etch feature. This results in

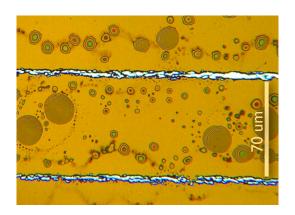


Figure 8.16: Optical micrograph showing an etch improperly terminated on a dielectric layer. Two 10 μm wide trenches (separated by 70 μm) were etched thru a silicon wafer using recipe SPECB. Prior to etching the silicon wafer was bonded to a sapphire backing wafer with wax. The trenches are backlit and the view is looking through the sapphire at the silicon-wax interface. The ragged appearance of the bottom side of the trenches is due to dielectric charging. Remedy: use Recipe 4 for the final 10 μm of the etch.

incomplete etching (swiss-cheese pattern) or severe undercutting on the wafer back side respectively. A special etcher configuration (STS SOI Upgrade Kit) and STS supplied recipe (eg NIST standard Recipe 4; NIST readers, see Ion Storage Wiki) interleave periodic low frequency (380 kHz) RF pulses that sweep away stray charges between etch/passivation cycles. To use this recipe, first process the wafer as usual stopping $10 \ \mu m$ before encountering the dielectric layer. Then use Recipe 4. Note that the etch rate of bulk silicon is reduced below that of SPECB for this recipe.

Common wafers with a dielectric etch termination layer include the following.

- silicon on oxide (SOI) wafers
- silicon wafers coated with thin film of silicon oxide or silicon nitride
- silicon wafers adhered to a backing wafer by wax or Cool Grease

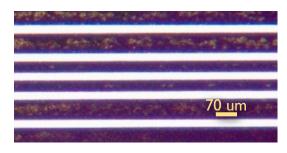


Figure 8.17: Optical micrograph showing an etch properly terminated on a dielectric layer.

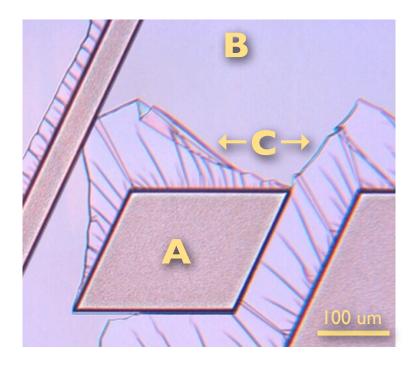


Figure 8.18: Optical micrograph of baked-on photoresist. If the process wafer temperature becomes too high during deep etching photoresist will burn on to the wafer. While acetone is an excellent solvent for photoresist, when burned is insoluble in acetone. The micrograph shows deep etched silicon (A), the unetched silicon surface (B), covered with photoresist during etching) and remnant snake skin like sheets photoresist after washing in acetone (C). Use of the ultrasonic bath with acetone almost always removes baked-on photoresist but can damage delicate structures. Shipley SVC-150 photoresist stripper at 80° C can often remove it without use of ultrasound as can piranha etch (see 8.7.6 on page 230). Resolution: lower the wafer temperature during processing by improving thermal contact to the backing wafer or lowering the backside chiller temperature set point.

8.7.1.5 deep etch pitfalls

This section consists of micrographs illustrating several of the most common fabrication errors associated with deep silicon etch. Remediary actions are suggested for

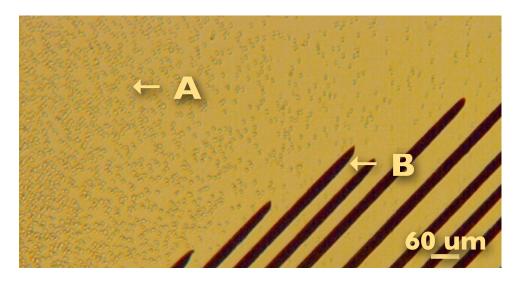


Figure 8.19: Optical micrograph showing excess fluorocarbon polymer. During a normal etch cycle the fluorocarbon polymer is fully etched away from surfaces normal to the plasma flux while persisting on channel sidewalls. If the process wafer surface is too cool during etching the polymer will not be fully etched and will accumulate on the wafer. In the micrograph the translucent $\sim 1~\mu m$ sized dots (A) are excess polymer in early stages of accumulation. The dark stripes (B) are deep etched silicon channels. If accumulation persists a nearly homogeneous layer will develop. The presence of this layer can also be identified by its extreme hydrophobicity. Resolution: raise the backside chiller temperature set point.

each.

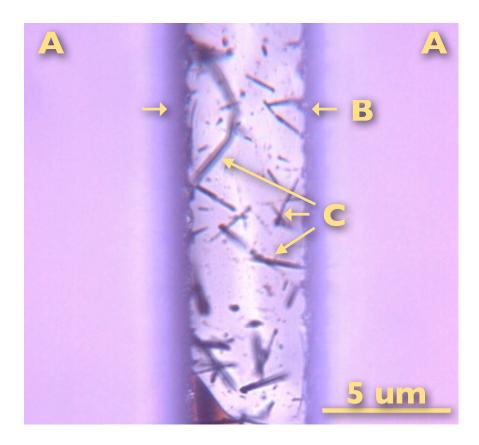


Figure 8.20: Depicted is a trench (B) etched into the surface (A) of a silicon wafer but not fully through to the back side. The camera focus is several μms above the bottom of the trench. There are many needle shaped features (aka grass) tens of μms in length, arrows C. They arise when moisture and sputtered contamination produce microscopic masks at various levels during etching. These masked areas are shielded from etching and form tall needles, some of which collapse laterally. These etch artifacts can appear when the process wafer surface temperature is too high. Resolution: lower the wafer temperature during processing by improving thermal contact to the backing wafer or lowering the backside chiller temperature set point. Also, dry the process wafer on a hot plate at 90° C for 10 minutes before etching (see STS documentation, [Flamm 90]).

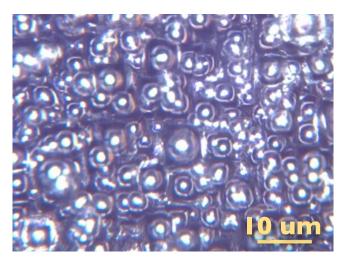


Figure 8.21: Photo of deep etched silicon surface morphology. This optical micrograph shows silicon surfaces when etch parameters are properly adjusted. Depicted in the top image are trenches (A) etched into the surface of a silicon wafer but not fully thru to the back side. The focus in micrograph is at the bottom of the trenches – photoresist coated silicon ridges (B) protrude upward beyond the field of view. The bottom image shows how properly etched surfaces appear: shiny with bubbly looking surface topology.

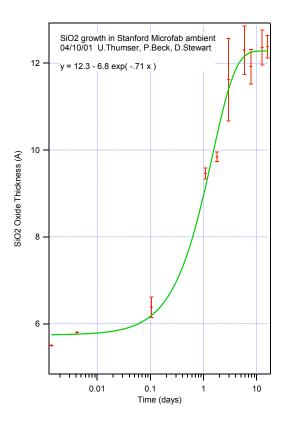


Figure 8.22: Native SiO_2 thickness on bare silicon. A bare silicon wafer quickly oxidizes at room temperature in air. The plot shows the oxide thickness over time for a wafer stripped of oxide by immersion in a 50:1 water:HF solution then left exposed to air. The thickness was measured using spectrometric reflectometry (Nanospec 250). It is expected that the oxide thickness is $\ll 0.6~nm$ at t=0. The measure film thickness doesn't approach zero at zero time due to limitations of the measurement technique. Data from the Stanford Nanofabrication Facility (M. Tang and U. Thumser.

8.7.2 Silicon oxide etching

Silicon oxide etch is a common MEMS process. Two techniques are common: a wet etch with a solution containing HF and a dry etch with a fluorine plasma. In this thesis both methods were used to remove bulk structural SiO₂ (eg in SOI wafer processing), to strip away native SiO₂ on doped silicon ion trap surfaces and to pattern oxide layers which served as the dielectric in MEMS capacitors. Neither method etches bulk silicon.

A 1-2 nm oxide forms on bare silicon in air at room temperature (see Figure 8.22 or [Madou 02]). Exposed dielectrics are known to be problematic to ion traps because they can support stray charges and it is unclear if such a very thin oxide layer might sustain surface charges. As a precaution, the silicon ion traps discussed in this thesis were processed to strip away this native oxide within 20 minutes of installation into a

Name	O_2 (sccm)	CHF_3 (sccm)	RF power (W)	RF DC BIAS (volts)	Pressure (torr)	
SiO_2 .RCP	25	350	120	-260	100e-3	
SiO_2 FAST.RCP	0	30	200	-350	40e-3	

Table 8.2: Chart showing typical SiO_2 etch recipe parameters for the Plasma Ops III etcher. Recipe SiO_2 FAST.RCP etches at a rate of about 25 nm/min for a fused quartz SiO₂ wafer. Recipe SiO_2 .RCP etches at a rate of 12 nm/min for a fused quartz wafer. It produces $\sim 45^{\circ}$ tapered side walls when used in conjunction with 510LA photoresist. Such a taper is necessary if continuity is desired for subsequently deposited metallization as when making capacitors. Note that 1 Torr is 133 Pa.

vacuum system. Both wet and dry etches were used in this application.

dry etch The dry plasma etching was performed in a Plasma Ops III etcher. In this device CHF₃ is the process gas. A plasma containing atomic fluorine is produced above wafer. Complex surface chemistry occurs at the surface which is responsible for etching; primary reaction products are SiF₄, CO and CO₂. Oxygen may be optionally introduced into the plasma to slowly degrade photoresist masks resulting in tapered (concave) etch sidewalls. Photoresist is the usual etch mask. The key process parameters are in Figure 8.2.

High energy ions in the plasma can charge surfaces on the process wafer to many hundreds of volts. In particular, catastrophic breakdown was observed across 3 μm vacuum gaps during processing of SOI wafers (see Figure 8.23 on the next page). The solution was to short all isolated conducting surfaces to ground prior to processing in plasma etcher.



Figure 8.23: The micrograph shows evidence of breakdown on a SOI structures due to charging in the Plasma Ops III oxide etcher.

wet etch The wet etch of SiO_2 made use of industry standard buffered oxide etch (BOE). BOE consists of 6 parts 40% ammonium fluoride, 1 part 49% hydrofluoric acid. The manufacturer specified etch rate at 16° C is 87 nm/min. BOE like most wet etches is isotropic and so results in undercutting (see Figure 8.24). When etching SiO_2 at the bottom of deep crevices (as in SOI processing) the solution was agitated on an orbital shaker.

Some precautions are in order for BOE. Titanium, a common thin film adhesion layer, is rapidly etched by BOE [Williams 03]. In the course of this thesis work it was observed that even buried titanium can be degraded by a BOE wet etch. This may be mitigated by thorough rinsing (with agitation) using deionized water (~10 min). Glass too is etched by BOE (eg 43 nm/min for Corning Pyrex 7740) and so Teflon containers



Figure 8.24: Figure showing aspect ratio of SOI oxide exposed to BOE wet etch. Using BOE with agitation, 4 μm thick SiO_2 was fully removed at the base of trenches 4-5 μm wide 100 μm deep in 35-40 minutes (100-114 nm/min). This technique was used in dv16m and dv16k series SOI ion traps. TODO ref to SOI trap section

should be used [Williams 03]. Note that HF is extremely dangerous. Read the MSDS.

Thin film thickness (including SiO₂) can be estimated by its color or ellipsometry ⁶

. Note too that oxide surfaces are hydrophobic while bare silicon surfaces are hydrophilic.

⁶ Optical fringes are visible in the sub wavelength thickness air-film-substrate cavity. There is a color vs thickness chart online.

8.7.3 Doped silicon backside alignment

Some devices require features on the front and back side of a wafer. At the outset of wafer processing it is common to etch registered alignment marks into the wafer surfaces.

Registration and pattern transfer can be done with several standard techniques.

Ordinary (undoped) silicon wafers are transparent in the infrared (IR). This is exploited by the NIST Karl Suss contact exposure tool to image etch/metallization patterns on the wafer backside when viewing from the front through the wafer bulk. This IR image is used to align a mask to the front side and expose a front side photoresist pattern. With this technique alignment mark registration to better than 5 μm is possible. Highly doped silicon is however highly absorbing in the IR and this technique isn't practical.

Other techniques rely on more expensive tools. For example, some wafer suppliers offer laser etching of front-back alignment marks to $0.5 \ \mu m$ resolution. This is only available for standard size wafers. A common in-house tool is commercial wafer alignment machines which solve this problem using computerized alignment platforms and front/back digital microscopes. Their cost at \$0.5 million is however prohibitive.

Inexpensive, repeatable backside alignment to about $5\mu m$, 0.01° accuracy was done in the NIST cleanroom using a simple kinematic approach discussed in Figure 8.25 on the next page. It makes use of a NIST in-house tool for easily fabricating high resolution photolithography masks.

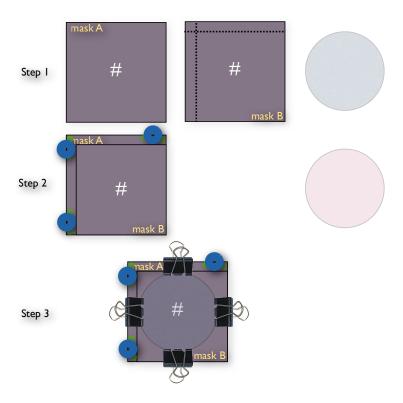


Figure 8.25: Kinematic backside alignment technique. Step 1: Masks A and B are 4 inch glass-chromium photolithographic plates patterned with identical alignment marks #. A glass cutting saw was used to cut fully thru mask B along the dotted lines, reducing its size by 0.5 inch on two sides. Step 2: Put Mask A on the stage of a microscope. Under an optical microscope slide mask B across the top of mask A, chromium sides touching. Apply a tiny bit of the epoxy to the edges of the masks so that it slightly wicks between the plates and provides viscous resistance to relative motion. Position mask B so its alignment pattern overlaps with that on mask A. Let the glue cure. Position three 0.25 inch thick, 1.0 inch diameter stainless steel posts atop mask A and flush against the edge of mask B as in the Figure. Apply epoxy to the stainless posts fixing them to mask A. Do not put any epoxy near the intersections between mask B and the stainless posts. Let the glue cure. Crack the tiny bit of glue fixing mask A to mask B and remove this glue with solvent. Apply photoresist to both sides of a 3 inch wafer. Step 3: Slide the wafer between the masks. Press mask B flush with the stainless posts fixed to mask A. Use binder clamps to hold the stack together. The masks remain well aligned even after sliding the silicon wafer between them. Expose as usual on the Karl Suss UV exposure tool. Use an etch technique (eg silicon etch for a silicon wafer) to transfer the photoresist pattern to each side of the wafer.

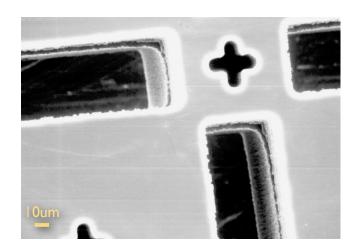


Figure 8.26: SEM micrograph of a silicon wafer showing front side to backside registration of an alignment pattern. The kinematic jig described in Figure 8.25 on the preceding page was used to transfer an alignment pattern to thick photoresist on both the front and back side of a 200 μm thick silicon wafer. Deep etches from both sides meet and reveal an alignment error of about 5 μm .

Name	Argon (mT)	Oxygen (mT)	Time (min)	DC Bias (V)	RF(W)
metal atop SiO_2	15	0	3	-350	25
standard clean $15-30$	0	2	-400 to -350	50	

Table 8.3: Table of standard argon plasma etch recipes in the HTS1 e-beam evaporator.

8.7.4 Metallization of silicon

Deposition of gold, copper, titanium and aluminum thin films are done in an e-beam evaporator. In a low pressure ($< 1 \times 10^{-6}$ Torr) environment a high energy (10 kV) electron beam (0-20 mA) is directed at one of several water cooled tungsten crucibles containing the process metals. The electron energy is deposited directly in the process metal causing it to melt. The metal vapor plume which results intersects the process wafer about 0.5 m away. The deposition rate (0.1-2 nm/sec) is controlled by the e-gun current. The chuck holding the process wafer is water cooled and acts as an RF anode for *in situ* plasma cleaning. The NIST deposition system used is named HTS1.

An argon plasma can be used to perform in situ cleaning of a wafer surface in advance of metal deposition. This is necessary in many cases to ensure good adhesion of the metal to the silicon. It slightly etches exposed surfaces.

An oxygen plasma etch may be used to strip off residual photoresist if its believed to be causing adhesion problems.

Gold is commonly used in ion traps owing to its high conductivity and the absence of a surface oxide. It does not stick to silicon oxide but Ti and Cr do [Williams 03]. Hence, these metals and are commonly used as an adhesion layer (10-50 nm) for gold. Titanium is not magnetic and is convenient to deposit on our e-beam evaporator, but requires care in process design as it is rapidly etched by HF (which in turn is used as an

silicon oxide etchant (see Section 8.7.6 on page 230). Titanium was used exclusively as a adhesion layer in the devices discussed in this thesis.

Chromium is attractive as an adhesion layer for Au because it is not etched by HF, however it is antiferromagnetic. That is, below the Neel temperature (for bulk Cr, $T_N = 311^{\circ}$ K [Zabel 99]) it is favorable for adjacent spins to antialign. The Neel temperature is analogous to the Curie temperature for ferromagnetic materials. That is, it is the temperature at which thermal energy becomes large enough to destroy microscopic ordering in the material, rendering it paramagnetic. Thin films of Cr are especially complex and exhibit a property called spin density wave (SDW) magnetism [Fawcett 88, Zabel 99]. Cr has not been used at NIST as an adhesion layer for Au in ion traps. In a neutral atom experiment a Cr adhesion layer was used and the resulting magnetic fields found to be negligible [Lev 06].

⁷ In his thesis work Ben Lev used Cr as a sticking layer for electroplated gold wires used to make mots in his thesis. Cr was also used as a sticking layer in the commercial hard disk platter he etched with a fine grating for the purposes of making a magnetic mirror for neutral atoms [Lev 06].

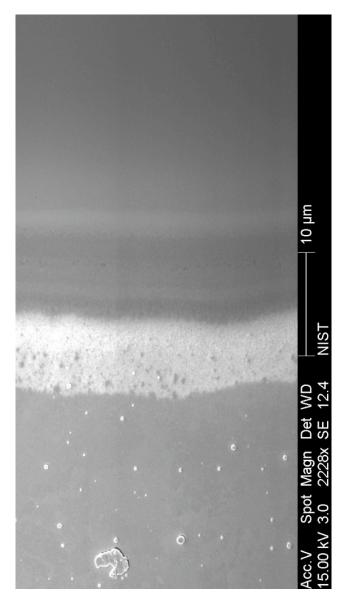


Figure 8.27: SEM showing contamination of a gold film deposited by e-beam evaporation. During deposition a stainless steel shadow mask (see Section 8.7.4.2 on page 216) was positioned over the wafer which shielded the right hand side from gold deposition. The left side is a $\sim 1 \mu m$ gold film using the FASTAU deposition recipe. The right hand side is bare silicon. The whitish strip in the middle is a transition between the two regions corresponding to the edge of the mask. The blobs on the left side are 200 - 500 nm in height as measured by a stylus profilometer. Debris of this size are not expected to cause trouble for the ion traps discussed in this thesis if they are made of gold. However, since it couldn't be ruled out that they might instead be dielectric care was taken to avoid them (e.g. recipe SLOWAU).

8.7.4.1 deposition of thick gold films

Gold films 1 nm to 1 μm are routine. For depositions > 200 nm in the NIST e-beam evaporator some care must be taken to prevent contamination by debris (see Figure 8.27). Films much thicker than 1 μm suffer from rough surfaces (> 500 nm rms) for reasons that are not well understood. The precautions in recipe SLOWAU permitted growth of up to 1.5 μm gold films with good surface quality. Unfortunately, this recipe

Name	Pressure (Torr)	$\mathrm{Al}\;(\mathrm{nm/s},\mathrm{nm})$	Ti (nm/s, nm)
FASTAU		1, 10	1, 10
SLOWAU		0.3, 10	0.3, 10

Table 8.4: Table of gold deposition recipes for the HTS1 e-beam evaporator. Note that the aluminum deposition step is only necessary if making Ohmic contacts to doped, bare silicon wafers.

did not always reproduce debris free films.

The FASTAU recipe can be considered the baseline recipe for deposition in HTS1. It consists of putting a wafer into the system and depositing as rapidly as possible. The SLOWAU recipe includes the following additional precautions beyond slow deposition rates.

- Don't use the communal gold crucible in HTS1 as it is used by many cleanroom
 users and may be contaminated. Instead, use a new crucible and gold pellets
 cleaned in solvents in an ultrasonic bath. Use a tungsten crucible, not a carbon
 crucible which may shed carbon flecks.
- In addition to deposition on the wafer surface, the interior of the HTS1 vacuum system is coated with metal during depositions. Some of these metals oxidize (eg Cu) when the vacuum is broken during wafer loading. Flakes from interior surfaces may fall into the process crucible during deposition. To reduce this likelihood check that the system has been recently cleaned. In addition, with the crucible removed use a clean stainless knife to scrape away the thick metal crust which forms at the rotating hearth aperture. Use the HEPA vacuum cleaner to remove flakes 8 on the following page.
- Inspect by eye the metal surfaces for all the crucibles to be used in a deposition.

Look for discoloration, carbon deposits or debris.

- Attach the process wafer to the water cooled chuck. Use all the screws on the
 metal retaining ring to achieve good thermal contact. The process wafer heat
 load is lower for lower deposition rates. Cool surfaces result in smaller gold grain
 sizes (personal correspondence (2007) Ron Folman of Ben-Gurion University,
 Israel).
- HTS1 has a mechanical shutter that optionally shields the process wafer from the metal plume. Keep the shutter closed while heating up a crucible using the e-beam. Adjust the e-gun current so metal deposits on the acoustic film thickness detector at a rate of 1 nm/sec. For the next 3-4 minutes proceed as follows. Dither the e-beam across the metal surface in the crucible 8. Inspect the molten metal by eye looking for islands of floating scum. Chase them with the e-beam until they are blasted away. You may see occasional sparks jumping from the crucible surface. Then, look by eye perpendicular to the metal flux for more sparks. If you don't see any sparks over a minute or so, lower the e-gun current to get the desired deposition rate, open the mechanical shutter and proceed with deposition.

8

⁸ Note NIST HTS1 users, these procedures can (easily) cause expensive damage to the e-beam evaporator. Talk to an expert first.

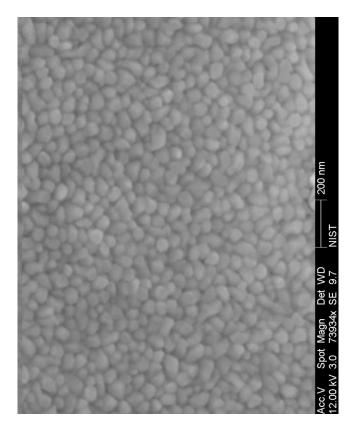


Figure 8.28: SLOWAU recipe performance: SEM showing 30-50 nm gold grains. This is the intrinsic surface roughness of a gold film 1 μm thick deposited in the NIST e-beam evaporator at room temperature for the SLOWAU recipe.

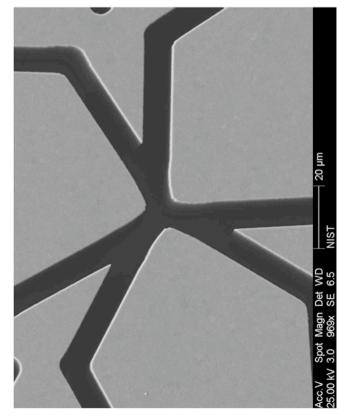


Figure 8.29: SLOWAU recipe performance: SEM showing a wide field of view of a 1 μm gold deposition. This illustrates the degree to which the SLOWAU recipe can reduce the prevalence of debris. The dark channels are trenches (> 100 μm deep) cut into the silicon.

8.7.4.2 shadow mask deposition

A shadow mask is a thin sheet of metal with apertures. It masks off parts of a

wafer during metallization in an e-beam evaporator. Use the following recipe to prepare

a silicon chip for metalization using a shadow mask.

(1) Thoroughly clean a sacrificial silicon backing wafer (front and back side).

(2) On a hotplate at 130° C bond one or two chips to the backing wafer using wax.

Use wax sparringly. No excess wax should protrude from under the chip at its

edges.

(3) Strip the native oxide off the wafer by doing a 30 sec BOE dip (see Section 8.7.6

on page 230) or 1 min in the Axic etcher with recipe SIO2 FAST.RCP (see

Section 8.7.2 on page 203). Complete the following steps in < 10 minutes to

prevent reoxidization of the silicon surface.

(4) Align the shadow masks to the chips under a stereoscope. Use Kapton tape to

hold the masks in place.

(5) Attach the backing wafer to the water cooled HTS1 wafer chuck.

(6) Proceed with the FASTAU or SLOWAU deposition recipes in Section 8.7.4.1 on

page 212. Use an Ar plasma clean if necessary.

(7) Release the chips from the backing wafer using step IV in Section 8.7.6 on

page 230.

Stainless shadow masks are laser machined by Solder Mask Inc. (www.soldermask.com).

The cost per mask was \$100 in lots of 1, same day shipping. The GERBER format is

used to specify the mask pattern. Typical specifications:

• material: stainless steel

• thickness: 250 μm

• resolution: $25 \ \mu m$

8.7.4.3 Ohmic contacts in heavily doped silicon

Care must be taken when making electrical contact to semiconductors. This section provides a brief overview of how doping influences semiconductor conductivity and what happens at metal-semiconductor interfaces.

In semiconductors there is band gap, a range of electron energies for which there are no available states in the crystal. States lying below (above) this gap are called the valence (conduction) band. The Fermi distribution predicts the temperature dependent statistical distribution of electrons among available states. Electrons populating the mostly empty conduction band can conduct electricity, as can holes (missing electrons) in the valence band. Undoped silicon at room temperature is a poor conductor because nearly all the available electron states in the valence band are occupied and there is negligible population in the conduction band.

Silicon is a semiconductor with a band gap of 1.1 eV and four valence electrons per lattice site [Sze 81, Kittel 96]. If a trivalent atom like B, Al or Ga is substituted for silicon it steals an electron from the valence band in order to satisfy the covalent bond with its neighbors. If many such substitutions are made, the silicon is then called p-type and has holes in the valence band. These holes permit electrical conduction. Conductivity results without additional electrons being excited to the conduction band.

The doped silicon used in this thesis work is p-type due to doping with Boron. The doping level is 0.1 - 1% resulting in an electrical conductivity of $0.0005 - 0.001 \ \Omega - cm$ (B*Si) [Sze 81]). The wafers were obtained from Virginia Semiconductor, Inc.

The fabrication of reliable contacts between metals and semiconductors is crucial for integrated circuits. Usually, a Schottky barrier occurs at a metal-semiconductor interface which has nonlinear, rectifying characteristics [Sze 81]. When a semiconductor is brought into contact with a metal, current flows so that their respective chemical

Metal	$\mid T \mid$	σ
B*Si	300	500-1000
Al	300	2.73
Au	300	2.27
Ag	300	1.63
Cu	300	1.73
Ti	273	40

Figure 8.30: Resistivity of common metals compared with the boron doped silicon (B*Si) used in this thesis [Lide 08]. The units for temperature T is $^{\circ} K$ and for resistivity σ is $\times 10^{-}6\Omega - cm$.

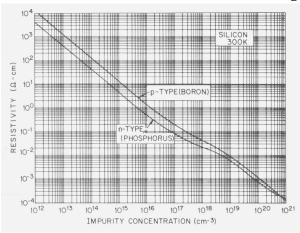


Figure 8.31: Resistivity vs impurity (dopant) concentration for silicon at 300° K [Sze 81].

potentials are equilibrated at the interface. A potential drop across the interface results along with a local depletion of charge carriers called a depletion layer. In lightly doped semiconductors this depletion region is wide and presents a barrier to conduction. However, if a sufficient DC electronic bias is present electrons have enough energy to exceed the barrier. That is, the current-voltage (I-V) response of the junction is nonlinear.

An ohmic contact is a metal-semiconductor interface with a negligible contact resistance relative to that of the bulk semiconductor. During device operation the voltage drop across an ohmic contact should be small relative to the drop across the whole device [Sze 81]. That is, the current-voltage (I-V) response of the junction is linear and symmetric. In highly doped semiconductors there are so many carriers that the depletion region is very narrow and conduction at room temperature is sometimes possible. Standard practice is to use aluminum as the conductor and to anneal at > 350° C [Card 76]. The exact conditions at semiconductor-metal interfaces which result in ohmic contacts are not fully understood by engineers. Considerations include metal type, the presence of oxide and water vapor at the interface and interdiffusion due to annealing [Card 76].

I made ohmic contacts between doped silicon and gold as follows. First, the native

silicon oxide was removed using a 90 second plasma etch 8.7.2 on page 203. Second, with only 1-2 minute exposure to air, the wafer was transferred to the e-beam evaporator. There, a 10 nm layer of Al was deposited on the silicon, then 10 nm Ti (as an adhesion layer) and finally 1000 nm Au. The quality of the junction was tested on a home built I-V measurement apparatus. It was found to be ohmic without annealing probably due to heavy doping. Vacuum processing for ion traps is a 3-4 day 200° C bake and it is expected to improve the junction conductivity. Gold-aluminum intermetallic compounds (aka purple plague) can degrade the contact but were not observed, probably due to the intervening Ti layer.

8.7.5 Wafer bonding

Semiconductor wafer bonding is a MEMS technique for adhering wafers together without the use of glue [Wallis 69], [Tong 99]). Bondable materials include silicon, oxidized silicon, glass and fused silica. The resulting bonds are robust and hermetic. They find application in MEMS device packaging and fabrication of multilayer semiconductor-insulator structures. The process is simple. Two highly polished, flat, hydrophilic surfaces are brought into contact and over several seconds their surfaces bond. The resulting bond is usually weak at room temperatures but can be made stronger with greater pressure and higher temperatures. The physics behind bonding is part electrostatic, part chemical.

For traps with few electrodes and a large ion-electrode separation (> 200 μ m), the traditional wafer bonding used mechanical screws. However, smaller traps with many trapping zones requires higher alignment precision than is practical using screws. A variety of alternative wafer bonding techniques were explored in the context of ion trap microfabrication. The required UHV pressures (< 1×10^{-11} Torr) and processing temperatures (200° C), excludes many common approaches including ordinary epoxy glue and solder due to outgassing. Technologies investigated include thermocompression bonding, anodic bonding and commercial silicon on insulator (SOI). Only the latter two are discussed in this thesis.

Wafer bonding was first demonstrated in 1969 by Wallis [Wallis 69]) for silicon and glass. Wallis bonded the borosilicate glass Corning 7740 Pyrex to silicon at 400° C with a 300 V DC bias in 1 min. His explanation of the attraction between silicon and glass is purely electrostatic, with long term adhesion at room temperature attributed to unspecified covalent chemical bonds at the wafer interface. Subsequently water adsorption at the wafer surfaces and resulting hydrogen bonds were implicated in both silicon-glass and silicon-silicon bonding.

Both chemical and electrostatic processes contribute to wafer bonding. This section begins with a practical guide to anodic wafer bonding and then discusses these bonding processes in detail. It concludes with comments on commercially available silicon on insulator (SOI) wafers.

8.7.5.1 waferbonding practice

Commercial bonding apparatus is available that simultaneously accommodates anodic, thermocompression and silicon direct bonding techniques and provides waferwafer alignment to better than 1 μm . However, at > \$0.5m dollars the cost is prohibitive. It turns out that its possible to build a simple anodic bonding setup for small scale bonding.

Early in my thesis work initial attempts at waferbonding 1 cm² silicon to 7070 glass (100 μm thick) were unsuccessful. Bonding was done in air at 400° C and electrical breakdown occurred at 300-400 V, too low for bonding. Breakdown occurs when the electron mean free path is just sufficient to allow build up of enough energy to ionize a gas molecule upon subsequent impact. The dielectric strength of air is 3×10^6 V/m, which is exceeded at 300 V for a 100 μm gap. Bonding at low pressure (1 × 10⁻³ Torr; 1 Torr is 133 Pa) and in 1 atmosphere of the electronegative gas SF₆ (whose breakdown is three times that of air) were of middling success [Madou 02, Thomson 28, Paschen 89]. Ultimately, it was found that bonding could be reliably accomplished with the following parameters and the apparatus in Figure 8.33 on page 223.

- 150 μm glass
- 400° C hot plate
- 500 V
- 30 min piranha dip within 6 hr of bonding (see Section 8.7.6 on page 230)
- 3 minutes per bond interface

Other bonding tips include the following. At least 15 minutes before bonding use

a dry nitrogen jet to knock any dust off the bonding apparatus. Preheat the bonding apparatus in advance of bonding. Always, inspect the chip surfaces for debris or scratches. As a gauge of wafer flatness, when chips are stacked look for < 6 Newtons fringes per cm across their surface.

Its not certain if success was due to cleaner surfaces after the piranha etch or if there is some favorable surface chemistry at work. I observe that wafers not cleaned in piranha would bond successfully only to fall apart after cooling to room temperature. Conversely, wafers recently washed in piranha formed bonds more quickly and they proved much more robust at room temperature. Compatible with this observation is observation by Seu, et al. that piranha makes glass more hydrophilic [Seu 07]). It is worth noting also that surface treatment with sodium silicate and other silicates is reported to permit bonding at temperatures as low as 150° C [Puers 97]. The efficacy of sodium silicate was not investigated experimentally. At any rate, the importance of surface chemistry was insufficiently appreciated early in my thesis work and should not be overlooked.

Bonding of wafer fragments $1 \text{ } cm^2$ in size can be initiated from a single needle point contact with the top wafer surface. This was helpful as final wafer alignment could then be confirmed with a microscope prior to bonding (see Figure 8.33 on the next page). Larger areas wafers require the use of electrodes commensurate with the wafer area. Silicon-7070-silicon structures as large as 3 inches in diameter were successfully bonded.

Wafers suitable for bonding were obtained from several manufacturers (see Section 8.7.5.5 on page 229). As a crude gauge of surface roughness and flatness, wafers that bonded easily had < 6 Newtons fringes per cm across their surface when placed on

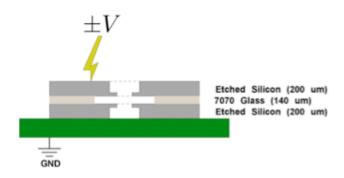


Figure 8.32: Side-on schematic view of two-layer silicon ion trap on the anodic bonding apparatus stage. A glass wafer sandwiched between a pair of patterned (etched) silicon wafers sits atop a grounded aluminum base plate. Bonding to the bottom (top) silicon layer takes place by applying potential -V (+V) for several minutes each polarity.

an optically flat glass plate.

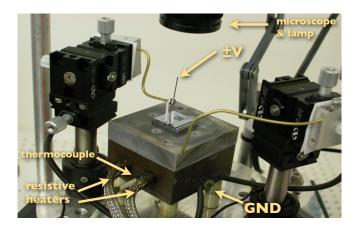


Figure 8.33: Anodic bonding apparatus for 1-3 cm² trap chips. The bonding platform is heated with resistive heaters regulated by a PID controller attached to a thermocouple. The platform itself is at ground and the high voltage potential is applied by a pair of needles on translation stages. Two alumina pins protrude from the stage surface. These pins pass thru alignment holes in the silicon and glass wafers. Wafer alignment to about $25 \mu m$ is possible using this approach. Not visible is a bell jar, vacuum apparatus and needle valve for bonding at low pressure or in a SF₆ environment. Also not visible, is an ammeter to measure the current traveling to the cathode in Figure 8.34 on page 225. The bonding takes place in a clean room hood (class 100) on a stage (see Figure 8.33).

8.7.5.2 electrostatic wafer bonding

To understand the electrostatic mechanism for wafer bonding, consider a capacitor formed by a glass slab thickness d sandwiched between two metal plates [Wallis 69]). At room temperature an electric potential V_0 applied across the plates produces a constant voltage drop and hence a electric field $E = V_0/d$. At elevated temperatures most glasses contain mobile cations in the form of Alkali metal atoms (Na+, K+); the anions remain fixed in place. As the capacitor temperature is increased cation mobility increases exponentially and cations following the electric field lines accumulate in the glass at the edge of the cathode. A current i flowing from the potential source to the cathode largely neutralizes the cations. The glass near the anode is left depleted of cations and it is in this polarized region where most of the capacitor voltage drop is concentrated. Imagine there is a tiny air gap $d_{\rm gap}$ between the anode and the glass and that the remaining potential drop is $V_{\rm gap} < V_0$. The electrostatic force across this gap is $F = \frac{1}{2}\epsilon_0 A E^2$ where here $E = V_{\rm gap}/d_{\rm gap}$ and A is the capacitor area. For example, for $V_{\rm gap} = 10~V$, $d_{\rm gap} = 10~{\rm nm}$, $F = 4.4 \times 10^6~N/m^2 = 640~{\rm psi}$. This force brings surfaces into close enough contact that bonding can happen.

Stress in bonded thin wafers can cause cracking if the coefficients of thermal expansion (CTE) are too dissimilar across the full bonding and operating temperature of a device. The CTE of Pyrex is well matched that to silicon. Corning 7070 Lithia Potash glass is another borosilicate whose CTE is engineered to match that of silicon but with a lower ionic content. This is disadvantageous for wafer bonding-higher temperatures and voltages are required-but is advantageous for RF Paul traps as its loss tangent is lower than Pyrex.

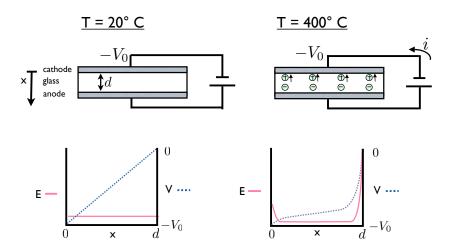


Figure 8.34: Figure illustrating the electrostatics responsible for anodic bonding. The electric potential (dashed, blue) and field (solid, pink) in the glass dielectric of a glass-filled capacitor are plotted at room temperature (20° C) and bonding temperature (400° C). Anodic bonding is accomplished when a silicon wafer is slipped between the glass and anode. Note that bonding temperatures are well below the softening point of both materials. Also, although ordinary silicon wafers have a high surface resistance (order $1 \times 10^5 \Omega - cm$), for the purposes of bonding the wafer can be treated as an equipotential surface.

8.7.5.3 direct wafer bonding

Room temperature wafer bonding (direct bonding) due to the formation of hydrogen bonds at the bond interface is possible for exceptionally flat, smooth and moreover hydrophilic surfaces. Direct bonding is common in industrial applications but it is technically challenging in laboratory environments as it relies on wafer geometry alone (vs electrostatic forces) to bring wafers into close enough contact (< 1 nm).

Silicon surfaces in air are naturally hydrophilic. This arises as follows. In air

Material	Loss Tangent (at 1 MHz)
fused silica	0.0002
alumina (99%)	0.0002
7070 glass	0.06
7740 glass	0.5

Table 8.5: Loss tangent of Corning 7070 and 7740 borosilicate glasses [Comeforo 67, Corning 99].

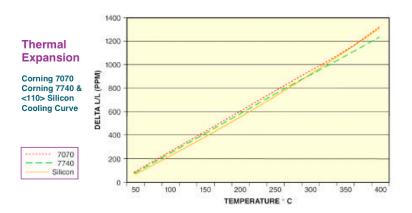


Figure 8.35: Thermal expansion of Corning 7070 and 7740 borosilicate glasses as a function of temperature [Corning 99].

 ~ 1 nm silicon oxide (SiO₂) grows on silicon surfaces. Free SiO₂ at the surface (SiO-Si) reacts with water vapor in air to form extended silanol (SiOH) complexes which are themselves hydrophilic. The silanol complexes readily adsorb water vapor forming a hydrogen bonded network of water molecules on the wafer surface SiOH: $(OH_2)_2$. When two thusly hydrated SiO₂ surfaces are brought into close contact, hydrogen bonds develop between the oxygen and hydrogen atoms of the adsorbed water SiOH: $(OH_2)_2$: $(OH_2)_2$: OHSi. This mechanism alone will bond surfaces at room temperature. It is energetically favorable for hydrogen bonds to form directly between silanols SiOH:OHSi, but this stronger bond only forms above 300° C. At 700° C silanol bonds give way to tightly bound (covalent) siloxane SiOSi. Details on this chemistry and its kinetics are discussed in [Stengl 89].

8.7.5.4 SOI wafers

Subsequent to the successful use of in-house anodic bonding of silicon to glass, commercial silicon on insulator (SOI) wafers were used to make traps. The cross section

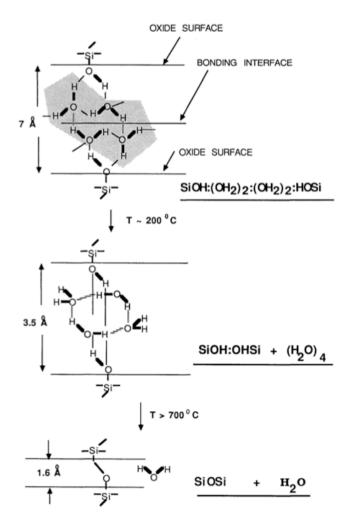


Figure 8.36: A proposed model for silicon wafer bonding mediated by hydrogen bonds between water molecules. Top: Bonding across an interface mediated by weak hydrogen bonds between water clusters (thin dashed lines): SiOH: $(OH_2)_2$: $(OH_2)_2$: OHSi. Middle: Bonding via hydrogen bonds between silanol groups: SiOH:OHSi. Bottom: Bonding via siloxane bonds: SiOSi. Figure from [Stengl 89].

of a SOI wafer is drawn in Figure 8.37.

Thermal oxide is the typical oxide for SOI wafers. Thermal oxide is grown by oxidation of a silicon wafer in an oven. The silicon reactant is derived from the wafer bulk and the oxides maximum thickness is diffusion limited to about 2 μm . SOI is a bonded stack of two such silicon wafers, separately oxidized. Hence, the maximum SOI



Figure 8.37: Figure showing a typical silicon on oxide (SOI) wafer in cross section. Note that the illustration is not drawn to scale.

box thickness is about 4 μm .

After bonding the oxide is often stripped from the exposed top and bottom surfaces. Commonly the top of the stack, the so called device layer, is thinned to between 100 nm and 100 μm . The remaining backing layer is called the handle layer.

Boron doped SOI wafers for this thesis work were obtained from the on-line inventory of Ultrasil, Inc. Typical cost was \$100-200 per wafer in lots of 1. Example specification:

- crystal orientation: <100>
- overall thickness: 360 +/-5 μm
- TTV: $< 2 \ \mu m$
- polish: double side polished (haze free)
- device layer: $4 \pm 0.5 \ \mu m$, boron doped (P type), 0.005-0.020 ohm-cm
- handle layer: $355 \pm 5 \ \mu m$, boron doped (P type), < 0.01 ohm-cm
- buried oxide layer: $4 \pm 0.2 \ \mu m$

Lower resistivity silicon and thicker oxide is available commercially by special order. For example, I received a quote from Virginia Semiconductor, Inc. for 30 wafers, \$375.00 each with the following specifications.

- polish: double side polished (haze free)
- device layer: $10 \pm 2 \mu m$, boron doped (P type), 0.0005-0.001 ohm-cm
- oxide layer: $10 \pm 10\%$
- handle layer: $400 \pm 10 \ \mu m$, boron doped (P type), 0.0005-0.001 ohm-cm

Oxide thicker than 4 μm can be produced by stress balanced plasma enhanced tetraethylorthosilicate (PETEOS). PETEOS oxide is used by the semiconductor industry as an intermetallic dielectric (IMD).

8.7.5.5 wafer manufacturers

Doped silicon wafers were obtained from Virginia Semiconductor, Inc. Typical wafer cost was \$170 per wafer in lots of 20. Typical specifications:

- crystal orientation: <100>
- dopant: boron (P type) 0.0005-0.001 ohm-cm
- bow: $< 20 \mu \text{m}$
- center thickness: 400 $\mu m \pm 15 \mu m$
- total thickness variation (5 point measurement): $<10 \ \mu m$
- surface: double side polished
- micro roughness: $\leq 5A$
- edge rounded: Yes

Corning 7740 and 7070 glass wafers were obtained from Sensor Prep Services Inc.

Typical cost for blank wafers was \$20-50 in lots of 5-20. For ultrasonically milled wafers
the cost was \$200 per wafer in lots of 5. Typical specifications:

- glass: 7070
- surface: roughness average (Ra) < 1.5 nm (aka bond quality SI superior finish)
- thickness: 150 $\mu m \pm 25 \mu m$
- hole diameter: ± 0.003 in
- hole taper: $\pm < 0.0015$ in
- hole location: ± 0.003
- overall pattern centering: < 0.007 in
- missing or bad holes: 1%
- chips around holes: < 0.003 in

Both chemical and electrostatic processes contribute to wafer bonding. They are discussed in the next two sections.

8.7.6 RCA wafer clean

MEMS processing may contaminate the process wafer with organic and inorganic substances. Two processes used in this thesis work require exceptionally clean surfaces: thermal oven wafer oxidation and anodic bonding. The industry standard cleaning process was developed in 1960s by Werner Kern at the Radio Corporation of America known as the RCA Standard Clean Process [Reinhardt 08]. It is a four step chemical process.

- (I) organic clean strip photoresist residue
- (II) oxide strip remove oxide and ionic contaminants embedded in the oxide
- (III) ionic clean remove remaining ionic contaminants
- (IV) solvent clean

I skip step III because there was no indication that ionic contamination was causing problems. I used a variant of I and II.

Step I An acid preparation called Piranha is used for the organic clean. The reagents are 1 part H_2O_2 (30-50% aqueous solution) and 3 parts H_2SO_4 by volume. Add the H_2O_2 to the H_2SO_4 as this order is less likely to splatter. Piranha is highly exothermic so combine ingredients slowly. Heat to 100° C, continuously agitating. Immerse the wafer in piranha using a teflon basket/clamp for 30 min. The acid remains chemically active for up to 4 hours after preparation. This step is compatible with bare silicon, glass, sapphire and SOI wafers. Most metals (including Ti and Au) and photoresist are rapidly degraded by piranha.

Step II A 5-10 minute BOE dip is used for the step II oxide strip. See Section 8.7.2 on page 203 for details. Be sure to rinse the wafers for at least 5 minutes in running deionized water.

Step IV In this step the devices are cleaned in VLSI grade acetone then isopropanol. First, if working with individual chips, put them in a teflor chip carrying

basket: one chip per carrier slot (see Section 8.7.6.1). For full 3 inch wafers use teflon edge grabbers. Rinse the devices with running deionized water for 30 seconds. Immerse in acetone and agitate gently for 30 seconds. If working with individual chips proceed one chip at a time. Squirt each chip with isopropanol and blow dry with a dry nitrogen jet. Do not let the solvents dry on the chips in the air.

It was observed that anodic bonding of silicon to 7070 glass was easier within several hours of cleaning. See Section 8.7.5 on page 220.

8.7.6.1 teflon chip holders

Delicate MEMS structures can be be easily damaged during processing in wet baths. If found that yield was higher when I used appropriate processing equipment and processed device chips in parallel instead of one at a time. In particular, the following Teflon structures proved helpful during wet etching steps. They are manufactured by Entegris, Inc.

Several 3 inch wafers can be processed in the same beaker using the following Teflon carriers.

- 3 inch wafer dipper, PFA (Teflon), p/n D14-0215, \$45.00/ea in lots of one Several dozen 1 cm² chips can be processed simultaneously in the following Teflon basket.
 - wafer holder, PFA (Teflon), p/n A14-01S-0215, \$71.00/ea in lots of one
 - wafer holder lid, PFA (Teflon), p/n A14-02S-0215, \$53.50/ea in lots of one
 - wafer holder handle, PFA (Teflon), p/n A029-0215, \$60.50/ea in lots of one

8.7.7 Electrical interconnect

Three techniques were used to attach wires to silicon MEMS devices: resistive welding and wire bonding. Each uses a different bonding mechanism and type of wire. Additionally, gap welding was used for electrical connections to other ion trap structures like Mg and Be ovens.

Resistive welding is appropriate for bonding 0.002-0.020 inch thick metal ribbon to flat circuit boards. It forms a bond by flowing a current between two points on the bonders tip through the target metals. They heats locally and a bond forms. The bonder I used is a Unitek, Inc. Light Force Weld Head. In my case the surfaces were gold ribbon and a metalized surface. Two surfaces commonly bonded to include alumina metalized with $1-3~\mu m$ gold (by silk screening using Dupont, Inc. 5062/5063 gold paste) and silicon metalized with 1 μm gold. Note that bonding is difficult with materials with good thermal conductivity like thick wire and solid metal slabs. Between bonds the tip was cleaned with a rough alumina chip (Unitek CPD 10-274-01). For the principles of bonding see [Unitek 01] and for practical advice see [Brackell 01].

Surface	Tip (Unitek)	Force (g)
Au-alumina	UTM224C	300-400
Au-silicon	UTM222L	160

The gold ribbon was supplied by Williams Advanced Metals, Inc.. It is 99.99% Au. The sizes used are 0.002×0.010 inch and 0.002×0.020 inch.

Current flows between two electrode points on the bonder tip which are separated from each other by a thin dielectric layer. It was observed that with properly tuned bonding parameters a plume of debris was emitted by the tip within several mm of the bond point. This debris discolored during a vacuum bake (200° C, 24 hours). This debris may be dielectric and could be problematic if it contaminated surfaces near the ions. This was among the reasons that wire bonding was used instead of resistive welding for MEMS ion traps after 2004.

Wire bonding is commonly used to connect metal pads on MEMS devices with pads on a chip carrier. It forms a bond between a wire and a pad by application of ultrasonic energy via a vibrating tip. The bonding force, power and duration are key to good bonds as is surface and bonding tip cleanliness. The wirebonder I used is a Kulicke and Soffa, Inc. KS 4523 manual bonder. I used it with a wedge bonding tip and 0.001 inch diameter gold wire. Good bonds to 1 μm thick gold bond pads on silicon wafers required heating of the wafer to 80° C. Bonding parameters are device dependent. Good starting parameters for the NIST KS 4523 with 0.001 inch gold wire bonding to gold pads are as follows.

- static force: 18-20 grams
- bond parameters: Power, Force and Time set to 2.0-3.0 (arbitrary units). Slowly
 increase if necessary.
- use enough force to squash the wire slightly, with minimum power and moderate time.

Gold wire was obtained from California Fine Wire, Inc. The wire specification was 99.99% Au, 0.001 inch diameter, 0.5 to 2.0% elongation and spooled 90 feet per spool.

The effect of baking (200° C in air for several hours) on wire bonds was investigated. After a bake the bonds were still strong but the gold wires were noticeably softer and more malleable. Air bridges 2-4 mm in length did not collapse.

Gap welding is an alternative to resistive/ultrasonic welding when bonding to ~mm size structures whose surfaces that are not necessarily flat. It forms bonds by running current thru two metal parts clamped between two metal electrodes. The strongest bond is formed between dissimilar materials with respect to alloy and conductivity. This also seems to discourage sticking to the bonder electrodes. I used a resistive metal alloy called Advance (45% Ni, 55% Cu) as an intermediate conductor between some metals which are otherwise difficult to bond together: Au, Cu, Al, W. Note in particular that

gold doesn't bond well to gold, nor Advance to Advance. Advance is sold under several trade names including Constantan, Copel, Alloy 294 and Cupron. Advance is available under then name Constantan from Goodfellow, Inc. (p/n 564-050-99).

8.7.7.1 wafer dicing saw

A dicing saw was used to cut thick glass and bonded wafer stacks. Blades appropriate for cutting silicon are immediately destroyed by contact with glass. Instead, special purpose resin blades impregnated with tiny diamond particles were used. These blades are made by Thermocarbon, Inc. under the trade name Resinoid. Suggested part numbers are below. The cost per blade is \$50 in lots of 1.

- 2 25M-5B-46RU7-3 good for glass
- 2 25M-5B-46R7-3 good for ceramic substrates and ferrites
- 2.25M: blade diameter 2.250 inch
- 5B: blade width 0.0050 + /- 0.0003
- 46: diamond particle size 46 μm
- RU7: resin diamond matrix is soft/medium good for glass
- R7: resin diamond matrix is medium/hard good for ceramic substrates and ferrites

Some rules of thumb for dicing.

- Blade cut depth should be no more than 10 times the blade thickness.
- Dress a new blade by wearing 4-5 mil off its diameter by making successive cuts on a glass plate. This gives a good quality edge and prevents wafer chipping.

Advice for dicing delicate structures.

- Use a silicon blade for silicon parts and a Resinoid blade for glass and bonded glass-silicon stacks.
- Use wax to attach the process wafer to a sacrificial silicon backing wafer. See Section 8.7.1.3 on page 196.

- Vibration during dicing can damage delicate structures. This can be mitigated by embedding the structures in the same wax used to attach the backing wafer.
 Cut some wax into mm size fragments. With the wafer stack on a hot plate at 130° C, drop the wax bits on the process wafer atop the delicate structures.
 The wax puddles should not protrude > 100 μm above the wafer surface else the dicing saw has clearance problems.
- Dice the wafer.
- Release the chips from the backing wafer in solvent as in Section 8.7.1.3 on page 196.
- Put the chips in a Teflon chip carrier.
- Wash the chips with acetone to remove any remaining protective wax. Remove
 one chip at a time from the acetone. Squirt each with isopropanol and blow dry
 with a dry nitrogen jet. Do not let the solvents dry on the chips in the air.

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