NBS 50 kHz Phase Angle Calibration Standard

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- Ceramics
- Fracture and Deformation [3]
- Polymers
- Metallurgy
- Reactor Radiation

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NBS 50 kHz PHASE ANGLE CALIBRATION STANDARD

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A detailed description is given of the features of
an electrical phase angle calibration standard designed
for operation over a frequency span of 2 Hz to 50 kHz. The
phase resolution of this calibrator extends from just
below 2 millidegrees at the low end of the frequency range
to about 5 millidegrees at the high end. The uncertainty
in the phase angle is a function of frequency, amplitude,
and amplitude ratio of the two outputs. It varies from
5 - 50 millidegrees.

The phase angle calibration standard is a source of
two sinusoidal signals with an accurately known phase
angle between them. The signals are generated using
digital waveform synthesis and are programmable in
amplitude (0-100 V) and in frequency (2 Hz-50 kHz).
Operation is controlled from a front panel keyboard, or
remotely via an IEEE-488 bus interface, under control of a
microprocessor. Selected signal parameters are displayed
on an alpha-numeric readout and can be transmitted over
the bus.

To ensure accuracy, the system uses an auto-zero
feedback loop that compensates for residual differential
phase shifts in the output amplifiers. The compensation
scheme measures the departure of the output phase angle
from true quadrature, for a nominal 90-degree setting, and
applies a correction to the computation of the digital
sine wave synthesis.

key words: calibration; digital waveform synthesis; phase
angle; phase meter; sine wave generator; standard.

1. INTRODUCTION.

The present publication describes in detail the design and operation of an audio-frequency phase angle calibration standard, with a frequency range from 2 Hz to 50 kHz, constructed at the National Bureau of Standards (NBS). A previous version of this standard (with a maximum 5 kHz operating range) has been described in NBS Technical Note 1144 [1][1]. The development of these standards was undertaken because of a need to provide a high accuracy audio-frequency phase angle reference, so that both manufacturers and users of phase measuring equipment could obtain consistent measurements throughout industry and other user communities.

The work was sponsored, in part, by the Department of Defense through the Calibration Coordination Group (CCG) which has a particular interest in the phase angle standard. The publication of a detailed description of the instrumentation system was suggested by the CCG to encourage commercial production of a phase angle standard based on the NBS design.

The principle of operation was described in a 1978 paper [2] and many of the circuit details of the earlier, 5 kHz version can be found in [1]. The present publication contains a description of the changes in both hardware, software, and operating procedures for the 50 kHz version of the NBS Phase Angle Standard. The revised specifications are shown in table 1.1[2]

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[1]Numbers in brackets refer to the literature references listed at the end of this report.

[2]In order to describe the system discussed in this report adequately, commercial equipment and instruments are identified by their manufacturer's name or model number. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

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Phase Angle:

     Range   -999.999 to +999.999 degrees
     Resolution   0.0014 degrees
                                (1 part in 2^{18})

Systematic Uncertainty (Equal Amplitude)

at 60 Hz	0.003 degrees
at 400 Hz	0.004 degrees
at 5 kHz	0.008 degrees
at 15 kHz	0.016 degrees
at 30 kHz	0.027 degrees
at 50 kHz	0.040 degrees

Systematic Uncertainty (Amplitude Ratio 7:1)

at 60 Hz	0.004 degrees
at 400 Hz	0.006 degrees
at 5 kHz	0.011 degrees
at 50 kHz	0.080 degrees

Output Frequency:

Range	2 Hz to 50 kHz
Resolution	1 Hz up to 5 kHz; 10 Hz above 5 kHz
Accuracy	0.06 %
Stability	1 ppm

Output Amplitude:

Effective Range	0.5 to 100.0 V rms
Resolution	steps of approx. 2 mV, up to 7 V
	steps of approx. 24 mV, 7 to 100 V
Accuracy	0.1 %

DC Offset Voltage

                              < 0.5 mV for Outputs to 7 V rms
                              < 5 mV for Outputs 7 to 100 V rms

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Table 1.1 Performance Specifications

2. DESIGN CONSIDERATIONS.

This section presents a brief overview of the features of the 50 kHz Phase Angle Standard that are significantly different from those of the 5 kHz version. Further information can be found in the appropriate sections describing the hardware and software in more detail.

2.1 Waveform Generation

The Phase Angle Standard is a signal source of two sine waves that are synthesized from sets of digital data. The digital data are computed so that the phase angle between the resulting pair of sine waves is precisely determined, and the data are then converted to sinusoidal voltages by dual digital-to-analog converters. This process is described in detail in [1]. As in the first version of the Phase Angle Standard, 16-bit digital-to-analog converters are used for output frequencies up to 5 kHz; these converters have the advantage of generating waveforms with high phase resolution, but are limited to maximum conversion rates of 400 kHz. Because of settling time limitations, the 16-bit converters cannot cope with the higher conversion rates needed to produce low distortion sine waves with frequencies from 5 kHz to 50 kHz. Therefore, for the upper range of frequencies, waveform generation is carried out by faster, 12-bit converters which permit 10 times higher conversion rates. The increase in speed is obtained at the cost of some loss of phase angle resolution as a consequence of the shorter word length. The implications of 12-bit quantization of the data used for waveform reconstruction on the theoretical and practical limitations of angular resolution are more fully discussed in [3].

The timing requirements for operating in the higher frequency range demand not only higher speed digital-to-analog converters, but also a change in operating mode. When synthesizing sinusoidal waveforms up to 5 kHz, a pair of new digital values is computed every 2.5 microseconds, an interval long enough for calculations to be carried out in real time. Above 5 kHz, however, when using the 12-bit digital-to-analog converters capable of up to 4 million conversions per second, the available interval is not sufficient for real-time calculations. The sets of selected values from which the waveform is reconstructed must therefore be calculated ahead of time and stored in random access memory. The stored values can then be transfered to the digital-to-analog converters at the required speed.

2.2 Quadrature Phase Detector

One of the critical components of the Phase Angle Standard system is the quadrature phase detector. It is part of the auto-zero feedback loop which corrects residual differential phase errors in the output amplifiers. The 5-kHz version of the NBS Phase Angle Standard uses resistive attenuators as part of the phase detector which are adequate for the lower frequency range, but unsuitable for the extended range up to 50 kHz. Therefore, the phase detector circuit has been redesigned to use binary inductive voltage dividers to

attenuate the signals to the appropriate levels. These voltage dividers are constructed with special torroidally wound transformers chosen for their low inherent phase errors [4].

Because inductive voltage dividers tend to saturate in the presence of even small dc currents, dc offset voltages in the signals to be attenuated have to be nulled. The dc offset in each channel is effectively removed by injecting a compensating current into the output amplifiers. The compensating current is adjustable under software control, and its magnitude is computed based on iterative measurements of the dc offset voltage by the system.

2.3 Instruction Set

The set of operating instructions for the Phase Angle Standard has been divided into two subsets; the Phase Calibration (normal) Mode and the Test (diagnostic) Mode. The first subset is almost identical with the operating instructions given in [1]; the diagnostic subset is designed to help with trouble-shooting procedures and provides more direct access to some of the hardware. The instruction set is more fully explained in chapter 3 below.

2.4 IEEE-488 Bus

An interface has been provided for a connection to an IEEE-488 bus which allows the Phase Angle Standard to be controlled remotely. Commands can be transmitted to the Phase Angle Standard and status information and messages can be returned to the instrument controller. Further details are given in chapter 5 on Hardware and chapter 6 on Software.

3. OPERATING INSTRUCTIONS

3.1 External Connections

(a) Power Cord. The power cord for the 120-volt 60-hertz line plugs into a receptacle at the left rear of the instrument. A 15-volt standby power supply is always energized whenever the cord is connected to the line.

(b) Output Connectors. The Reference and Variable output voltage signals are available through the lower two BNC connectors at the rear of the instrument.

3.2 Front Panel Controls

(a) Power Switch. The toggle switch on the left-hand side of the front panel controls a solid-state relay which connects the 120-volt power line to the instrument power supplies.

> Note: A 15-volt power supply remains on even when the switch is in the "off" (stand-by) position to provide the control current for the solid-state power relay.

(b) Keyboard. The Phase Angle Standard is operated from push-button keys on the front panel arranged as a 12-button Command keyboard and a 12-button Numerical keyboard. Ease of operation was an important criterion in the design and layout of the controls. In the normal phase angle calibration (PHASE CAL.) mode, the desired function is selected by pressing a command key and the operating parameters are then entered on the numerical keyboard. Details of these key entry sequences for various functions are shown in diagrammatic form in tables 3.1 to 3.6. Additional information can also be found in chapter 3 of [1]. With minor exceptions the main operating procedures are the same for the 5 kHz and 50 kHz versions of the Phase Angle Standard.

(c) STOP and RUN. In the normal (PHASE CAL.) mode the STOP and RUN function perform the following actions:

Actuating the STOP key inhibits further computation by the waveform generating microprocessor and sets the output amplitude to zero on both channels. Also, the default restart address of this microprocessor, "06," is set up internally and displayed on the readout. The address can be changed, if desired, by entering two hexadecimal digits. (For instance, a program starting at address "A0" provides dc output voltages proportional to phase angles or offset angles entered from the keyboard. This program can be used to test the digital-to-analog converters.)

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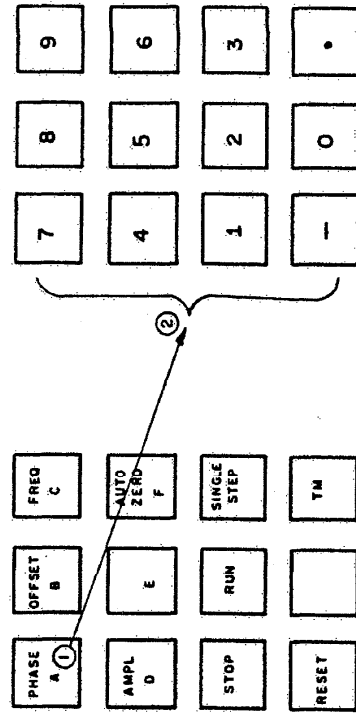
PHASE ANGLE

① Select PHASE function.

② Enter phase angle on numeric keyboard.

   Note: (a) Range: - 999.999 to 999.999 degrees.

   Note: (b) 3 digits after the decimal point must be entered to complete entry.

   Note: (c) If 3 digits are entered ahead of the decimal point, the decimal point will be entered automatically.

③ Repeat step② to enter new phase angle.

④ To correct entry before entry is completed, repeat steps① and ②

Table 3.1

OFFSET ANGLE
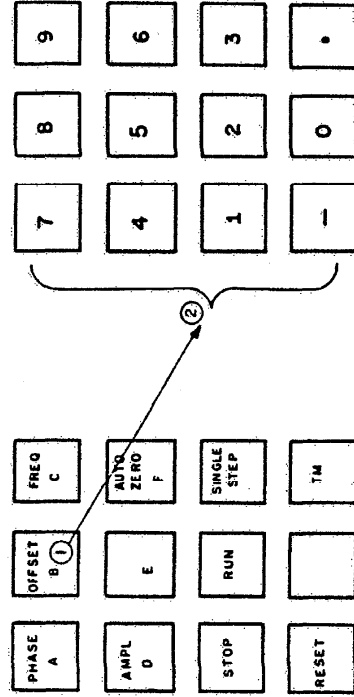
① Select OFFSET function.

② Enter offset angle on numeric keyboard.

   Note: (a) Range: 999.999 to 999.999 degrees.

   Note: (b) 3 digits after the decimal point must be entered to complete entry.

   Note: (c) If 3 digits are entered ahead of the decimal point, the decimal point will be entered automatically.

③ Repeat step② to enter new offset angle.

④ To correct entry before entry is completed, repeat steps① and②.

Table 3.2

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AMPLITUDE SETTING (PHASE CAL. MODE)
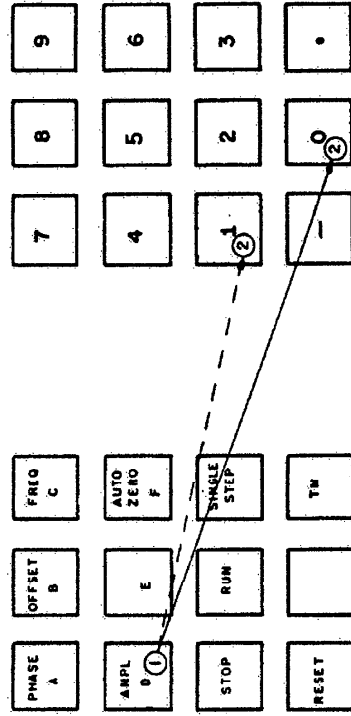
① Select AMPLITUDE function.

② Select either channel "0" (Reference), or channel "1" (Variable).

③ Enter 4-digit output voltage (Volts, rms).

   Note: Ranges 0.000 to 7.071
                  7.080 to 99.99
                  and 100.0

     Note: Amplitude setting displayed on readout is rounded to 12-bit resolution.

④ Repeat step ③ to enter new amplitude on the same channel.

⑤ To correct entry before entry is completed, repeat steps ①, ②, and ③.

Table 3.4

FREQUENCY

① Select FREQUENCY function.

② Enter frequency in Hz.

   Note: Range 2.Hz to 50000.Hz.

③ Enter decimal point to complete entry.

④ Repeat steps ② and ③ to enter new frequency.

⑤ To correct entry before entry is completed, repeat steps ①, ②, and ③.

Table 3.3
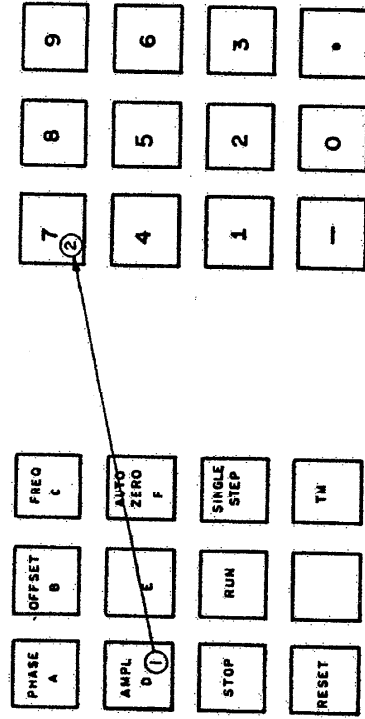
SEVEN-VOLT MODE

① Select AMPLITUDE function.
② Enter "7".

Note: The seven-volt mode connects the output of the filter amplifier directly to the output to provide a nominal 7.071 V rms.

Table 3.5

AUTO-ZERO
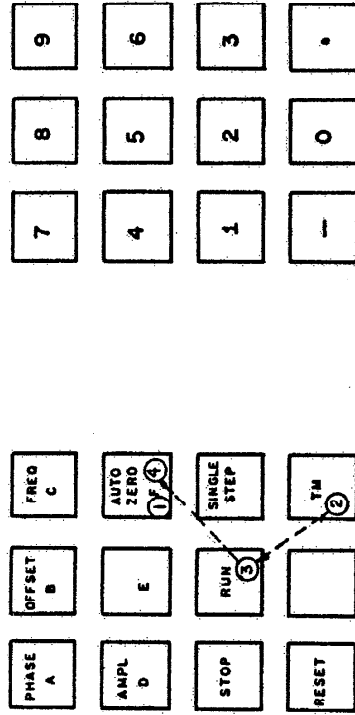
① Select AUTO-ZERO function.

Notes: (a) The auto-zero function should be activated whenever
    (i) one amplitude is changed, or
    (ii) both amplitudes are changed, or
    (iii) the frequency is changed from the 2 Hz to 5 kHz range to above 5 kHz, or vice versa.

    (b) To display corrections determined at each iteration of the auto-zero procedure, the TEST MODE must have been activated prior to selecting the AUTO-ZERO function by the following procedure:

② Select TEST MODE.
③ Select normal mode [RUN Key].
④ Select AUTO ZERO.

Table 3.6

When the RUN key is subsequently pressed, the amplitudes are restored to their previous values, and the waveform generating microprocessor restarts at the address indicated ("06" for normal operation).

Note: If the RUN key is activated without first operating the STOP function, an error condition will exist because no starting address for the microprocessor has been set up. The error condition can be cleared by operating any other (valid) command key.

(d) RESET. The RESET key is linked directly to the display and keyboard control microprocessor and restarts the Phase Angle Standard to its default (power-on) setting, whatever its present state. It can be used to reinitialize the system in case of a temporary malfunction, or if the system does not restart by itself after external power is interrupted.

(e) Test Mode. In addition to the normal operating mode (PHASE CAL. MODE), the Phase Angle Standard can be switched to a TEST MODE. This mode allows more direct interaction with certain hardware components for diagnostic purposes. It provides the capability to access microprocessor memory locations which store the signal amplitude and attenuator settings in binary form and to modify these values from the keyboard. With a suitable choice of entered values, individual bit-lines leading to the output amplitude and phase detector attenuator control can be checked (using the AMPL key or the PHASE key respectively). At the same time the relays associated with these functions can be tested.

Other test functions available in the TEST MODE permit exercising of the signal channel interchange relay which is located at the input to the phase detector circuit (using the STOP key), digital measurement of the phase detector output (SINGLE STEP key), manual and automatic adjustment of the dc offset in both output channels (OFFSET key), and changing the tolerance and delay parameters used with the auto-zero procedure (blank key between RESET and TM).

The TEST MODE also provides a readout of the auto-zero correction determined by the system at both the auto-zero frequency and the current operating frequency (AUTO ZERO key). This information is useful as a check of the auto-zero performance.

To accommodate the instructions for the extra functions of the test mode and entry of hexadecimal numbers without adding additional keys, multiple key-stroke commands are necessary. These begin with the TM key (lower right-hand command key) followed by one or more command keys and hexadecimal number entries. Details of key-stroke sequences required for various functions can be found in tables 3.7 to 3.14.

Note: For hexadecimal entries in the TEST MODE, the command keys marked A to F are used in addition to the numerical keyboard.

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PHASE DETECTOR ATTENUATOR SETTING
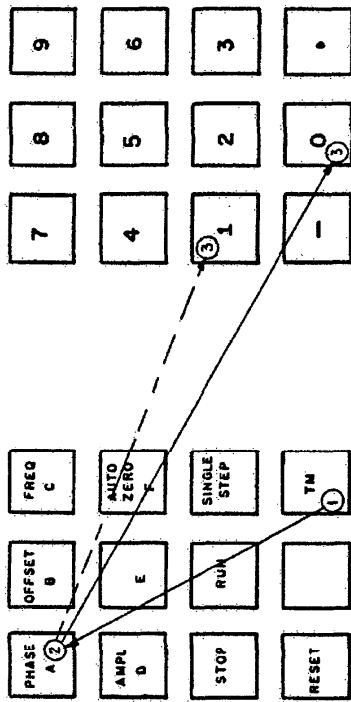
① Select TEST MODE.

② Select PHASE Detector Attenuator.

   Note: Display shows position of channel reversing switch.

③ Select either channel "0" (REF), or channel "1" (VAR).

④ Enter four hexadecimal digits.

   1st and 2nd digit - 00 to 7F control attenuator relays
   3rd digit - no function
   4th digit - if digit is odd (least significant bit "High")-low range
                                                    (0-7 volts)
            - if digit is even (least significant bit "Low")-high range
                                                    (7-100 volts)

Note: The attenuator is disconnected if bit 1 is "High"
      (4th digit is either 2, 3, 6, 7, A, B, E, or F)

Table 3.7

AUTOMATIC PHASE DETECTOR ATTENUATOR SETTING
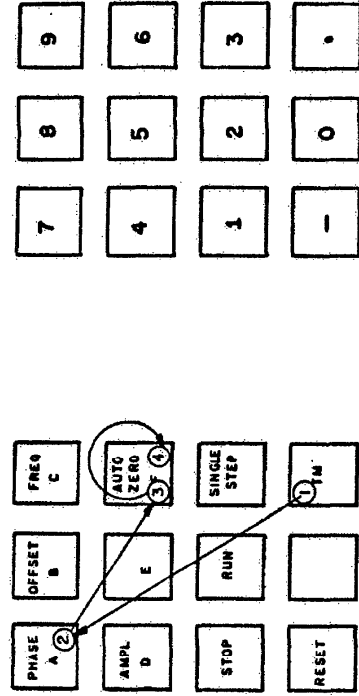
① Select TEST MODE.

② Select ATTENUATOR.

③ Set both attenuators automatically to appropriate values for
   auto-zero operation and display channel "0" setting.

④ Display channel "1" setting.

Note: Second line of display shows position of channel reversing switch.

Table 3.8

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AUTOMATIC DC OFFSET CONTROL

① Select TEST MODE.

② Select DC OFFSET.

③ Select Automatic Operation.

④ Select either channel "0" (REF) or
   channel "1" (VAR).

Note: Second line of display shows dc offset as measured by "Digitizer".
      (Hexadecimal numbers in two's complement).

Table 3.10

DC OFFSET CONTROL
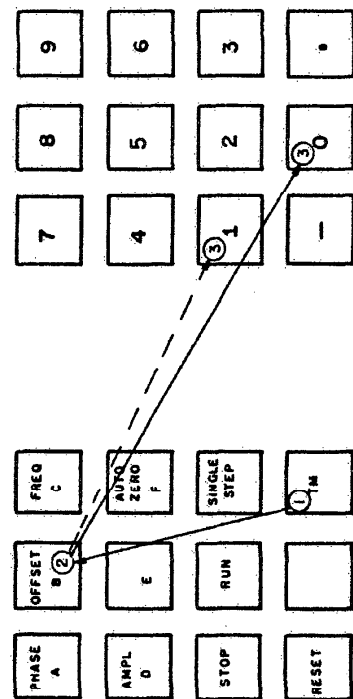
① Select TEST MODE.

② Select DC OFFSET.

③ Select either channel "0" (REF.) or
   channel "1" (VAR).

④ Enter two hexadecimal numbers.

Note: Second line of display shows dc offset as measured by "Digitizer".
      (Hexadecimal numbers in two's complement).

⑤ Repeat step④ if desired.

Table 3.9

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DISPLAY OF AUTO-ZERO CORRECTION
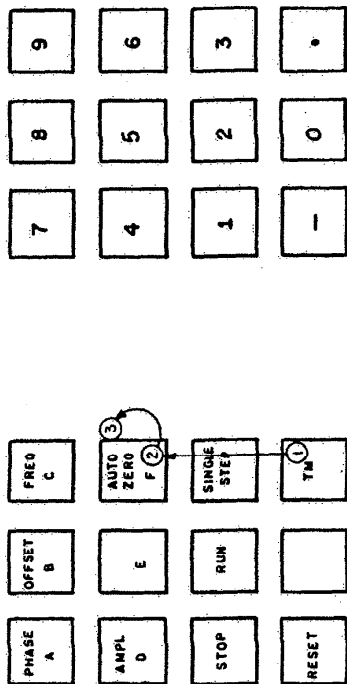
① Select TEST MODE.
② Display auto-zero correction adjusted for selected output frequency.
③ Display auto-zero correction as determined at 4096 Hz or 32.77 kHz.

Table 3.12

AMPLITUDE SETTING (TEST MODE)

① Select TEST MODE.
② Select AMPLITUDE.
③ Select either channel "0" (REF) or channel "1" (VAR).
④ Enter 4-digit hexadecimal numbers.

Repeat step ④ if desired.

Hexadecimal Amplitude Control Format:

BITS:	1st Digit				2nd Digit				3rd Digit				4th Digit			
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

```
0    12-Bit Amplitude                          Range
```
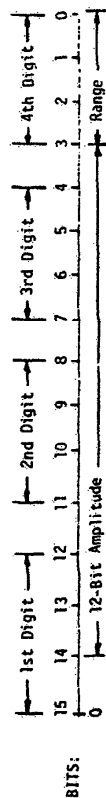
```
0-7 V Range     Bit 0 High
7-100 V Range   Bit 0 Low
7-Volt Range    Bit 0 & Bit 1 High
16-Bit Converter Bit 2 Low
12-Bit Converter Bit 2 High
```

Table 3.11

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RETURN FROM TEST MODE TO NORMAL OPERATING MODE

Keypad: PHASE A | OFFSET B | FREQ C

AMPL D | E | AUTO ZERO F

STOP | RUN ② | SINGLE STEP

RESET | | IM ①

Numeric keypad: 7 8 9 / 4 5 6 / 1 2 3 / - 0 .
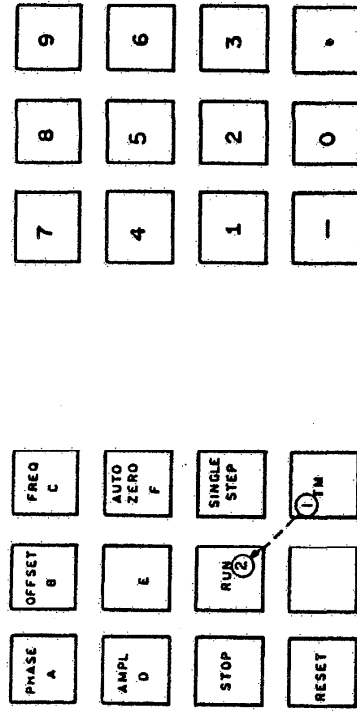
① From any TEST MODE operation.
② Select PHASE CAL. MODE [RUN key].
   (Normal operating mode).

Table 3.14

CHANNEL REVERSING SWITCH
(of PHASE DETECTOR)

Keypad: PHASE A | OFFSET B | FREQ C

AMPL D | E | AUTO ZERO F

STOP ④② | RUN | SINGLE STEP

RESET ③ | | IM ①

Numeric keypad: 7 8 9 / 4 5 6 / 1 2 3 / - 0 .
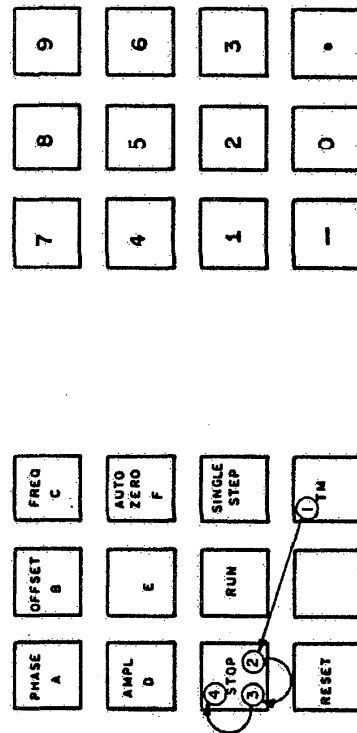
① Select TEST MODE.
② Select CHANNEL SWITCH [STOP key].
③ NORMAL position.
④ REVERSE position.

Table 3.13

DIGITIZER (A/D CONVERTER)

① Select TEST MODE.
② Convert and display output from Phase Detector Circuit Board [SINGLE STEP Key].

Note: Repeat step ② for additional conversions.

Table 3.15

READING DELAY (WAIT) AND AUTO-ZERO
TOLERANCE ADJUSTMENT

① Select TEST MODE.
② Select delay time (WAIT).

Enter 4-digit hexadecimal number   (decimal equivalent ≈ milliseconds).

③ Select auto-zero tolerance.

Enter 4-digit hexadecimal number.

Note: (a) Number entries are optional and can be repeated to make changes in delay time or tolerance setting.

(b) A "0000" entry will set default values for either delay time or tolerance.

Table 3.16

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3.3 Error Messages

Table 3.17 shows the error messages the system can display and the remedial action to be taken.

ERROR MESSAGE	FAULT	REMEDIAL ACTION
HIGH FREQUENCY	Frequency selected above 50 kHz	Enter correct frequency
LOW FREQUENCY	Frequency selected below 2 Hz	Enter correct frequency
HIGH VOLTAGE	Amplitude selected above 100 volts	Enter correct amplitude
SYSTEM STOPPED	Waveform generating processor clock stopped	Push 'STOP,' then 'RUN,' enter frequency, or 'RESET'
FIFO FULL	Command register overflow	Reset system, push 'RESET'
DC OFFSET	Dc offset adjustment out of range	Readjust dc offset controls on the appropriate Output Circuit Board
PROM 1 (2,3,4,5)	Read-only memory faulty or misread	Retry 'RESET,' if fails, replace PROM integrated circuits (Ckt. Bd. D11)
UNDEFINED FUNCT.	Illegal entry	Re-enter command or parameter

Table 3.17 Error Messages

4. OPERATING PRINCIPLES

4.1 Introduction

As already briefly mentioned in chapter 2, the Phase Angle Standard generates two sinusoidal output waveforms with an adjustable and accurately known relative phase angle. The output sine waves can be applied directly to a phase meter under test to check its calibration.

The phase angle, frequency, and amplitudes for each channel can be set from the front panel keyboard or from a controller using the IEEE-488 bus. The key strokes entered, or message data bytes sent over the IEEE-488 bus, are interpreted by an 8-bit microprocessor that converts the ASCII format of the commands and operating parameters into an internal binary code. The internal code in turn controls the functions of the Phase Angle Standard and routes commands and data over various busses or dedicated lines. A generalized block diagram of the system is shown in figure 4.1.

The output waveforms are generated by a digital signal processor consisting of a high-speed 20-bit microprocessor, dual-channel digital-to-analog converters, low-pass filters, and amplifiers. The internal arrangement of the 20-bit processor and its instruction code are described in detail in chapter 5 of [1].

4.2 Method of Signal Generation

The output waveforms are generated by direct digital synthesis. Sets of data points, spaced at equal time intervals along the waveforms, are calculated so that they correspond to instantaneous values of the amplitude, as shown in figure 4.2. The digital data are converted to voltages using dual-channel digital-to-analog converters followed by amplifiers with appropriate filtering to remove the harmonic components introduced by the sampled-data process. A more complete description of the basic waveform generation scheme can be found in [1]. As pointed out already in chapter 2, the details of the process vary somewhat with the frequency range.

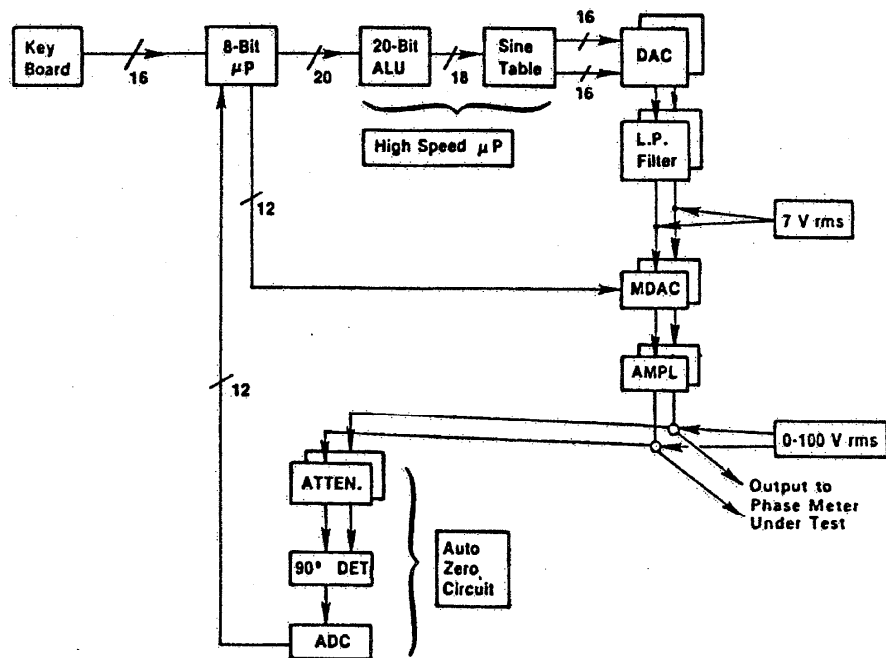**Functional Block Diagram of NBS Phase Standard**

Figure 4.1
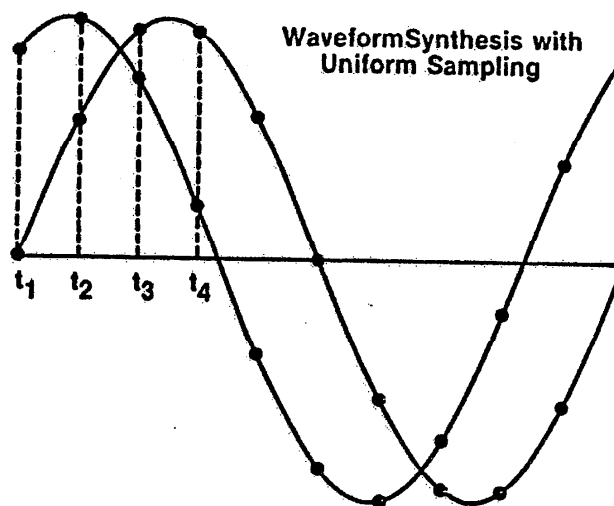
Figure 4.2

4.2.1 Signal Generation from 2 Hz to 5 kHz

For sinusoidal output frequencies up to, and including, 5 kHz, the digital data from which the waveforms are synthesized are computed in real time. The number of sample points per waveform is selected from a binary sequence with 64 samples at the highest frequency, 5 kHz, and increasing up to 131072 samples at 2 Hz. The number of samples is chosen so that the sampling rate remains in the band from 200 kHz to 400 kHz for all sinusoidal output frequencies in the range from 2 Hz to 5 kHz. Referring to figure 4.2, the sampling points, t_i, along the time axis are equivalent to "instantaneous" phase values for each sinusoid, referenced to the appropriate zero crossing. The choice of the two initial phase values, at time t_1, then determines the relative phase angle of the output waveforms. The calculations for a set of data points involve the following steps:

(a) determination of the "instantaneous" phase value for each of the two waveforms,

(b) computing the sine function for the instantaneous phase values,

(c) storing the computed values for each channel so that they are available to be applied to the digital-to-analog converters at the proper time, and

(d) determining the appropriate sampling time intervals.

(a) Two 20-bit accumulators, one for each channel, compute and store the instantaneous phase values. The initial value loaded into the accumulator is the binary equivalent of the phase angle (or offset angle) entered through the keyboard. For each subsequent data point, a phase increment (equivalent to 360 degrees divided by the number of sample points per waveform) is added until the waveform is completed. To start the next waveform, the initial phase value, or a new value, is reloaded into the accumulator and the computing procedure is repeated.

(b) The instantaneous phase values from the accumulator are converted to their corresponding sine function using a look-up table and interpolation algorithm which is implemented in a special hardware module. The resulting angular resolution is 2^{18} (0.0014 degrees) and the sine value is expressed as a 16-bit, two's complement number. The total conversion time is less than 400 ns. The Angle-to-Sine/Cosine Converter circuit board is described in more detail in [1].

(c) The pair of sine values required for each data point are calculated sequentially, and the results of the calculation are stored in corresponding locations of two banks of 1024-word random access memories. The modulo-1024 memory address register, pointing to the current location in memory, is incremented after every read operation, so that every memory location is traversed in rotation.

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(d) During a memory read operation a strobe pulse, derived from a crystal controlled frequency synthesizer, latches the 16-bit data into each digital-to-analog converter channel. The synthesizer has four decimal digits of resolution in each of the two frequency ranges used (200-400 kHz; 2-4 MHz), and the strobe frequency is set by the 8-bit system control microprocessor. The microprocessor uses a look-up table to determine the number of sample points per waveform, and then calculates the strobe pulse rate so that the desired sinusoidal output frequency of the Phase Angle Standard is obtained .

The numerical data latched into each converter channel are held stable until the next strobe pulse enters new data. During the stable period, the data are fed to the digital-to-analog converters and are finally converted into output voltages while at the same time the next pair of values is computed.

4.2.2 Signal Generation from 5 to 50 kHz

While it is necessary to store only one digital word at a time for each channel for outputs up to 5 kHz, the entire set of points on a particular waveform must be stored in the random access memory for the frequency range from 5 kHz up to 50 kHz . Complete waveform storage is necessary because the digital-to-analog conversion rate required at these frequencies does not provide a long enough time interval between data points for real-time calculations.

Each data point of a set that defines the waveform is computed and stored in one of the 1024 locations of the memory bank using the same procedure as for low frequency generation. The strobe frequency (timing pulse rate) is set equal to one tenth of the final conversion rate which leaves enough time to carry out the calculations. As soon as all the data are stored, further computation is inhibited by trapping the waveform generating microprocessor in a "do-nothing" program loop. The strobe pulse rate from the independent frequency synthesizer is then increased by a factor of ten, so that the output sine wave of the Phase Angle Standard has the desired frequency. This rate change is accomplished by changing the least significant bit of the range setting which switches the crystal controlled frequency synthesizer to its next higher range (x100 kHz to x1 MHz).

As before, the number of data points per waveform is selected from a binary sequence with a minimum of 64 samples at the highest output frequency, 50 kHz, and increasing the number of samples to 1024 at output frequencies just above 5 kHz. The choice is made so that the resulting sampling rate (strobe frequency) falls in the 2-to 4-MHz band.

4.3 Digital-to-Analog Converters

To accommodate the conversion rates for both frequency ranges, two types of digital-to-analog converters are necessary. For output frequencies from 2 Hz to 5 kHz, a 16-bit converter is used which settles in 2.5 microseconds, the minimum time interval between strobe pulses in that range. The advantage of the 16-bit digital-to-analog converter is its inherent low quantization noise and therefore lower harmonic distortion in the sine waves synthesized from its output. Also, the 16-bit word length, coupled with a minimum number of 64

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samples per waveform, permits a theoretical phase resolution of better than 0.001 degrees with the waveform reconstruction scheme employed [3].

In the upper frequency band, from 5 kHz to 50 kHz, the available time between strobe pulses can be as short as 0.25 microseconds, so that faster 12-bit digital-to-analog converters must be used. The 12-bit wordlength limits the theoretical phase resolution that can be achieved and raises the harmonic distortion of synthesized sine waves because of higher quantization noise. However, with 64 samples per waveform, theoretical analysis shows that an average resolution of better than 0.005 degrees is still possible (see reference [3]).

The stepped sine waves produced by either the 16-bit or 12-bit digital-to-analog converters are passed through low-pass filters which remove the harmonics introduced by the sampled-data process. For each converter type, separate active filters are used with cut-off frequencies appropriate for the respective sampling rates.

4.4 Output Amplifiers

As shown in figure 4.1, the seven-volt signal passes from the active low-pass filter to the programmable amplitude control (multiplying digital-to-analog converter, MDAC in the figure) where it is attenuated with a resolution of 2^{12} steps. The attenuated signal is then passed through a low-voltage amplifier to provide 0 to 7.07 volts at the output terminal. For output voltages from 7.07 to 100 volts, an additional amplifier is inserted into the signal path with a (nominal) fixed gain of 14.14. Because the additional amplifier introduces a 180-degree phase shift, a compensating adjustment in the output phase angle is made by the waveform generating microprocessor.

The gain-adjustable amplifiers can be bypassed by selecting the SEVEN-VOLT-MODE from the keyboard. The output is then taken directly from the active filter with a nominal amplitude of 7.071 volts. To minimize differential phase shifts caused by the amplifiers, both channels are simultaneously switched to the Seven-Volt-Mode. Resetting either channel to a different amplitude also switches the other channel from the Seven-Volt Mode to the gain-adjustable mode at a nominal amplitude setting of 7.07-volt.

4.5 Auto-Zero Correction

The output amplifiers, and particularly the filter circuits, are carefully matched so that corresponding channels on the two output circuit boards have nearly identical frequency response characteristics. The match cannot be perfect, however, and small residual differential phase errors will remain and have to be corrected. The auto-zero procedure measures the deviation from the ideal response at quadrature and applies the result of the measurement to the waveform generating circuits in the form of a digital phase angle correction.

Because of the well matched filter characteristics, the differential phase errors vary essentially linearly with frequency in each of the two frequency ranges. It is therefore sufficient to carry out the auto-zero determination at only one frequency in each range, and the appropriate

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correction for the actual frequency in use is then calculated. The two values chosen for the auto-zero determination, 4096 Hz and 32.77 kHz (32768 Hz rounded up), are convenient, numerically, for calculating the corrections at other frequencies. Also, these frequencies lie near the upper end of their respective ranges where the error is larger.

The iterative auto-zero procedure repeatedly determines the departure from true quadrature of the output of the Phase Angle Standard and applies a correction to the waveform generator until the quadrature error falls within preset tolerances. The default values of the tolerances for the low and high frequency ranges are approximately equivalent to 2.75 and 5.5 millidegrees respectively.

To eliminate any possible errors in the phase detector itself, measurements are made at +90 and -90 degrees, and again with the signal channels interchanged. Internal feedback in the phase detector compensates for possible dc offsets in the input signals, reversing the 90-degree angles compensates for dc offsets in the output of the phase detector, and interchanging channels compensates for possible phase offsets in the detector circuitry.

Before actually measuring the quadrature error, the auto-zero procedure performs a self-calibration to determine the sensitivity of the detector circuit for the particular signal amplitudes applied. The sensitivity calibration factor establishes the relation between the phase detector output voltage and the angular correction necessary to modify the output of the waveform generator. To prevent overshoot when the correction determined by this procedure approaches its final value, the incremental angular correction resulting from the iteration is reduced below the calculated value (by a factor of two) when the quadrature error is within twice the tolerance value. This more gradual approach to the final value generally will add only one or two additional iterations, but, on the other hand, it will prevent prolonged oscillation around the final level of the correction in most cases.

Since the phase detector must handle a wide range of input signals, programmable attenuators condition the signal in each channel. As indicated in chapter 2, the attenuators consist of specially wound torroidal, 7-bit, binary inductive voltage dividers that have very low inherent phase shift. The input and the output of the dividers are buffered with operational amplifiers. When the Phase Angle Standard is not in the auto-zero mode, the attenuators are disconnected from the circuit, but the phase detector input amplifiers always remain in the circuit so that they present a constant load to the outputs of the Phase Angle Standard. With the attenuators disconnected, either signal from the output of the Phase Angle Standard can be routed through the phase detector input amplifier directly to the digitizing circuit to measure its dc-offset voltage.

The voltage output from the phase detector circuit board is connected to the Digitizer Circuit Board (A13), where it is filtered and amplified by an instrumentation amplifier before being digitized using a 12-bit, dual-slope analog-to-digital converter. The filtering removes the ripple from the quadrature detector stage during the auto-zero determination and removes the ac component from the signal when measuring the dc offset. A differential input connection prevents small voltage differences between ground planes of the two circuit boards from introducing offsets into the signal.

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After the final auto-zero correction has been determined, the output phase angle is set to zero and the frequency originally selected is restored. The correction is adjusted for the frequency in use, and it is applied automatically to any subsequent phase angle setting until another auto-zero procedure is performed.

5. 50-kHz HARDWARE MODIFICATIONS.

5.1 General Remarks.

In redesigning the NBS Phase Angle Standard to extend its frequency range to 50 kHz, it was possible to use the same backplane connections as in the 5-kHz version of the standard with few exceptions. This was a convenience, particularly during the transition stage when both sets of circuit boards could be operated in the same system. As development work progressed, a few additional backplane connections were installed without destroying the compatability with the circuit boards of the 5-kHz version.

To reduce heat and power dissipation, all relays on the Output and Phase Detector circuit boards are of the latching type, and the necessary switching pulses are generated by a combination of relay driver logic hardware and software. Major circuit changes involve the Output, Phase Detector, Digitizer, and Memory-Latch boards. Only relatively minor modifications have been necessary in the Synthesizer (strobe pulse generator) and microprocessor circuit boards. A special board has been added for the IEEE-488 bus interface. The arrangement of the circuit boards in the card cage as viewed from the front panel access door is shown in figure 5.1

5.2 Output Circuit Board.

The circuit boards located in position A7 and A9 generate the two Phase Angle Standard output voltages. These two boards are identical and contain the analog waveform generating circuits and the amplitude control circuits (figure 5.2a).

5.2.1 Waveform Generating Circuits

The digital data, from which the output waveform is generated, are transfered from memory to a set of latches on the Memory-Latch circuit board (D4) with every strobe pulse. The output data from these latches is then connected by separate, dedicated 16-bit busses to the Output Circuit Boards (A7 and A9) where the data are again latched into a pair of octal registers, U1-U2. The double latching buffers the data and helps to reduce noise picked up during transfer from the Memory to the Output circuit. The second latch delays the information by an additional clock (timing pulse) period but does not affect the throughput rate.

As shown in the circuit diagram, figure 5.2, the input pins of the 16-bit and 12-bit digital-to-analog converters (U3 and U4) are connected in parallel to the output of the 16-bit latches so that the 12 most significant bits always feed both converters simultaneously. The current outputs of each converter are connected to the summing junction of a separate active filter (AR2-AR3 and AR1) which has a 3-dB frequency of 25 kHz (4-pole Butterworth) or
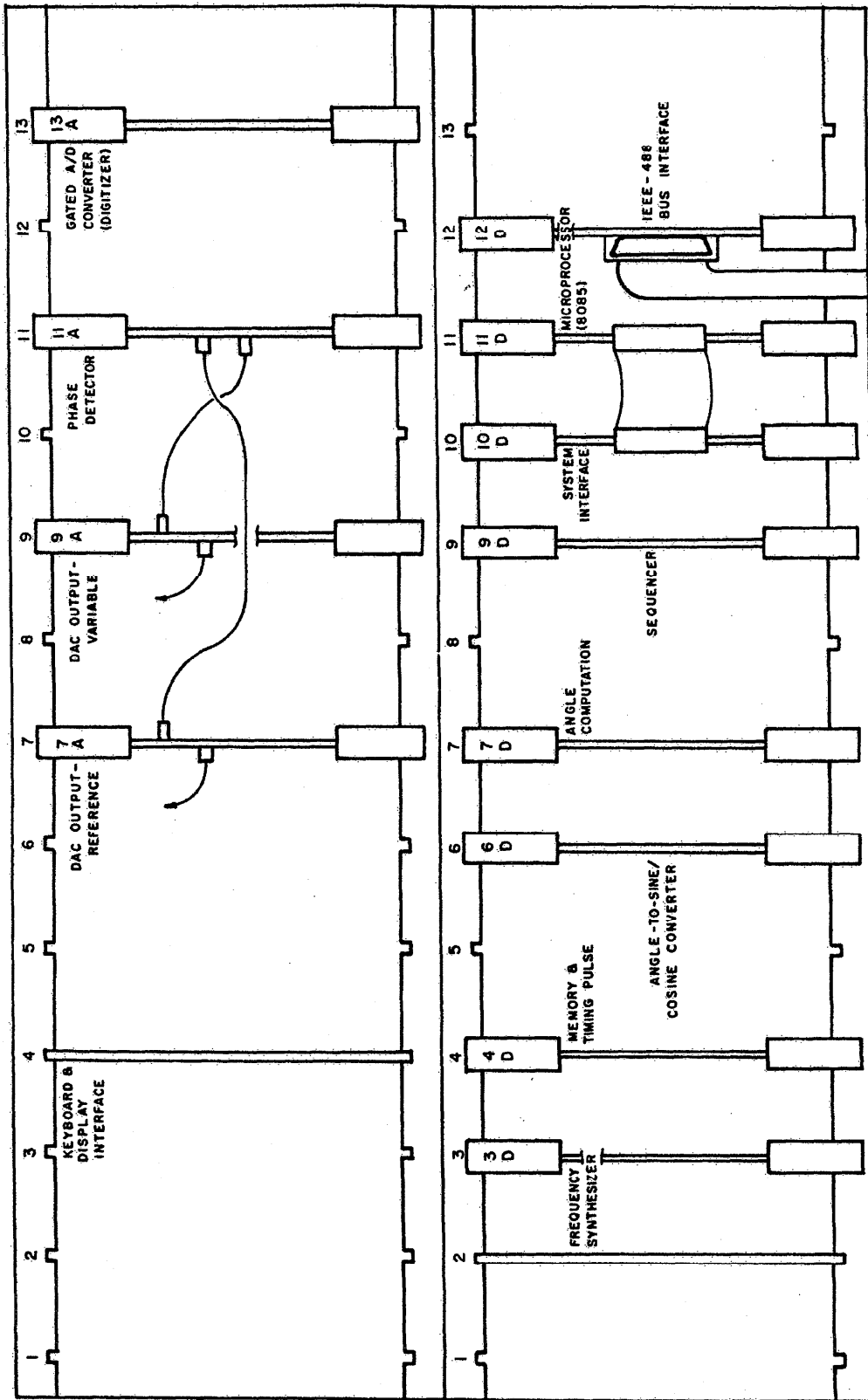
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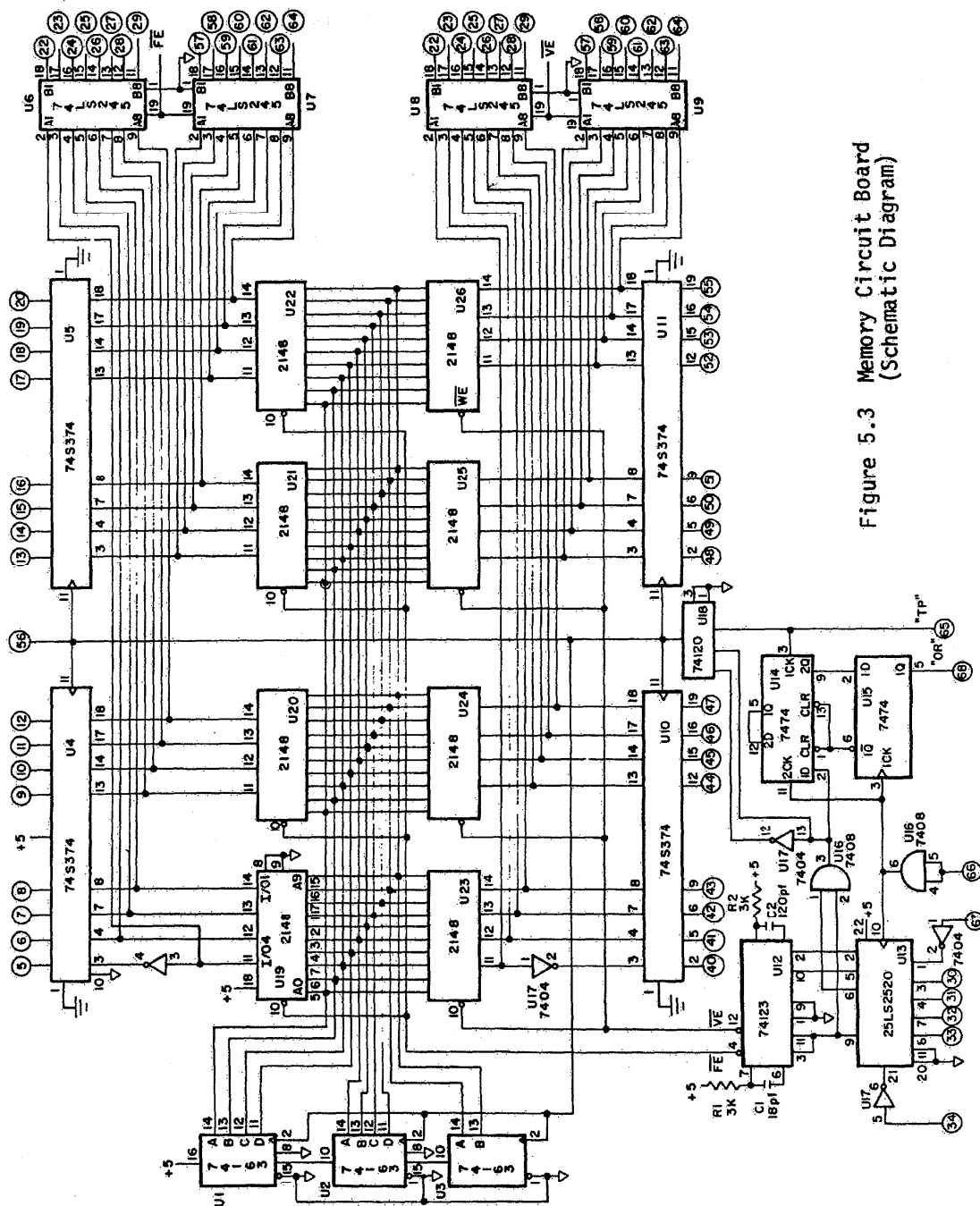Figure 5.1 Circuit Board Arrangement, Card Cage (Front View)

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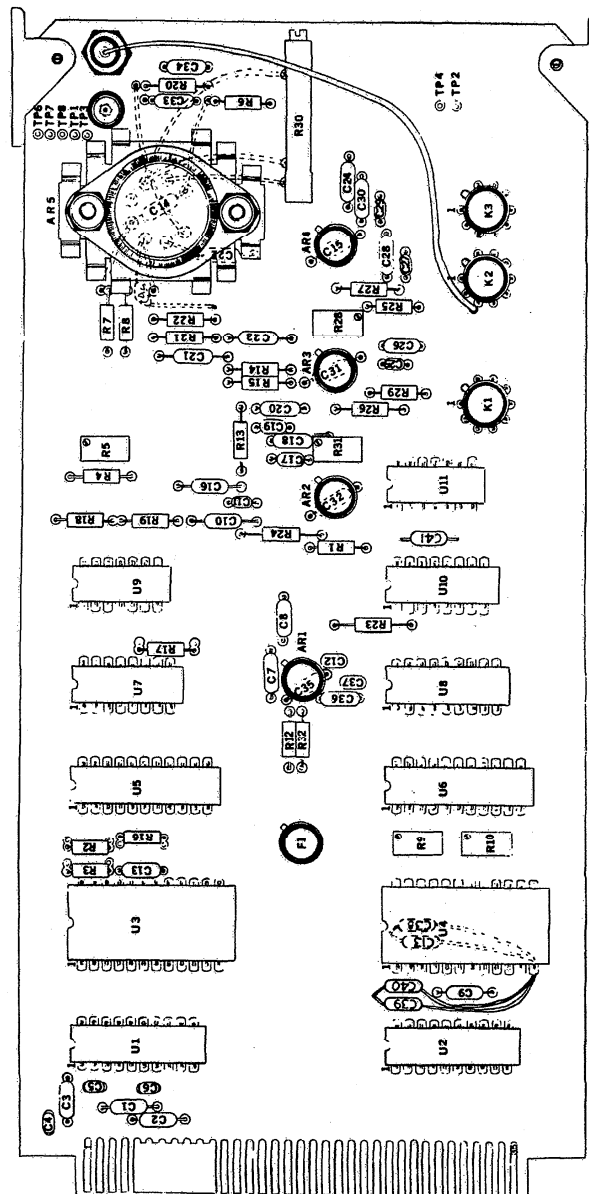Figure 5.3 Memory Circuit Board
(Schematic Diagram)

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Figure 5.2(b) Output Circuit Board (Parts Layout)

310 kHz (2-pole Butterworth) for the 16-bit and the 12-bit channels respectively. Both converters produce an analog output waveform at all times, irrespective of the selected frequency range, though only the appropriate converter is connected through a relay (K1) to the rest of the circuitry.

5.2.2 Amplitude Control

The programmable amplitude control and associated amplifiers are common to the signal paths from both the 16-bit and 12-bit converters. From the active filter the signal is routed through relay (K1) to a 12-bit multiplying digital-to-analog converter (U8) which is configured as a resistive attenuator with 2^{12} steps, providing output voltages from 0 to 7.069 volts in approximately 2 millivolt increments. Depending on the position of a second relay (K2) in the signal path, the attenuated voltages can be fed either to the output connector of the Phase Angle Standard, or switched (through relay K3) to the high voltage amplifier (AR5) which has a fixed gain of 14.14 and provides outputs from 7.1 to 100 volts.

The amplitude control information, range selection, and dc offset adjustment are encoded on a 16-bit bus in a binary format as shown in table 5.2 which gives examples of the composite code formats. If the bus information contains amplitude control settings, this is indicated by bit 15 being "low." Bits 3 to 14 then contain the 12-bit digital input to the multiplying digital-to-analog converter. At the same time, the amplitude range selection is controlled by setting bit 0 "high" for the low-voltage range or "low" for the high-voltage range. For the Seven-Volt-Mode, both bit 0 and bit 1 are set "high," thereby selecting the appropriate relay connections which bypass the amplitude control multiplying digital-to-analog converter, and the information in bits 3 to 14 then has no effect on the output voltage. The selection of the 16-bit or 12-bit conversion channel is encoded in bit 2 which is set "low" for the 16-bit converter. If the bus contains dc offset information, bit 15 is set "high," and bits 7 to 14 then contain the 8-bit control setting for the dc-offset adjustment.

The 16-bit bus is connected to latches U5-U6, for the amplitude and range information, and also to the digital-to-analog converter used for dc-offset control, U7, which has its own internal latch. As mentioned, the most significant bit, edge connector pin 13, selects the two functions by enabling either the latches or the 8-bit digital-to-analog converter. The range information is further decoded by U10 which also generates the pulses to operate the relays using the software controlled pulse signal at edge connector pin 31.

The digital-to-analog converter for the dc-offset compensation has an actual output voltage range from 0 to +10 volts. This range is modified to provide an effective range from -5 to +5 volts by applying a fixed negative 5-volt bias through resistor network R18-R19. The converter voltage output, and the the bias voltage, are connected through high-value resistors (R3 and R17) to the summing junctions of the two active filter input stages with the resistors chosen to provide appropriate ranges of dc-offset compensation currents.

```
===================================================================================
                        Control Bits                        Output Voltage

Bit No.  15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
-----------------------------------------------------------------------------------
          0  0  0  0  1  0  0  1  0  0  0  0  1  c  0  1        0.499
          ..............................................        .....
          0  1  0  1  1  0  1  0  1  0  0  0  0  c  0  1        5.000
          ..............................................        .....
          0  1  1  1  1  1  1  1  1  1  1  1  1  c  0  1        7.069

          0  x  x  x  x  x  x  x  x  x  x  x  x  c  1  1        7-V-Mode

          0  0  0  0  1  0  0  1  1  0  0  1  1  c  0  0        7.50
          ..............................................        ....
          0  1  0  1  1  0  0  1  1  0  0  1  1  c  0  0        70.00
          ..............................................        .....
          0  1  1  1  1  1  1  1  1  1  1  1  1  c  0  0        99.98

          1  0  0  0  0  0  0  0  0  x  x  x  x  x  x  x        -5*(00)**
          ..............................................        ..   ..
          1  1  1  1  1  1  1  1  1  x  x  x  x  x  x  x        +5 (FF)
-----------------------------------------------------------------------------------
```

*DC offset compensation, effective voltage source range from -5 V to +5 V
**Corresponding hexadecimal digits displayed on readout in Test Mode.

c= 0 for 16-bit conversion channel; c= 1 for 12-bit conversion channel
x= don't care

bit 0 and bit 1 are range control bits;
bit 15 is the dc offset/amplitude select.

```
===================================================================================
```

Table 5.2 Amplitude/Range/DC Offset Control (Binary) Format

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5.3 Memory Circuit Board.

As explained in chapter 4, for outputs with frequencies above 5 kHz, the digital data for an entire waveform must be stored so that data can be converted at megahertz rates. Two banks of memory with 1024 16-bit words each are provided for the waveform data storage and are shown as U19-U22 and U23-U26 on the circuit diagram, figure 5.3. The first memory bank is dedicated to the "reference output" channel and the other to the "variable output" channel. A modulo 1024 counter (U1-U3) furnishes the memory address for both banks and always points to the current location.

The pair of 16-bit data words computed by the waveform generating processor, one for each output channel, are transmitted successively along the 16 most significant bits of the 20-bit data bus to pairs of octal bus transceivers (U6-U7,U8-U9). A bus instruction (see chapter 5 of [1] for details), generated by the processor and latched into U13, directs the data word to the designated data bank and inserts it at the location given by the address counter. The instruction initiates a (ground true) write pulse, 'FE' or 'VE' for the reference or variable channel respectively, which enables the corresponding transceivers and writes the data into the appropriate memory.

The strobe pulse (timing pulse), originating in the frequency synthesizer (Circuit Board D3), arrives at edge connector pin 65 ("TP" on the circuit diagram), passes through clock control chip U18, and latches the contents of the memory locations specified by the address counter into the octal latches U4-U5 and U10-U11. The strobe pulse is also used to advance the counter to the next memory address. A third function of the strobe pulse is to acknowledge to the processor that the data have been read out of memory. This acknowledgement takes the form of a 1-bit signal that modifies the program flow of the waveform generating hardware so that the calculation of the next pair of data points can be initiated. The bit is "OR'ed" into the next address register of the sequencer section of the 20-bit processor (circuit board D9) which causes the processor to exit from its wait-loop. Details of this action are described in chapter 5 of [1].

For output frequencies up to 5 kHz, the action described above is repeated for every sampled data point. Above 5 kHz, a similar procedure is followed until all 1024 memory locations have been filled with the waveform data. The frequency synthesizer is then switched to its next higher range (range 7) which increases the strobe rate by a factor of ten. At the same time edge connector pin 67 is driven high so that the octal latch, U13, is cleared and the inputs to the AND gate, U16, are driven low. Consequently, the input at one of the D-type flip-flops, U14, is at a low level which prevents the propagation of the acknowledge ("OR") signal to the output edge-connector pin 68. As mentioned above, without this signal, the the waveform generating program remains idling, trapped in an endless loop. No new data are therefore computed and stored in memory until a software command resets the waveform generating processor.