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NBS Phase Angle Calibration Standard

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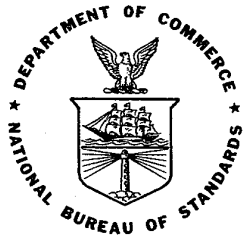
Calibration Coordination Group



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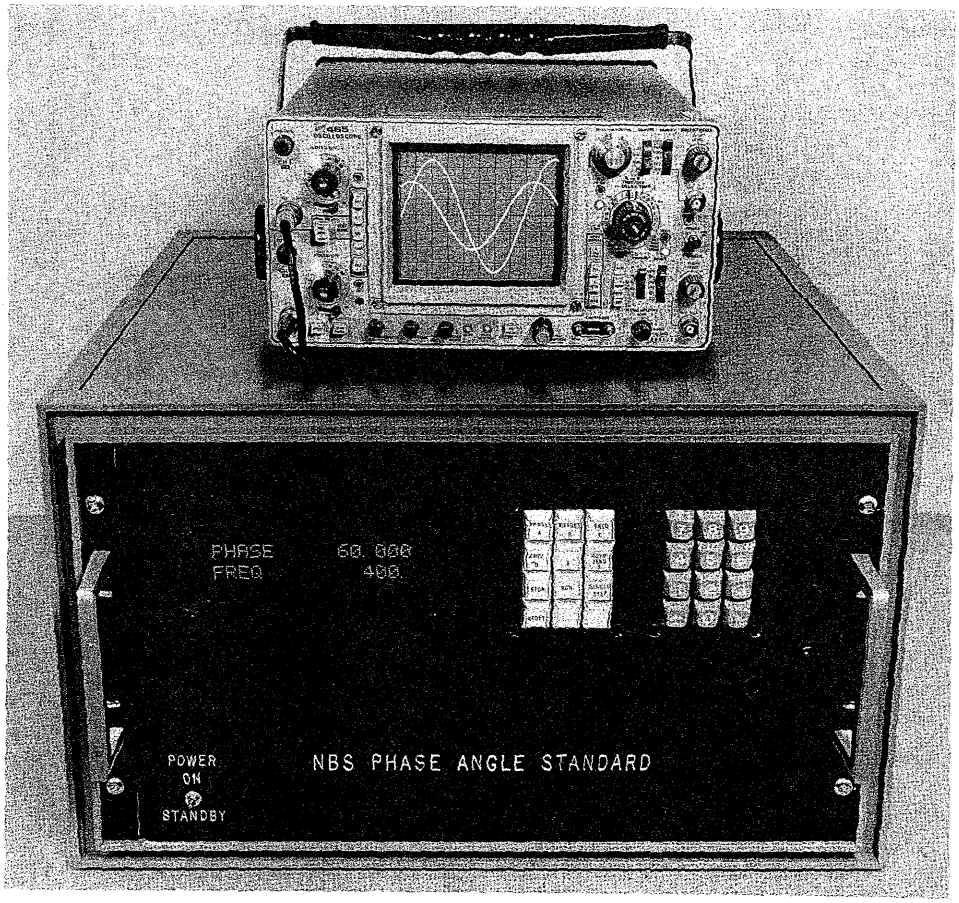

NBS Phase Angle Calibration Standard

NBS PHASE ANGLE CALIBRATION STANDARD

R. S. Turgel, N. M. Oldham,
G. N. Stenbakken, and T. H. Kibalo

A detailed description is given of the construction and operation of a calibration standard designed for use with phase meters. The resolution of the calibrator is approximately 2 millidegrees and its accuracy is of the order of 5-10 millidegrees depending somewhat on frequency and amplitude ratio of the output.

The calibration standard is a source of two sinusoidal signals with an accurately known phase angle between them. The signals are generated using digital sinewave synthesis and are programmable in amplitude (0-100 V) and in frequency (2 Hz-5 kHz). Operation is controlled from a front panel keyboard (or remotely with an adaptor) under control of a microprocessor. Selected parameters are displayed on an alpha-numeric readout.

To ensure accuracy, the system has an auto-zero feedback loop that compensates for residual differential phase shifts in the output amplifiers. The compensation scheme measures the departure of the output signals from true quadrature and applies a digital correction to the computing circuits of the sinewave generator.

Key words: calibration; digital; microcomputer; phase angle; sinewave generator; standard; synthesis.

1. INTRODUCTION

This publication was written to describe in detail the operation and construction of an audio-frequency phase angle calibration standard developed at the National Bureau of Standards. The work was undertaken because of a need to provide a reference, so that both manufacturers and users of phase measuring equipment could obtain consistent measurements throughout industry and other user communities.

This work was sponsored, in part, by the Department of Defense through the Calibration Coordination Group (CCG) which has particular interest in the phase angle calibration standard. They suggested the publication of a detailed description of the instrumentation system in order to encourage commercial production of phase angle standards using the National Bureau of Standards design.

Table 1.1 Space performance specifications

Phase Angle:	
Range	-999.999 to +999.999 degrees
Effective Resolution	0.0014 degrees (1 part in 2^{18})
Accuracy	
at 5.0 volts equal amplitude 1 to 500 Hz	±0.005 degrees
at an amplitude ratio of 20, up to 100.0 volts, 1 to 5 kHz	±0.020 degrees
Total Harmonic Distortion	
at 500 Hz	<0.01%
at 5 kHz	<0.05%
Output Frequency:	
Range	1 Hz to 5000 Hz
Resolution	1 Hz
Accuracy	0.1%
Stability	1 ppm
Output Amplitude:	
Range	0.25 to 100.0 V rms
Resolution	steps of approx. 2mV to 5 V steps of approx. 40mV from 5V to 100 V
Accuracy	±0.1%
Noise:	
DC to 100 kHz	<0.01%
100 kHz to 10 MHz	<0.05%
DC Offset Voltage	<1mV

The principle of operation was described in a paper written in 1978 [1].[1] This paper, however, did not go into details of the circuitry, nor did it discuss the hardware and software features that make this calibration standard particularly convenient to use. The present publication contains, in addition, the results of the development work since that time including microprocessor controlled parameter entry, programmable output voltages, and other features. The specifications for the present version of the NBS Phase Angle Calibration Standard are shown in table 1.1.[2]

2. DESIGN PHILOSOPHY

2.1 Introduction

Traditionally, calibration standards have been designed with the primary aim of high accuracy, often at the expense of complications in the operating procedures. In the present design, an attempt has been made to combine high accuracy with simplicity of operation. With the trend towards automatic testing, it was also important to provide for compatibility with automatic test equipment. This capability requires response time compatible with automatic systems.

2.2 Operator Interaction

Making the instrument "friendly" to the user is often overlooked, or perhaps sacrificed during the inevitable compromises that are part of the design process. However, good calibrations require more than an accurate standard. How well the accuracy of the standard is "transferred" to the instrument to be calibrated depends on the entire calibration process which involves the operator and, consequently, the man-machine interface.

Therefore, particular attention has been paid to this aspect in the development of the Phase Angle Standard by keeping the number of special instructions that need to be remembered by the operator as low as possible and by keeping the steps necessary for each function in a logical sequence. Almost all functions can be initiated with a single button, and numerical entries are limited to the number of digits essential to provide the operating parameters. To assist the user, prompting and

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[1] Numbers in brackets refer to the literature references listed at the end of this report.

[2] In order to adequately describe the system discussed in this report, commercial equipment and instruments are identified by manufacturer's name or model number. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

diagnostic messages are displayed on the alpha-numeric readout and are self-explanatory, so that there is no need to refer to look-up tables to decode the error messages.

While a complete and meaningful self-test of both digital and analog circuitry is a desirable goal, it would have added an unreasonable amount of complications both in hardware and software. However, some of the critical digital control functions are tested in the present system. During initialization of the instrument, a cyclic redundancy procedure checks the integrity of the program instructions and, more importantly, the correction tables which are also stored in read-only memory. Also, during this procedure the identification number of the critical hardware module, for which the correction tables are designed, is briefly displayed on the readout and thereby provides a visual check that the firmware and hardware modules are compatible. At the end of the initialization and self-check routine, rather than leaving the system in its quiescent state, default parameters are automatically entered. These provide a low-level, low-frequency output of the Phase Standard that can be used for a quick visual check on an oscilloscope which assures the operator that the system is operating properly.

Care has also been taken in the design to enable recovery of the system from externally-induced faults, such as large voltage spikes, which might interfere with the orderly execution of the operating program. In many cases the system will recover by itself, but recovery to the default values can always be accomplished using the 'RESET' control.

2.3 Accuracy and Stability

In manual operation, speed of response and settling of the system after parameter changes are of secondary importance, because human reaction time is usually long compared to system time constants. In the environment of automatic test equipment, however, system response time has to be orders of magnitude faster to be compatible. Traditional approaches using reactive circuit elements to produce the desired phase shift in the output signal are generally not well suited, if rapid response is required. In the present design, therefore, digital techniques have been used which are not constrained by the same response time limitations, and, in addition, offer superior long-term stability. As explained in more detail in section 4, the waveforms of the output signals and the phase angle between them are primarily determined by digital methods.

3. OPERATING INSTRUCTIONS

3.1 External Connections

(a) Power Cord. The power cord for the 120-volt, 60-hertz line plugs into a receptacle at the left rear of the instrument. Standby power to the heaters of the digital-to-analog converter voltage reference and a power relay logic board is supplied whenever the cord is connected to the 120-volt line, regardless of the position of the power switch.

(b) Reference and Variable Phase Output. The two output signals are available through the lower two BNC connectors at the rear of the instrument. A toggle switch provided near the connectors should be in the 'up' (NORMAL) position for normal operation. (For an explanation of the function of the toggle switch, see section 4.5.)

(c) Fuse. A 3AG 3A fuse is used in the screw-type fuse holder. The use of fuses of higher current rating might damage the ac-line filter at the power cord connector.

(d) External Sync. Connection. (No connector on the rear panel is provided in the present version of the instrument, but an internal connection is available, if required.) A TTL (5 volts dc max.) input to override the internally generated sampling pulse is located at the backplane, pin (23) on circuit board D3. External pulse rates must be between 200 kHz and 400 kHz for proper operation of the system.

3.2 Front Panel Controls

(a) Power Switch. The toggle switch on the left-hand side of the front panel provides a control current to a solid-state relay which connects the 120 - volt ac power line to the main power supplies of the instrument. (See also section 3.1(a).) Turning on the power lights up the display and initializes the system the same way as the 'RESET' function described in (b8) below. If the display does not light up, check the fuse at the rear of the instrument, near the line cord. (See section 1(c) above for fuse replacement.)

After initialization the instrument will output two 1-volt rms 500-Hz sinewaves with a 60 degree phase angle, and the display will show

PHASE 60.000
FREQ 500.

If this message is not displayed correctly, push the 'RESET' key, hold it down for a second and release. This will initialize the system. Before any measurements are made, the 'AUTO ZERO' function should be activated by depressing the 'AUTO ZERO' key. (See section (b4) below.)

During initialization, the microprocessor instruction code and correction tables stored in the read-only memory are checked. If a data storage error is detected, a message will be displayed. The instrument should then be reinitialized using the 'RESET' key. If the error persists, the read-only memories affected should be replaced.

(b) Keyboard. The keyboard is divided into two sections of 12 'command' keys and 12 numerical keys.

Note: Three of the keys have no command functions. They are reserved for future expansion.

The readout normally displays two parameters at a time, such as phase angle and frequency. The parameter that can be modified by numerical key entries is indicated by underlining. The completion of a command that changes the operating conditions is indicated by a beep tone, as well as by a change in the display format. However, merely recalling a previously set parameter to the display does not generate a beep tone.

(b1) Phase. Depressing the 'PHASE' key recalls the phase setting previously selected and displays it on the top line. This action does not change the phase of the output signals. Depressing the 'PHASE' key also initiates the phase angle entry mode, indicated by underlining the word "PHASE" on the display. Using the numerical keys, a new value for the phase setting can be selected. Numerical entries for the phase angle may contain a minus sign, decimal point, and from three to six digits, however, all three digits after the decimal point must always be entered.

Note: If three digits are entered to the left of the decimal point, a decimal point will be inserted automatically.

Numerical entries are shown left adjusted on the display as each digit is entered, and are shown right adjusted after the command has been executed, and the output has been changed to the selected phase angle. Corrections can be made before the entry is completed by depressing the 'PHASE' key. This will again display the previous value and cancel the partially entered new value. Corrections can be made after the entry is completed by reentering the corrected value through the numerical keyboard without using the 'PHASE' key first.

(b2) Offset. The offset adjustment displaces the reference output relative to the variable output, so that the resulting phase angle is the difference between the "Phase" and "Offset" values selected. The operation of the 'OFFSET' key is similar to that of the 'PHASE' key described in the section (b1) above. Normally, the Phase Standard is used with the offset equal to "0.000." In some cases, however, it is convenient to set the offset to a non-zero value. For instance, if the scale of the instrument under test cannot conveniently be zeroed, an offset adjustment can then make the instrument read "zero."

Example: A phase setting of 30.000 degrees and an offset of 0.150 degrees results in an effective phase difference in the output of 30.000 - 0.150 = 29.850 degrees.

(b3) Frequency. Depressing the 'FREQ' key displays the previously selected frequency value on the lower line of the display. This action does not change the value of the frequency of the output. Depressing the 'FREQ' key also initiates the frequency entry mode, indicated by underlining the word "FREQ." A new value can then be entered from the numerical keyboard. The entry is completed by depressing the decimal point key. Integral values from 1 Hz to 5000 Hz can be entered. Digits are shown left adjusted on the display until the entry

is terminated with a decimal point. The output is then changed to the selected frequency, and the new value is displayed, right adjusted.

If a value outside the permitted range is selected, an error message will be displayed:

```
++++++ERROR++++++
HIGH FREQ

++++++ERROR++++++
LOW FREQ
```

To correct errors, depress the 'FREQ' key and enter the new numerical value, terminating it with a decimal point.

Note: Setting of a new value for the frequency automatically initiates a check of the synthesizer which generates the timing pulse. If the pulse rate is out of its normal range, an error message will be displayed. (See 'Error Messages,' section 3.3 below) The error message will always be displayed if the frequency is set to 1 Hz and can usually be ignored in that case.

(b4) Amplitude. Amplitude is adjusted separately for the reference phase output (Channel 0) and the variable phase output (Channel 1). Depressing the 'AMPL' key prompts further input by displaying in the lower line

```
AMP. CHAN. ?
```

The correct response to this request is a numerical key entry of either "0" (Reference) or "1" (Variable). All other numerical responses are ignored.

Once the channel has been selected, two messages either

```
REF. AMP. , or

VAR. AMP.,
```

will be displayed. The desired amplitude is then entered in volts in the range of 0.000 to 100.0 volts rms. Four digits must be entered at all times, although under some conditions not all will be displayed. The amplitude control has a 'high' and a 'low' range which are automatically selected, depending on whether the chosen amplitude is above or below 5.007 volts. The resolution of the high range is approximately 0.02 volts, and that of the low range 0.002 volts rms. Numbers will be displayed, left adjusted, as they are entered. When the entry is complete, the amplitude of the selected channel is changed to a new value. Because the resolution of the programmable output is limited, not every voltage level can actually be attained. The value keyed in therefore is adjusted to the nearest permissible voltage, which is then displayed, right adjusted. A reminder, "AUTO ZERO?," will also be displayed

indicating that after a change in amplitude, it is normally necessary to operate the auto-zero function. (See section (b5) below.)

Note: As a safety precaution, it is advisable to depress the 'STOP' key before connecting or disconnecting the output signal leads. This action will set both output amplitudes to zero, so that the leads can be handled safely. Pushing the 'RUN' key will restore previously selected parameters. (See also the note following section (b5) below.)

Errors can be corrected by depressing the 'AMPL' key, channel select ("0" or "1"), and then entering the corrected voltage level.

(b5) Auto-Zero. Depressing the 'AUTO-ZERO' key initiates the auto-zero function. (For details of auto-zero action, see section 4.0, Operating Principles.) While this function is in operation, the display will read:

* AUTO ZEROING *

A beep will be heard at intervals to indicate that the auto-zero routine is executing its function. Termination is indicated by displaying:

PHASE 0.000

The output is then adjusted so that the phase angle is zero degrees.

Note 1: The auto-zero function determines a correction for residual phase errors which are a function of the output amplitudes and frequency, and is automatically applied to the phase angle settings chosen. Changing the frequency will automatically adjust the correction to a new value appropriate to the frequency chosen. However, every time the amplitude of either channel is changed, an 'auto-zero' operation should be performed to determine a new correction.

Note 2: Normally, the auto-zero function is completed in less than one minute. On rare occasions, a glitch occurs which causes the auto-zero routine to determine an incorrect calibration factor. It is then possible for the auto-zero function to run considerably longer, or get into an endless loop. Therefore, if the routine does not settle within one minute, depress the 'RESET' key to reinitialize the system, and key in the desired operating parameters.

(b6) Stop. Depressing the 'STOP' key inhibits the clock pulse of the high-speed microprocessor that generates the output signals. The word "STOP" and the default hexadecimal address "06" will be displayed on the upper line.

While in the 'Stop' mode only certain functions can be performed, as explained below:

(i) The 'RUN' key can be used to restart the high-speed microprocessor, see (b7).

(ii) The 'SINGLE-STEP' key can be used (mainly for diagnostic purposes), see (b8).

(iii) The high speed processor starting address can be modified: numerical keys from 0 to 9 and special keys marked A to F modify the hexadecimal starting address of the high speed microprocessor, and the modified address is shown on the display. Address modification is used only for troubleshooting , or calibration of the digital-to-analog converters.

Note 1: If the address has been inadvertently modified, operating the 'STOP' key again will restore the "06" address used for normal operation.

Note 2: As a safety precaution both output amplitudes are set to zero volts by the 'Stop' function. Therefore, before connecting or disconnecting the meter under test, the 'STOP' key should first be used.

(b7) Run. The 'RUN' key restarts the high-speed microprocessor at the hexadecimal address displayed. It also restores the previously selected amplitudes, frequency, phase, and offset settings.

Note: Certain operations, such as resetting the phase or frequency, can only proceed when the high-speed processor is running.

(b8) Single-Step. The 'SINGLE-STEP' key operates the high-speed microprocessor through its program, one step at a time. The single-step mode is used mainly for diagnostic purposes and is not needed for normal operation.

(b9) Reset. Momentarily depressing the 'RESET' key initializes the system in the same way as the turning-on of the power switch. The reset action interrupts the current operation and proceeds to the initializing routine which sets the following parameters:

Output voltage on both channels: 1.000 volts
Frequency: 60 hertz
Phase angle: 60.000 degrees
Offset: 0.000 degrees

Note: The initializing routine does not include the auto-zero function, so that if measurements are made at the 1-volt amplitudes set by the routine, the 'AUTO ZERO' key should first be depressed.

During initialization, the microprocessor instruction code and correction tables stored in the read-only memory are checked. If an error is detected, a message will be displayed, e.g.,

++++++ERROR++++++
PROM 1

The instrument should then be reinitialized using the 'RESET' key. If the error persists, the read-only memories affected should be replaced.

Note: At the beginning of the initialization, a message identifying the ROM set is momentarily displayed, e.g.,

-- PROM SET 11A-32

The alpha-numeric designation identifies the board position and serial number of the phase detector circuit board. The designated board was used to determine the correction tables during the calibration process. These tables are part of the information stored in the ROM, and are matched to the phase detector board; therefore, no other phase detector should be used with this set of ROMs. (See also section 4.6.)

3.3 Error Messages

The table below shows the error messages that the system can display and the remedial actions required.

Table 3.1 Error messages

ERROR MESSAGE	FAULT	REMEDIAL ACTION
HIGH FREQ	Frequency selected out of range	Enter correct frequency see section (b3)
LOW FREQ	Frequency selected below 1 Hz	Enter correct frequency see section (b3)
HIGH VOLTAGE	Amplitude selected above 100 volts	Enter correct amplitude see section (b4)
SYSTEM STOPPED	High-speed processor clock not running	Push 'STOP', then 'RUN' see sections (b6, b7)
TIMING PULSE	Pulse frequency out of range	Check frequency synthesizer
UNDEFINED FUNCT.	Illegal command e.g., 'RUN' not preceded by 'STOP'	Consult operating instructions for procedure
PROM 1 (2,3,4)	Read-only memory faulty	Replace ROM integrated circuit on circuit board D-11

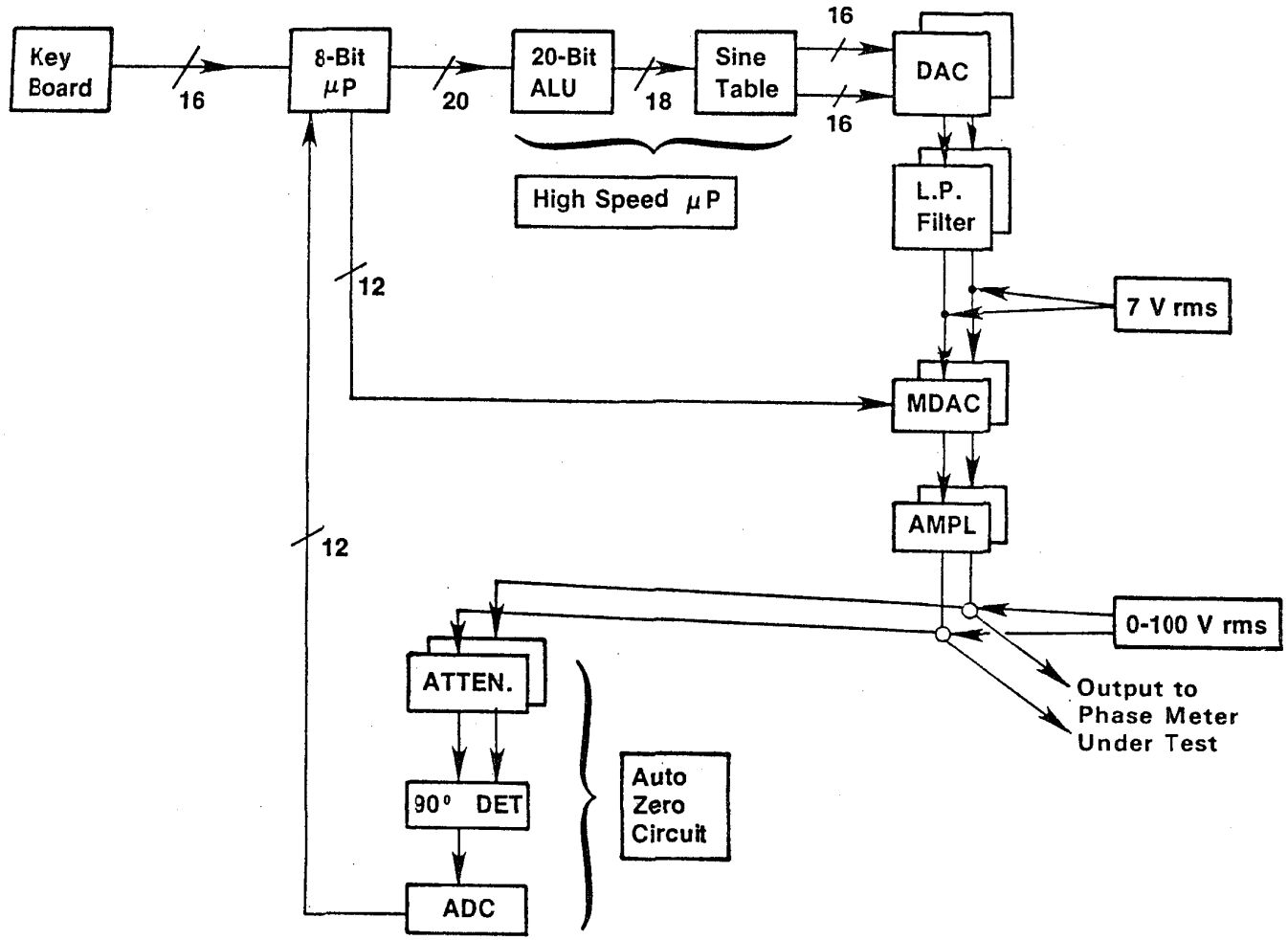


Figure 4.1 Functional Block Diagram

4. OPERATING PRINCIPLES

4.1 Introduction

The Phase Standard is a calibrator which produces two sinusoidal output signals with an accurately known phase angle between them. The signals can be applied directly to the phase meter under test in order to check its calibration.

The output phase angle, frequency, and amplitudes are adjustable from the front panel keyboard (or remotely, if a special interface circuit board is provided).

4.1.1 Method of Signal Generation

The sinusoidal output signals are generated by calculating instantaneous amplitude values at equal time intervals along both desired waveforms and by converting these sets of numerical data points to analog output voltages using a pair of digital-to-analog converters (dual-channel) with appropriate filtering.

4.2 Operator Interfaces

Referring to the block diagram, figure 4.1, operating parameters, such as phase angle, signal frequency, and amplitudes, are entered by the operator on the keyboard shown at the top left of the diagram. An 8-bit microprocessor (μP), interprets the key strokes and converts the information into binary signals that allow a high-speed, 20-bit microprocessor to generate the numerical data for the desired waveforms.

4.3 High-Speed Processor

The phase angle and frequency information from the keyboard, in binary form, is latched into registers of the arithmetic-logic unit (ALU). This unit converts the location of sample points along the time axis, t_1, t_2, t_3, etc. on figure 4.2, to corresponding angles from which the sinusoidal waveform can then be calculated. To calculate the instantaneous values of the sine function at these points, the angular values are converted to their corresponding sine values using a look-up table and interpolation technique. This conversion is carried out by special circuitry indicated on the diagram, figure 4.1, as 'SINE TABLE'.

The phase angle (phase difference) between the two waveforms is determined by the relative magnitudes of the instantaneous values calculated for each waveform at successive sampling times t_1, t_2, etc. These values are calculated sequentially and then stored temporarily in pairs, so that they can be applied simultaneously to both digital-to-analog converters.

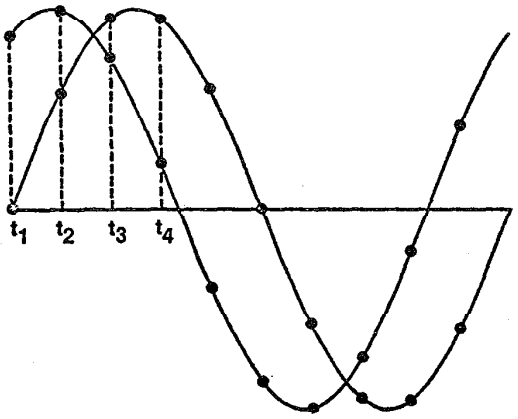


Figure 4.2
Waveform Synthesis with Uniform Sampling

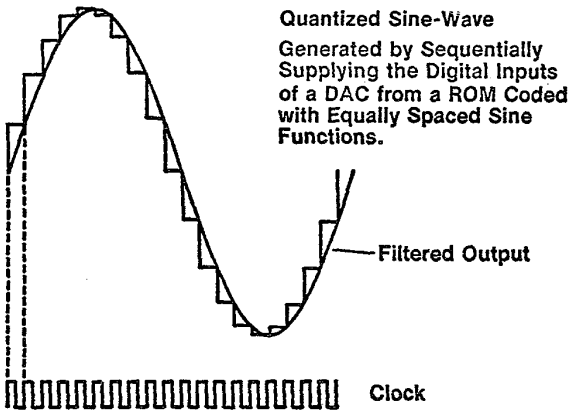


Figure 4.3
Stepped Sinewave

4.4 Digital-to-Analog Converters (DAC)

The 16-bit numbers obtained from the output of the SINE TABLE module are strobed simultaneously into two parallel digital-to-analog converters where they are converted to voltages which produce two stepped sine functions (figure 4.3). The strobe timing pulse, which is independent of the system clock, is derived from a crystal controlled synthesizer. The synthesizer frequency is set by an algorithm in the 8-bit processor which takes into account the desired signal output frequency and the appropriate number of sample points along the waveform for each cycle.

The step-like output is smoothed by analog low-pass filters which remove the frequency components introduced by the sampling process. The number of samples per waveform is varied in a binary sequence so that the sampling rate remains between 200,000 and 400,000 samples per second.

4.5 Output Amplifier Circuits

At the output of the filter circuits two sinusoidal signals are obtained with amplitudes of 7.07 volts rms.

Note: These signals are fed directly to the output terminals of the Phase Standard when the toggle switch at the rear panel is in its 'down' (7-volt) position.

To obtain output signals with other amplitudes, the 7-volt signals are fed to programmable attenuators (MDAC in figure 4.1), and output amplifiers (AMPL), which are controlled with binary signals derived from the 8-bit microprocessor, in response to keyed-in amplitude information.

4.6 Auto-Zero Circuit

Even with the most careful construction, the amplifier, filter, and attenuator circuits cannot be made electrically identical. They can, therefore, introduce small differential phase errors in the two output channels. The magnitudes of these errors will depend on the amplitude settings in each output channel, and they are also linearly dependent on the frequency.

To compensate for these errors, an auto-zero circuit is provided that determines the appropriate correction and applies it in numerical form to the registers of the arithmetic unit of the high-speed microprocessor that generates the waveforms.

The auto-zero circuit relies on the characteristics of a quadrature phase detector (90 deg. DET), which samples the output of the phase standard. In operation the output of the Phase Standard is set to a frequency near the top of the range, where the sensitivity is high, and to a nominal phase angle of 90 degrees. If there are no phase errors, the output of the phase detector will then be zero, and in that case no

correction will be applied. If small errors are present, a positive or negative output voltage is obtained from the phase detector which is digitized by an analog-to-digital converter (ADC). The digital output is fed to the 8-bit microcomputer which calculates the appropriate corrections. This correction is then applied to the waveform generator and produces a small change in the phase angle of the output. The procedure is repeated until the phase detector indicates that quadrature has been obtained. The final value of the correction is then retained in the memory of the 8-bit microcomputer.

To eliminate any possible errors in the phase detector itself, measurements are made at +90 and -90 degrees, and with the inputs interchanged. Internal feedback in the phase detector compensates for possible dc offsets in the signals, reversing 90-degree angles compensates for dc offsets in the output of the phase detector, and interchanging channels compensates for possible phase offsets in the detector circuitry.

Since the phase detector must handle a wide range of input signals, it has internal programmable attenuators which are coupled to the amplitude selection circuits. At unequal amplitudes, these attenuators produce additional small phase errors which are compensated for by correction tables built into the firmware (ROM) of the 8-bit microcomputer.

After the final correction has been determined by the auto-zero operation, it is automatically applied to all subsequent phase angle settings of the Phase Standard. Since the frequency relation of these corrections is highly predictable, the corrections will be automatically modified by the firmware of the processor when a different output frequency is selected. Changing either or both amplitudes, however, requires the redetermination of the corrections with the auto-zero function.

5. HIGH-SPEED PROCESSOR OPERATION

5.1 Architecture

The function of the high-speed processor is to generate the waveforms required for the Phase Standard. For this purpose the angular sampling intervals have to be calculated as well as the corresponding values of the sine function. Physically, the high-speed processor is divided into four modules, each of which is assembled on a separate circuit board (see sections 7.2.1 - 7.2.4).

The bit-slice, high-speed processor is composed of a sequencer to control program flow, an arithmetic-logic unit to carry out the angular interval calculations, a special purpose computation circuit to calculate the sine/cosine function, and a set of registers (latches) with control circuits to strobe the numerical values contained in them into the dual analog-to-digital converters.

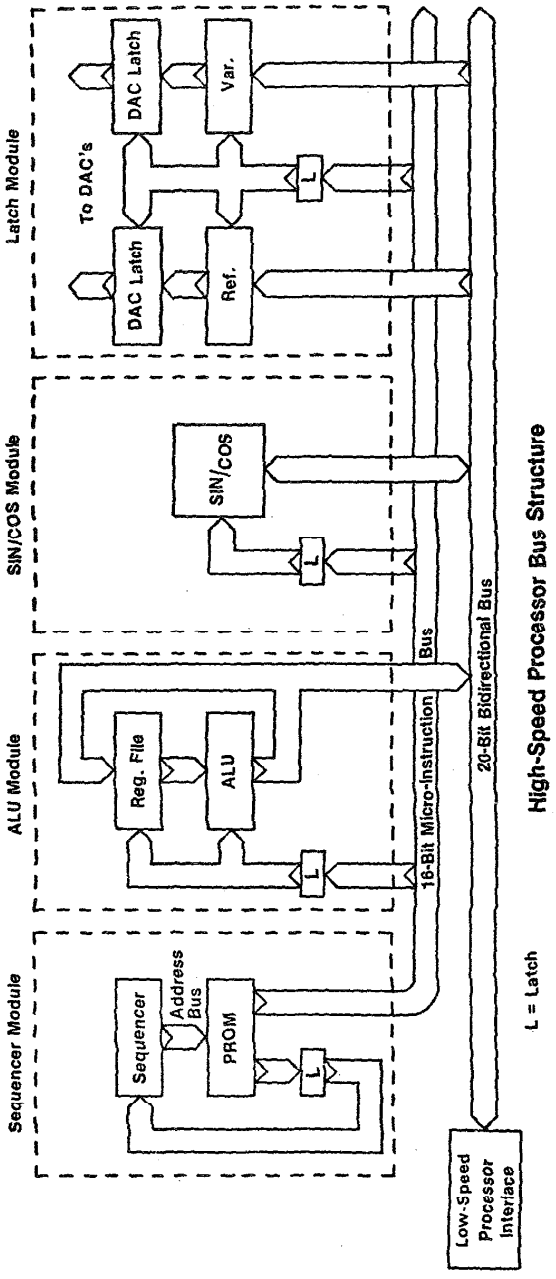

Sequencer Module
Sequencer
Address Bus
PROM
L
ALU Module
Reg. File
ALU
L
SIN/COS Module
SIN/COS
L
Latch Module
To DAC's
DAC Latch
Var.
L
DAC Latch
Ref.
Bus
16-Bit Micro-Instruction
20-Bit Bidirectional Bus
L = Latch
Low-Speed Processor Interface
High-Speed Processor Bus Structure

Figure 5.1

5.1.1 Bus Structure

The modules of the high-speed processor communicate using a 20-bit bidirectional data bus, and a 16-bit unidirectional instruction bus. The 8-bit memory (PROM) address bus is internal to the sequencer module. In addition two sets of dedicated data lines connect the output latches to the digital-to-analog converters (see figure 5.1). Several control lines are used to resolve bus priorities and for handshake communication with the 8085 processor.

5.1.2 Data Flow

The numerical data handled by the high-speed processor consist principally of binary angles, which correspond to the sampling time intervals along the waveform, and the binary values of the corresponding sines of these angles. The angular values are 20 bits wide, and the sine function values are 16 bits wide, left adjusted, so that in both cases the most significant bit (MSB) represents the sign of the numerical value, following the convention for two's complement notation.

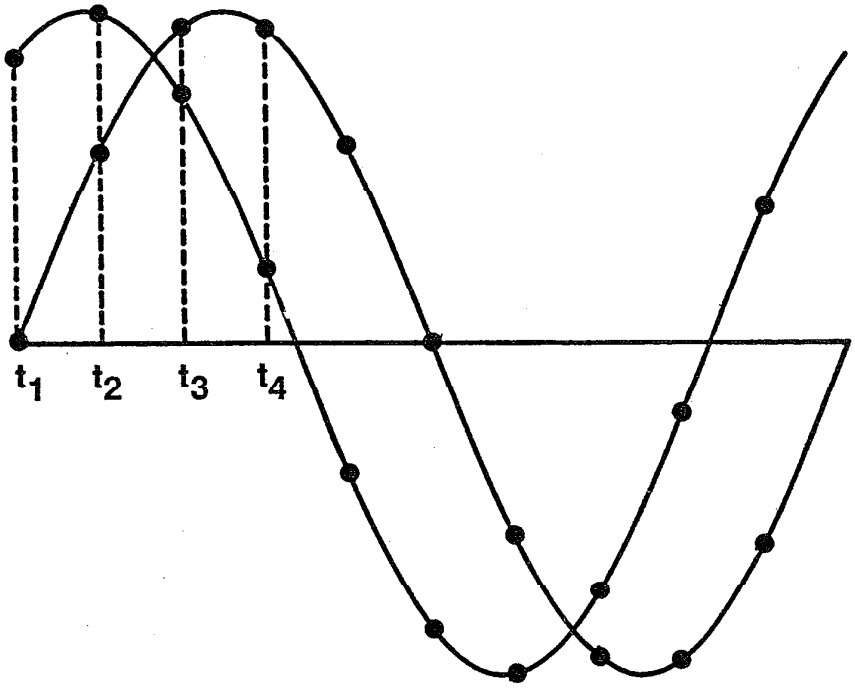
5.1.3 Initial Values

The sample points for each successive cycle of the waveform are calculated by the high-speed microprocessor independently of the previous waveforms to avoid propagation, for more than one cycle, of errors which could be caused by glitches. The starting values for these calculations are obtained from data computed in the 8085 microprocessor using the parameters entered through the keyboard. These initial values are transferred from the low-speed processor interface unit along the 20-bit bus and stored in a 4-word register file which is located in the ALU module (figure 5.1) and has the capability of simultaneous read and write functions. The output of the register file is connected directly to the input of the arithmetic-logic unit. The information stored in the four-word register file is organized as follows:

File '0' contains the last output from the arithmetic unit so that chain calculations can be performed;
File '1' contains the angular increment between sample points;
File '2' has the starting point of the 'variable' phase output;
File '3' contains the starting point of the 'reference' phase output.

5.1.4 Angle Calculations

The type of arithmetic-logic unit used has eight internal registers which serve as accumulators. Register '0' is used for the 'reference' output waveform, register '1' for the 'variable' phase output waveform, and register '4' is used as a control.



Waveform Synthesis with Uniform Sampling

Figure 5.2

The registers are initialized by loading

file '3' into register '0',
file '2' into register '1',
and file '1' into register '4'.

The contents of registers '0' and '1' then contain the first pair of angular values which, after conversion to their respective sine values and further conversion to output voltages, represent the first set of data points at time t_1 (see figure 5.2).

During subsequent steps the angular increment contained in file '1' is added to the contents of each register so that registers '0' and '1' will successively contain the angular values corresponding to sample times t_1, t_2, etc. as shown on figure 5.2. The binary arithmetic system is designed to operate in a modulo 360 degree mode, that is 359.999 degrees correspond to full scale in binary, and 360 degrees are equivalent to zero. The angular increment (an integer power of two) is chosen so that continued addition of the increment will always retrace the same set of angular values.

The function of register '4' can be thought of as that of a counter and a flag. If the addition of n increments to registers '0' or '1' is required so that they again contain their starting values, then n additions to register '4' will bring its contents to "full scale," since it was originally set to zero. The nth addition will again set the contents to zero, except that the carry generated during the addition will change the sign bit (MSB) to a 'one' (negative). A status line from the arithmetic logic unit transmits this condition to the sequencer where it is used to modify the program sequence, and causes the initial values from the file to be loaded again into the appropriate internal registers of the arithmetic-logic unit.

5.1.5 Angle-to-Sine Conversion

The results of the angle calculations are put on the 20-bit bus and latched into data registers on the SIN/COS conversion module. The conversion hardware (see section 7.2.3) has an input resolution of 18 bits and therefore the MSB (sign bit) and LSB of the 20-bit bus are ignored. The 18-bit angle is converted to its corresponding sine function value which is expressed as a two's complement binary 16-bit number and which is transferred to the 16 most significant bits of the 20-bit bus. The conversion proceeds asynchronously and the data inputs and outputs of the module are isolated from the data bus during the conversion. To transfer the data to and from the module, instructions residing on the 16-bit microinstruction bus (see figure 5.1) are decoded and held in an instruction register in the module. The instructions serve to latch data from the 20-bit data bus to the input of the angle-to-sine conversion circuit (mnemonic 'SL'), or enable the output of the tri-state drivers (mnemonic 'BU'), so that the converted data is fed back onto the bus.

5.1.6 Temporary Data Storage

From the SIN/COS conversion module, data are transferred via the 20-bit bus to holding registers, latches where they are stored before being strobed into the digital-to-analog converters. Since instantaneous output values for both waveforms are computed sequentially, they must first be stored in separate 'reference' and 'variable' phase registers until the timing pulse simultaneously transfers them via two 16-bit DAC buses to the digital-to-analog converters (see section 5.3 and figure 5.1).

5.2 Instruction Set

The instructions for the high-speed processor are contained in a 256 by 16-bit programmable read-only memory. The size of the microinstruction word has been chosen as a compromise between execution speed and memory size. The instruction cycle time is dictated by the propagation delay in the 20-bit arithmetic logic circuitry, and overall timing requirements are influenced by the maximum conversion rate of the digital-to-analog converters, as well as the angle-to-sine conversion time.

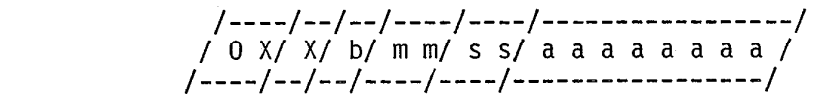
To provide a sufficient number of bits to control all necessary functions, there are three instruction formats, one for the control of program sequence, a second for arithmetic operations, and a third for bus control. Some of the bus instructions are also available in the arithmetic (ALU) format, to permit more compact coding.

5.2.1 Instruction Formats

Instructions are 16 bits wide with the most significant bit labeled "Bit 15" and the least significant "Bit 0." Bits 15 and 14 identify the instruction type; the remainder of the bits are divided into various fields associated with a particular function depending on the instruction type.

5.2.2 Sequencer Instructions

Sequencer instructions determine the address of the next microinstruction in the read-only memory. In the present version of the Phase Standard only four sequencer instructions are used. The others are listed for reference only. The general format is:



X = Don't care
b = conditional branch enable
1/0 = enable/disable

m m = address generating mode
  00 = program counter
  01 = address register
  10 = top of internal stack
  11 = instruction register

s s = sequencer stack control
  0X = stack disabled
  10 = "pop" stack, (decrement stack pointer)
  11 = increment stack pointer and "push" current contents of program counter to the top of the stack.

a...a = 8-bit address
  used when instruction contains an address

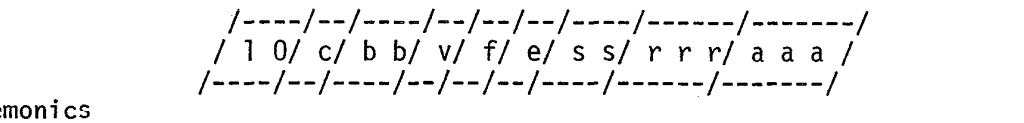
The above microinstructions are used in combination as shown in table 5.1.

Table 5.1 Sequencer instructions

Mnemonic	Binary Instruction	Hexadecimal Equivalent
AR	00 0 0 10 00 0000000	0400
	Jump to address previously loaded into Address Register	
Hexadecimal addresses are modified when the Phase Standard is in the "STOP" mode, from the keyboard or remotely. The address selected is loaded into the address register when the "RUN" or "SINGLE STEP" commands are activated.		
JM	00 0 0 11 00 aaaaaaaa	0Caa
	Unconditional jump to 8-bit address in instruction	
JM OR	00 0 1 11 00 aaaaaaaa	1Caa
	Conditional jump to 8-bit address as modified by one or more bits OR'ed with the address in the instruction. ('OR' bits are generated by the system hardware.)	
Note: The address must have an"0" in the bit position(s) that are to be OR'ed with the condition word.		
PC (NOP)	00 0 0 00 00 00000000	0000
	Increments program counter by 1	
Note: During ALU and BUS instructions, the sequencer instruction register is zeroed, so that the system steps through the instructions sequentially.		
JS	00 0 0 11 11 aaaaaaaa	0Faa
	Jump to subroutine at address "aaaaaaaa"	
Current contents of program counter are pushed on the stack		
RS	00 0 0 10 10 XXXXXXXX	0AXX
	Return from subroutine	
Stack pointer is decremented and top of stack is the return address.		

5.2.3 Arithmetic-Logic Unit Instructions

ALU instructions control the angle computation process as well as data flow from and to the 20-bit bus. The microinstruction format is:



Mnemonics

c = sine/cosine select
- [CS] 0 = cosine
- [SI] 1 = sine

b b = bus control
- 00 = not used
- [SL] 01 = data latched into SIN/COS module
- [BU] 10 = output from SIN/COS module transferred to bus
- [TM] 11 = timing pulse enable (see section 5.2.4)

[VE] v = 'variable'phase output latch

[FE] f = 'reference' phase output latch

e = ALU output enable, transfers computed result to bus
- [OE] 0 = enable
- 1 = inhibit

s s = source file
- [S0] 00 = file 0, ALU output
- [S1] 01 = file 1, angular increment
- [S2] 10 = file 2, initial value for 'variable' phase
- 11 = file 3, initial value for 'reference' phase

r r r = destination register in arithmetic, logic register stack
- [R0] 000 = register 0
- [R1] 001 = register 1
- [R7] 111 = register 7

a a a = arithmetic logic unit function
- [+D+1] 000 = add (input data+1) to register
- [+D] 001 = D+1+Rx → Rx
- 010 = D AND Rx → Rx, (Logic AND)
- [LD] 011 = D → Rx (Load register)
- 100 = Rx → output
- 101 = D OR Rx → Rx, (Logic OR)
- 110 = D XOR Rx → Rx, (Exclusive OR)
- [LC] 111 = -D → Rx, (Load complement of input data into register)

Note 1: If the output is enabled, the results of any of the operations can be transferred to the bus.

Note 2: The mnemonic, in brackets in the table above, are used in the listing of the program for the high-speed processor. For example,

LD R0 WITH S3 OE

Load ALU register '0' with contents of source file '3' and enable the output to transfer the data to the bus.

5.2.4 Bus Instructions

The currently implemented bus instruction format duplicates certain of the ALU microinstructions in section 5.2.3. The need for a separate format arises, because there is no "do nothing" (NOP) function in the ALU instruction set, and bus control is needed while keeping the contents of the ALU registers unchanged. Also, additional data manipulation instructions are made available for future expansion of Phase Standard functions. The instruction format is as shown in the table below:

```
/----/--/----/--/--/--/----------------/
/ 1 1/ c/ b b/ v/ f/ e/ X X X X X X X X /
/----/--/----/--/--/--/----------------/
```

Mnemonics

X = Don't care

c = sine/cosine select
[CS] 0 = cosine
[SI] 1 = sine

b b = bus control
00 = not used
[SL] 01 = data latched into SIN/COS module
[BU] 10 = output from SIN/COS module transferred to bus
[TM] 11 = timing pulse enable (see section 5.2.4)

[VE] v = 'variable' phase output latch
[FE] f = 'reference' phase output latch

Note: In the program listing "bus instructions" are identified by a "##" symbol.

5.3 Execution and Timing

The program execution must take into consideration three separate timing cycles. The arithmetic unit (ALU) requires 200 nanoseconds per clock cycle, the sine function converter requires somewhat more than 300 nanoseconds per conversion, and the timing pulse which initiates the digital-to-analog conversion is repeated at intervals varying from 2.5 to 5 microseconds depending on the frequency chosen for the synthesized output signal.

5.3.1 Pipelining

After the memory address has been determined by the sequencer during one clock cycle, the instruction contained in that memory location is latched in one of several instruction registers located in each of the high-speed processor modules. These registers are indicated by small rectangles (L) on figure 5.1. The instructions are decoded and are arranged so that, for instance, the sequencer module only retains sequencer instructions in its instruction register, while ALU/BUS instructions are transferred in the other modules. The instruction is therefore held stable during an entire clock period. During a sequencer or bus instruction cycle the clock signal to the ALU is inhibited, so that the ALU register contents remain unchanged. During an ALU/BUS instruction cycle the sequencer instruction register is set to zero. The all-zero instruction causes the current address in the program counter to be incremented by one.

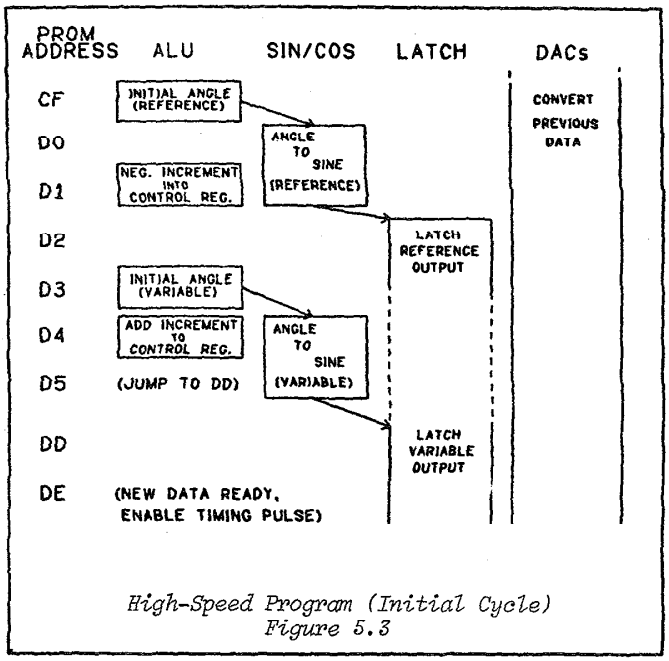
To make more efficient use of the processor, data are latched and isolated from the bus while being processed in the various subsystem modules. Where possible the ALU is carrying out an additional operation while previously calculated angles are converted to their sines. This is shown in figures 5.3 and 5.4 where the instructions are shown in a two-dimensional diagram in which each row is labeled with the PROM address containing the instruction, and each column shows the module on which the instruction acts. Data transfer via the bus are indicated by arrows. As can be seen, two clock periods, 400 nanoseconds, allow sufficient time for the sine conversion, while permitting simultaneous additional operations to be carried out by the ALU or sequencer. Similarly, each pair of output values is computed during the digital-to-analog conversion of the previous pair.

5.3.2 Delayed Execution

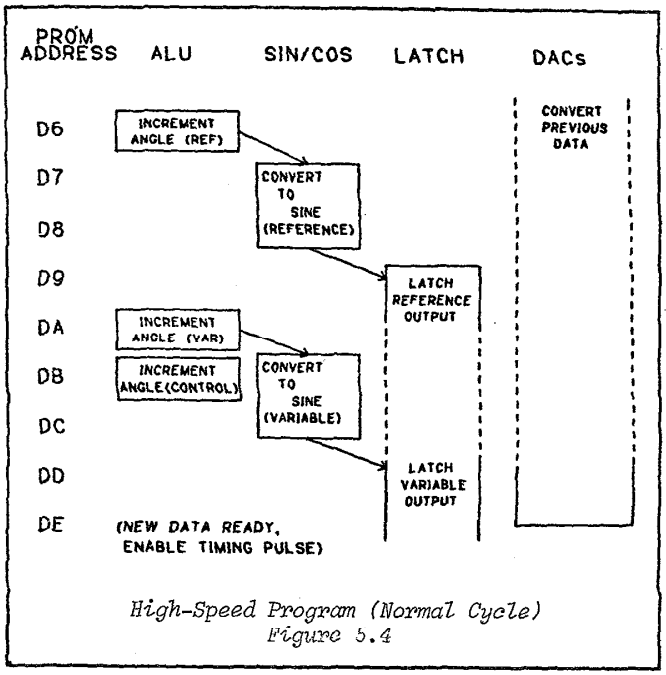
The task of microprogramming is eased, if related instructions can be combined even though they are not executed at the same time. For instance, the "output enable" instruction is combined with the appropriate ALU instruction, although the enable pulse is needed only after the ALU operation has been completed, that is one clock cycle later. Similarly, the execution of various bus control functions is delayed relative to the system clock. Proper timing is assured by hardware delay circuits which are necessary, because all microinstructions are executed in a single clock cycle, so that there are no "sub-cycles" for various phases of the execution. Figures 5.5 and 5.6 show microinstruction timing diagrams. Instruction can be identified by reference to the program listing in section 5.3.5 and figures 5.3 and 5.4.

5.3.3 Conditional Branching

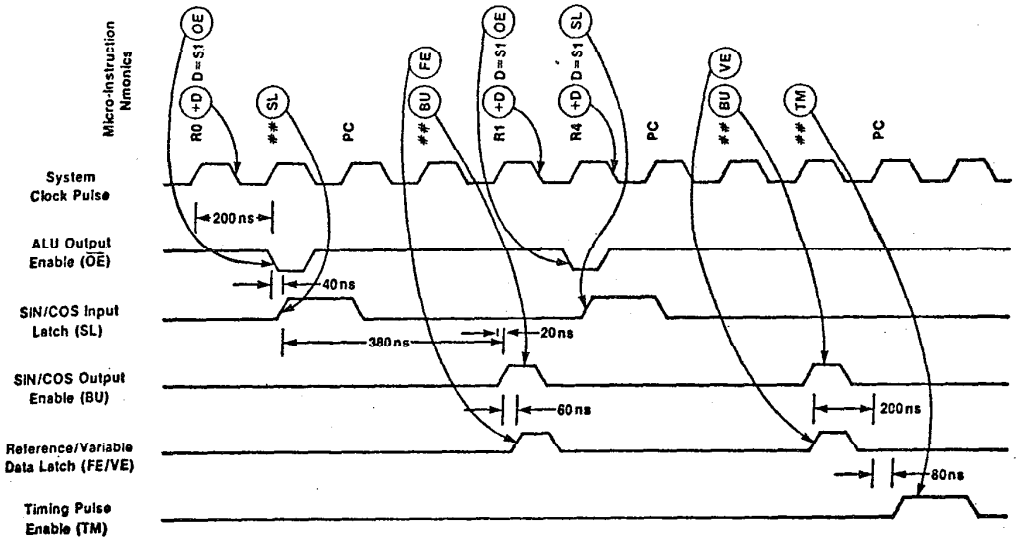
The sinewave generating program has two main branches and two wait loops. For the beginning of the cycle of the output waveform (figure 5.3), the first point is calculated from parameters entered through the



High-Speed Program (Initial Cycle)
Figure 5.3



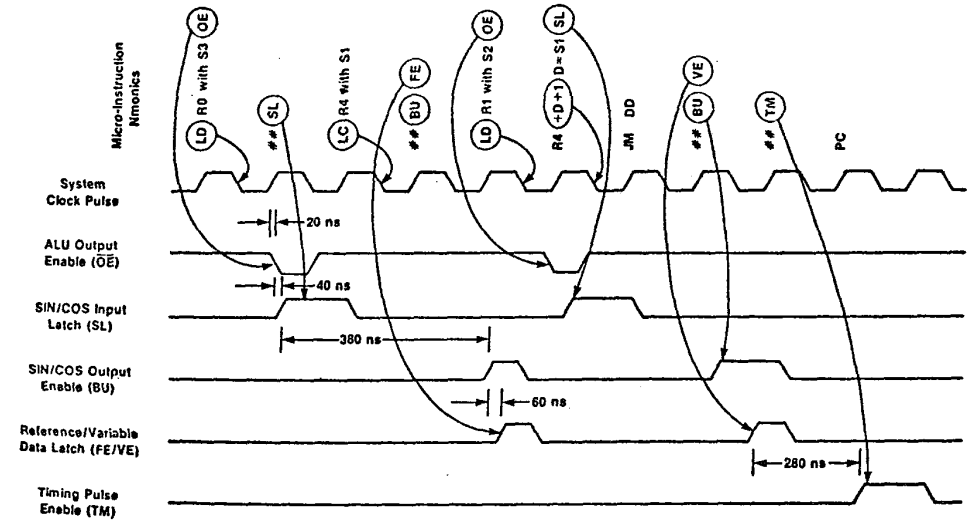
High-Speed Program (Normal Cycle)
Figure 5.4



Timing Diagram of High-Speed Processor (Normal Cycle)

Figure 5.5

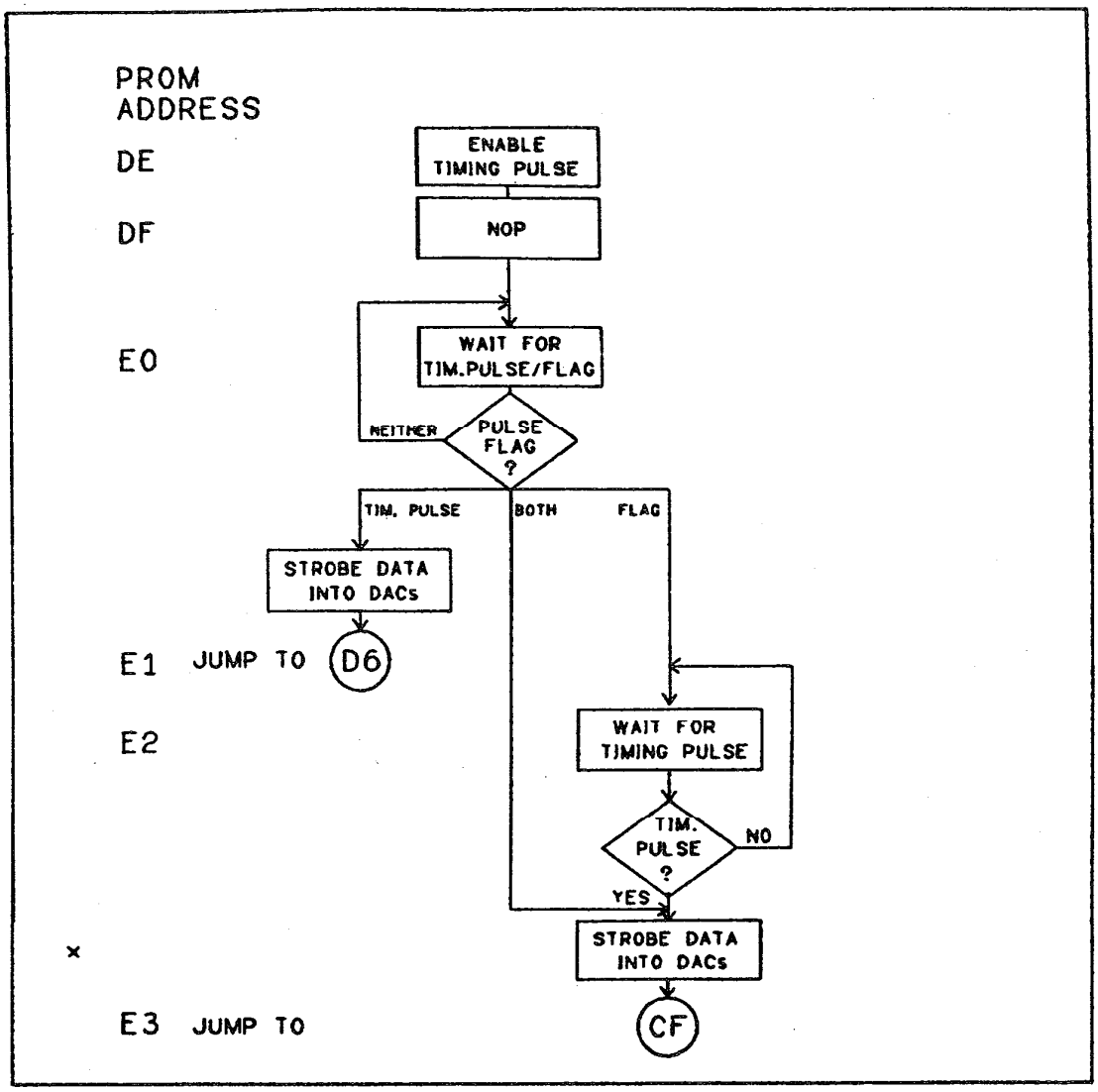
Note: Instructions are latched onto the instruction bus with the leading edge of the clock pulse, but execution is delayed as indicated by the arrows.



Timing Diagram of High-Speed Processor (Initial Cycle)

Figure 5.6

Note: Instructions are latched onto the instruction bus with the leading edge of the clock pulse, but execution is delayed as indicated by the arrows.



High-Speed Program (Branching)

Figure 5.7

keyboard, and starts at memory address 'CF.' The remainder of the points on each waveform are calculated in a loop which begins at memory address 'D6' (figure 5.4) in which the angles corresponding to the sampling points are successively incremented. After each set of new data has been calculated and an enable instruction has been given to permit the timing signal to strobe the new data to the analog-to-digital converters, the program goes into a wait loop (figure 5.7), to wait for the timing pulse. When the timing pulse arrives, the data are strobed to the converters, and a bit is 'ORed' in the sequencer to modify the 'next address.' The program then proceeds to 'E1' from where it jumps back to the beginning of the loop at address 'D6.'

Just before the end of the cycle of the output waveform, the contents of the control counter (internal ALU register R4) change sign. This sign change is used to flag the end of the cycle, and a second 'OR' bit then transfers the program to address 'E2' where it again waits for the timing pulse. When the timing pulse arrives, the 'OR' bit associated with the timing pulse causes a transfer of the program to 'E3.' From there a jump to 'CF' is executed, which is the beginning of the loop of the program that reinitializes the data. Should both the 'flag' and timing pulse occur simultaneously, both 'OR' bits are applied, and the program transfers directly from address 'E0' to 'E3.'

5.3.4 Bus Arbitration

The 20-bit bus is used not only for data transfer from the ALU to the SIN/COS module and from there to the output latch registers, but also to transfer the initial parameters from the control microprocessor (8085) interface to the register file in the ALU module. Since these processes are asynchronous, bus contention must be arbitrated. A hardware priority circuit (see section 7.2.2) resolves this problem. To prevent possible overlap, bus access is enabled only during the second half of every clock period. The following priorities have been established (see also table 7.1):

1. SIN/COS module output
2. ALU output
3. Angular increment
4. Initial point on 'variable' phase waveform
5. Initial point on 'reference' phase waveform.

5.3.5 Sinewave Generating Program

The program shown in table 5.2 uses the instructions described in section 5.2 and follows the diagrams shown in figures 5.3 to 5.7. Further understanding can be gained from the descriptions in sections 5.3.1 to 5.3.3.

Table 5.2 Sinewave Generating Program

Memory Address	Hexadecimal Instruction	Mnemonic Instruction	Comments
00	0400	AR	Jump to address in addr.
06	0CCF	JM CF	Jump to initializing loop
CF	A0C3	LD R0 WITH S3 OE	(S3) → R0 → bus
D0	E900	## SL	bus → SIN/COS module
D1	A167	LC R4 WITH S1	Complement (S4) → R4
D2	F300	## BU FE	(SIN/COS) → ref. latch
D3	A08B	LD R1 WITH S2 OE	(S2) → R1 → bus
D4	A960	R4+D+1 D=S1 SL	(R4)+(S1)+1→R4;bus→SIN/COS (This operation sets R4=0 and transfers data from bus to the SIN/COS module)
D5	0CDD	JM DD	continue at 'DD'
D6	A041	R0+D D=S1 OE	(R0)+(S1) → R0 → bus
D7	E900	## SL	bus → SIN/COS module
D8	0000	PC (NOP)	increment prog. counter
D9	F300	## BU FE	(SIN/COS)→bus→ref. latch
DA	A049	R1+D D=S1 OE	(R1)+(S1) → R1 → bus
DB	A961	R4+D D=S1 SL	(R4)+(S1)→R4;bus→SIN/COS
DC	0000	PC	increment prog. counter
DD	F500	## BU VE	(SIN/COS)→bus→var. latch
DE	F900	## TM	enable timing pulse
DF	0000	PC	increment prog. counter
E0	1CE0	JM E0 OR	wait timing pulse/flag
E1	0CD6	JM D6	loop back to 'D6'
E2	1CE2	JM E2 OR	wait for timing pulse
E3	0CCF	JM CF	loop back to 'CF'
E4	0400	AR	jump to addr. in addr.

Note: The following notation convention has been used: The contents of a symbolic address are indicated by enclosing the symbolic address in parentheses, e.g.:

(R0) = Contents of register '0'
"Rx" refers to the accumulator registers in the ALU
"Sx" refers to the register file external to the ALU
"→" arrows indicate data flow, e.g., (R0)+(S1) → R0 → bus, means that the contents of R0 are added to the contents of S1, the result is stored in R0 and also transferred to the bus.

5.4 Auxiliary Programs

In addition to the main program for sinewave generation outlined above, an auxiliary program for a static check of the digital-to-analog converters is contained in the read-only memory and described in section 5.4.2 below.

5.4.1 Accessing Memory Locations in the Read-Only Memory (PROM)

When the STOP command key is depressed the default address "06" is shown on the display. This is the starting address of the sinewave generation routine. However, the starting address can be modified to access any of the 256 locations of the read-only memory by using the numerical and hexadecimal keys on the front panel keyboards, and the modified address will be displayed. The RUN or SINGLE-STEP command initializes the sequencer by first transferring the address from the display to the sequencer address register and then setting the memory address to zero. As a next step, the sequencer executes the instruction at location '00.' This instruction selects the contents of the address register as the next memory address, and program execution then proceeds from there.

5.4.2 Static Check of Digital-to-Analog Converters

The program permits setting the input code to the converters from the keyboard, or through equivalent remote instructions. In normal operation phase angle or offset information entered through the keyboard (or remotely) is first converted into two's complement scaled binary code where 359.999 represents "+ full scale," 360.000 represents "- full scale," 180.000 represents "+ half scale," -180.000 represents "- half scale," etc. To generate sinewaves these binary angles are applied to the angle-to-sine conversion circuits. To check various output levels of the digital-to-analog converters, the binary angles are directly applied to the converters without first going through the sine function module. Equivalent input codes, expressing the binary input to the converters in terms of decimal angles will be found in section 8.3.1. The OFFSET setting determines the code for the converters in the reference channel, and the PHASE entry determines the binary code for the converter in the 'variable' phase channel. Once selected, the converter inputs will be repeatedly applied at a rate dependent on the frequency setting of the Phase Standard.

Using the symbols similar to those in section 5.3.5, the coding for the converter test program is shown below.

Table 5.3 Digital-to-analog converters test

Memory Address	Hexadecimal Instruction	Mnemonic Instruction	Comments
00	0400	AR	jump to address in addr. reg.
A0	A2C3	LD R0 WITH S3 OE FE	set "Phase" for reference ch.
A1	0000	PC	increment prog. counter
A2	A48B	LD R1 WITH S2 OE VE	set "Offset" for variable ch.
A3	0000	PC	increment prog. counter
A4	F900	## TM	enable timing pulse
A5	0000	PC	increment prog. counter
A6	1CA6	JM A6 OR	wait timing pulse
A7	0CA0	JM A0	loop back to 'A0'
A8	0400	AR	jump to addr. in addr. reg.

6. MICROCOMPUTER CONTROL

6.1 Microcomputer (8085) Architecture

(For details see the "INTEL" Microcomputer Systems User's Manual)[3].

6.1.1 Microprocessor Unit (see also section 7.3.1)

The 8-bit microprocessor uses a multiplexed 16-bit address and an 8-bit data bus. The program is stored in 8 kilobytes of EPROM (erasable programmable read-only-memory), and 4 kilobytes of RAM (random access memory). The RAM chips also contain input/output (I/O) ports which provide 33 parallel bit paths for communication with the Microcomputer Interface Unit described below.

6.1.2 Microcomputer Interface Unit (see also section 7.3.2)

The interface unit is designed to decode instructions and transmit data generated by the microcomputer to various components of the Phase Standard system. Data are received from the microcomputer over a 16-bit unidirectional bus and transmitted to the microcomputer over a 15-bit bus. The interface serves to make communication between the Phase Standard system and the microcomputer substantially independent of the particular type of microprocessor used, as long as the microcomputer is configured to have a 16-bit parallel I/O channel.

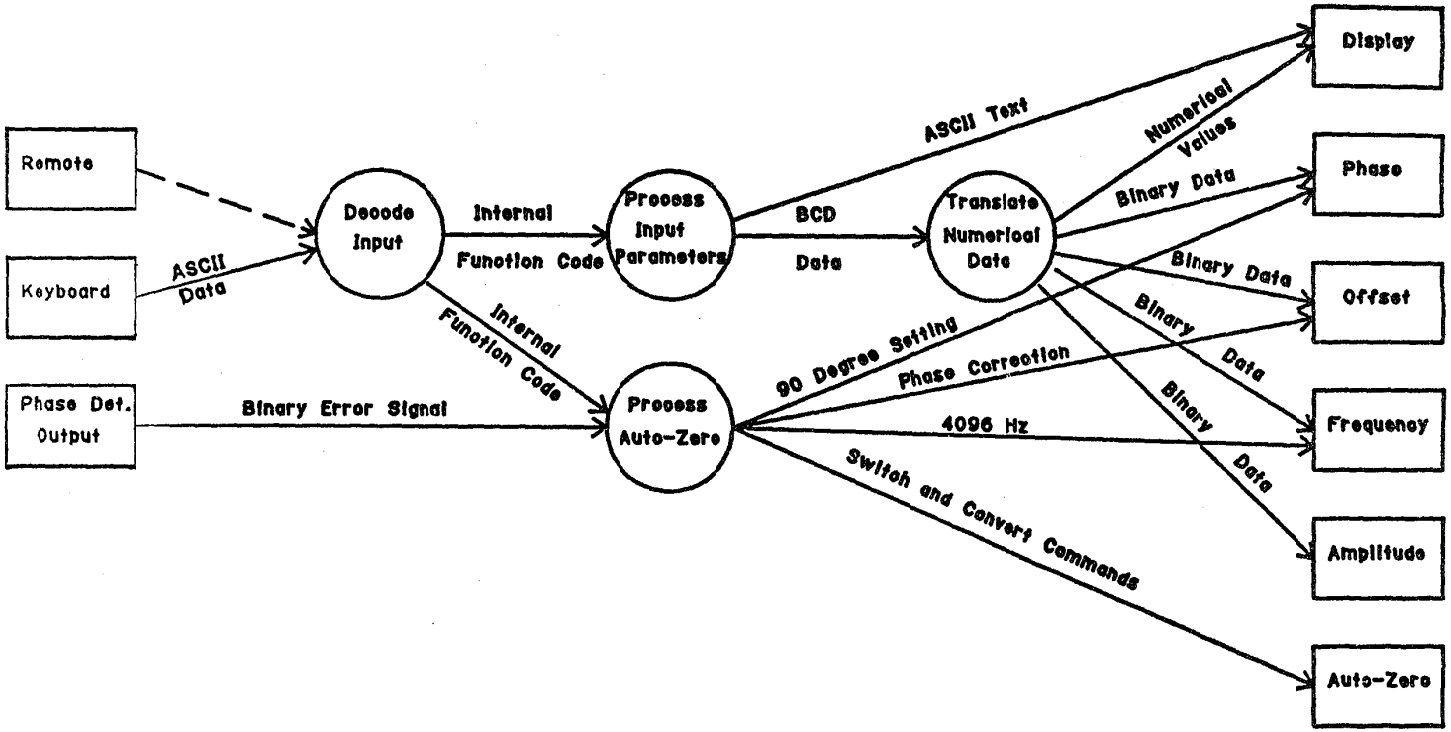
Information is formatted so that the least significant eight bits of the data word transmitted from the microcomputer constitute an instruction or destination address and are decoded by the interface.

The codes used are shown in table 6.1. The remaining eight most significant bits of the data word transmitted contain binary numerical information or ASCII characters.

This numerical or ASCII information is latched, one byte at a time, into 8-bit registers connected to the low-speed 16-bit and the high-speed 20-bit buses (see section 5.1.1 and figure 5.1). Similarly, data coming from the system to the interface is latched into registers and then transmitted to the microcomputer via the 15-bit I/O lines.

Table 6.1 Interface codes

Bits 4 3 2 1 0	Function
0 0 0 0 0	--Not Assigned--
0 0 0 0 1	Multiplying D/A Converter, Reference Phase Amplitude
0 0 0 1 0	Multiplying D/A Converter, Variable Phase Amplitude
0 0 0 1 1	Phase Detector Channel A, Attenuator Setting
0 0 1 0 0	Phase Detector Channel B, Attenuator Setting
0 0 1 0 1	A/D Converter, Convert Command
0 0 1 1 0	Display, Strobe Pulse
0 0 1 1 1	Display, Load Command
0 1 0 0 0	Sequencer System Clock Synchronizer, Set
0 1 0 0 1	Sequencer System Clock Synchronizer, Reset
0 1 0 1 0	Synthesizer Latch Clock Pulse
0 1 0 1 1	Sequencer Address Register Enable
0 1 1 0 0	A/D Converter Preset (Override Command)
0 1 1 0 1	Phase Det. Channel Reversing Switch, Normal (Ref=A)
0 1 1 1 0	Phase Det. Channel Reversing Switch, Reverse (Var=A)
0 1 1 1 1	Buzzer
1 0 0 0 0	--Not Assigned--
1 0 0 0 1	Low-Speed 16-Bit Bus, Least Significant 8 Bits Enable
1 0 0 1 0	Low-Speed 16-Bit Bus, Most Significant 8 Bits Enable
1 0 0 1 1	High-Speed 20-Bit Bus, Least Significant 4 Bits Enable
1 0 1 0 0	High-Speed 20-Bit Bus, Intermediate 8 Bits Enable
1 0 1 0 1	High-Speed 20-Bit Bus, Most Significant 8 Bits Enable
1 0 1 1 0	Angular Increment Ready Signal
1 0 1 1 1	Phase Angle Ready Signal
1 1 0 0 0	Offset Angle Ready Signal
1 1 0 0 1	A/D Converter Output Enable, Interface Latch Enable
1 1 0 1 0	Interface to Microcomputer Output Enable
1 1 0 1 1	Sequencer Zero Set
1 1 1 0 0	Sequencer Clock Synchronizer, Mode 0
1 1 1 0 1	Sequencer Clock Synchronizer, Mode 1
1 1 1 1 0	--Not Assigned--
1 1 1 1 1	--Not Assigned--



Data Flow Diagram

Figure 6.1

6.1.3 Data Flow

During communication between the microcomputer and the rest of the system the following information is transmitted:

Via the 20-bit bus (to the high-speed ALU):

1. Phase angle setting
2. Offset (angle) setting
3. Angular increment (determines number samples per cycle).

Via the 16-bit bus:

4. Reference phase amplitude setting
5. Variable phase amplitude setting
6. Synthesizer setting (timing pulse frequency)
7. Sequencer ROM starting address (hexadecimal)
8. ASCII characters to the display
9. Auto-zero phase detector output (to 8-bit microcomputer).

Figure 6.1 shows a schematic diagram of the relationships between data input and output from the 8085 microcomputer system. Input from the keyboard (or through a remote connection) is in the form of ASCII characters. These are decoded and provide an internal function code which determines how the input parameters (usually numerical) are going to be processed. The decimal (BCD) input values from the keyboard are converted into binary data which is transmitted to the high-speed processor and other parts of the system to set the phase angle, offset, frequency, and amplitude of the output signals.

For the auto-zero correction, there is an additional source of input data, the binary error signal from the phase detector. A separate data processing program module initiates the phase detector measurements and handles the algorithms to convert the error signal into an appropriate phase correction.

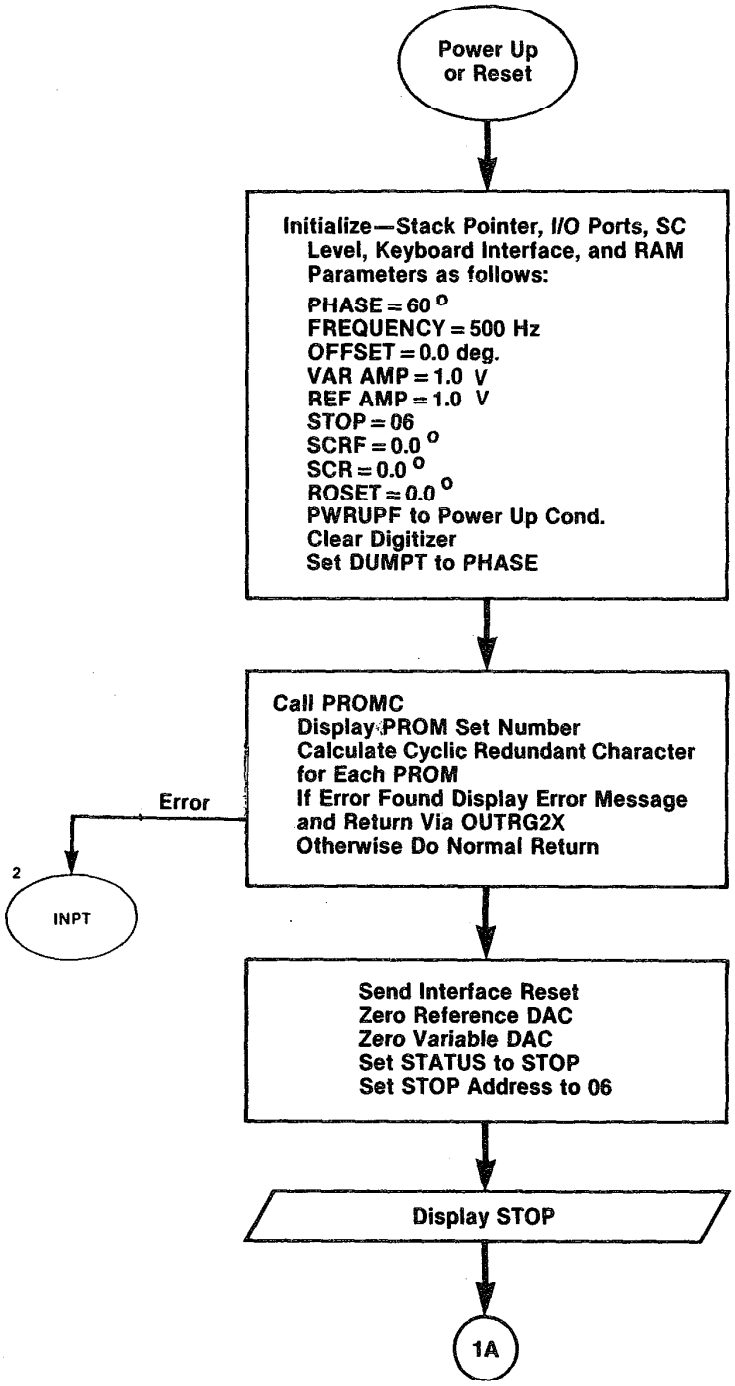
6.2 Microcomputer (8085) Software

6.2.1 Power Up/Reset Routines

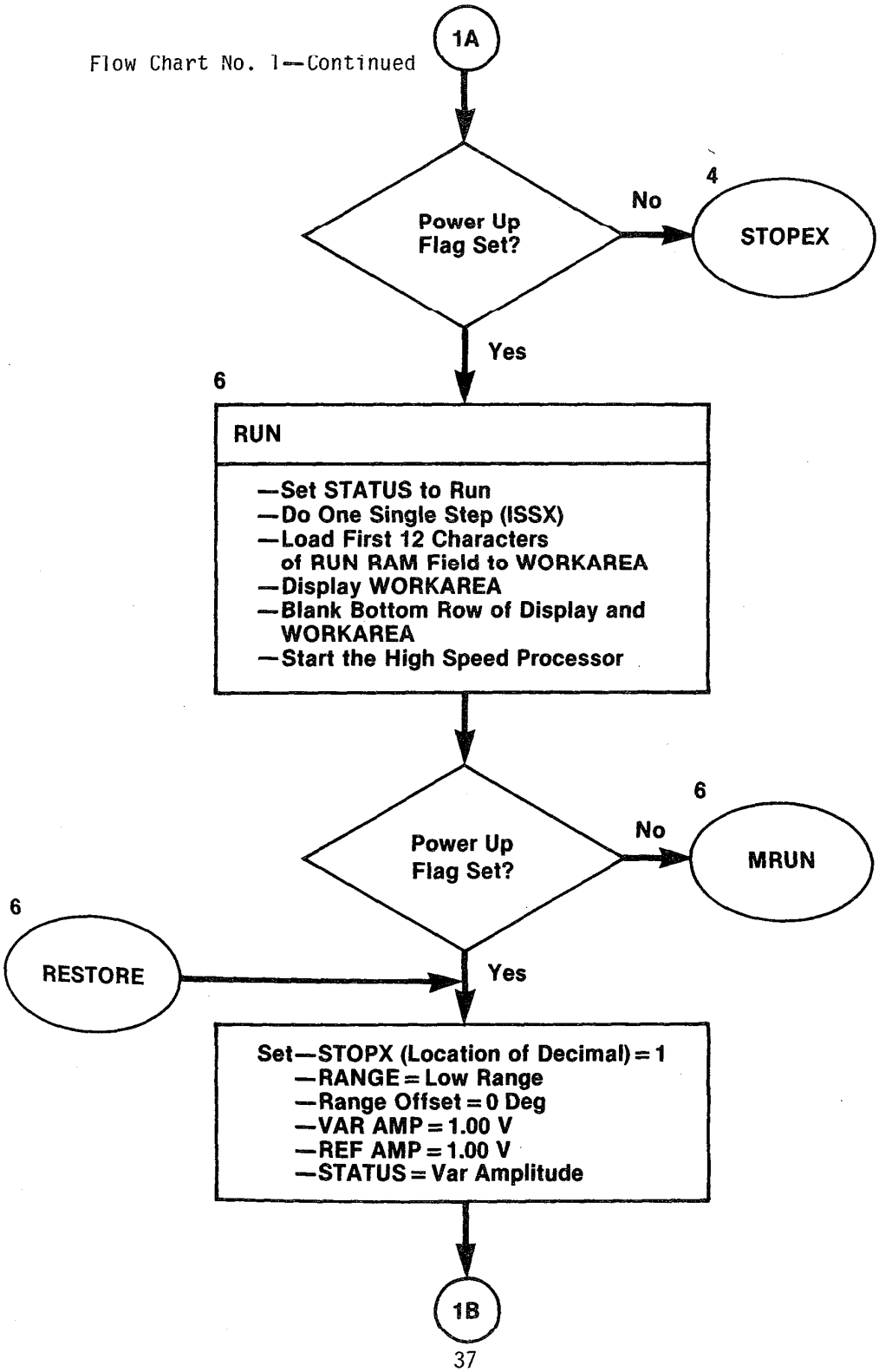
(Refer to flowchart number 1.) This software module first initializes the microcomputer and then sets up the start-up parameters for the waveform generator indicated on the chart. Initialization of the microcomputer configures the I/O ports, keyboard interface, pointers, and registers. It also stores the images of all display messages into the random-access memory, so that they can be retrieved and modified by subsequent program action.

The routine then sets a 'power-up' flag which modifies the action of other routines used during the initialization.

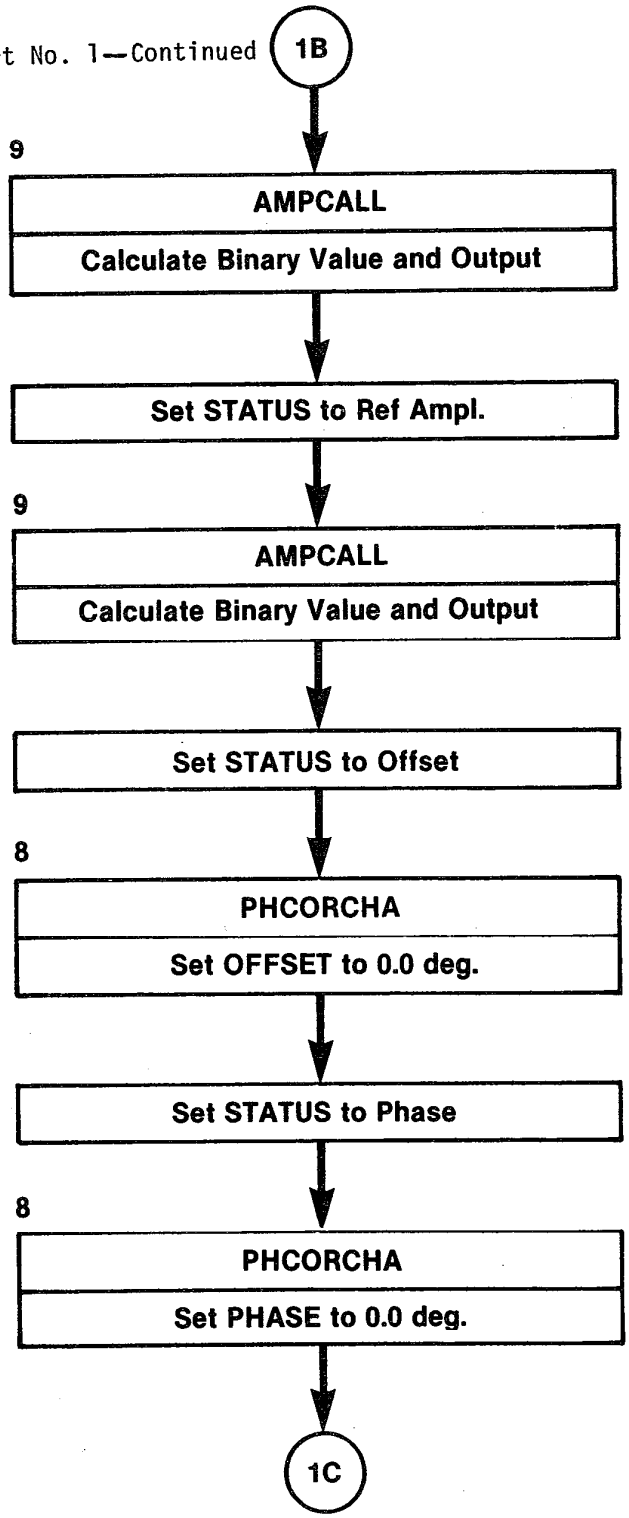
Flow Chart No. 1
Power Up/Reset Routines



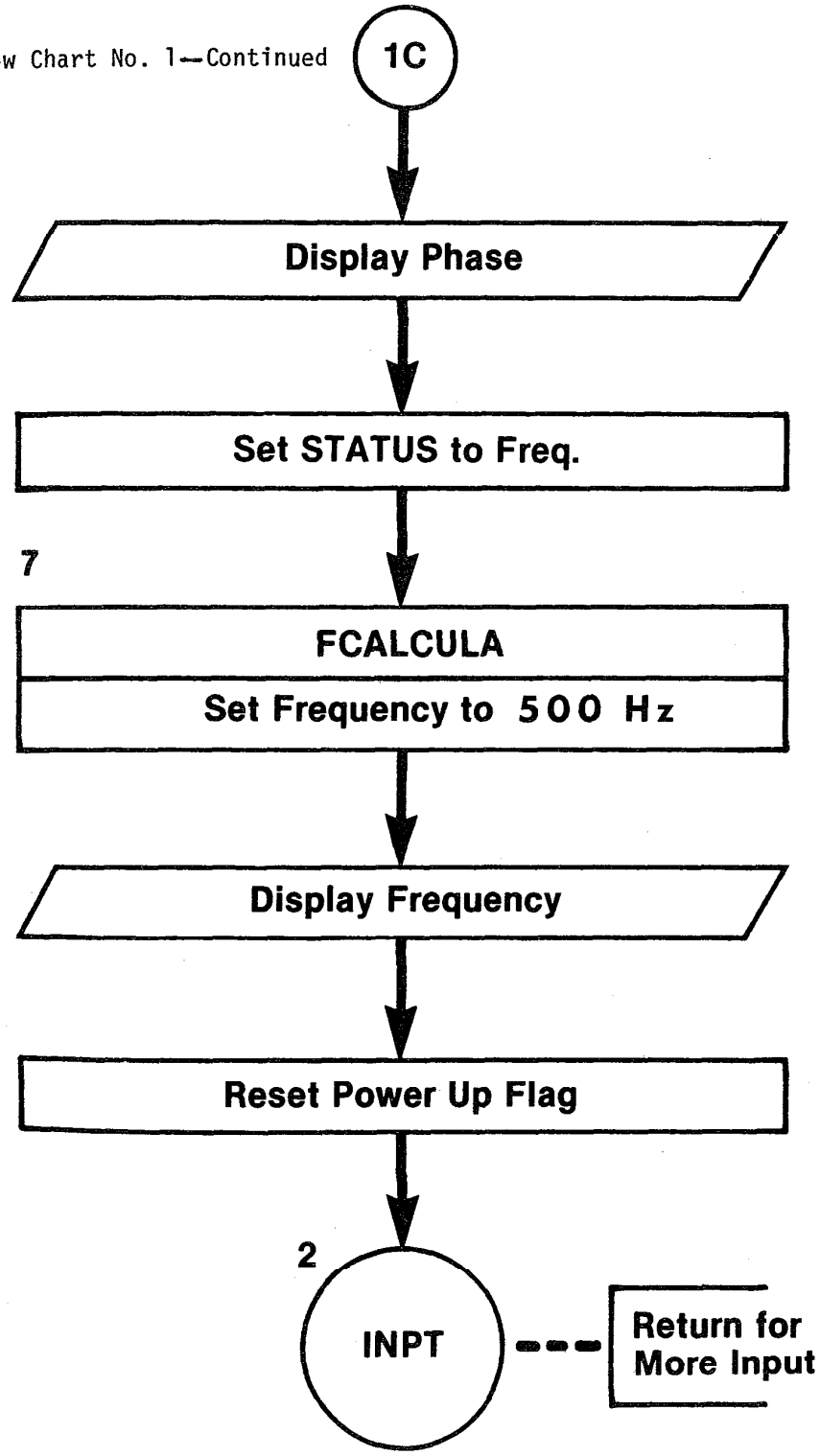
Flow Chart No. 1—Continued



Flow Chart No. 1—Continued



Flow Chart No. 1—Continued



In a second phase, a 16-bit cyclic redundancy check* is carried out on all four PROM chips, and, if errors are detected, a message is displayed locating the faulty chip. While this check is in progress, an identification number of the PROM set is displayed on the readout for visual verification.

If no errors are detected in the cyclic redundancy check, program control passes to the 'stop' routines (see flowchart number 4). These routines set both output amplitudes to zero, disable the clock of the high-speed processor, and display the message "STOP," as well as the hexadecimal starting address of the high-speed processor "06." Since the 'power-up' flag is set, the computer does not wait for further input, but proceeds immediately to the 'run' routine (see flowchart number 6). Similarly, amplitudes, phase angle, offset, and frequency are set successively to the initial default values, before the program returns to the input routine.

6.2.2 Input Routines

(Refer to flowchart number 2.) The input routine monitors the 'interrupt' and 'frequency check' flags. If the 'frequency check' flag is set, the program branches and tests an error signal generated by the hardware. The error signal indicates that the frequency of the sampling pulse, 'TP' (which triggers the digital-to-analog conversion in the high-speed processor, see section 7.2.4), is outside its normal bounds. An error message is then displayed.

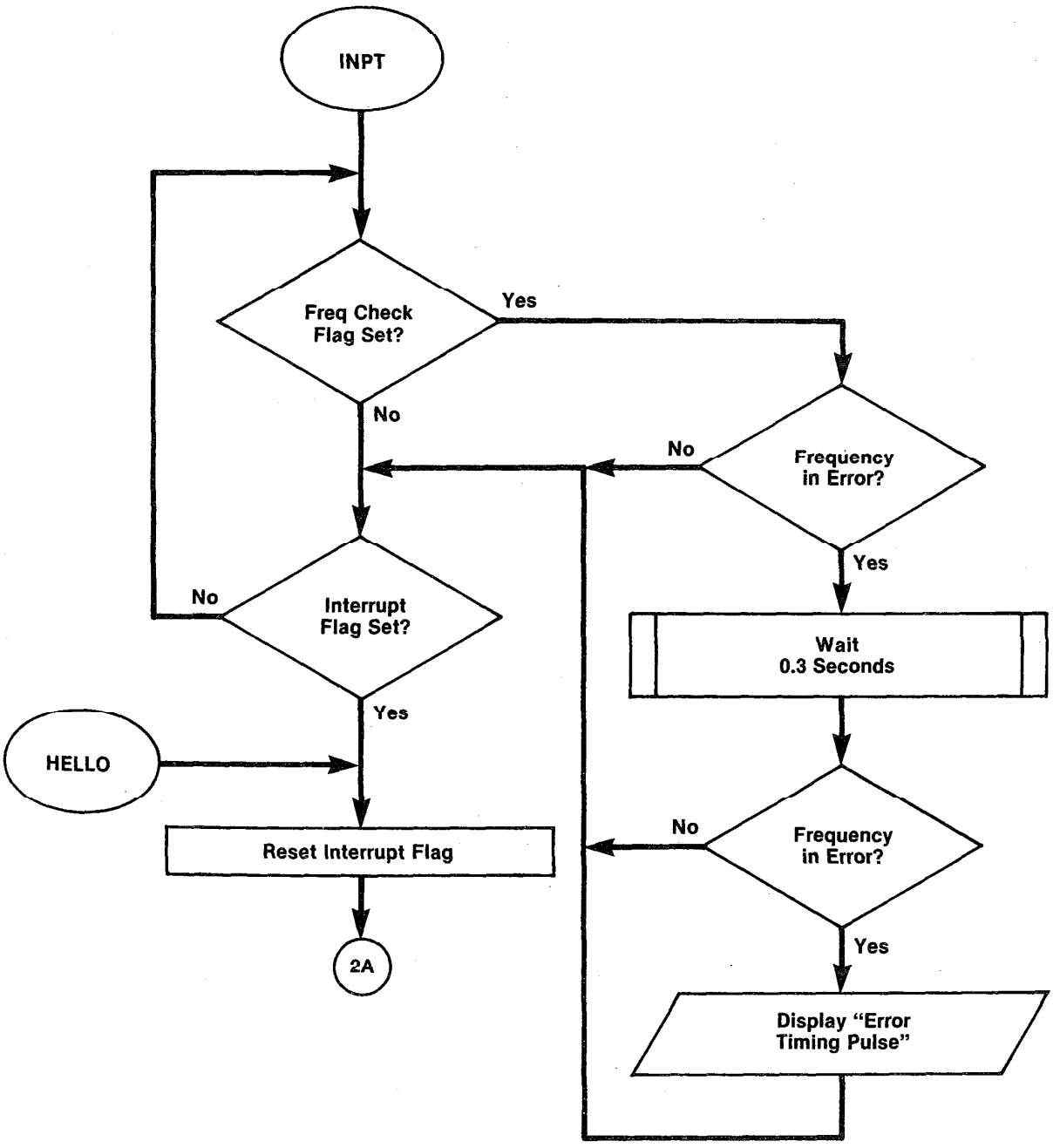
The input routine resumes by testing the 'interrupt' flag which is set whenever a key is depressed on the keyboard. The key is identified by a subset of alpha-numeric ASCII symbols (including decimal point and minus sign) which is decoded by the program. The program branches and, if the character is alphabetic, an internal code associated with the system function or quantity selected by the key is assigned to 'STATUS.' The name of the function and its associated numerical parameter is displayed on the readout.

For the 'amplitude' function an additional step is included to select either channel '0' or '1' (reference or variable phase output). For 'auto-zero,' since the routine does not require numerical input, the program proceeds directly to the series of subroutines that execute the auto-zero function. (See flowchart numbers 11, 13, 12 and 8.)

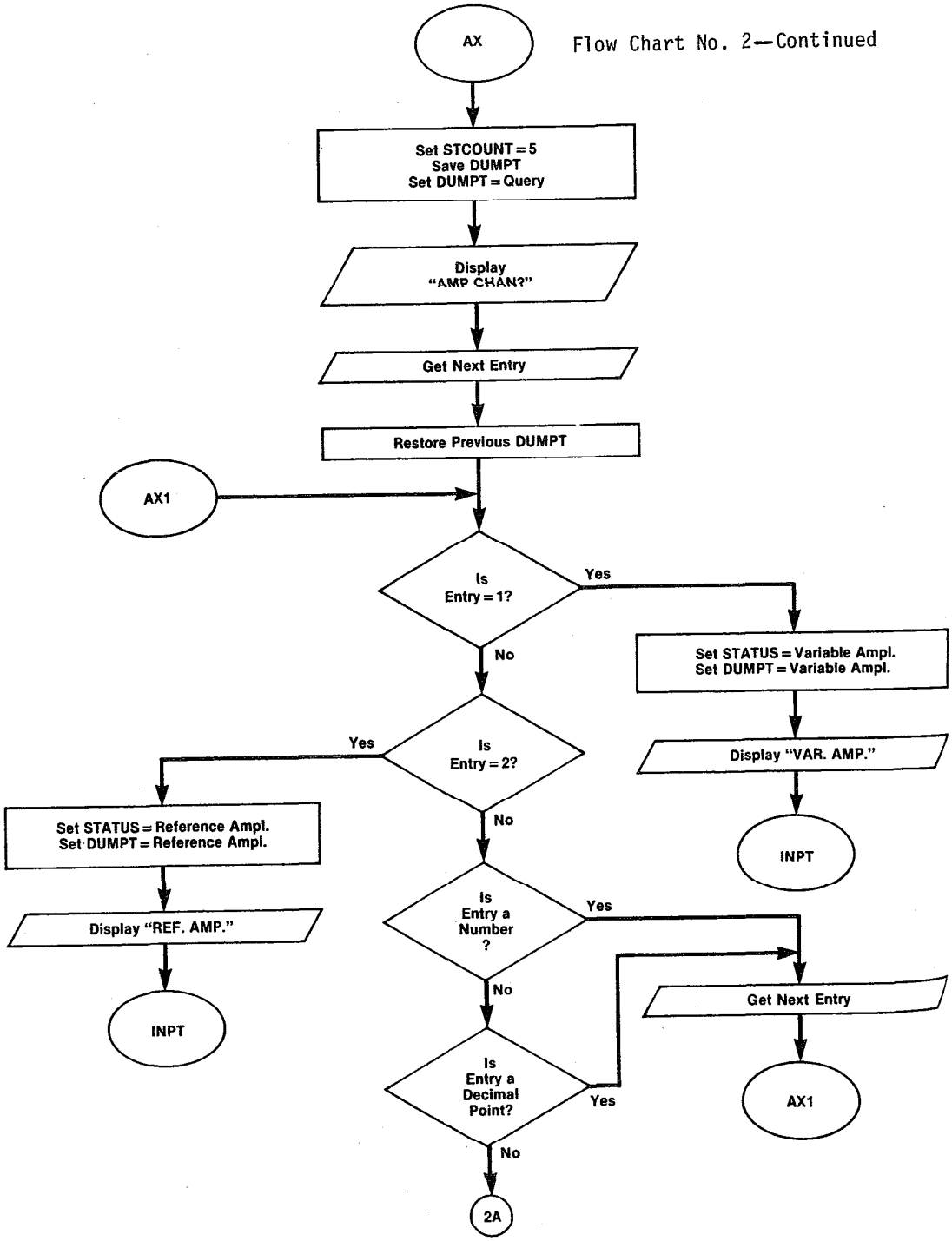
If the keyed-in character is numeric, control is transferred to NUMERIC to process the information. (See section 6.2.3 and flowchart number 3.)

*$x^{16} + x^{12} + x^5 + 1$

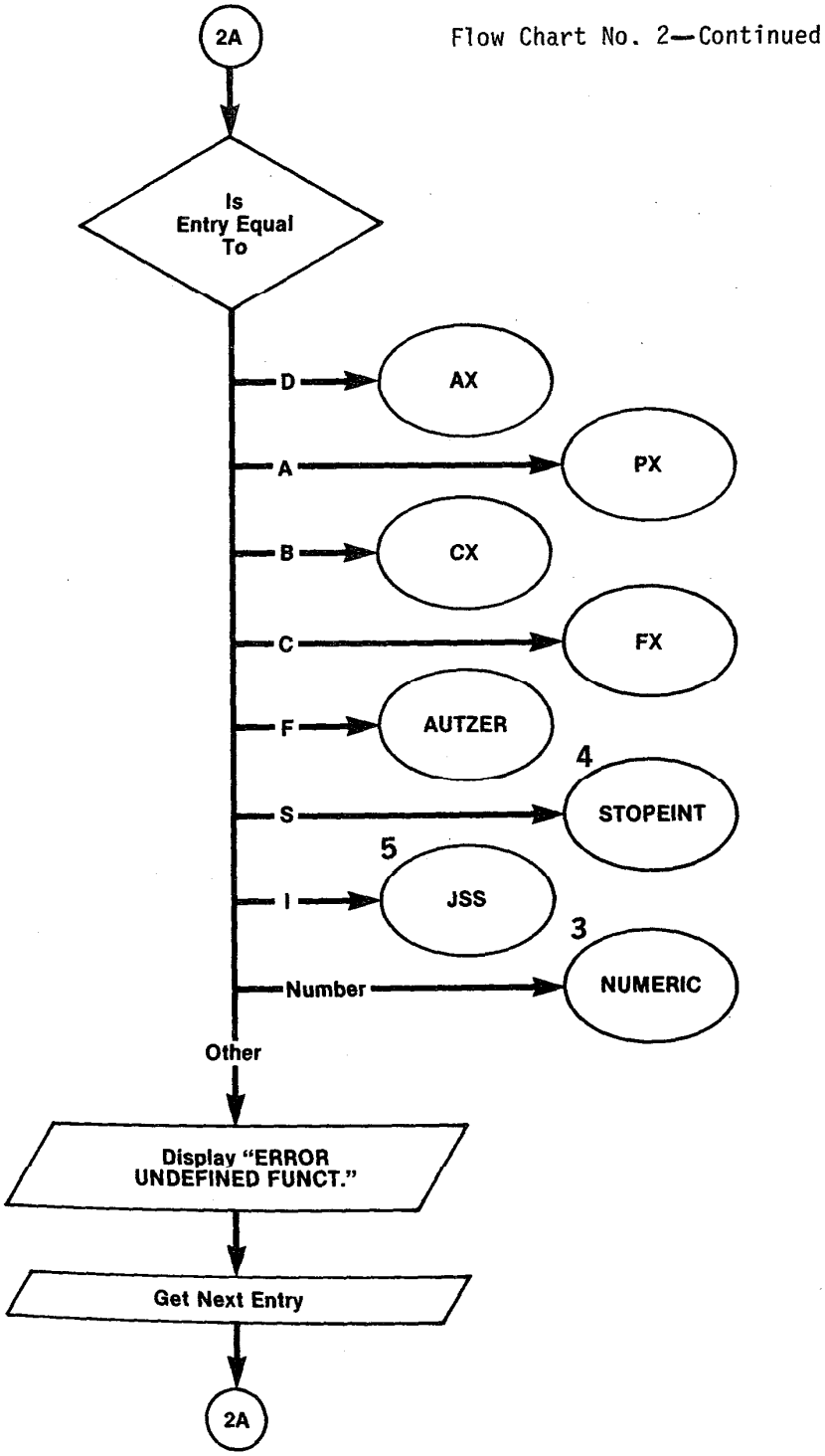
Flow Chart No. 2
Input Routines



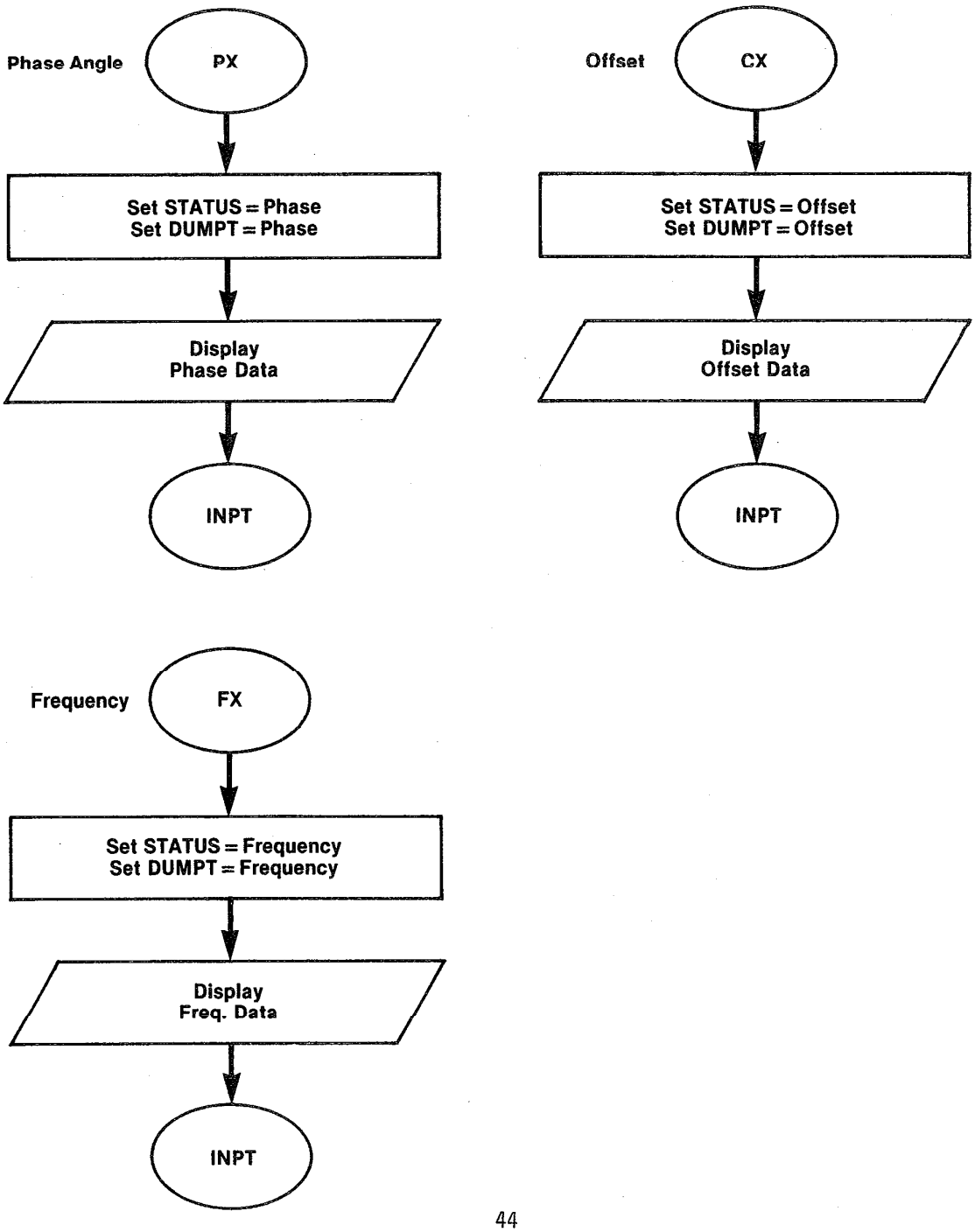
Flow Chart No. 2—Continued



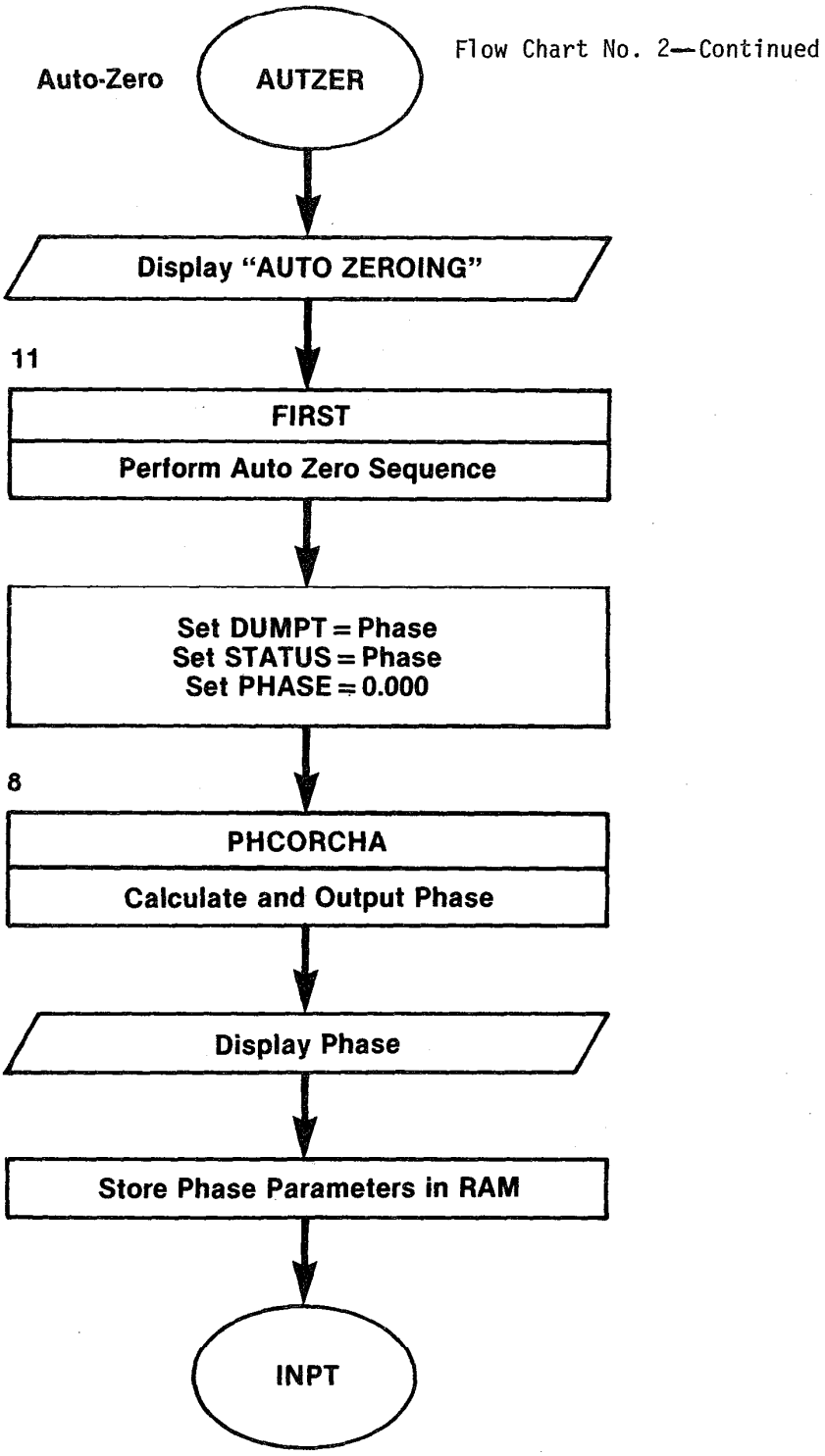
Flow Chart No. 2—Continued



Flow Chart No. 2—Continued



Flow Chart No. 2—Continued



6.2.3 Number Handling Routines

(Refer to flowchart number 3.) The first numerical entry initializes the display buffer. Since the number of digits required for various functions is not the same, the program checks the STATUS variable to determine which function is active, and branches to the appropriate routines. On the display, the numbers entered appear left-adjusted until the entry is complete and the system operating parameters have been modified. Then the number is reformatted, to insert a leading zero when needed, and appears right-adjusted on the display.

(a) Phase/Offset. An initial entry can be either:

(i) A non-zero numeral.

A jump first to NUMERHD then to HANNUM is executed, where the number is loaded into the buffer (WORKAREA, and displayed.

(ii) Zero.

A zero is loaded into the buffer and displayed, but the buffer and display pointers are left unchanged, pointing to the first data field, so that subsequent entries will overwrite the zero.

(iii) A decimal point.

A jump to NUMERHD is executed. The 'decimal' flag is set, a digit counter is preset to three, and the decimal point is displayed.

(iv) A minus sign.

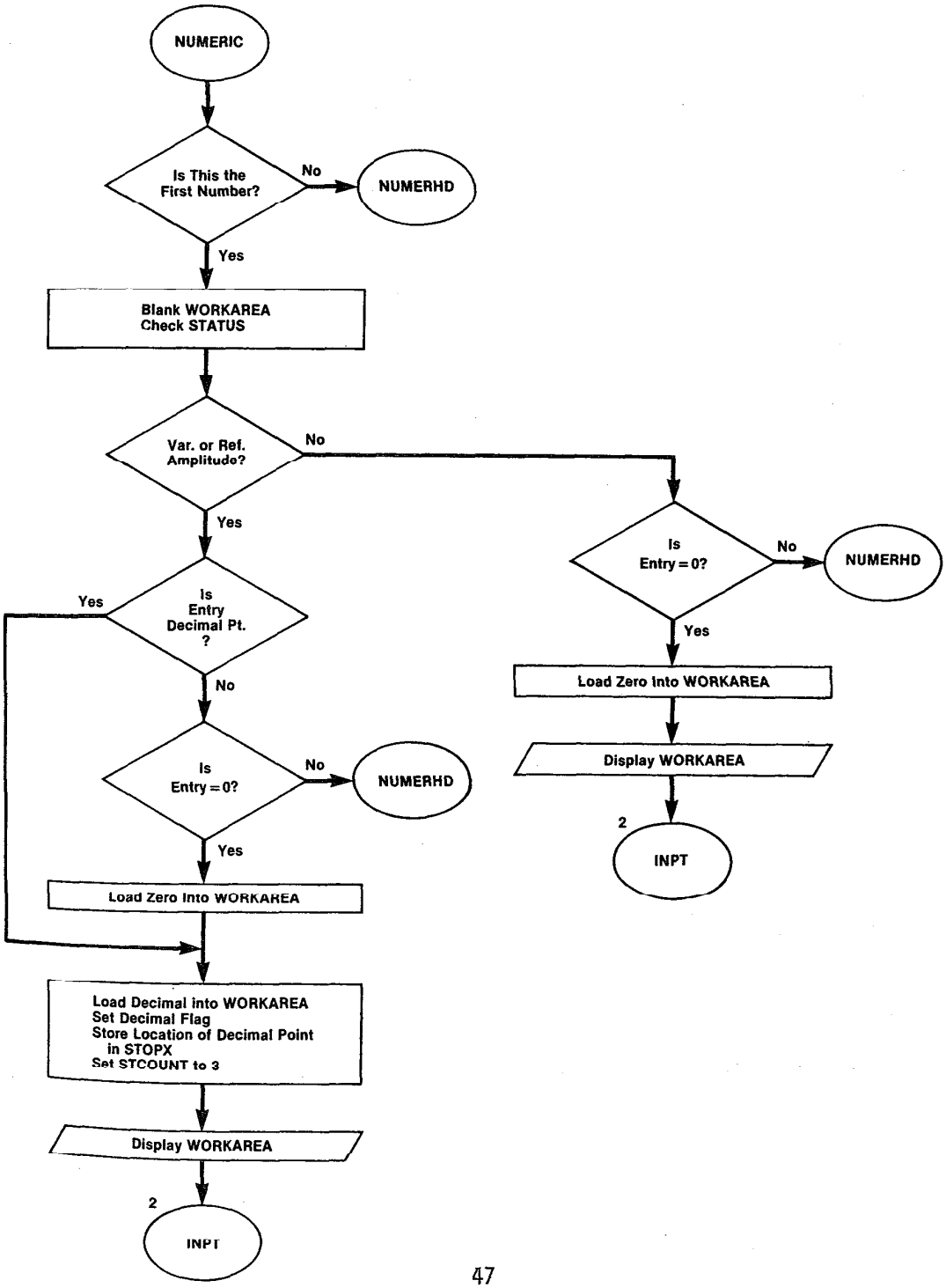
A jump to NUMERHD is executed, the 'sign' flag is set, and the minus sign is loaded into the buffer and displayed.

A subsequent entry can be either:

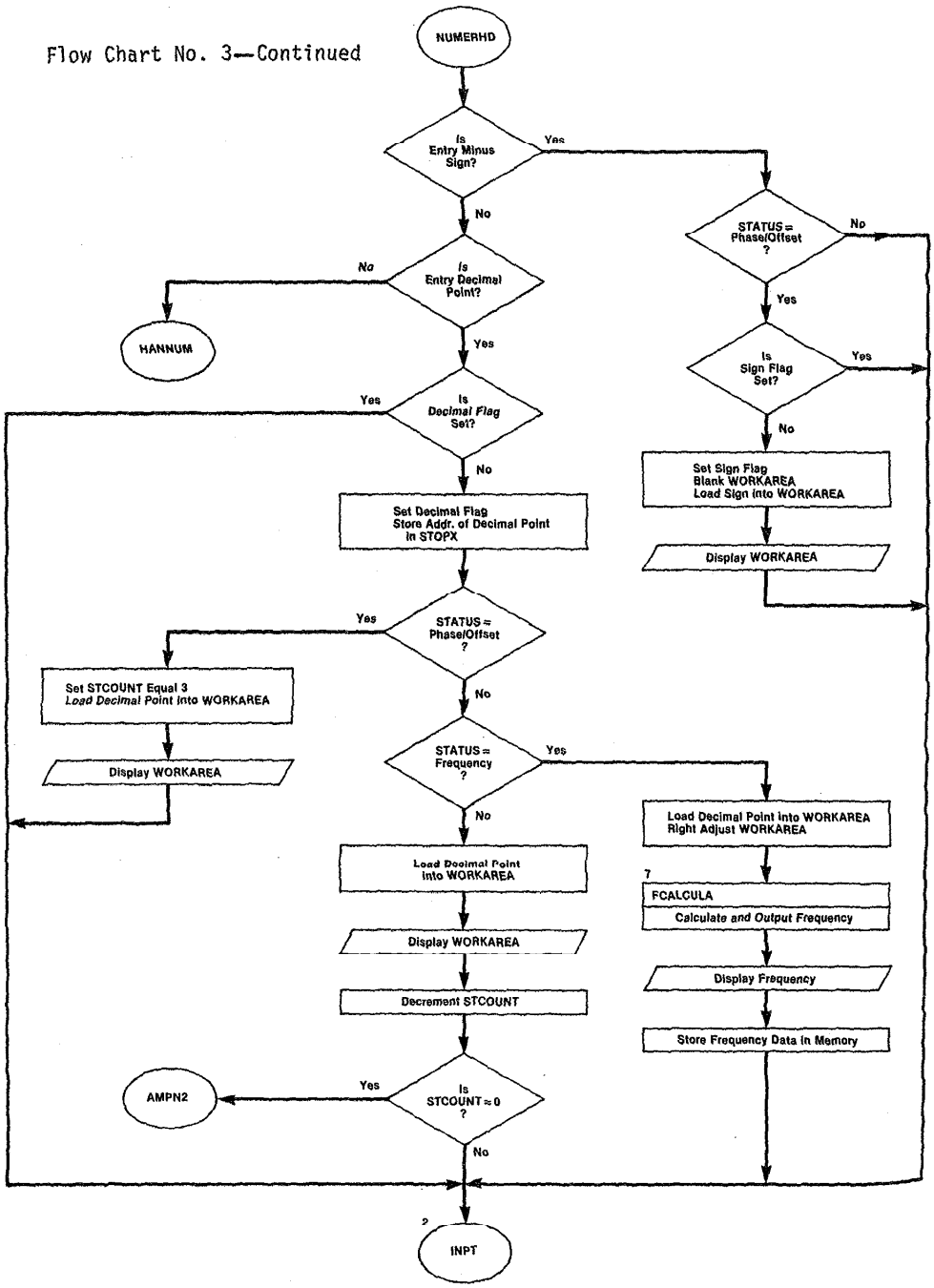
(i) A numeral.

A jump to HANNUM is executed via the NUMERHD routine. If neither the 'decimal' or 'sign' flags are set, each numeral, up to the third, is loaded into the buffer and displayed. After the third character, or the fourth if the 'sign' flag is set, a decimal point is automatically entered into the buffer and displayed, the decimal flag is set, and the digit counter is preset to three. If the 'decimal' flag is set, and three more digits have been entered, the entry is right-adjusted

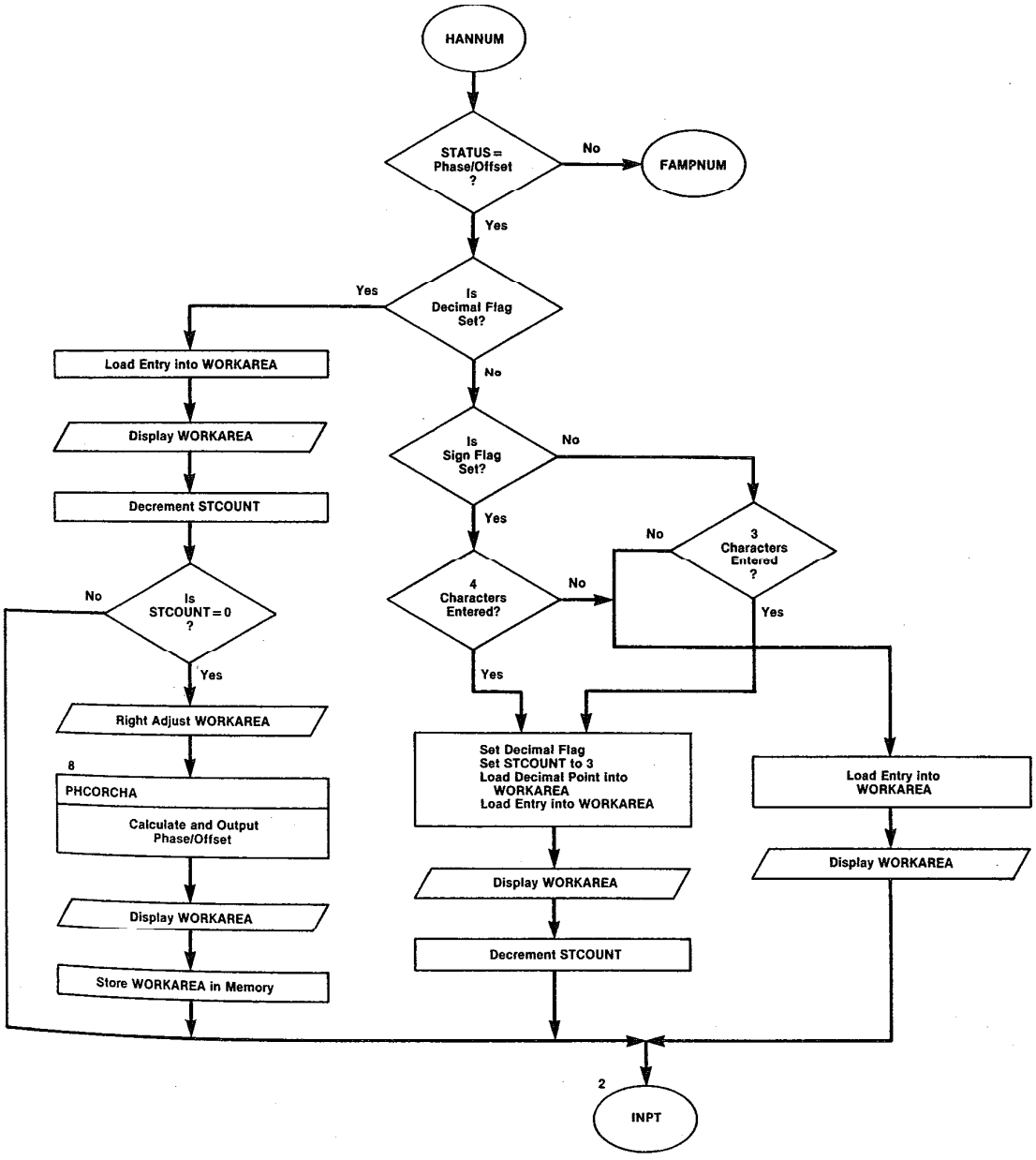
Flow Chart No. 3
Number Handling Routines



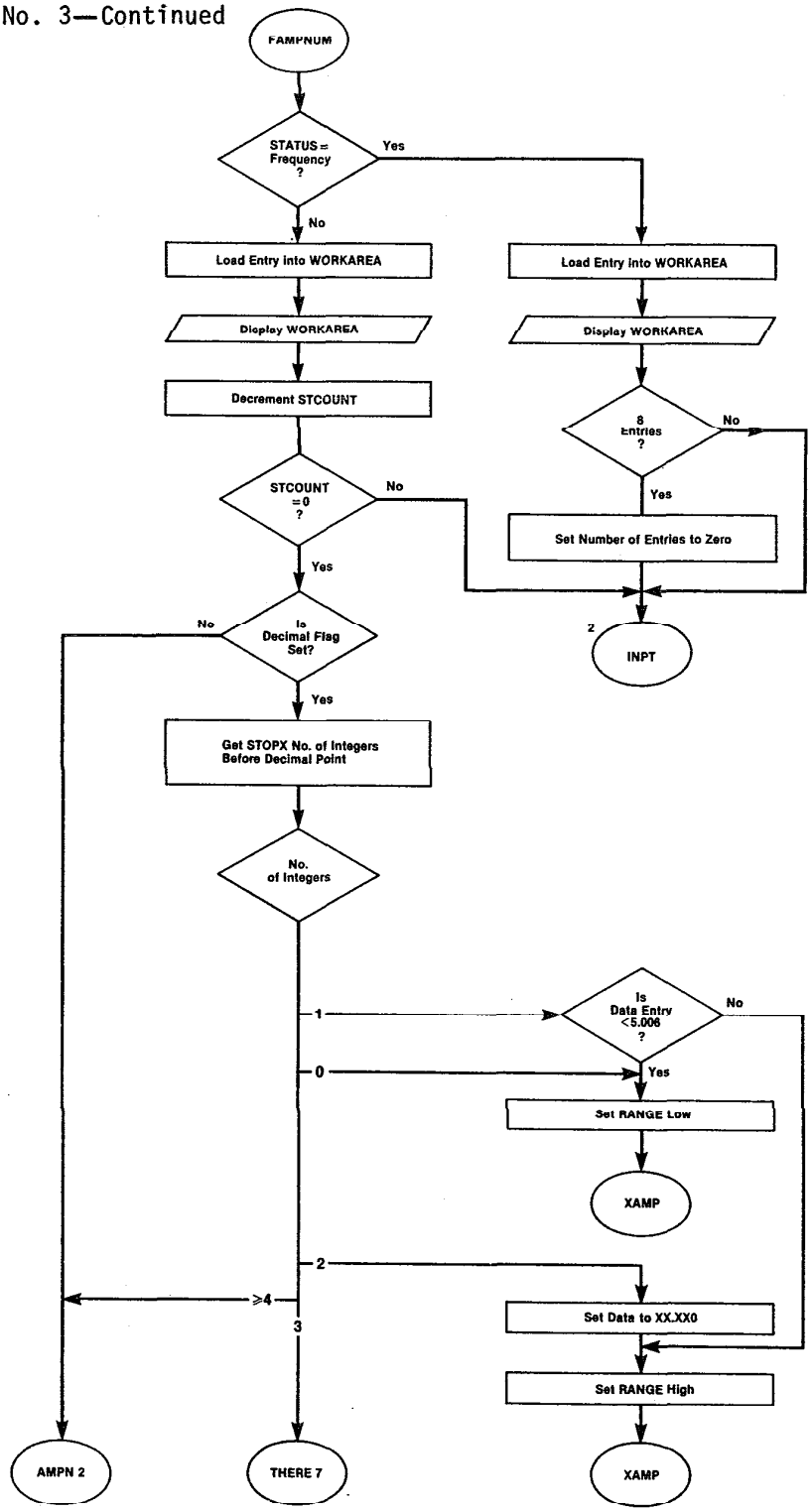
Flow Chart No. 3—Continued



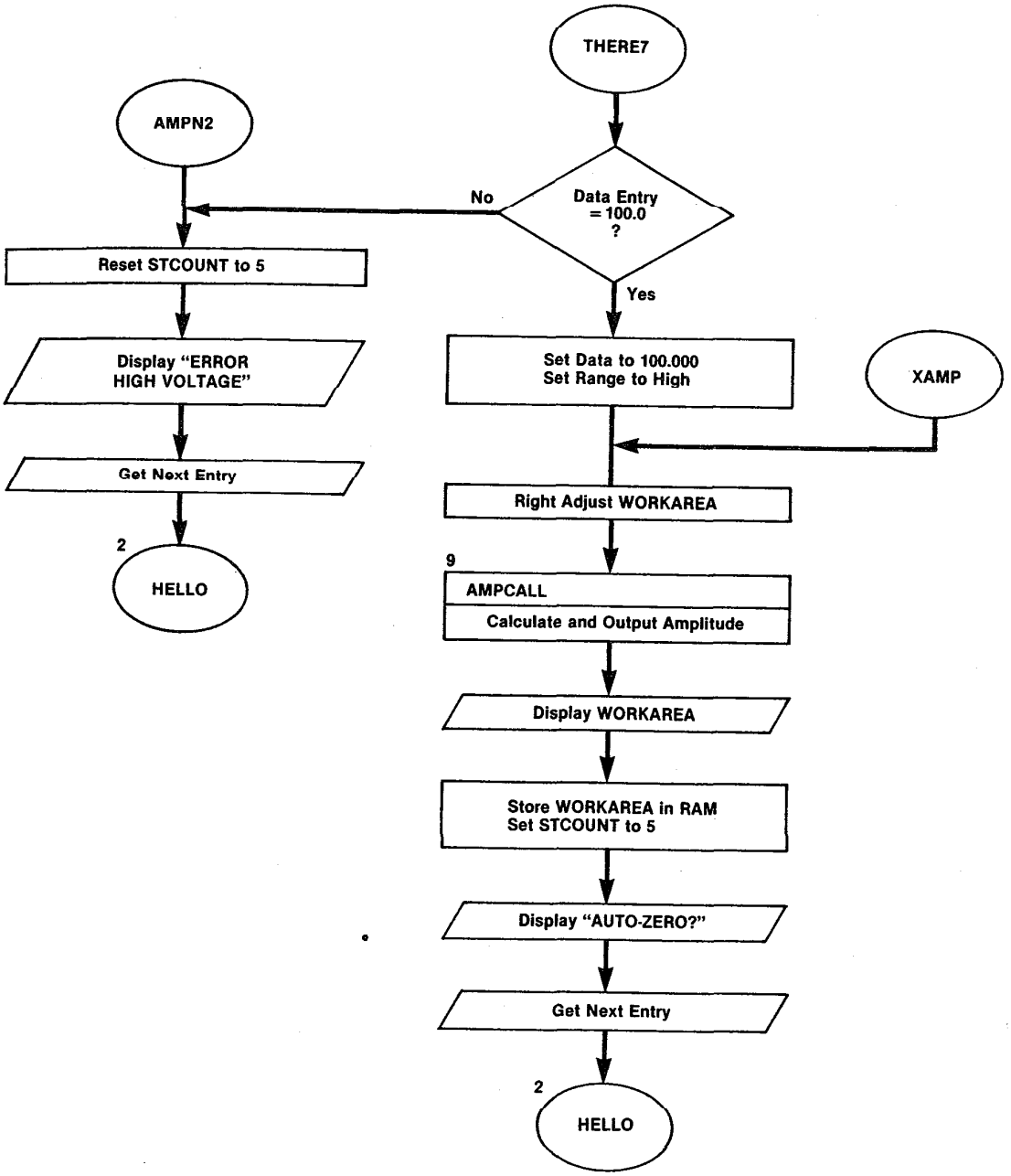
Flow Chart No. 3—Continued



Flow Chart No. 3—Continued



Flow Chart No. 3—Continued



and reformatted if required. Subroutine PHCORCHA (see section 6.2.8, flowchart number 8) is called to carry out the formatting and conversion to binary as well as sending the binary angle to the high-speed processor.

(ii) A decimal point.

Entering a decimal point causes a jump to NUMERHD. If the 'decimal' flag is already set, the entry is ignored and the routine looks for further input. Otherwise, a decimal point is added to the buffer, the 'decimal' flag is set, and the decimal point is displayed.

(iii) A minus sign.

Entering a minus sign resets all display pointers, blanks the numerical field of the display and the corresponding buffer area, unless another minus sign has been entered previously. It therefore acts as the first character in an entry. After conversion from decimal to binary, if the 'sign' flag is set, the two's complement of the binary value is formed before transfer to the high-speed processor.

(b) Amplitude. The initial entry can be:

(i) A non-zero digit.

An initial non-zero digit causes a jump to FAPNUM via NUMERHD and HANNUM, where the digit is stored in the working buffer and displayed, the digit count is reduced by one, and the program returns for further input.

(ii) Zero.

An initial "zero" is loaded into the buffer and displayed. In addition, an automatic decimal point is inserted into the buffer and the display. The 'decimal' flag is set and the location of the decimal point is stored in a separate counter (STOPX). This is necessary, because the number of places after the decimal point needed to set the amplitude varies, while for the phase angle or offset angle, for instance, three places after the decimal point are always required. The digit (down) counter is then preset to three, allowing for a total of four digits including the leading zero to complete the entry.

(iii) A decimal point.

An initial decimal point causes the same actions as (ii) above, except that zero is not entered into the buffer or display.

Subsequent numerical amplitude entries can consist of:

(i) Digits.

A jump to FAMPNUM enters and displays the digit. If the digit counter (STCOUNT) is zero and the decimal flag is set, the number of integers ahead of the decimal point is obtained from STOPX. This number is used to determine whether the amplitude is in the high or low range. For an entry with more than two places ahead of the decimal point, or one that is greater than 5.006, the high range is selected. An entry of more than four digits, or a value greater than 100.0, causes an error message to be displayed.

Whenever the decimal flag is set and the 4th digit has been entered, the contents of the buffer are right-adjusted, and routine AMPCALL (see flowchart number 9) calculates the binary value of the amplitude setting and transmits it to the output voltage control and phase detector attenuator circuits. Since the resolution of the voltage control is limited, the digits to be displayed are rounded to agree more closely with the actual output levels that can be set. Before returning for more input, a message is displayed to remind the operator to use the auto-zero function.

(ii) Decimal point.

A decimal point causes a jump to NUMERHD. If the 'decimal' flag is already set, the entry is ignored and the routine returns for more input. Otherwise, the 'decimal' flag is set, the number of digits ahead of the decimal point are stored in STOPX, the digit count is decremented, the buffer and display pointers are advanced, and the decimal point is loaded into the working buffer and is displayed.

(c) Frequency. The initial entry can be:

(i) A non-zero digit.

A jump to FAMPNUM via NUMERHD, and HANNUM is executed, the digit is entered into the buffer and the display, and the pointers are advanced.

(ii) Zero.

Zero is entered into the buffer and display, but the pointers remain unchanged so that a subsequent entry will overwrite the initial zero.

(iii) A decimal point.

A jump to NUMERHD is executed, the decimal point is loaded into the buffer, and the contents of the buffer are reformatted and right-adjusted. The buffer then contains "0." Subroutine FCALCULA is called to calculate the binary and BCD outputs, but since zero is an illegal frequency value, an error message is displayed.

Subsequent frequency entries can be either:

(i) A digit.

When a digit is entered, a jump to FAMPNUM via NUMERHD and HANNUM is executed. The numeral is entered into the buffer and displayed, and the buffer and display pointers are advanced. If more than eight digits are entered, the buffer and display pointers are reset to their initial positions so that a new value can be entered.

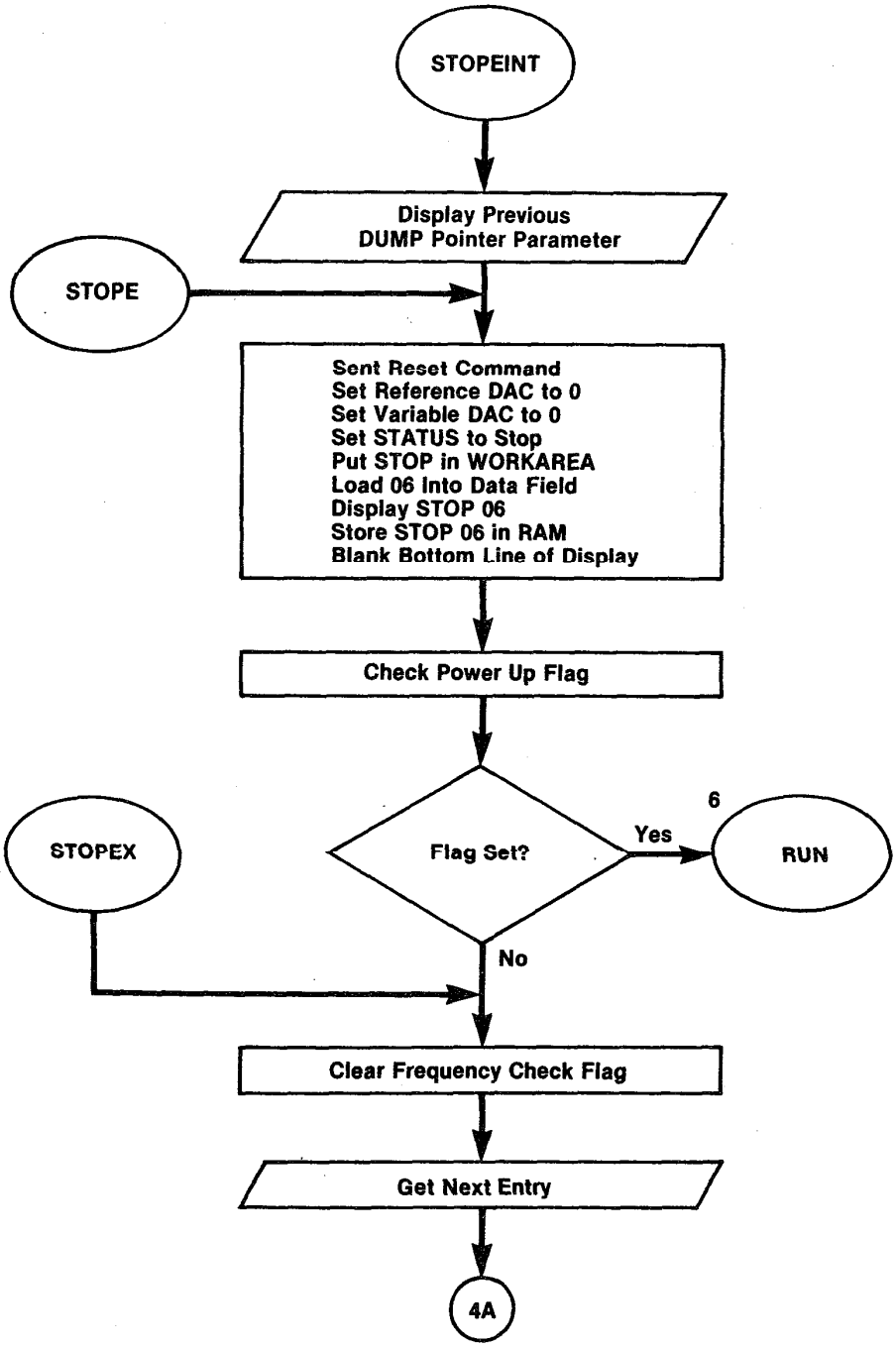
(ii) A decimal point.

A decimal point will cause a jump to NUMERHD and on testing the current value of STATUS, the program branches to a routine in which the decimal point is placed in the buffer. The number entered is then right-adjusted, and subroutine FCALCULA (see flowchart number 7) is called to compute the angular increment, which determines the number of samples per cycle, and the BCD setting of frequency synthesizer that controls the timing pulse rate. The output frequency is then displayed, and the program returns for further input.

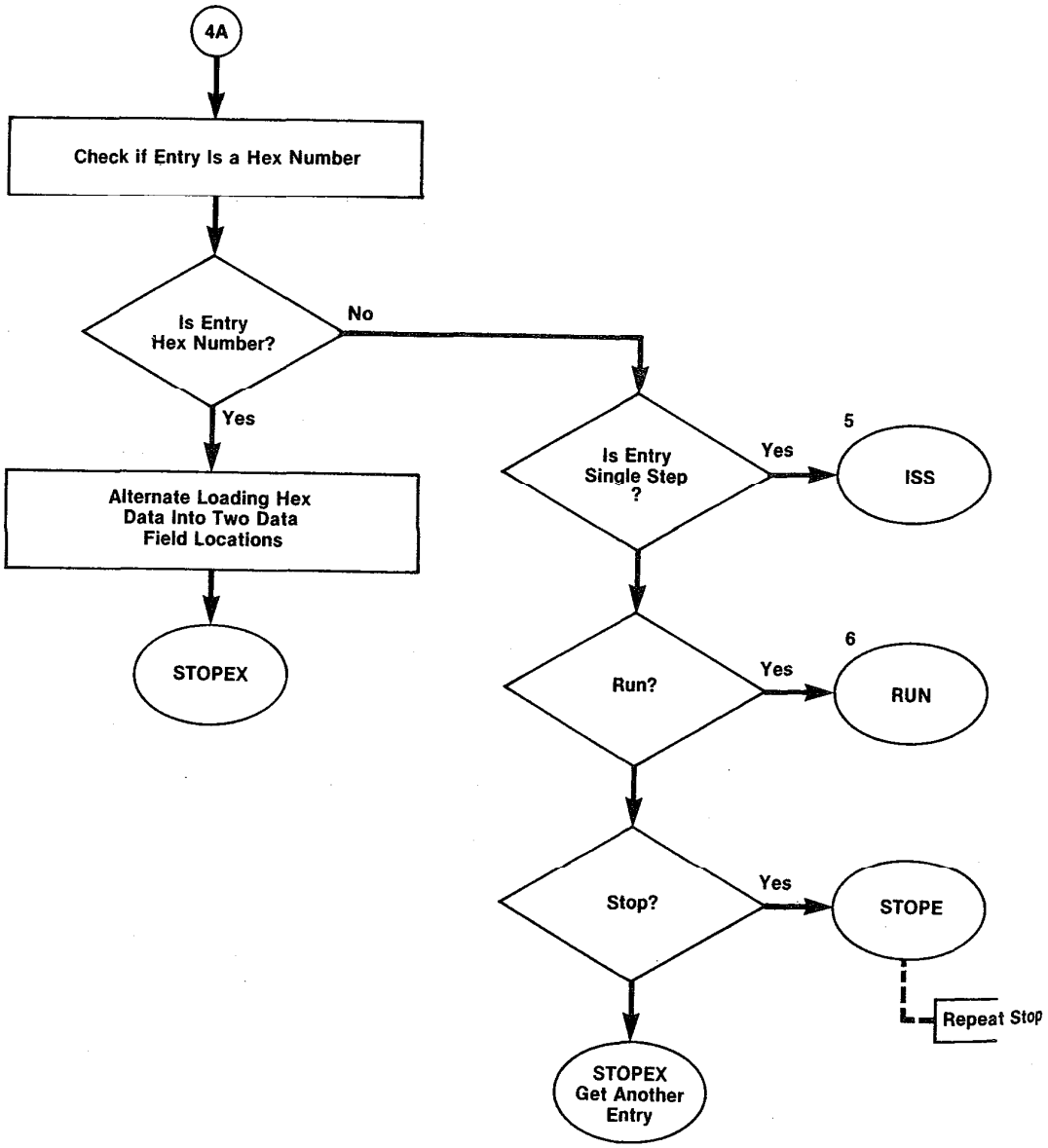
6.2.4 Sequencer Stop Routine

(Refer to flowchart number 4.) The high-speed processor is stopped by sending a reset command to the pulse synchronizer which blocks the system clock from reaching the sequencer (see section 7.2.1, figure 7.15 and 7.16). The amplitudes from both output channels are then set to zero to prevent a dc voltage from remaining on the output leads which could cause either electrical damage or shock. The message "STOP 06" is loaded into the working buffer and is also displayed in the top line of the readout while the bottom line is blanked. The hexadecimal address "06" is the starting point for the normal routine in the high-speed processor.

Flow Chart No. 4
Sequencer Stop Routine



Flow Chart No. 4—Continued



If the 'power-up' flag is not set (see section 6.2.1), the routine is then ready for further input. To prevent a possible error message because of a fault indication from the timing pulse circuit, which at this point would be meaningless, the 'frequency check' flag is first cleared. Parameter entry is limited to hexadecimal numbers and to three commands: 'Single-Step,' 'Run,' and 'Stop.' All other keys are ignored. To enter hexadecimal numbers the numerals 0 to 9 on the numerical keyboard are used as well as the top six keys on the 'function' keyboard, which are interpreted as numerals 'A' to 'F' instead of their usual function.

The routine decodes the hexadecimal number and loads two hexadecimal digits into the data field in the buffer and on the display. If more than two digits are entered, previous entries will be overwritten, so that it is easily possible to correct entries. If one of the permitted commands is used, the program will jump to ISS (single-step), RUN, or will reenter the 'stop' routine via entry point STOPE.

6.2.5 Sequencer Single Step Routine

(Refer to flowchart number 5.) The 'single-step' routine performs two distinct functions:

(1) Immediately after a 'stop' command (entry point ISS), the routine sends commands to the sequencer of the high-speed processor to execute a jump to the hexadecimal address which is loaded into the working buffer (of the 8085 microcomputer) as part of the 'stop' routine. This function is carried out by subroutine ISSX which also resets the voltage and attenuator controls to their original settings, that is, the values they had before being set to zero by the 'stop' command.

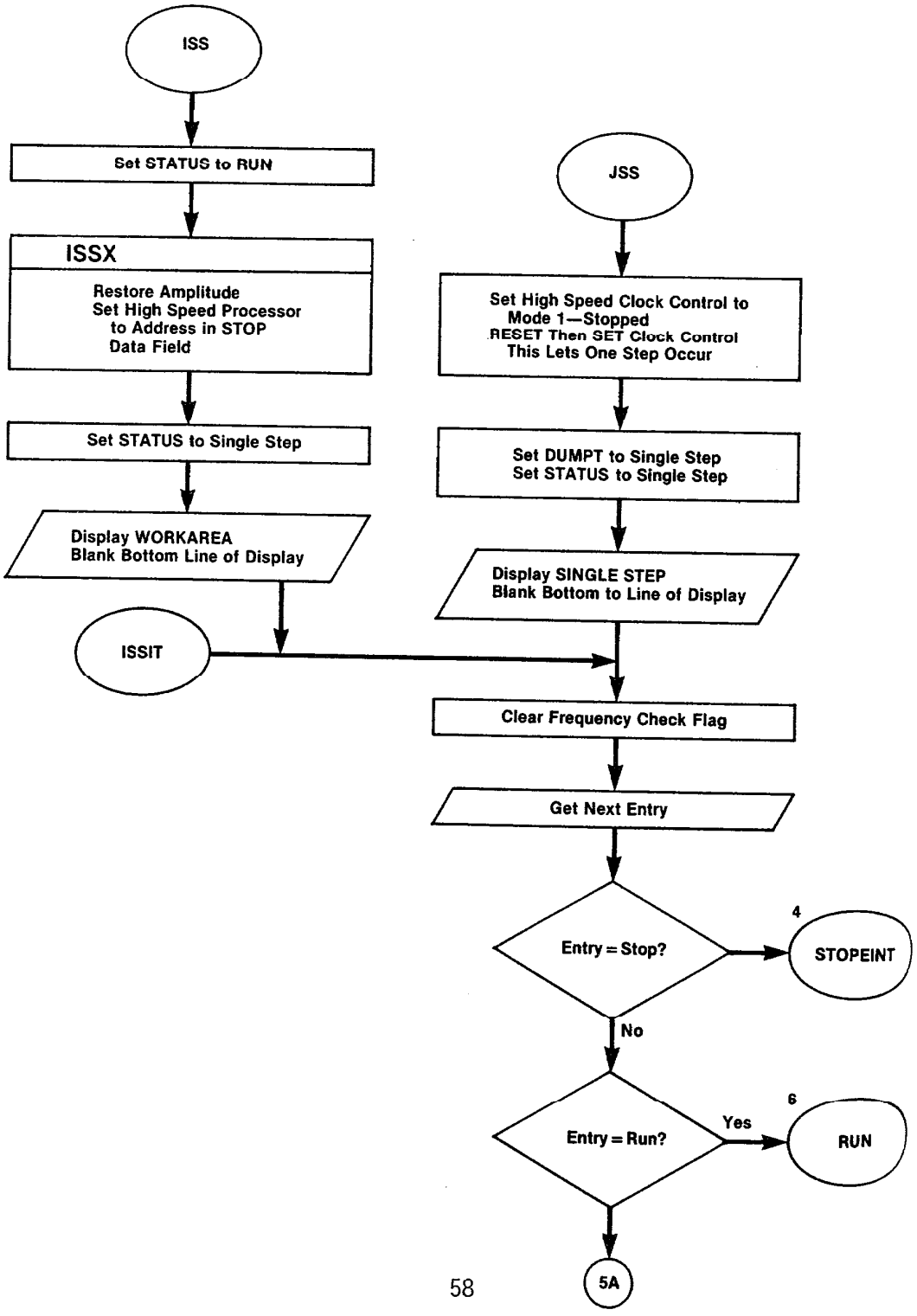
(2) At any other point, the routine (entry point JSS) programs the system high-speed clock so that the sequencer progresses through the PROM program one step at a time.

For the first function of the single-step routine the following series of commands are sent to the sequencer:

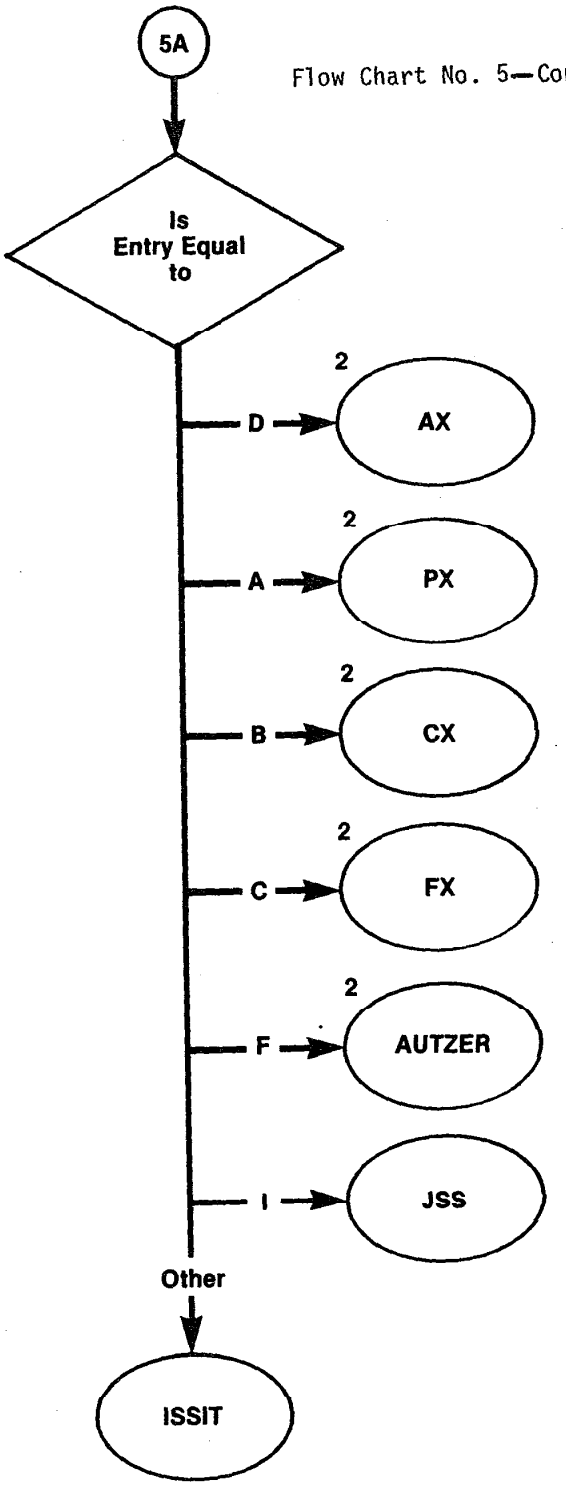
(a) The sequencer program counter is set to zero. PROM location '0' contains an instruction which loads the contents of the sequencer address register into the program counter so that this address becomes the effective starting point.

(b) The sequencer clock pulse synchronizer is set to 'mode 1.' This allows only one clock pulse from the high-speed system clock to reach the processor every time a 'set' command is given.

Flow Chart No. 5
Sequencer Single Step Routine



Flow Chart No. 5—Continued



(c) The hexadecimal address from the STOP data field is loaded onto the upper eight bits of the 16-bit bus. This prepares the transfer to the sequencer 'address register.'

(d) The 'register enable' command is loaded into the lower 8 bits of the 16-bit bus. The command is decoded on the Interface Board (see sections 7.2.1 and 7.3.2) and latches the address into the sequencer.

(e) A reset and set command is sent to the clock pulse synchronizer. These two commands act on the clock pulse synchronizer (see section 7.2.1) to allow one clock pulse to the system.

The second function of the 'single-step' routine is carried out by the branch with entry point JSS. Using commands as in (b) and (e) above, a single clock pulse is allowed to pass through to the system, so that the sequencer will advance to the next PROM location under control of the high-speed processor program. 'SINGLE-STEP' is displayed on the readout and the bottom line is blanked. The 'frequency check' flag is cleared to prevent a possible meaningless error message. The program is then ready for entry of the next command. The entry routine is similar to that described in section 6.2.2, except that the 'run' command is also recognized, but all numerical entries are ignored.

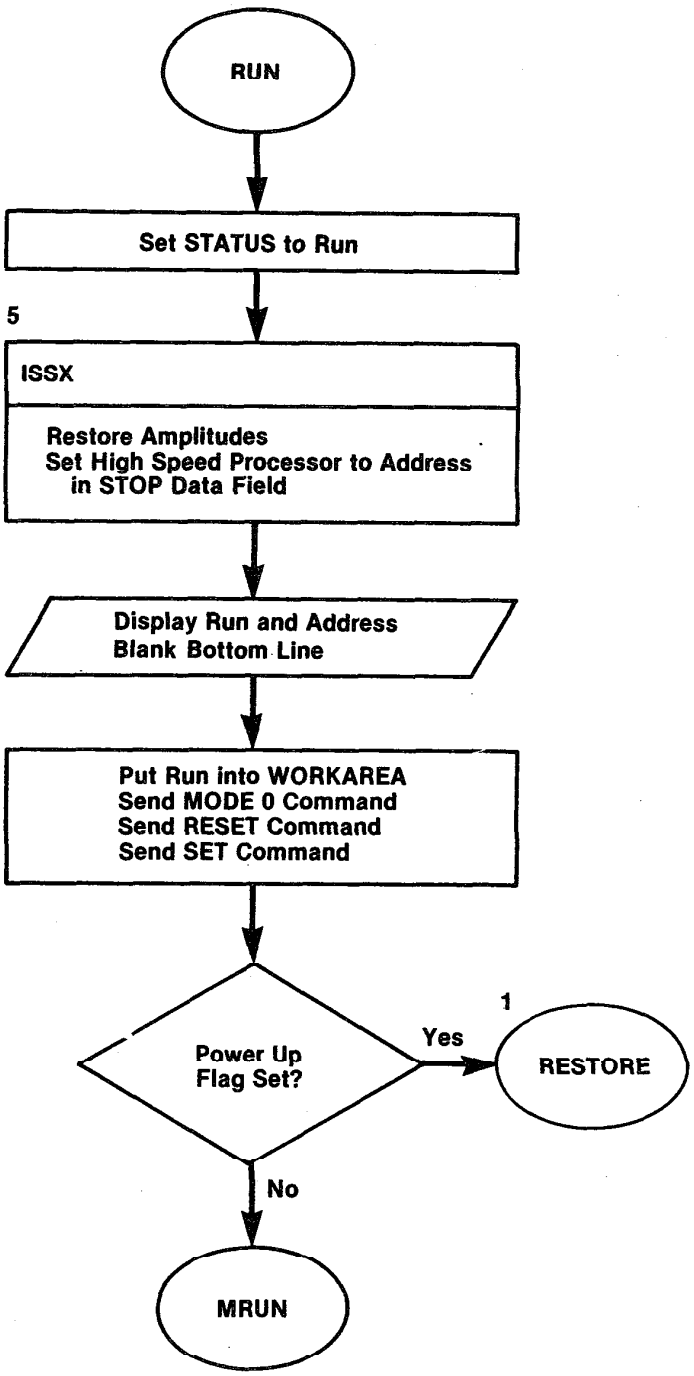
6.2.6 Sequencer Run Routine

(Refer to flowchart number 6.) The 'run' routine first calls subroutine ISSX (see section 6.2.5), which transfers the starting address from the working buffer to the sequencer of the high-speed processor. It also restores the output amplitude and attenuator settings to the selected values which have been changed to zero by the 'stop' command. The word "RUN" is displayed on the top line of the readout, while the bottom line remains blank. The sequencer is set to 'mode 0' (continuous clock pulse train), and a reset and set command are issued to start the clock pulses (see section 7.2.1). When the 'power-up' flag is not set, the 'frequency check' flag is set to enable the detection of timing pulse errors, and the program waits for the next entry from the keyboard. A numerical keyboard entry is ignored, and an alphabetic character causes a jump to the HELLO entry point of the input routine (see section 6.2.2, flowchart number 2).

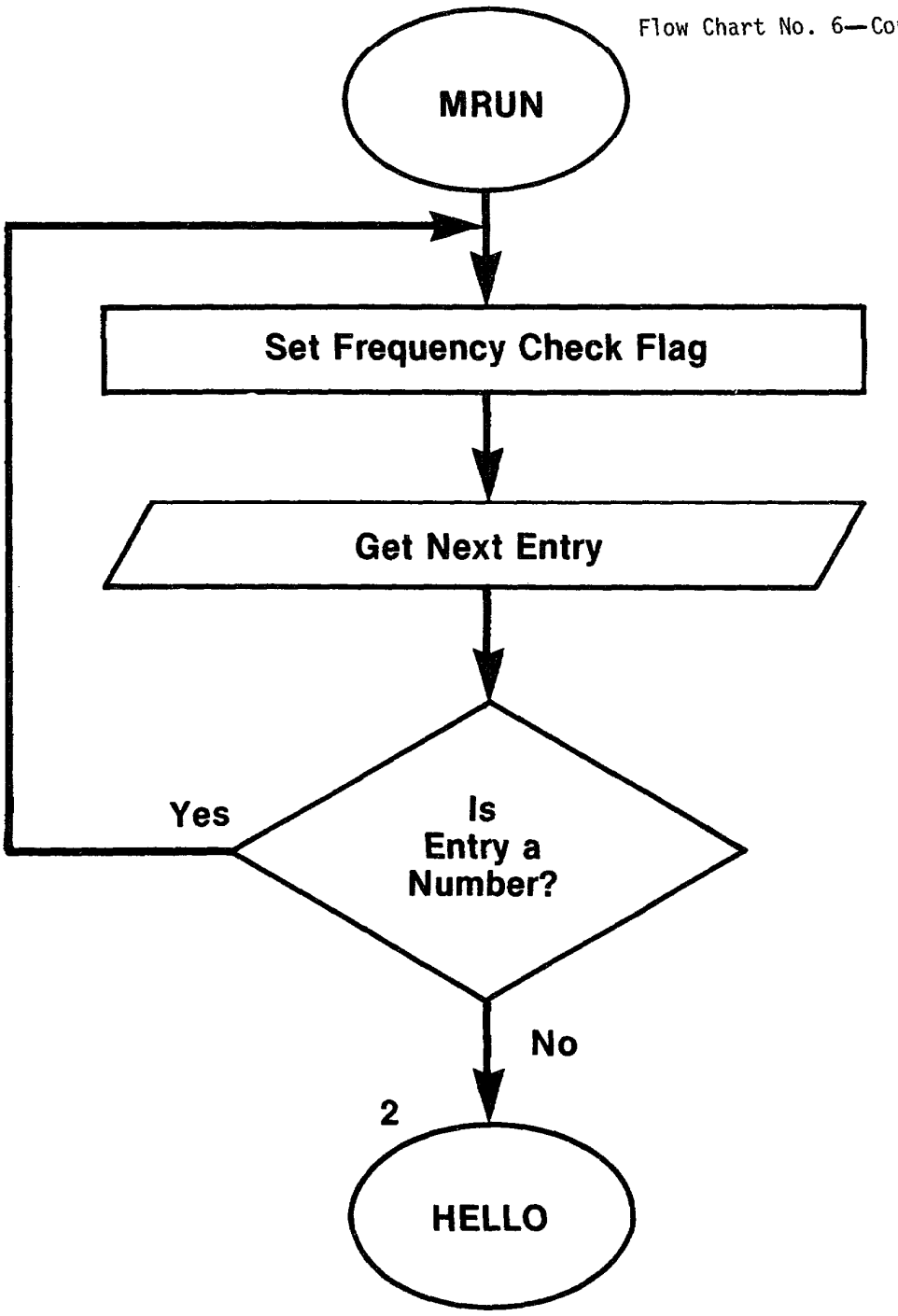
6.2.7 Frequency Calculations

(Refer to flowchart number 7.) If the entry exceeds 5000 or is zero, an appropriate error message is displayed. A valid entry is converted from ASCII to binary and the binary value is used to adjust the auto-zero correction and to calculate the phase angle increment that determines the number of sample points per cycle. This number, which is always a power of two, is used to compute the sampling frequency required by multiplying it with the binary value of the output frequency. To set

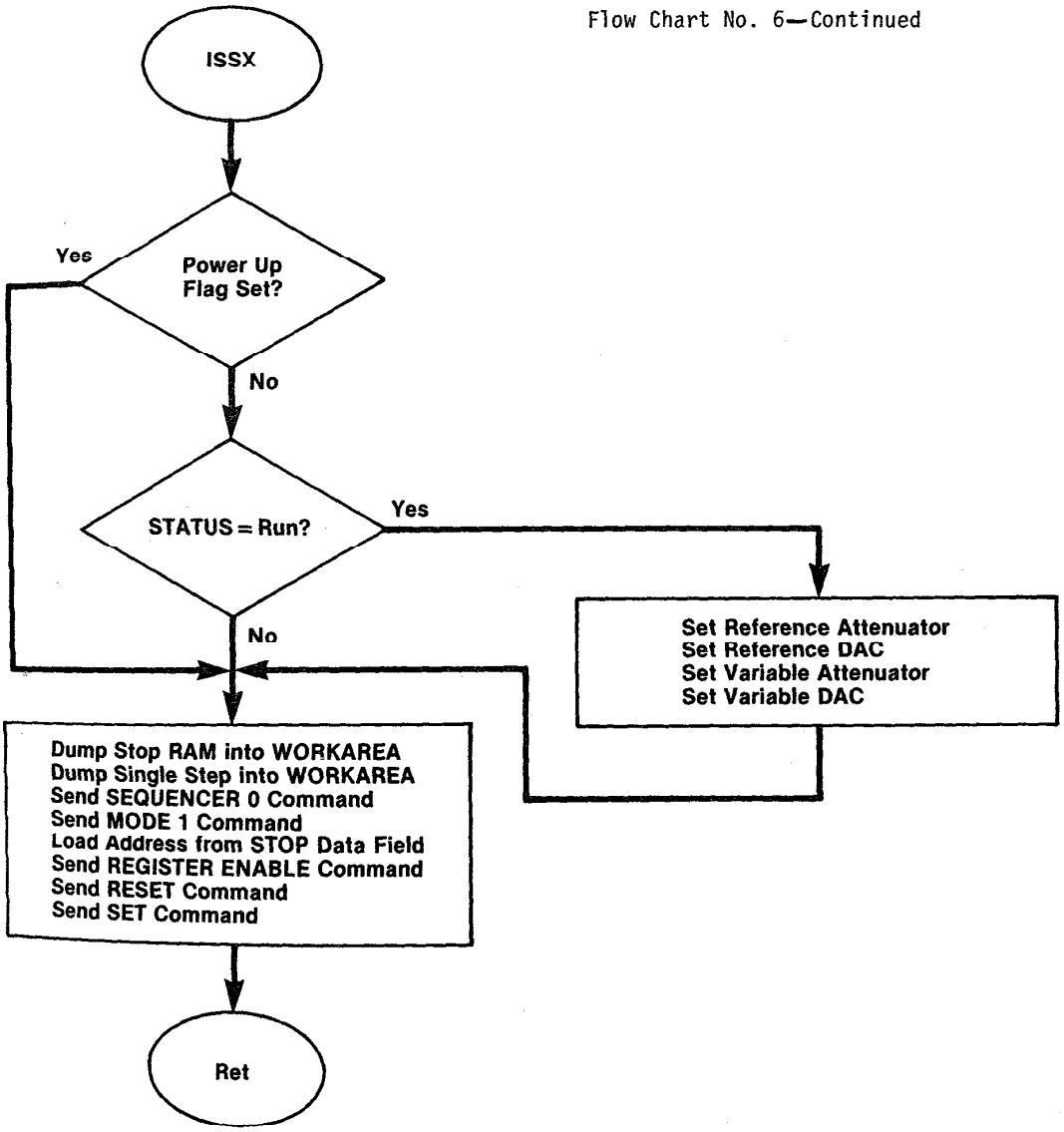
Flow Chart No. 6
Sequencer Run Routine



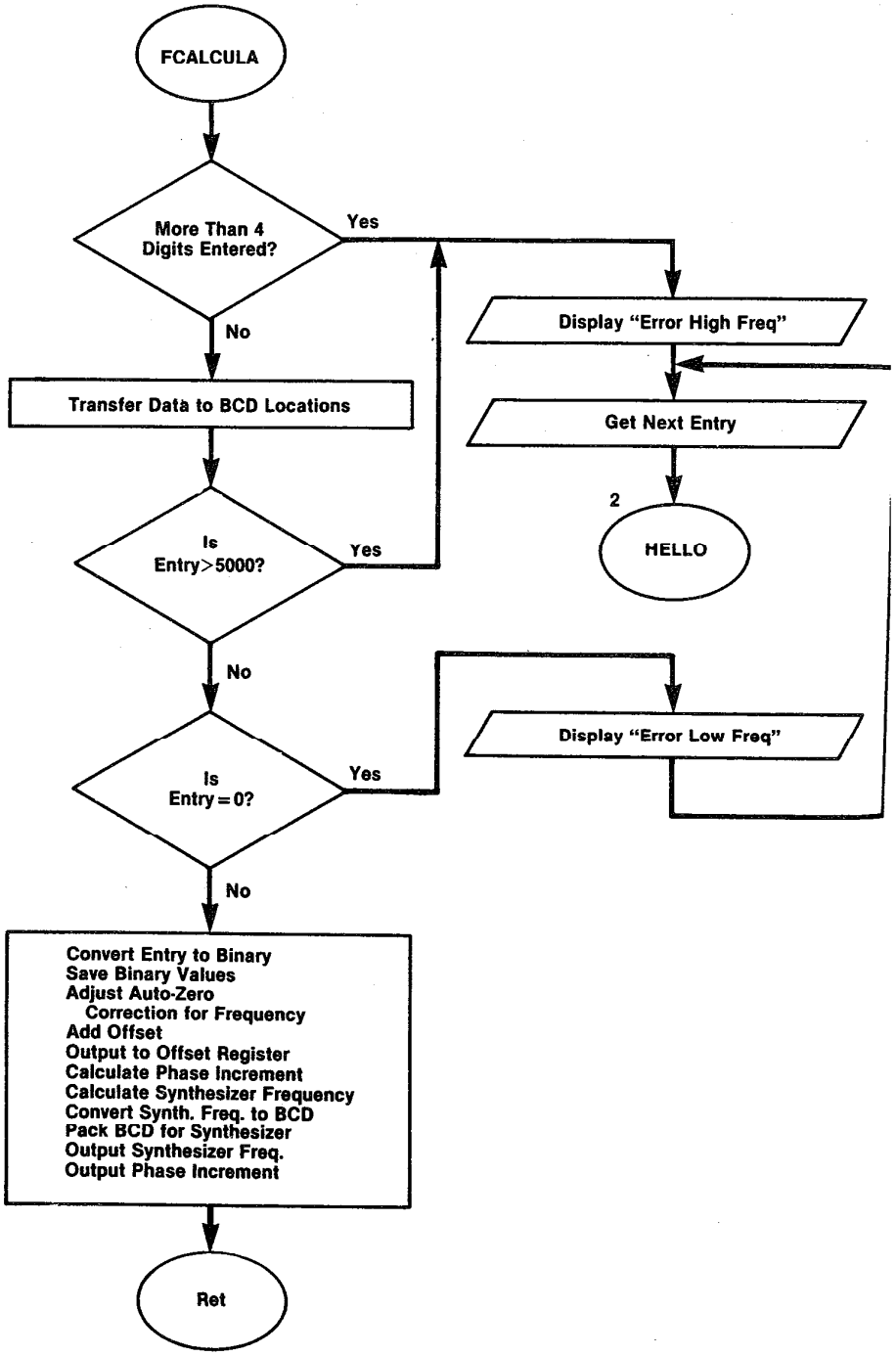
Flow Chart No. 6—Continue



Flow Chart No. 6—Continued



Flow Chart No. 7
Frequency Calculations



the synthesizer, the sampling frequency has to be reconverted to BCD and packed into the appropriate format.

The routine has the following outputs:

(a) The adjusted auto-zero correction (added to the offset, 20-bit binary)
(b) The synthesizer frequency (packed BCD)
(c) The phase increment (20-bit binary).

6.2.8 Routines for Setting Phase Angle and Offset

(Refer to flowchart number 8.) The main object of this set of routines is to convert the keyed-in decimal phase angles to binary numbers which are then sent to the ALU section of the high-speed processor. The decimal value is converted to a 20-bit scaled binary number, where 359.999 degrees corresponds to

"plus full-scale"= 0111 1111 1111 1111 1111

and 360.000 degrees corresponds to

"minus full-scale"= 1000 0000 0000 0000 0000.

The module 360 binary number system automatically takes care of any phase angle greater than 360 degrees. Conversion of such angles will set the sign bit to 1, but the angle-to-sine (hardware) conversion ignores the sign bit, so that 360.000 degrees appears as 0.000 degrees and 360.001 the same as 0.001, etc. Similarly, angles larger than 720 degrees will cause a carry bit which is also ignored.

For conversion, the decimal angle is stored as a six-digit BCD, positive integer. A look-up table with 40-bit entries corresponding to units, tens, hundreds, etc. is used to perform the actual conversion into binary. Table values are added repeatedly, with the number of additions corresponding to the numerical value of each digit. This method is fairly rapid and has the advantage that various scaled conversions can be handled by merely changing the look-up table.

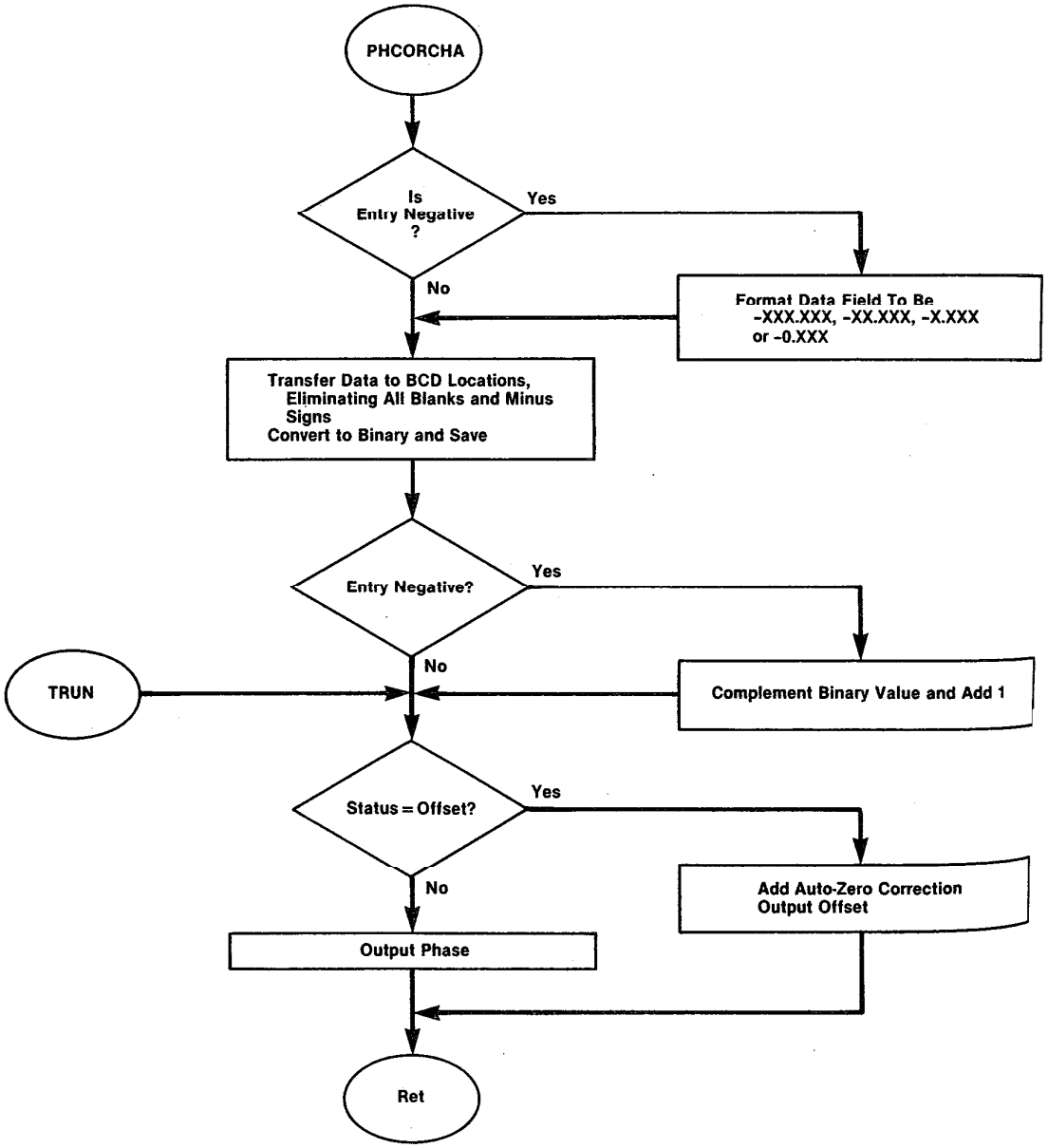
For negative numbers, the 'sign' flag is set, and the binary number is changed into a negative value in two's complement format. If the converted angle is an 'offset' rather than a 'phase' angle, the auto-zero correction and range offset are added to the result. The adjusted binary number is then transmitted via the 20-bit bus to the ALU section of the high-speed processor.

6.2.9 Routines for Setting Amplitude

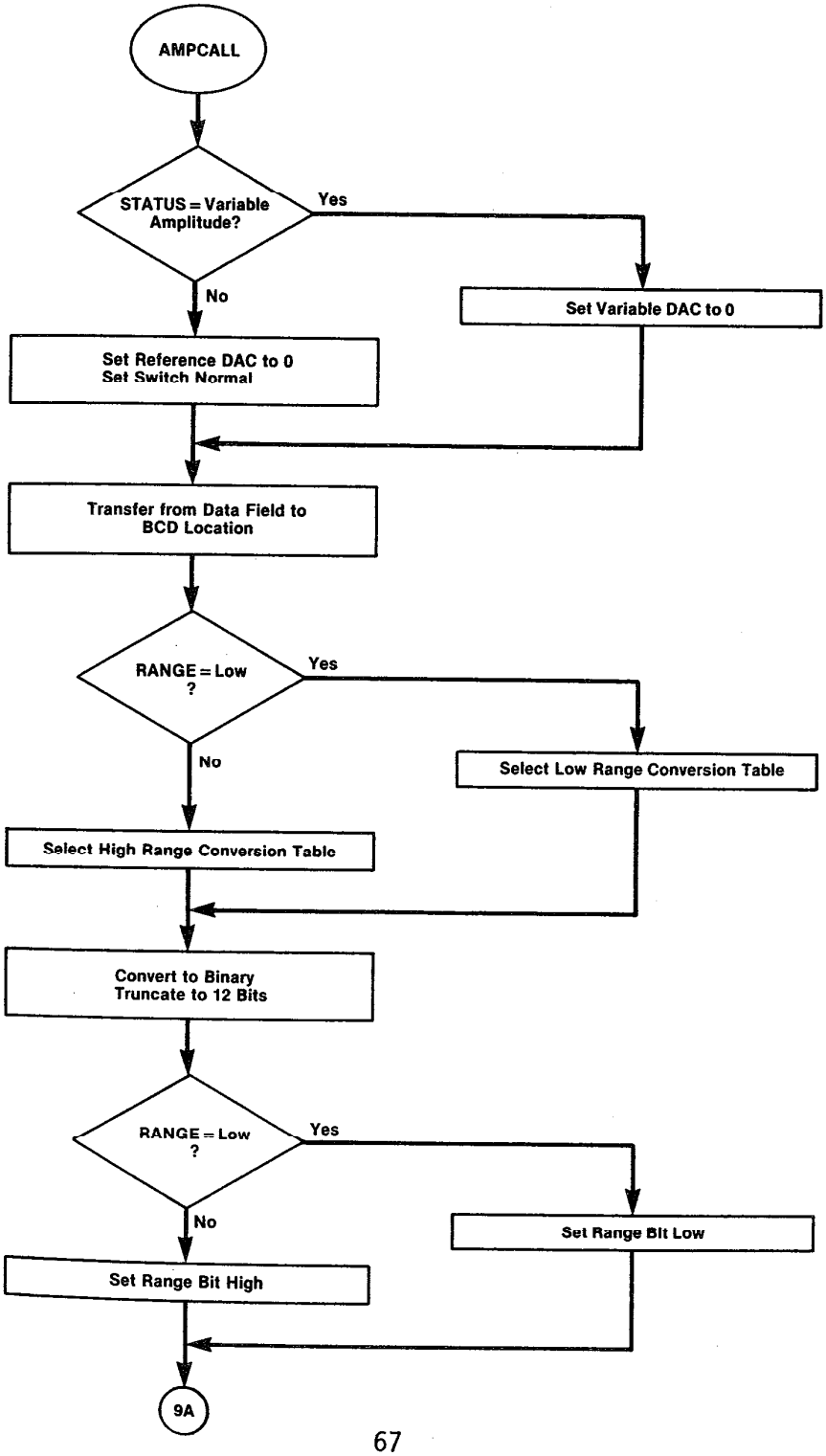
(Refer to flowchart number 9.) Since each output channel can be adjusted independently, a channel select entry is required. This modifies the STATUS byte (see flowchart number 2). The AMPCALL routine therefore checks the STATUS byte to determine whether the 'reference' or 'variable' phase channel is to be set. The appropriate voltage control circuit, a multiplying digital-to-analog converter (MDAC, see figure

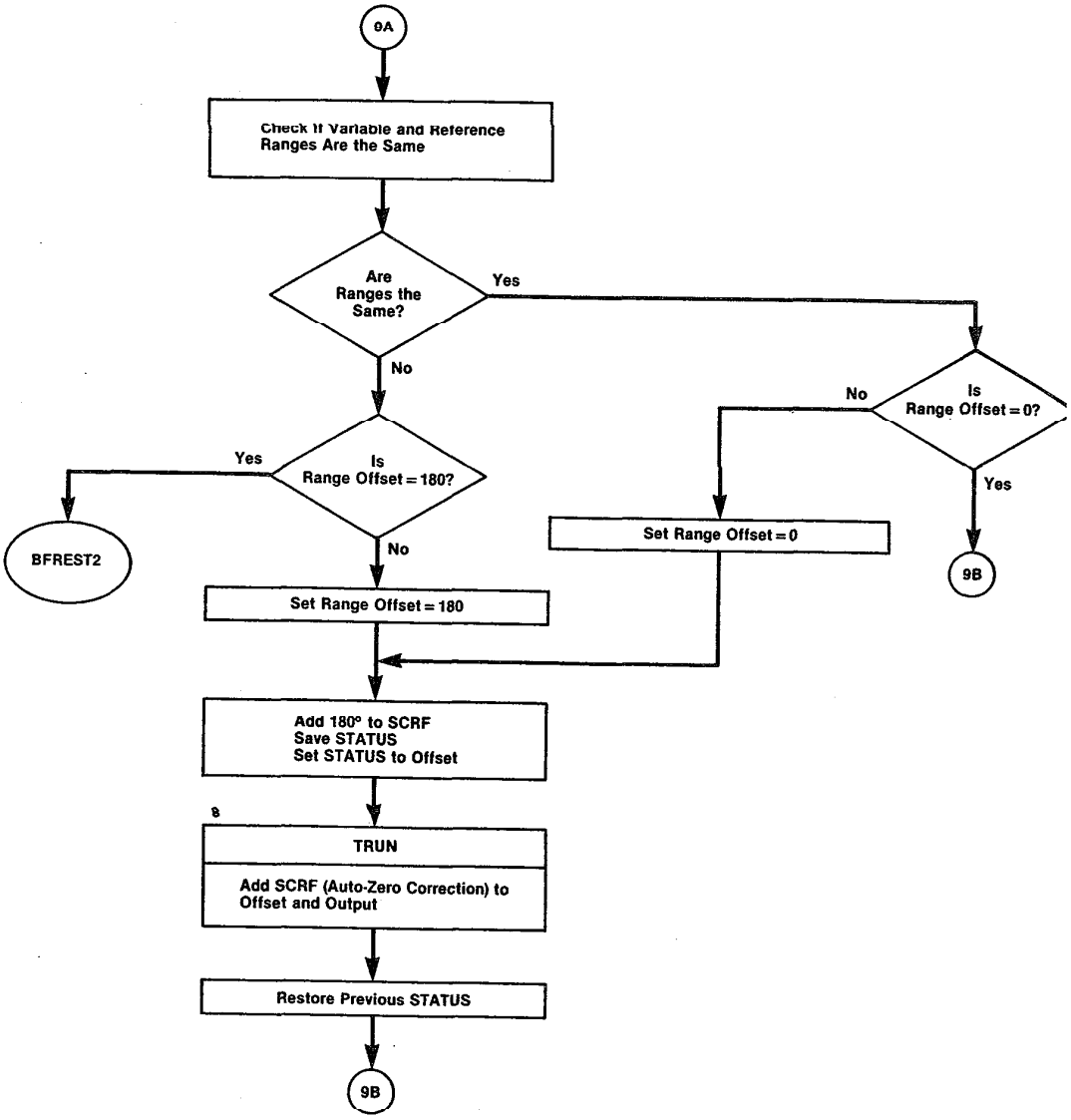
Flow Chart No. 8

Routines for Setting Phase Angle and Offset

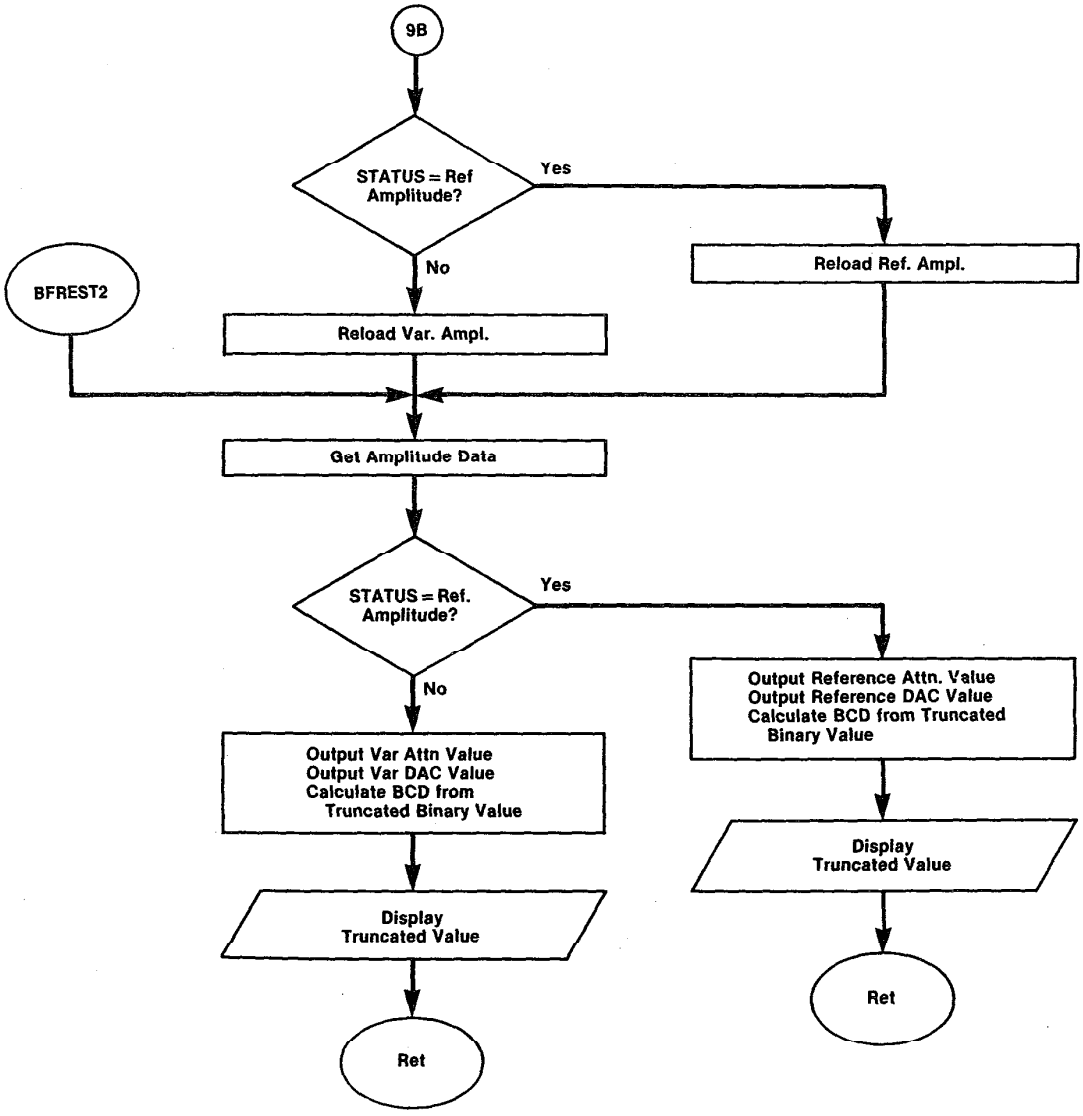


Flow Chart No. 9
Routines for Setting Amplitude




9A
Check if Variable and Reference Ranges Are the Same
Are Ranges the Same?
Yes
No
Is Range Offset = 180?
Yes
BFREST2
No
Set Range Offset = 180
Is Range Offset = 0?
No
Yes
Set Range Offset = 0
9B
Add 180° to SCRF
Save STATUS
Set STATUS to Offset
8
TRUN
Add SCRF (Auto-Zero Correction) to Offset and Output
Restore Previous STATUS
9B

Flow Chart No. 9—Continued



4.1), is first of all set to zero. This prevents possible damage to other circuit components during the switching procedure. The amplitude data entered from the keyboard are then transferred to the BCD buffer. Whether the high or low range of the amplifiers is required is determined by the number handling routines (see flowchart number 3, FAMPNUM); the range selected is now tested to determine the decimal-to-binary conversion table needed. The conversion is carried out by repeated addition of table values for each decimal digit. The result is truncated to 12 bits, which corresponds to the resolution of the voltage control MDACs, and a range bit is merged with the result.

Because the high-range output amplifiers introduce a 180 degree phase inversion, a 180 degree 'range offset' is added if only one of the channels has a high range output. If both ranges are the same, either high or low, the range offset is set to zero. The range offset, together with the auto-zero correction, is added to the phase offset (entered through the keyboard) and is transmitted to the offset register in the ALU section of the high-speed processor. In the process of transferring this offset data, the STATUS byte is changed and must now be reset. The appropriate amplitude data are recalled, so that they can be sent to the voltage control DACs via the 16-bit data bus. However, before the amplitude is set to a new value, the corresponding phase detector attenuator must first also be readjusted to protect the phase detector from overvoltage.

After setting the voltage control and attenuator, the output level to be displayed is calculated. The starting point for this calculation is the 12-bit truncated binary value used to set the amplitude. This number is reconverted to BCD (and then to ASCII) and put into the display buffer.

6.2.10 Bus Handshake

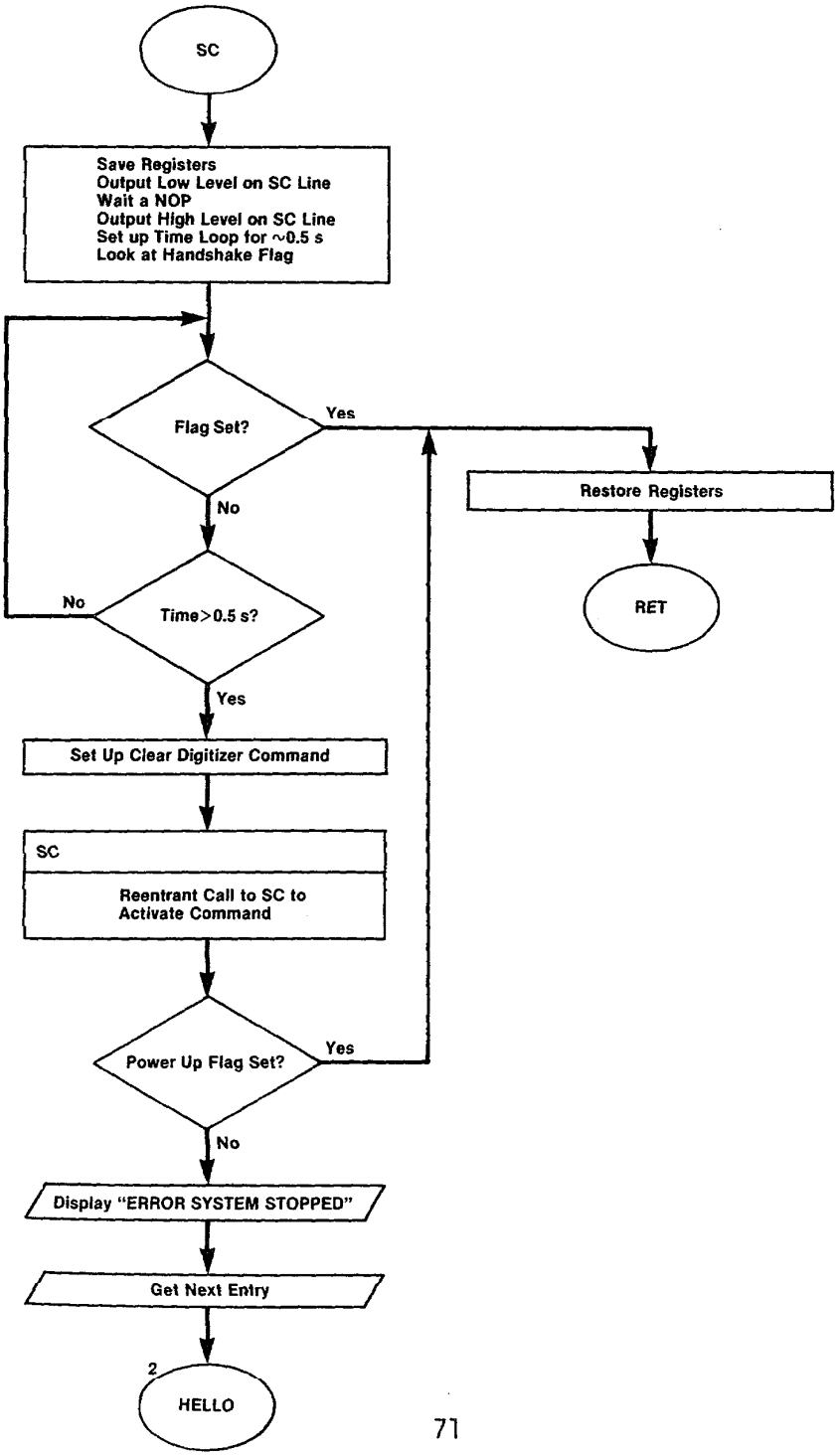
(Refer to flowchart number 10.) The 8085 microcomputer and the high-speed processor run on independent clocks. Data between the two systems must therefore be transferred asynchronously. A 'set control' pulse is sent from the 8085 and an acknowledge 'flag' is returned from the high-speed processor when sending phase, offset, and angular increment data. The same set of signals is used also with the digitizer which converts the analog output from the phase detector. The 'set control' starts the analog-to-digital conversion, and the 'flag' signals its completion.

The 'set control' pulse also serves to latch data into the interface unit which then returns a 'flag' signal after a short delay.

The SC routine sends out a negative going pulse and waits for the return flag. The half-second waiting time was chosen to accommodate two types of digitizers. The routine returns normally if the flag is set within the waiting period. If the flag signal is not returned, it is most likely that the digitizer is not properly initialized. A signal is

Flow Chart No. 10

Bus Handshake
(Set Control/Flag)



then set up to clear the digitizer, and a reentrant call to SC sends a 'set control' pulse to the interface board to activate the 'clear' command. In this mode the flag is returned directly from the interface unit, unless another error condition exists. In that case an error message is displayed before the routine returns for more input.

6.2.11 Initializing of the Auto-Zero Function

(Refer to flowchart number 11.) Before the actual auto-zero determination can take place, several preliminary operations are necessary:

(a) Working 'registers' (in memory) are initialized. This includes the 'normal' and 'reverse' calibration factors (NORCAL, REVCAL), as well as the 'software correction register' (SCR) which holds the offset angle that is fed back to the high-speed processor.

(b) The auto-zero process is carried out at a frequency of 4096 Hz; therefore, the frequency is set to this new value and the original frequency information is saved.

(c) The 'offset' is set at 0.000 and the previous value entered from the keyboard is saved.

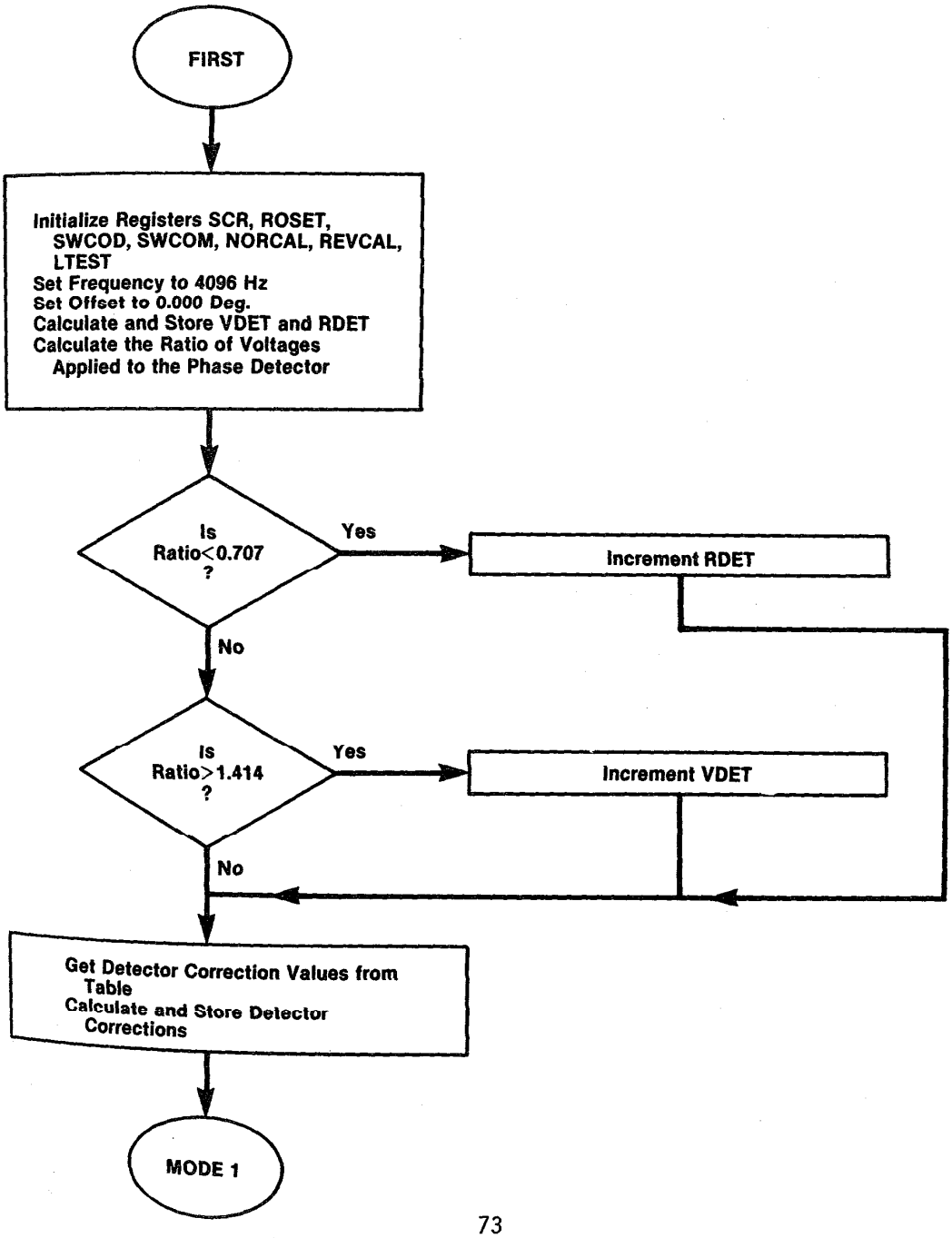
(d) The output voltage setting for each channel as well as the phase detector attenuator settings are determined and stored.

Proper operating conditions for the phase detector require that the input voltages after attenuation are approximately equal, within a ratio of 0.707 to 1.414. If the ratio calculated from the voltage and attenuator settings falls outside these limits, the appropriate attenuator is adjusted by one step. Since the attenuators introduce a phase error, a correction is applied which is calculated from a table stored in the read-only memory (PROM). (The values in this table are obtained by calibration of the particular phase detector included in the system. The identification of the set of PROMs displayed during initialization of the system contains the serial number of the phase detector.)

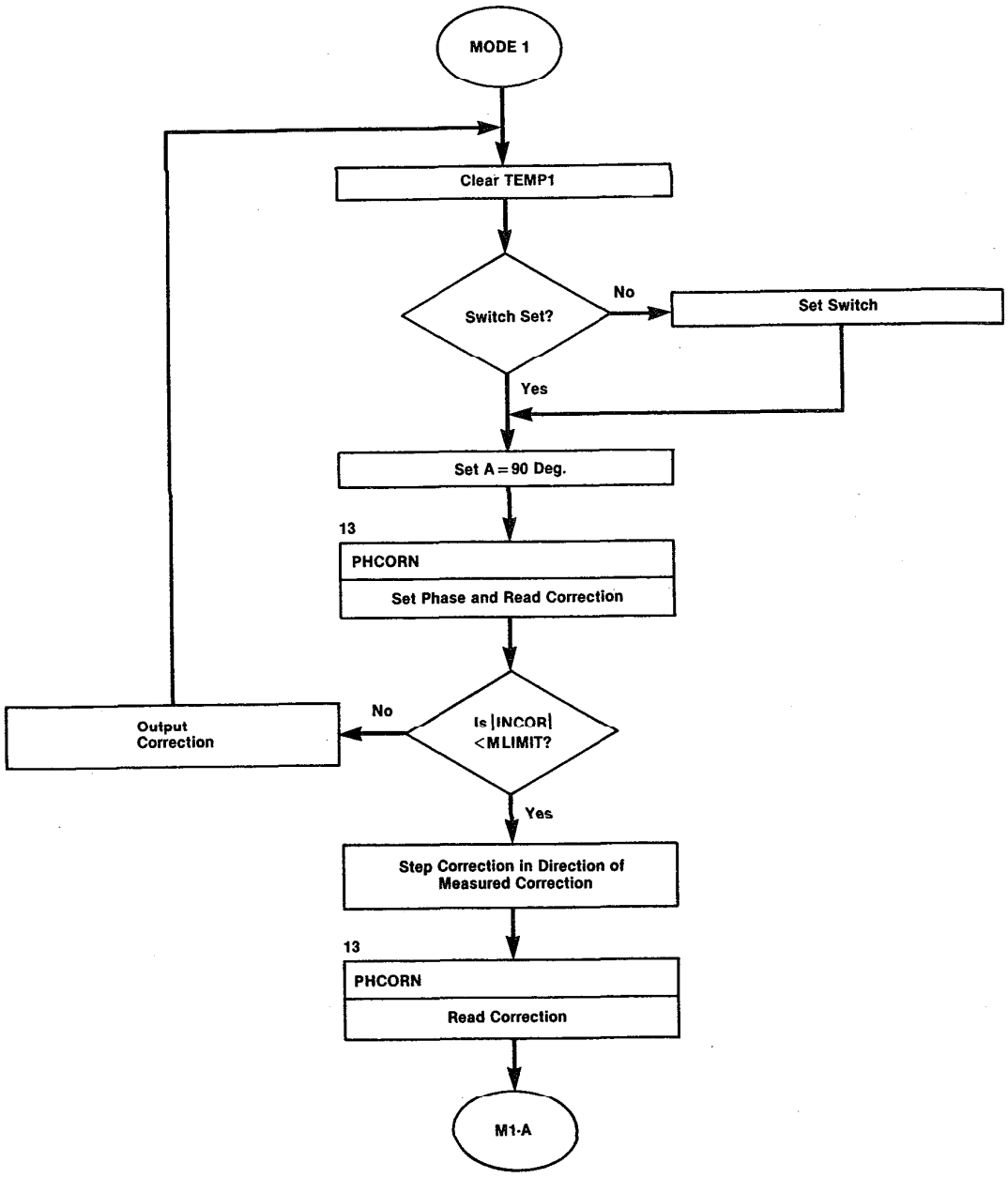
After these initial steps, the routine proceeds to MODE 1, where the transfer characteristic of the phase detector is calibrated. For the final adjustment, the phase detector output is effectively close to a null, and therefore insensitive to calibration constants; nevertheless it is important to determine the calibration constant to optimize response. Both excessive overshoot and correction steps that are too small delay reaching the desired null condition, or in some cases may even prevent ever reaching it.

The channel interchange switch (on the phase detector circuit board, see section 7.2.7) is set to 'reverse,' the phase angle to 90 degrees, and subroutine PHCORN is called to obtain the value of the phase detector output. If that value is above an established limit, a

Flow Chart No. 11
Initializing of the Auto-Zero Function



Flow Chart No. 11—Continued



correction is applied to the 'offset' register in the ALU which has the effect of bringing the input to the phase detector closer to quadrature. The procedure is then repeated. If the measurement is within the limit, the phase angle is further offset by a predetermined step, and another measurement is made by calling PHCORN, in order to determine the slope of the detector transfer characteristic.

A second determination is made with the switch in the 'normal' position. The two calibration factors are usually fairly close in magnitude, but if their ratio is too large, they are discarded and redetermined once more. The larger of the two is then selected and used in the remainder of the auto-zero program (see section 6.2.12, flowchart number 12).

6.2.12 Auto-Zero Four-Way Measurement of Correction

(Refer to flowchart number 12.) The principle of the auto-zero correction is described in section 4.6 where the reason for the four-way measurement is explained. Four measurements of the phase detector output are made:

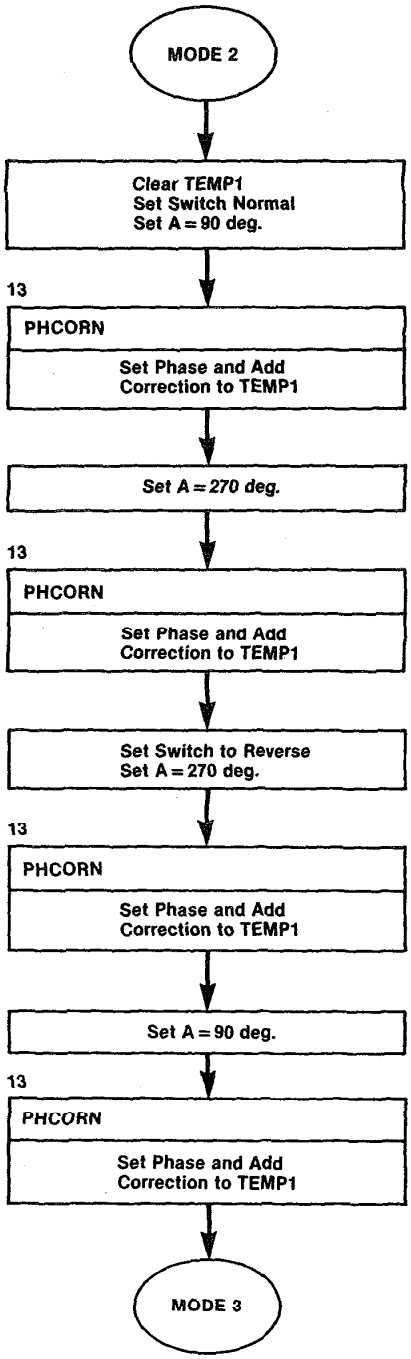
Condition	Phase Angle	Channel Switch
1	+90 Degrees	Normal
2	-90 Degrees	Normal
3	-90 Degrees	Reverse
4	+90 Degrees	Reverse

These four measurements are averaged by summing the two "+90" measurements and subtracting the two "-90" (270 degrees) measurements and dividing the result by four. After the conditions are set up, the actual measurement is carried out by calling subroutine PHCORN. The average, which has been modified by the calibration constant, is then added to the 'software correction register' (SCR) and output to the high-speed processor after adding the range offset. This correction procedure is repeated until the incremental difference between successive correction values is less than the established final tolerance (approximately 0.5 millidegrees).

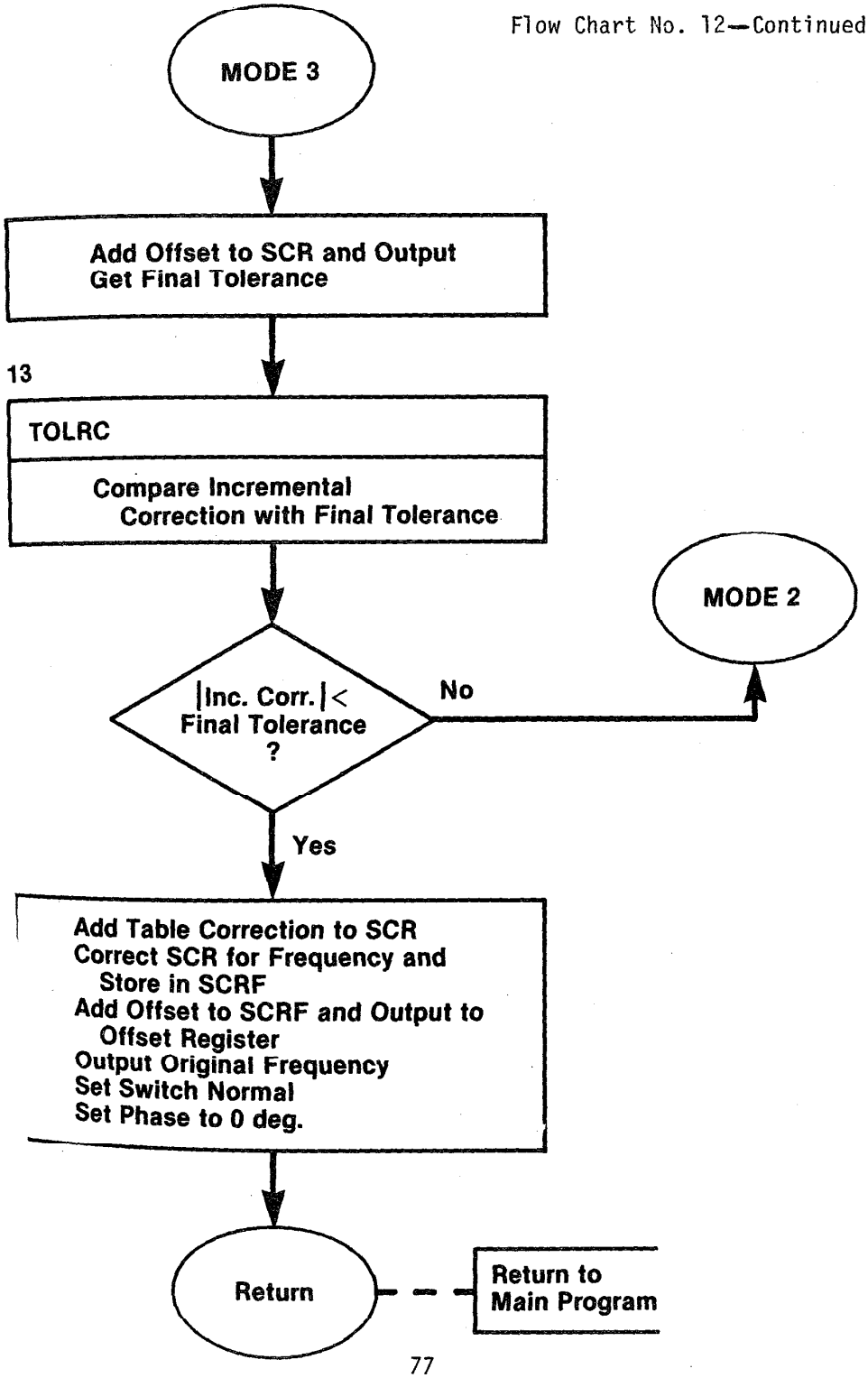
As a final step, the values from the correction table are added to take care of the residual phase shift in the phase detector attenuators. The overall correction is then adjusted for the original frequency selected, the output frequency is reset to the original value, the channel switch is set to 'normal,' and the phase angle is set to 0.000.

Flow Chart No. 12

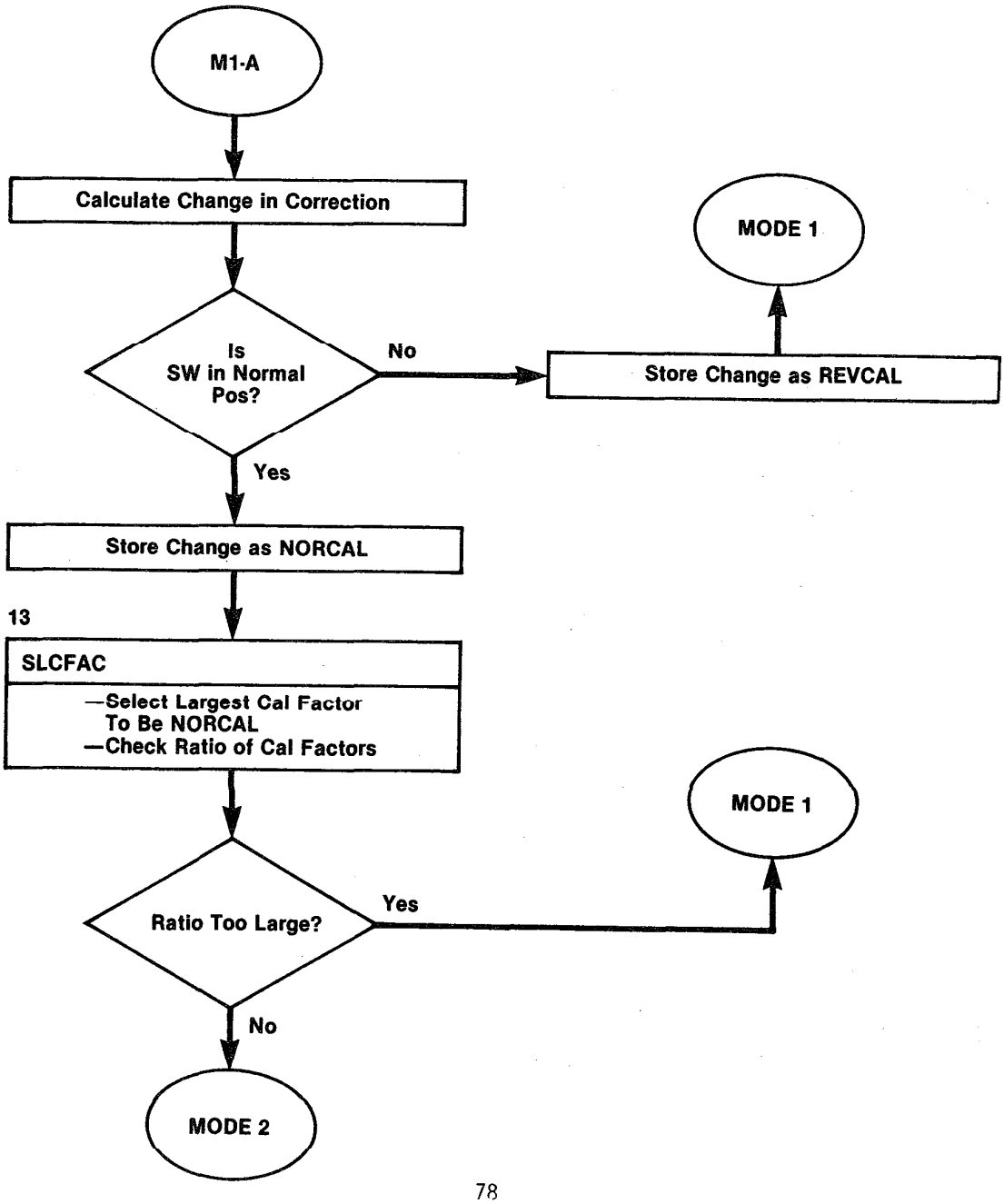
Auto Zero Four-Way Measurement of Incremental Correction



Flow Chart No. 12—Continued

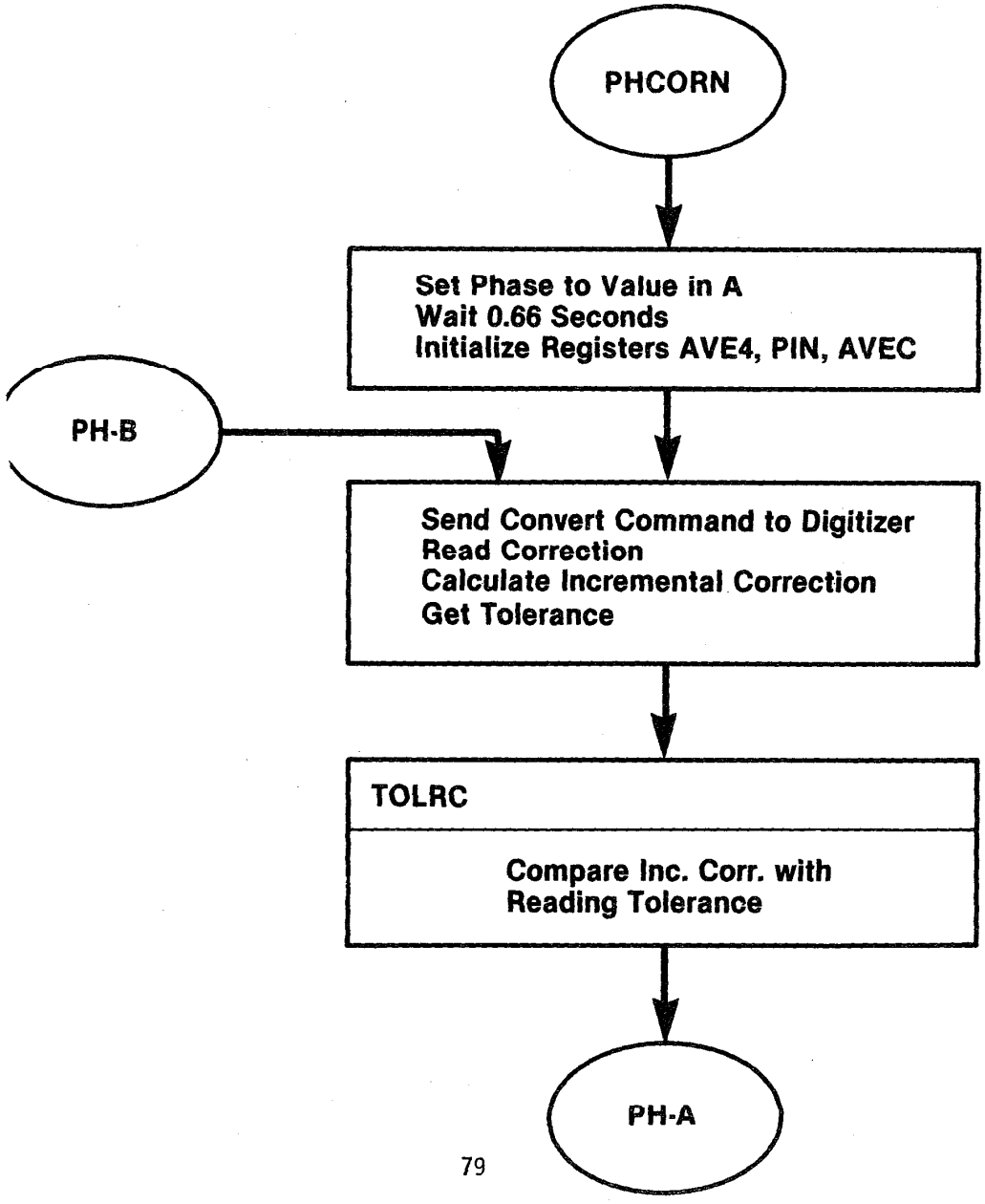


Flow Chart No. 12—Continued

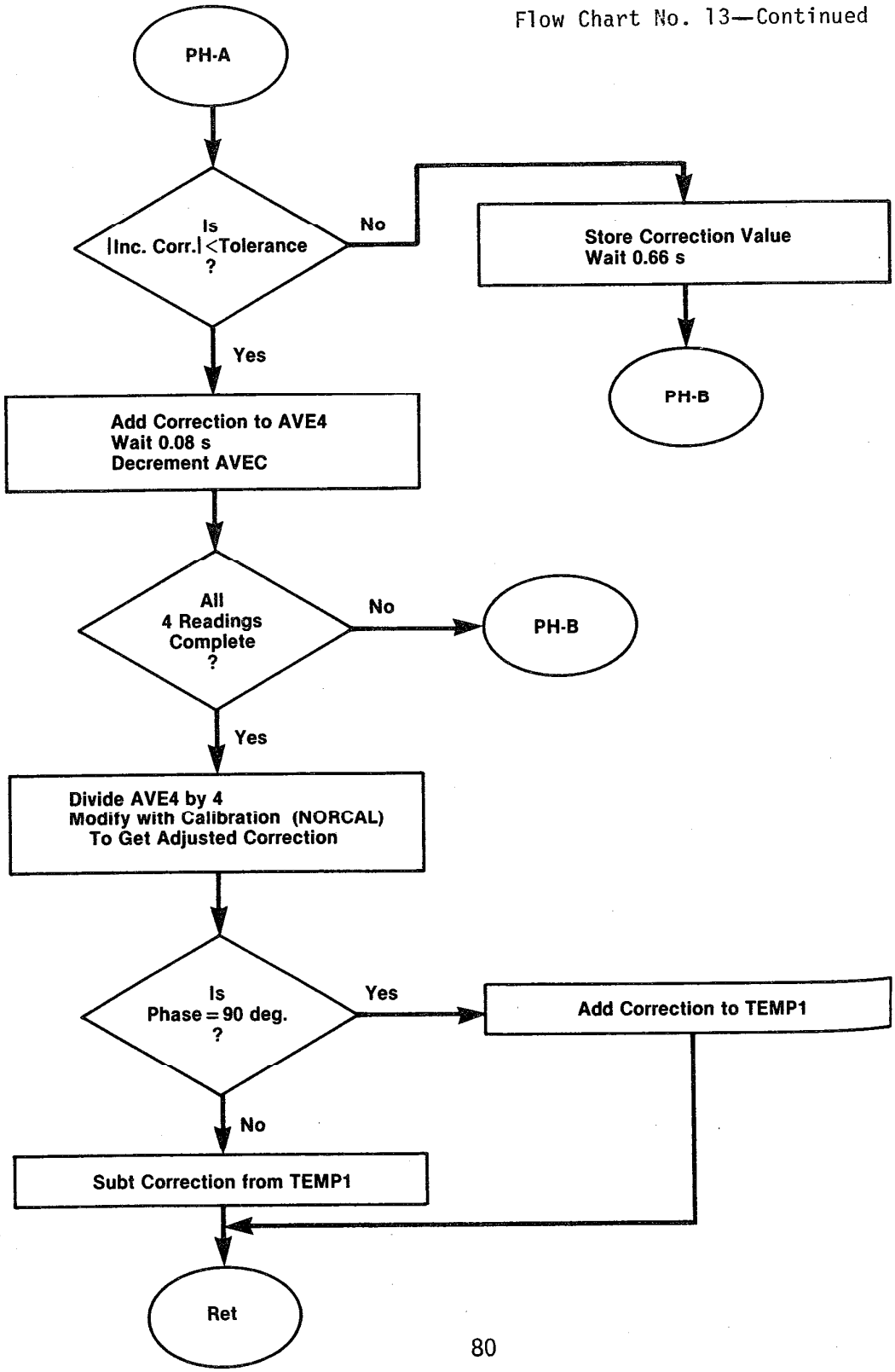


Flow Chart No. 13

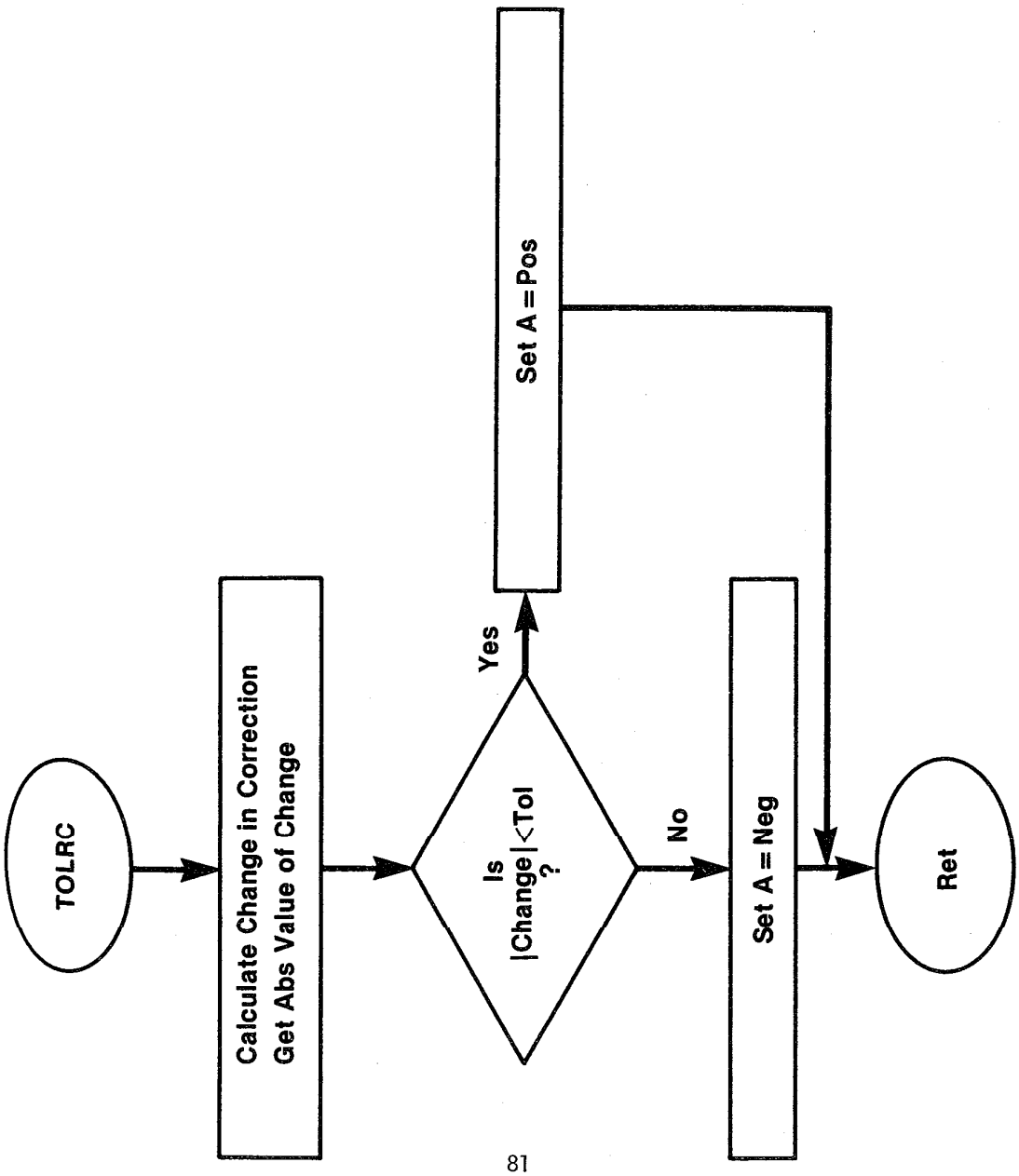
Subroutines for Auto-Zero Determination



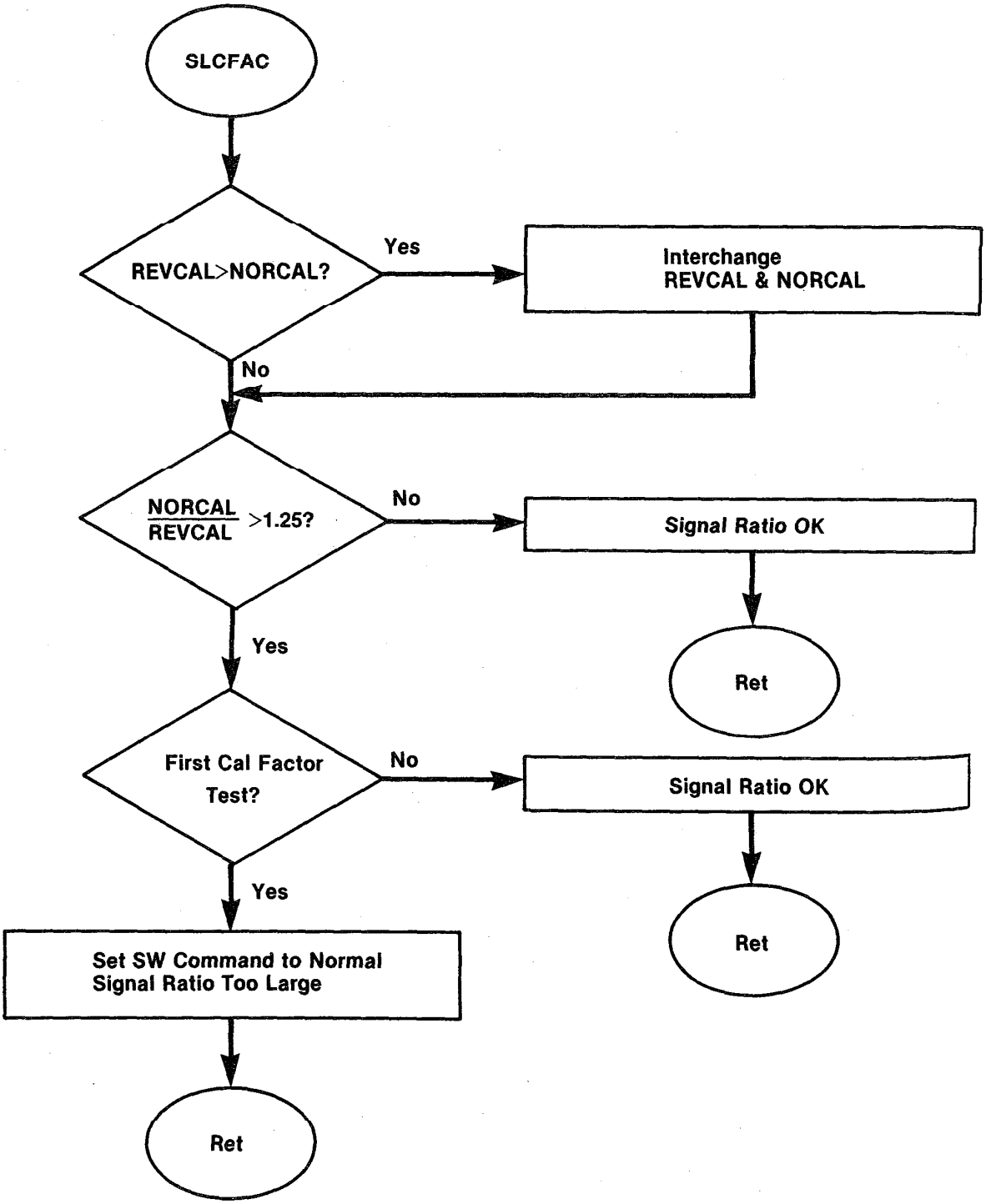
Flow Chart No. 13—Continued



Flow Chart No. 13—Continued



Flow Chart No. 13—Continued



6.2.13 Subroutines for Auto-Zero Determination

(Refer to flowchart number 13.)

(a) Subroutine PHCORN. This subroutine makes a measurement of the phase detector output and determines whether the reading obtained is valid. The first operation is to set the phase angle and the value of that angle is passed to the subroutine through the accumulator. A 0.66-second waiting period follows to let the phase detector settle to the new value. Then a series of four readings is taken under the same conditions and averaged. The incremental difference between successive readings is checked to make sure that the phase detector output has settled. If the new reading differs by more than the 'reading' tolerance, it is repeated. After all four readings have been taken, the average is divided by the calibration factor and either added or subtracted from TEMP1, depending on whether the phase is set to +90 or -90 (270) degrees. TEMP1 acts as temporary storage for the correction until measurements have been made under all four conditions (see section 2.7.12 above).

(b) Subroutine TOLRC. This routine compares the absolute value of the difference between two measured corrections to a tolerance value. If the tolerance is larger, the accumulator is made positive, otherwise it will be negative.

(c) Subroutine SLFAC. This subroutine determines which of the two calibration factors (NORCAL, REVCAL) is the larger. If necessary, it exchanges them to make NORCAL always the larger. The routine then determines if NORCAL exceeds REVCAL by more than 25 percent. If it does, the calibration constants are redetermined once more.

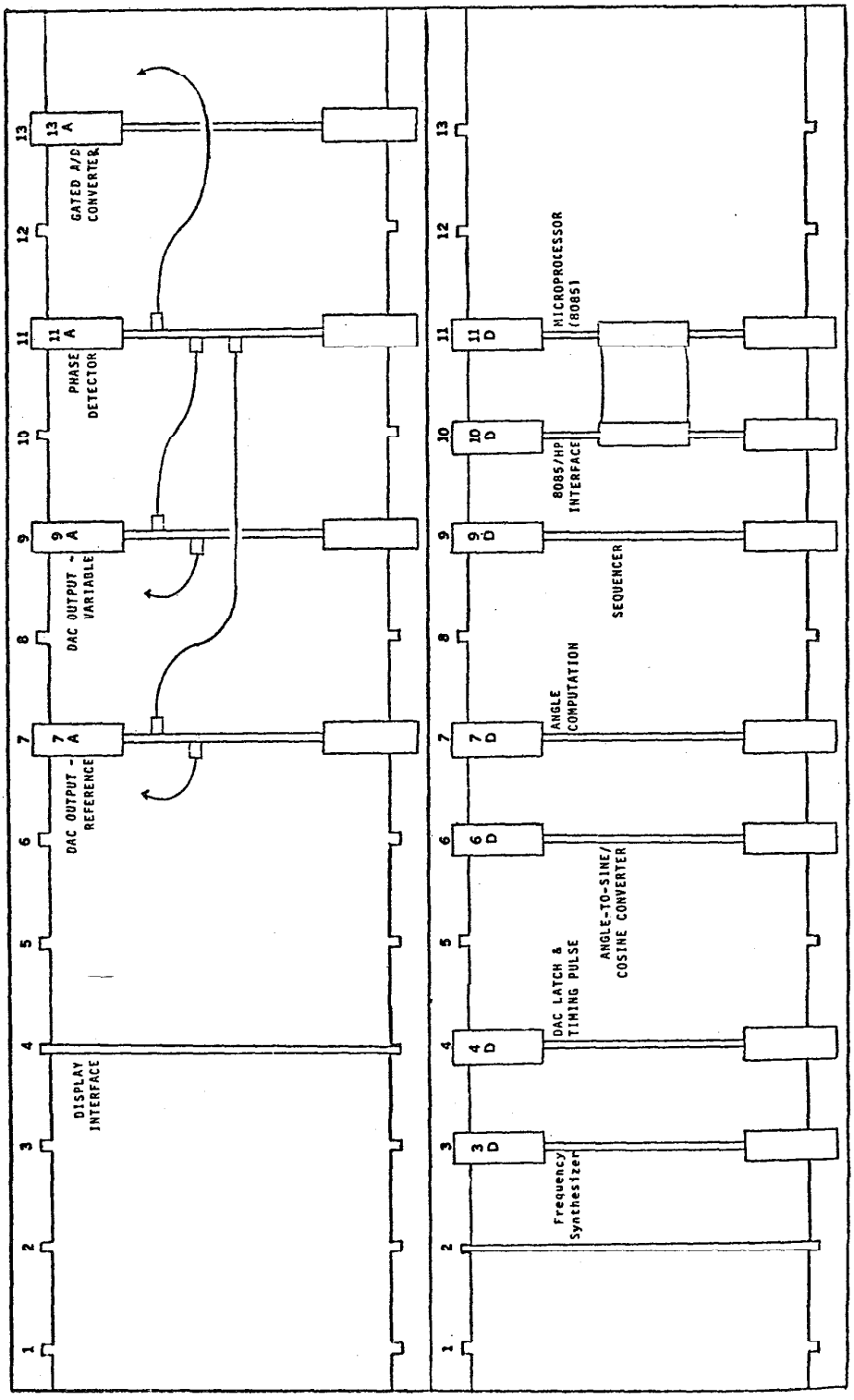
7. DESCRIPTION OF HARDWARE

7.1 Physical Layout

7.1.1 Circuit Assembly

The Phase Angle Standard circuitry is assembled on eleven 4.5" x 9.25" cards which are mounted in two 19" card cases stacked one on top of the other (see figure 7.1). The bottom cage contains the digital circuitry (D) required to produce two 16-bit sine functions which are applied to the analog circuitry (A) in the top card cage.

A 32-character, alpha-numeric display and two 12-button keyboards are mounted on the front panel which is a hinged door of the instrument enclosure containing the two card cages. Electrical connections from the display to the microcomputer are made through the 'Display Interface' board (figure 7.1). The wiring diagrams for the keyboards are shown in figures 7.35 and 7.36 (see section 7.3.3). The card cage backplane



Card Cage (Front View)

Figure 7.1

wiring lists are shown on figures 7.3 to 7.14. Each backplane wiring diagram shows one backplane connector (70 pins) and the connections from other circuit boards to each pin used. For each pin, the name of the signal or of the bus, or the value of the supply voltage is indicated. Also shown is the name of the other circuit board and corresponding pin number, except when the connection is part of a bus in which case only the bus designation is given.

The circuit boards are accessible for servicing and removal by opening the hinged front panel. Numbering of the circuit diagrams corresponds to the slot positions in the card cage shown in figure 7.1.

7.1.2 Power Supplies

Various power supply voltages are required to operate the digital and analog circuitry (see figure 7.2). These supplies are mounted on the instrument's back panel which plugs into the rear of the card cage unit through a 24-pin, 5-ampere connector. (See figure 7.2 for the wiring code.) The ac line enters the power supply through the back panel, and is connected through a solid-state relay controlled from a front panel switch.

7.1.3 Enclosure

The front and back panels (10 1/2 x 19 in) are mounted in an enclosure 21 inches wide, 17 1/2 inches high, and 21 1/2 inches from front to back (exclusive of handles).

Power Supply Connector Wiring Code

Pin Numbers	
1, 2, 11, 12, 13, 14, 23, 24	Chassis and Power Cord Ground
3, 4, 15, 16	+5 volts, 10 amperes
5, 17	+15 volts, 1 ampere
6, 18	-15 volts, 1 ampere
7	-150 volts, 100 mA
8	-15 volts, 50 mA
9	+150 volts, 25 mA
10	-12 volts, 15 mA
19	+150 volts, 100 mA
20	+15 volts, 50 mA (tied to front panel power switch)
21	+ Input to Power Relay (from front panel power switch)
22	+5 volts or Ground (from rear panel amplitude select switch)

Figure 7.2

Power Supply Connector, Position A 3

Backplane Wiring List

Connects To: Pin No.	Function	Backplane Connector	Function	Connects To: Board Name	Pin No.
Power Supply Connector		36 o-o 1		Power Supply Connector	
		37 o-o 2			
		38 o o 3			
		39 o o 4			
(5),(17)	+15 Volts	40 o o 5			
		41 o o 6			
(6),(18)	-15 Volts	42 o o 7			
		43 o o 8			
		44 o o 9			
		45 o o 10			
		46 o o 11			
		47 o o 12			
(19)	+150 Volts	48 o o 13			
		49 o o 14			
(7)	-150 Volts	50 o o 15			
		51 o o 16			
		52 o o 17			
(20)	+15 Volts	53 o o 18			
		54 o o 19			
(8)	-15 Volts	55 o o 20			
		56 o o 21			
		57 o o 22			
(21)	Power Relay	58 o o 23			
		59 o o 24			
(22)	'7V'/'Normal'	60 o o 25			
	Switch	61 o o 26			
		62 o o 27			
(9)	+150 Volts	63 o o 28			
		64 o o 29	-12 Volts		(10)
		65 o o 30			
		66 o o 31			
		67 o o 32			
		68 o o 33			
		69 o o 34			
		70 o-o 35			

Figure 7.3

Display and Keyboard Interface, Position A 4

Backplane Wiring List

Connects To: Pin No.	Board Name	Function	Backplane Connector	Function	Connector Pin Numbers "3M"	"IEE"	Intfc D10
			36 o-o 1				
			37 o-o 2	Ground	1	1	
			38 o o 3	Ground	18	2	
			39 o o 4	Ground	2	3	
			40 o o 5	V_{BB},150V Com	19	4	
			41 o o 6	V_{CC}, +5 Volts	3	5	
			42 o o 7	V_{CC}, +5 Volts	20	6	
			43 o o 8	Ready	4	7	
			44 o o 9	Spare	5	8	
			45 o o 10	Strobe	21	9	(30)
			46 o o 11	Clock (Ground)	6	10	
			47 o o 12	Backspace,+5V	22	11	
			48 o o 13	Character 2^1	7	12	(9)
			49 o o 14	Character 2^2	23	13	(8)
			50 o o 15	Character 2^3	8	14	(7)
			51 o o 16	Character 2^5	24	15	(5)
		Keyboard	52 o o 17	Character 2^0	9	16	(10)
		Edge Conn.	53 o o 18	Character 2^4	25	17	(6)
(29)*			54 o o 19	Load	10	18	(29)
(30)*		D	55 o o 20	Character 2^7	26	19	(3)
(31)*		H	56 o o 21	Character 2^6	11	20	(4)
(32)*	Function	A	57 o o 22	Char.(MSB) b^6	27	21	(13)
(33)*		B	58 o o 23	DMA, +5 Volts	12	22	
(34)*	Keyboard	C	59 o o 24	Blank, +5 V	28	23	
(35)*		J	60 o o 25	Clear, +5 V	13	24	
		L	61 o o 26	Char. b^1	29	25	(18)
	Ground	P	62 o o 27	Char. b^2	14	26	(17)
(28)*		P	63 o o 28	Char. b^3	30	27	(16)
(27)*		H	64 o o 29	Char. b^4	15	28	(15)
(26)*	Number	C	65 o o 30	Underbar	31	29	(11)
(25)*		B	66 o o 31	Char. b^5	16	30	(14)
(24)*	Keyboard	L	67 o o 32	V_{GG}, -12 Volts	32	31	
(23)*		D	68 o o 33	V_{GG}, -12 Volts	17	32	
(22)*		A	69 o o 34	Key(Pin removed)	33	33	
(20)*	Functn K'bd	S(F)	70 o-o 35	V_{BB}, +150 V	18	34	

* Pin numbers refer to Microcomputer Board D-11

Figure 7.4

Digital-to-Analog Converter Circuit Board, Positions A7 & A9

Backplane Wiring List

Connects To: Pin No.	Board Name	Function	Backplane Connector	Function	Board Name	Connects To: Pin No.
		Ground	36 o-o 1	Ground		
Ref Var A7 A9		+5 Volts	37 o-o 2	+5 Volts		
		+15 Volts	38 o-o 3	+15 Volts		
		-15 Volts	39 o-o 4	-15 Volts		
(5)(40)		MSB 15	40 o o 5			
(6)(41)		Bit 14	41 o o 6			
(7)(42)		13	42 o o 7			
(8)(43)		12	43 o o 8			
(9)(44)		11	44 o o 9			
(10)(45)	Digital	10	45 o o 10			
(11)(46)	Data from	9	46 o o 11			
(12)(47)	Regis. D4	8	47 o o 12			
(13)(48)		7	48 o o 13	MSB 15		
(14)(49)		6	49 o o 14	Bit 14		
(15)(50)		5	50 o o 15	13		
(16)(51)		4	51 o o 16	12	Ampl.	
(17)(52)		3	52 o o 17	11	Contr.	
(18)(53)		2	53 o o 18	10	Bits	
(19)(54)		1	54 o o 19	9		Low-Speed
(20)(55)		LSB 0	55 o o 20	8		16-Bit
			56 o o 21	7		Bus
			57 o o 22	6		
			58 o o 23	5		
			59 o o 24	LSB 4		
		-150 Volts	60 o o 25		Bit 3	
			61 o o 26		2	
		+150 Volts	62 o o 27		1	
			63 o o 28		0	
			64 o o 29			Ref Var
			65 o o 30			
			66 o o 31	Latch Strb Intrfc D10		(68)(67)
		-15 Volts	67 o-o 32	-15 Volts (Oven)		
		+15 Volts	68 o-o 33	+15 Volts (Oven)		
	Digital Ground		69 o-o 34	Digital Ground		
	Digital Ground		70 o-o 35	Digital Ground		

Latch Strb=Latch Strobe; Intrfc=Interface; Regis.=Register.

Figure 7.5

Phase Detector Circuit Board, Position A-11

Backplane Wiring List

Connects To: Pin No.	Board Name	Function	Backplane Connector	Function	Connects To: Board Name	Pin No.
		Ground	36 o-o 1	Ground		
		+5 Volts	37 o-o 2	+5 Volts		
		+15 Volts	38 o-o 3	+15 Volts		
		-15 Volts	39 o-o 4	-15 Volts		
			40 o o 5			
			41 o o 6	'Ref' Latch Intrfc	D10	(66)
			42 o o 7	'Var' Strobe Intrfc	D10	(65)
			43 o o 8			
			44 o o 9			
			45 o o 10			
			46 o o 11		Digtz A13	(6)
			47 o o 12		VarDAC A9	(12)
			48 o o 13	MSB 15		
			49 o o 14	Bit 14		
			50 o o 15	13		
			51 o o 16	12		
			52 o o 17	11		
			53 o o 18	10		
			54 o o 19	9	Low-Speed	
			55 o o 20	8	16-Bit	
			56 o o 21	7	Bus	
			57 o o 22	Not 6		
			58 o o 23	Used 5		
			59 o o 24	4		
			60 o o 25	3		
			61 o o 26	2		
			62 o o 27	1		
			63 o o 28	0		
			64 o o 29			
			65 o o 30			
			66 o o 31		Intrfc D10	(21)
			67 o o 32		Intrfc D10	(22)
			68 o o 33			
			69 o o 34			
		Digital Ground	70 o-o 35	Digital Ground		

Digtz=Digitizer; Intrfc=Interface; VarDAC= Variable Channel DAC

Figure 7.6

Digitizer (Analog-to-Digital Converter) Circuit Board, A13

Backplane Wiring List

Connects To: Pin No.	Board Name	Function	Backplane Connector			Function	Connects To: Board Name	Pin No.
		Ground	36	o-o	1	Ground		
		+5 Volts	37	o-o	2	+5 Volts		
		+15 Volts	38	o-o	3	+15 Volts		
		-15 Volts	39	o-o	4	-15 Volts		
		MSB 15	40	o o	5			
		Bit 14	41	o o	6	Ripple Sync. Phas	A11	(11)
		13	42	o o	7			
		12	43	o o	8			
		11	44	o o	9			
		10	45	o o	10			
	Low-Speed	9	46	o o	11			
	16-Bit	8	47	o o	12			
	Bus	7	48	o o	13			
		6	49	o o	14	Conv. Compl. Intf	D10	(31)
		5	50	o o	15			
		4	51	o o	16	Conv. Command Int	D10	(69)
		3	52	o o	17			
		2	53	o o	18	$\overline{OE}$ Intf	D10	(34)
		1	54	o o	19			
		LSB 0	55	o o	20			
			56	o o	21			
			57	o o	22			
			58	o o	23			
			59	o o	24			
(23)	Intfc D10		60	o o	25			
			61	o o	26			
			62	o o	27			
			63	o o	28			
			64	o o	29			
(34)	Sequ. D9	10 MHz Clk	65	o o	30			
			66	o o	31			
			67	o o	32			
			68	o o	33			
			69	o o	34			
		Ground	70	o-o	35	Ground		

Intfc=Interface; Conv.= Convert; Compl.=Complete; Sequ.=Sequencer
Phas =Phase Detector; Clk=Clock.

Figure 7.7

Frequency Synthesizer Circuit Board, Position D 3

Backplane Wiring List

Connects To: Pin No.	Board Name	Function	Backplane Connector	Function	Board Name	Pin No.
		Ground	36 o-o 1	Ground		
		+5 Volts	37 o-o 2	+5 Volts		
			38 o o 3			
(64)	Intfc D10	Latch Clck	39 o o 4			
		MSB 15	40 o o 5	MSB 15		
		Bit 14	41 o o 6	Bit 14	MSD	
		13	42 o o 7	13	in	
		12	43 o o 8	12		
		11	44 o o 9	11		
		10	45 o o 10	10		
	Input Data	9	46 o o 11	9		16-Bit
	After	8	47 o o 12	8		Low-Speed
	Latching	7	48 o o 13	7		Bus
	(not connected	6	49 o o 14	6		to: D10
	on backplane)	5	50 o o 15	5		
		4	51 o o 16	4		
		3	52 o o 17	3		
		2	53 o o 18	2	LSD	
		1	54 o o 19	1	in	
		LSB 0	55 o o 20	LSB 0		
			56 o o 21			
			57 o o 22			
			58 o o 23			
			59 o o 24	Output(Main) Reg.D4		(65)
			60 o o 25	Output(Aux.1)		
			61 o o 26	Output Enable		
			62 o o 27	Output(Aux.2)		
			63 o o 28	4 Range		
			64 o o 29	2 tied to		
			65 o o 30	1 Hex Switch		
	+5V from	Synthesizer	66 o o 31			
		+5 Volts	67 o o 32			
		+15 Volts	68 o o 33			
			69 o o 34			
		Ground	70 o-o 35	Ground		

Figure 7.8

Output Register (Latch) Board, Position D 4

Backplane Wiring List

Pin No.	Connects To: Board Name	Function	Backplane Connector	Function	Connects To: Board Name	Pin No.
		Ground	36 o-o 1	Ground		
		+5 Volts	37 o-o 2	+5 Volts		
			38 o o 3			
			39 o o 4			
		MSB 15	40 o o 5	MSB 15		
		14	41 o o 6	14		
		13	42 o o 7	13		
To: 'Variable' DAC A9		12	43 o o 8	12	To: 'Reference' DAC A7	
		11	44 o o 9	11		
		10	45 o o 10	10		
		9	46 o o 11	9		
		8	47 o o 12	8		
		7	48 o o 13	7		
		6	49 o o 14	6		
		5	50 o o 15	5		
		4	51 o o 16	4		
		3	52 o o 17	3		
		2	53 o o 18	2		
		1	54 o o 19	1		
		LSB 0	55 o o 20	LSB 0		
			56 o o 21	Timing Pulse Err D11		(18)
		Bit 11	57 o o 22	MSB 19		
		10	58 o o 23	Bit 18		
	20-Bit High-Speed Bus To: D10	9	59 o o 24	17	20-Bit High-Speed Bus To: D10	
		8	60 o o 25	16		
		7	61 o o 26	15		
		6	62 o o 27	14		
		5	63 o o 28	13		
		4	64 o o 29	12		
(24)	Synth. D3 Timng Pls		65 o o 30	Bit 9		(46)
(60)	Sequ. D9 Sys. Clck		66 o o 31	10	Instruc.	(45)
	Timng Pulse Err LED		67 o o 32	11	Bus	(44)
(21)	Sequ. D9 Tim. "OR"		68 o o 33	12	To: D9	(43)
(32)	Intfc D10 Reset		69 o o 34	MSB 15		(40)
	Ground		70 o-o 35	Ground		

Intfc=Interface; Sequ.=Sequencer; Synth.=Synthesizer;
Timng Pls=Timing Pulse.

Figure 7.9

Sine/Cosine Conversion Circuit Board, Position D 6

Backplane Wiring List

Connects To: Pin No.	Board Name	Function	Backplane Connector	Function	Connects To: Board Name	Pin No.
		Ground	36 o-o 1	Ground		
		+5 Volts	37 o-o 2	+5 Volts		
			38 o o 3			
			39 o o 4			
(40)		MSB 15	40 o o 5	MSB 19		
(41)	Instruction	Bit 14	41 o o 6	Bit 18		
(42)	Bus	13	42 o o 7	17		
(43)	To: D9	12	43 o o 8	16		
(44)		11	44 o o 9	15		
			45 o o 10	14		
			46 o o 11	13	20-Bit	
			47 o o 12	12	High-Speed	
			48 o o 13	11	Bus,	
			49 o o 14	10	To: D10	
			50 o o 15	9		
			51 o o 16	8		
			52 o o 17	7		
			53 o o 18	6		
			54 o o 19	5		
			55 o o 20	4		
(66)	Angle D7	$\overline{BU}$ R.S.	56 o o 21	3		
(67)	Angle D7	$\overline{BU}$	57 o o 22	2		
			58 o o 23	1		
			59 o o 24	LSB 0		
(60)	Sequ. D9	Sys. Clck	60 o o 25			
			61 o o 26			
			62 o o 27			
			63 o o 28			
			64 o o 29			
			65 o o 30			
			66 o o 31			
			67 o o 32			
			68 o o 33			
			69 o o 34			
		Ground	70 o-o 35	Ground		

Angle=Angle Computation(ALU);R.S.=Ready Signal;Sequ.=Sequencer

Figure 7.10

Angle Computation (ALU) Circuit Board, Position D 7

Backplane Wiring List

Pin No.	Connects To: Board Name	Function	Backplane Connector	Function	Connects To: Board Name	Pin No.
		Ground	36 o-o 1	Ground		
		+5 Volts	37 o-o 2	+5 Volts		
			38 o o 3			
			39 o o 4			
(40)		d4 MSB 15	40 o o 5	MSB 19		
(41)		d3 14	41 o o 6	Bit 18		
(42)		SIN/COS 13	42 o o 7	17		
(43)		d2 12	43 o o 8	16		
(44)		d1 11	44 o o 9	15		
(45)		VE 10	45 o o 10	14		
(46)	Instruct.	RE 9	46 o o 11	13	20-Bit	
(47)	Bus	$\overline{OE}$ 8	47 o o 12	12	High-Speed	
(48)	To: D9	S1 7	48 o o 13	11	Bus,	
(49)		S0 6	49 o o 14	10	To: D10	
(50)		A2 5	50 o o 15	9		
(51)		A1 4	51 o o 16	8		
(52)		A0 3	52 o o 17	7		
(53)		I2 2	53 o o 18	6		
(54)		I1 1	54 o o 19	5		
(55)		I0 LSB 0	55 o o 20	4		
			56 o o 21	3		
(19)	Intrf D10	INCR R.S.	57 o o 22	2		
(59)	Intrf D10	PHAS R.S.	58 o o 23	1		
(61)	Intrf D10	OFST R.S.	59 o o 24	LSB 0		
(60)	Sequ. D9	Sys. Clck	60 o o 25	INCR Enabl	Intrf D10	(58)
		Carry out	61 o o 26	PHAS Enabl	Intrf D10	(60)
(20)	Sequ. D9	Negative	62 o o 27	OFST Enabl	Intrf D10	(62)
		Overflow	63 o o 28			
		Zero	64 o o 29	$\overline{GW}$	Intrf D10	(63)
		ALU Clock	65 o o 30			
(56)	Sine D6	BU R.S.	66 o o 31			
(57)	Sine D6	$\overline{BU}$	67 o o 32			
			68 o o 33			
			69 o o 34			
		Ground	70 o-o 35	Ground		

Figure 7.11

Sequencer Circuit Board, Position D 9

Backplane Wiring List

Connects To: Pin No.	Board Name	Function	Backplane Connector	Function	Connects To: Board Name	Pin No.
		Ground	36 o-o 1	Ground		
		+5 Volts	37 o-o 2	+5 Volts		
			38 o o 3			
			39 o o 4			
(40)		MSB 15	40 o o 5	R3 ⎫	Intrf D10	(3)
(41)		Bit 14	41 o o 6	R2 ⎬ MSS	Intrf D10	(4)
(42)		13	42 o o 7	R1 ⎭	Intrf D10	(5)
(43)		12	43 o o 8	R0	Intrf D10	(6)
(44)		11	44 o o 9	R3 ⎫	Intrf D10	(7)
(45)		10	45 o o 10	R2 ⎬ LSS	Intrf D10	(8)
(46)		9	46 o o 11	R1 ⎭	Intrf D10	(9)
(47)	Instruction	8	47 o o 12	R0	Intrf D10	(10)
(48)	Bus	7	48 o o 13			
(49)	To: D7	6	49 o o 14	Ground		
(50)		5	50 o o 15	Ground	Unused	
(51)		4	51 o o 16	Ground	PROM	
(52)		3	52 o o 17	Ground	Address	
(53)		2	53 o o 18	Ground	"OR" Bits	
(54)		1	54 o o 19	Ground		
(55)		LSB 0	55 o o 20	$\overline{\text{ALU "OR"}}$	Angle D7	(62)
			56 o o 21	TP "OR"	Regis D4	(68)
(33)	Intrf D10	Set	57 o o 22	MSB 7 ⎫		
(32)	Intrf D10	Reset	58 o o 23	Bit 6 ⎪		
		$\overline{\text{Source Clk}}$	59 o o 24	5 ⎪		
		Source Clk	60 o o 25	4 ⎪	PROM Address Bus	
			61 o o 26	3 ⎪		
(28)	Intrf D10	$\overline{\text{RE}}$	62 o o 27	2 ⎪	(No Backplane Connection)	
(27)	Intrf D10	MODE1	63 o o 28	1 ⎪		
(26)	Intrf D10	MODE0	64 o o 29	LSB 0 ⎭		
(25)	Intrf D10	Sequ. Zero	65 o o 30	$\overline{\text{CE1}}$,$\overline{\text{CE2}}$	Connected	
			66 o o 31	$\overline{\text{OE}}$	To Ground	
			67 o o 32			
			68 o o 33	5 MHz out		
			69 o o 34	10 Mhz out	Digtz A13	(65)
		Ground	70 o-o 35	Ground		

Intrf=Interface;Instruct=Instruction;MSS=Most Significant Slice
LSS=Least Significant Slice;Sequ.=Sequencer;TP=Timing Pulse

Figure 7.12

Interface Unit Circuit Board, Position D 10

Backplane Wiring List

Connects To: Pin No.	Board Name	Function	Backplane Connector	Function	Board Name	Pin No.
		Ground	36 o-o 1	Ground		
		+5 Volts	37 o-o 2	+5 Volts		
		MSB 19	38 o o 3	MSB 15		
		Bit 18	39 o o 4	Bit 14		
		17	40 o o 5	13		
		16	41 o o 6	12		
		15	42 o o 7	11		
		14	43 o o 8	10		
	20-Bit	13	44 o o 9	9	16-Bit	
	High-Speed	12	45 o o 10	8	Low-Speed	
	Bus	11	46 o o 11	7	Bus	
	(Origin)	10	47 o o 12	6	(Origin)	
		9	48 o o 13	5		
		8	49 o o 14	4		
		7	50 o o 15	3		
		6	51 o o 16	2		
		5	52 o o 17	1		
		4	53 o o 18	LSB 0		
		3	54 o o 19	INCR R.S.	Angle D7	(57)
		2	55 o o 20			
		1	56 o o 21		PhsDet.A11	(31)
		LSB 0	57 o o 22		PhsDet.A11	(32)
(25)	Angle D7	INCR Enbl	58 o o 23		Digitz A13	(60)
(58)	Angle D7	PHAS R.S.	59 o o 24			
(26)	Angle D7	PHAS Enbl	60 o o 25		Sequ. D9	(65)
(59)	Angle D7	OFST R.S.	61 o o 26		Sequ. D9	(64)
(27)	Angle D7	OFST Enbl	62 o o 27		Sequ. D9	(63)
(29)	Angle D7	GW	63 o o 28		Sequ. D9	(62)
(39)	Synth D3	Synth Clk	64 o o 29		Displ. A4	(19)
(7)	PhsDet A11	Var Clck	65 o o 30	Displ Clck	Displ. A4	(10)
(6)	PhsDet A11	Ref Clck	66 o o 31	Conv.Compl	Digitz A13	(14)
(31)	DAC A9	Var Clock	67 o o 32	Reset	D9(58), D4	(69)
(31)	DAC A7	Ref Clock	68 o o 33	Set	Sequ. D9	(57)
(16)	Digitz A13	Conv Com	69 o o 34	ADC OE	Digitz A13	(18)
		Ground	70 o-o 35	Ground		

Angle=Angle Computation(ALU);Conv.Compl=Coversion Complete;
Digitz=Digitizer;Displ Clck=Display Clock Pulse;
INCR R.S.='Increment' Ready Signal; PhsDet=Phase Detector;
Synth=Synthesizer.

Figure 7.13

8085 Microcomputer Circuit Board, Position D 11

Backplane Wiring List

Connects To: Pin No.	Board Name	Function	Backplane Connector	Function	Connects To: Board Name	Pin No.
		Ground	36 o-o 1	Ground		
		+5 Volts	37 o-o 2	+5 Volts		
			38 o o 3			
			39 o o 4			
			40 o o 5			
			41 o o 6			
			42 o o 7			
			43 o o 8			
			44 o o 9			
			45 o o 10			
			46 o o 11			
			47 o o 12			
			48 o o 13			
			49 o o 14			
			50 o o 15			
			51 o o 16			
			52 o o 17			
			53 o o 18	Tim Pls err Regis D4		(21)
			54 o o 19			
			55 o o 20			(70)
			56 o o 21			
			57 o o 22			(69)
			58 o o 23			(68)
			59 o o 24			(67)
			60 o o 25		Display	(66)
			61 o o 26			(65)
			62 o o 27		and	(64)
			63 o o 28			(63)
			64 o o 29		Keyboard	(55)
			65 o o 30			(56)
			66 o o 31		Interface	(57)
			67 o o 32			(58)
			68 o o 33			(59)
			69 o o 34			(60)
			70 o-o 35			(61)

Figure 7.14

7.2 Signal Generation (High-Speed Processor)

7.2.1 Sequencer

(Refer to circuit diagram D9, figure 7.15.) The program of the high-speed processor which controls the digital waveform synthesis is stored in programmable read-only memory (PROM) I, J, K, and L on the 'Sequencer' board. The function of this board is to step through the PROMs and generate 16-bit instruction words which are applied to the instruction bus on edge connector pins (40)-(55). This bus contains three types of instructions:

(a) Sequencer Instructions. Special instructions allow the sequencer to jump to different PROM locations. When the most significant bit (pin 40) of the instruction word is a zero, the 'load' pin of A, B, C, and D (counters here used as registers) is enabled, and the next clock pulse loads the instructions from the bus back into the sequencer E and F. (See section 5.2.2 for a description of sequencer instructions.)

(b) ALU Instructions. This set of instructions is used for angle computation. The two most significant bits of the instruction word, '1 0,' are decoded by the ALU board. (See section 5.2.3 for ALU instructions.)

(c) Bus Instructions. This set of instructions is characterized by '1 1' in the two most significant bits of the instruction word. (See section 5.2.4 for description of the coding.)

To start the program in the normal mode, the register enable, $\overline{RE}$, at edge connector pin (62) is pulled low and provides a 'low' at pin (1) of E and F. This enables the sequencer address register, and with the next clock pulse, the 8-bit starting address (located on edge connector pins (5)-(12)) is loaded onto the PROM address bus (edge connector pins (22)-(29)). (A LED readout displays the PROM address as two hexadecimal digits.) The contents of the PROMs corresponding to that address then appear on the instruction bus. On the next clock pulse (from the 5 MHz system clock) the sequencer increments the address by one least significant bit. The new PROM address generates a new set of instructions from the stored high-speed program. The PROM address can be modified in several ways:

(i) The address can be OR'ed with external bits via gates Q and R when these are enabled by a sequencer instruction. Edge connector pins (14)-(21) are available for external 'OR' bits.

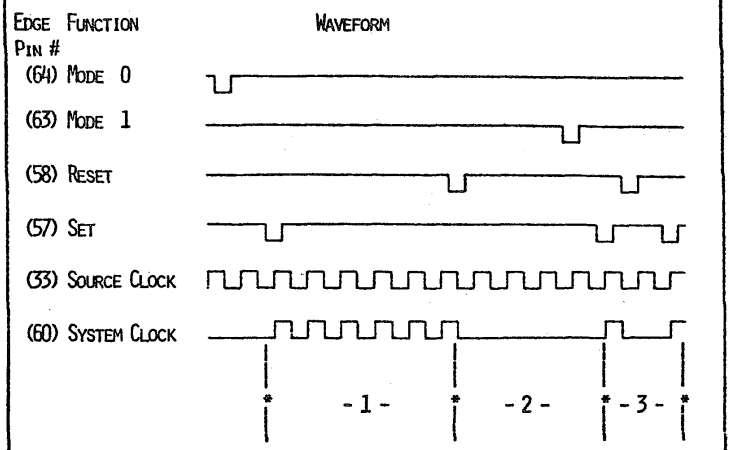
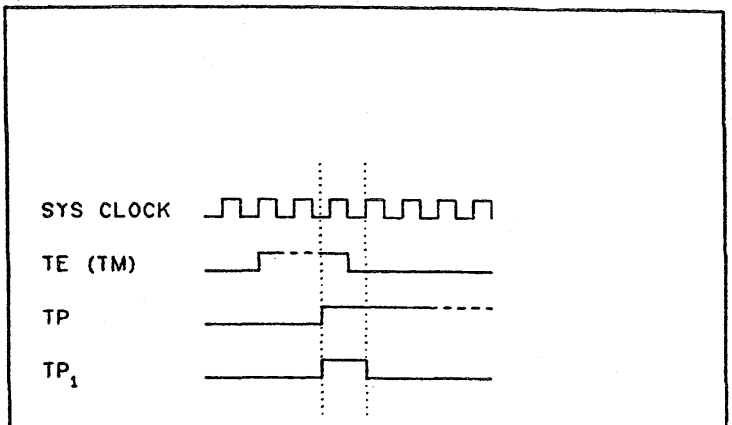
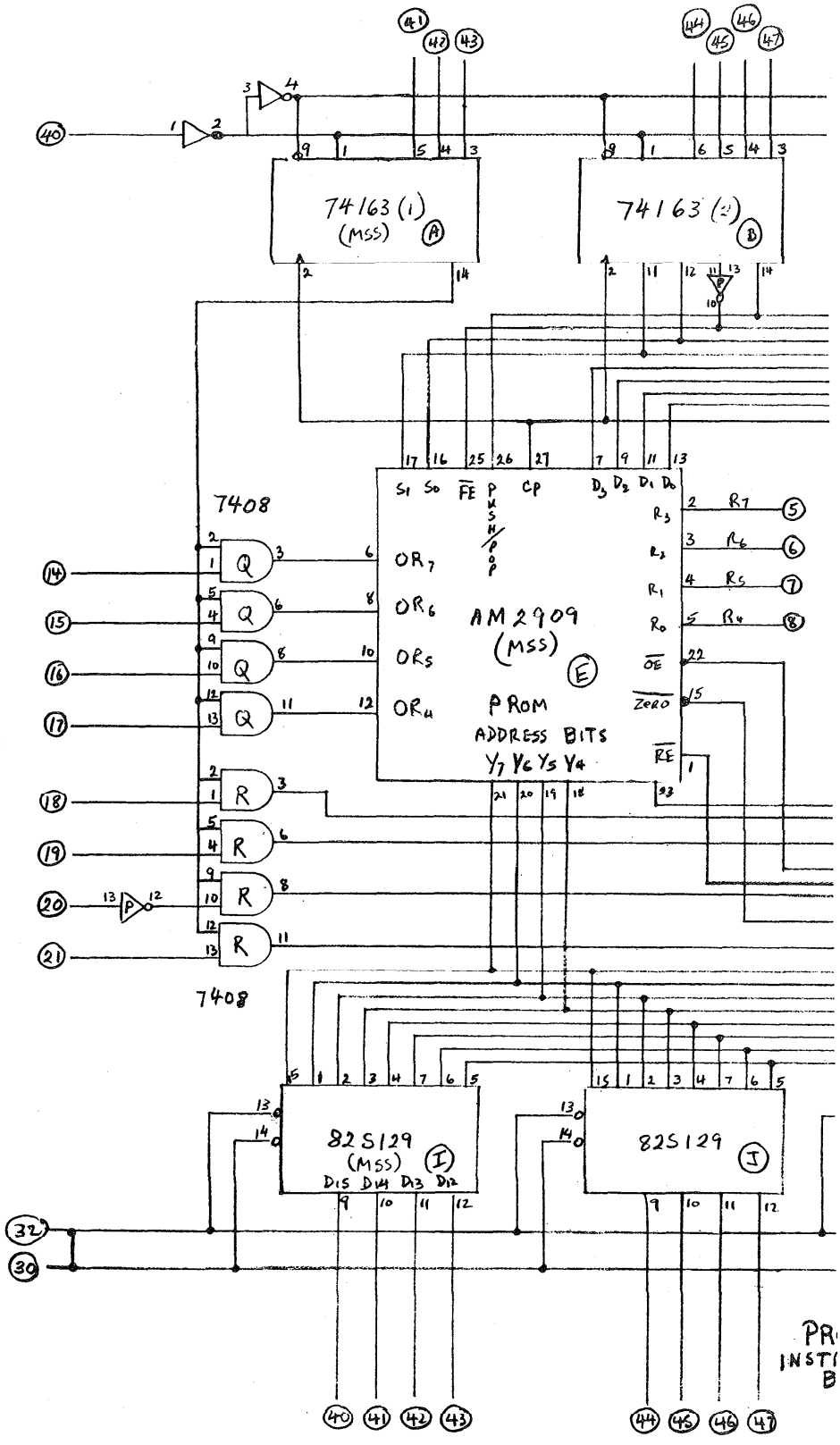


Figure 7.16 System Clock Control

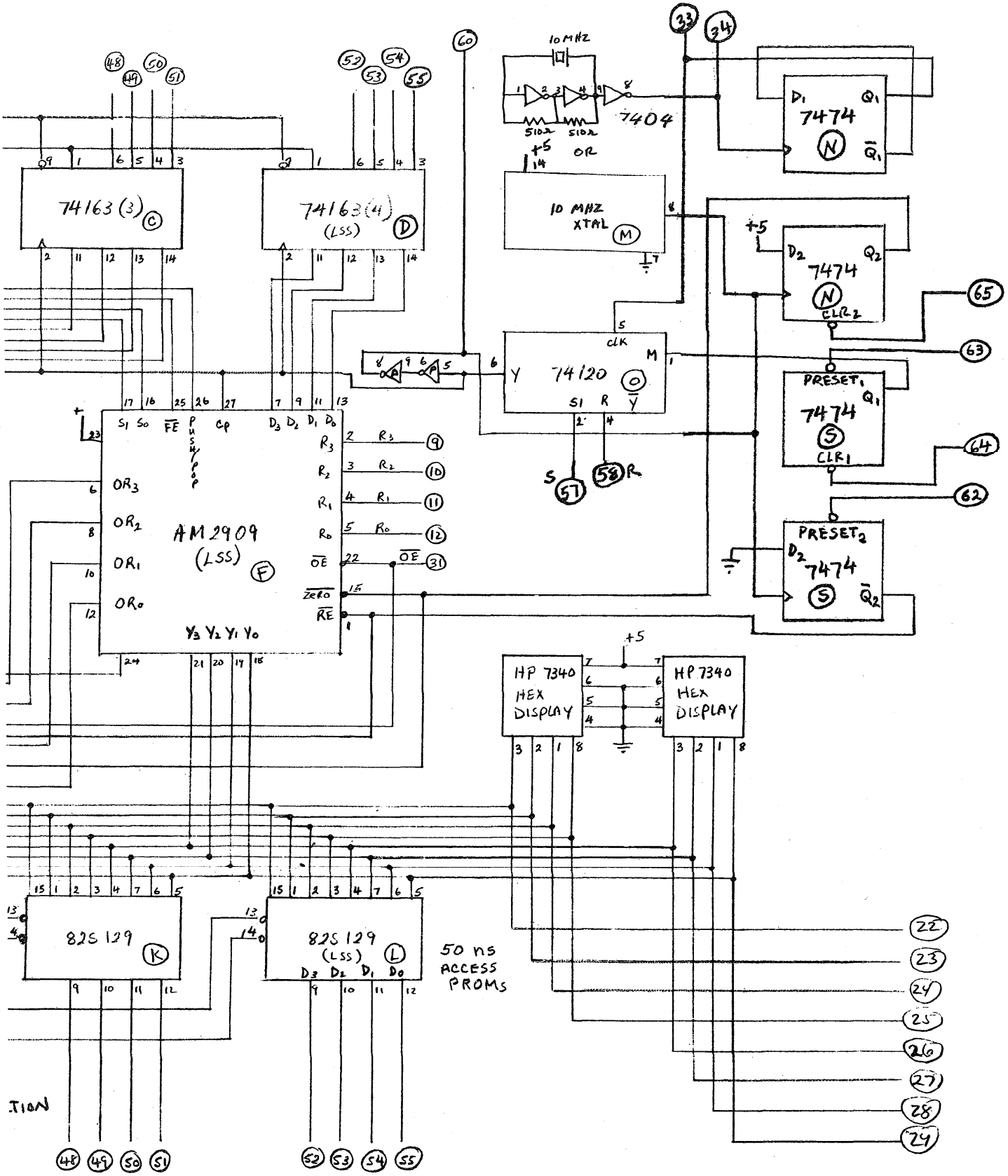


TIMING PULSE DIAGRAM

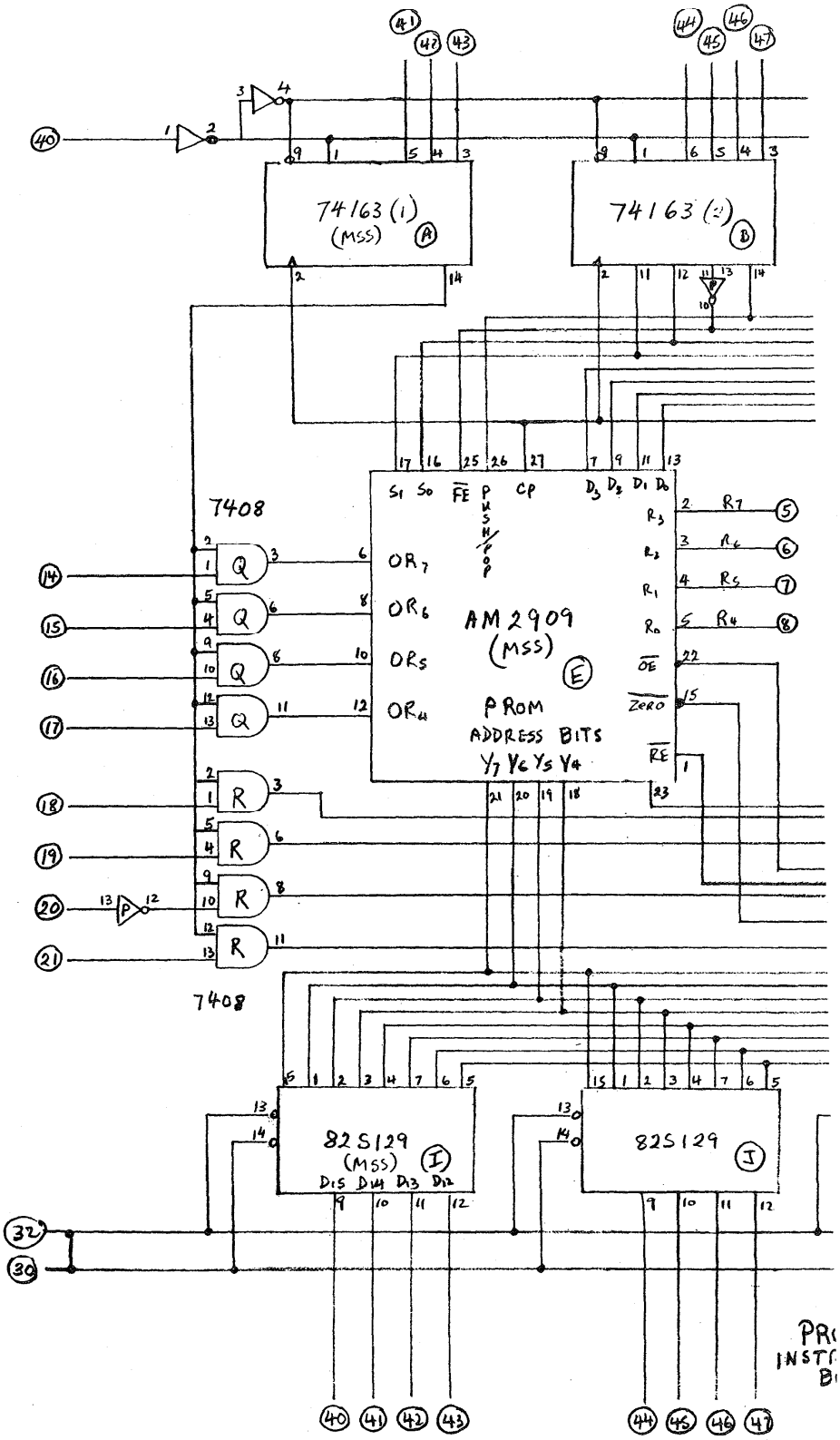
Figure 7.20


74163 (1)
(MSS)
A
74163 (2)
B
7408
AM2909
(MSS)
E
PROM
ADDRESS BITS
Y7 Y6 Y5 Y4
OR7
OR6
OR5
OR4
OE
ZERO
RE
7408
82S129
(MSS)
I
D15 D14 D13 D12
82S129
J

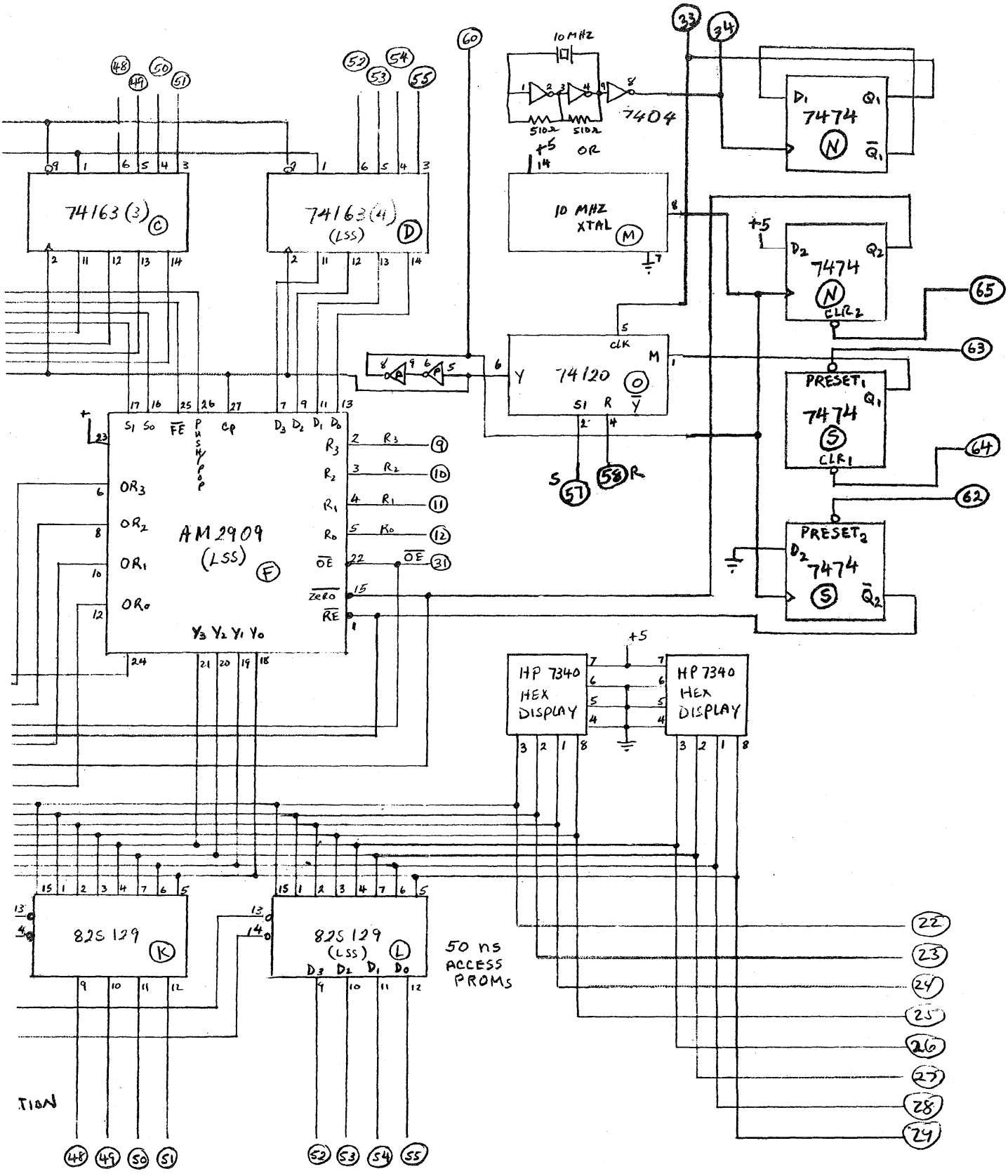
Fig



7.15 Sequencer Circuit Diagram D9


74163 (1)
(MSS) A
74163 (2) B
7408
AM2909
(MSS) E
PROM
ADDRESS BITS
Y7 Y6 Y5 Y4
7408
825129
(MSS) I
825129 J

Fig



.15 Sequencer Circuit Diagram D9

(ii) The address can be set to zero with a 'low' on edge connector pin (65).

(iii) The eight LSBs of the instruction bus can be used as jump address in a sequencer instruction. (See section 5.2.2 for more details.)

The output of a 10-MHz crystal, M, at edge connector pin (34), is reduced to 5 MHz by divider N (available at edge connector (33)) which is the source of the high-speed system clock. Flip-flop S, and pulse synchronizer O, provide the three operating modes of the system clock shown in figure 7.16:

1. 'RUN': With the mode pin on O set low ((64) pulsed low), the system clock will appear at (60) on the negative going edge of the input at pin (57).

2. 'STOP': The negative going edge at R (58) disables the system clock (60).

3. 'SINGLE STEP': With the mode pin at O set 'high,' as a result of a 'low' pulse at (63), the synchronizer O is set in the single pulse mode. A negative going pulse at R arms the synchronizer, and a subsequent negative going pulse at S sets up the device so that the next clock pulse can go through to (60). The synchronizer must be rearmed with a pulse at R and set with a pulse at S before another single clock pulse can be passed.

7.2.2 Angle Computation (ALU)

(Refer to circuit diagram D7, figure 7.17.) The angle computation board consists of a 20-bit arithmetic-logic unit (ALU) which sets up and increments the individual angles used to produce both waveforms. The starting angles of each waveform ('offset' for the 'reference' output and 'phase' for the 'variable' output), and the angle 'increment' (INC), which determines the number of steps in the waveform, are sent from the 8085 over the 20-bit bus to storage register files H, I, J, K, and L. The values are loaded into the internal registers of the ALUs C, D, E, F, and G at the start of each period of the output waveform (see section 5.1.4). The initial angles are then loaded sequentially onto the 20-bit bus through tri-state buffers in the ALU.

While the 20-bit angles, in two's complement binary format, are converted to their respective sine values on board D6 and then sent on to the digital-to-analog converters, the initial angles are incremented in the ALU and the process is repeated to obtain the next pair of output values. The ALU can be operated with a 5-MHz clock by using look-ahead carry generators A and B.

ALU instructions are latched from the instruction bus into M and N (instruction codes are described in detail in section 5.2.3). Decoding

of the two most significant bits of the instruction word by O and Q provides a signal which enables latches M and N, and the ALU itself only when the instruction word is recognized as an ALU instruction.

Five priority interrupts for gaining control of the 20-bit bus are described in table 7.1.

Table 7.1 Bus priority (request)

Signal Priority	Name	Source Board No.	Edge Connector Pin No.	Description
1 (Highest)	"BU"	D6	(66)	Sine function is ready to be transmitted to the latch.
2	"ALU"	D7	On board	Angle is ready to be transmitted to the SIN/COS converter.
3	"INC"	D10	(57)	'Increment' (caused by a keyed in frequency change) is waiting to be transmitted from the 8085 to the ALU.
4	'PHASE'	D10	(58)	'Variable' starting angle ready for transmission from the 8085 interface.
5 (Lowest)	'OFFSET'	D10	(59)	'Reference' starting angle ready for transmission from the 8085 interface.

Priority encoder U handles the arbitration while decoder V ensures that only one enable line at a time will be activated. Table 7.2 describes the output enable lines.

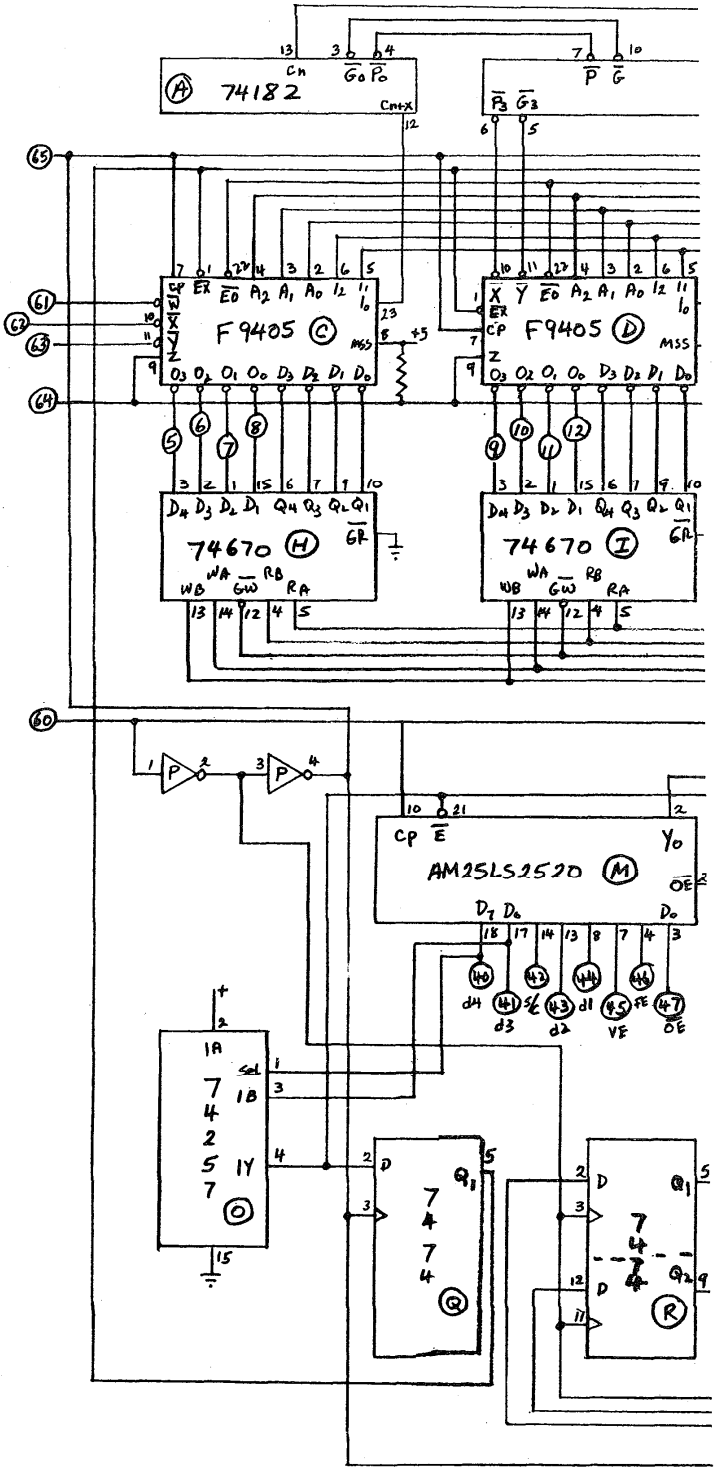


Fig. 7.17 ALU Circui

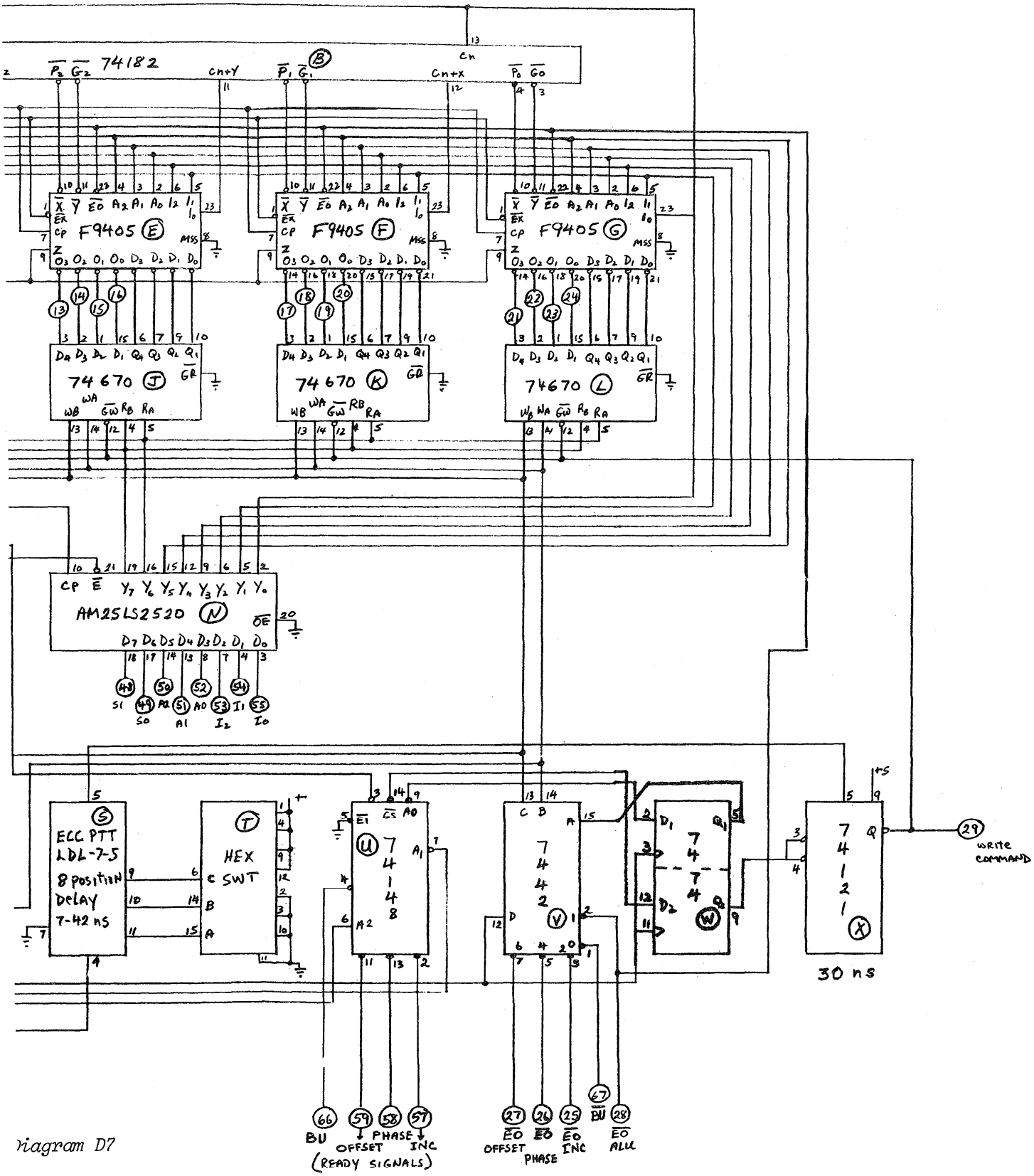

74182
F9405 E
F9405 F
F9405 G
74670 J
74670 K
74670 L
AM25LS2520 N
ECC PTT
LDL-7-5
8 position
Delay
7-42 ns
HEX
SWT
30 ns
write command
BU
OFFSET
PHASE
INC
(READY SIGNALS)
BU
EO OFFSET
EO PHASE
EO INC
EO ALU

Diagram D7

Table 7.2 Bus priority (acknowledgement)

Signal Priority	Name	Destination Board No.	Edge Connector Pin No.	Description
1 (Highest)	"BU"	D6	(67)	Loads sine function on 20-bit bus.
2	"ALU"	D7	On board	Loads angle on bus.
3	"INC"	D10	(57)	Loads 'increment' on bus.
4	'PHASE'	D10	(58)	Loads 'phase' angle on bus.
5 (Lowest)	'OFFSET'	D10	(59)	Loads 'offset' angle on bus.

Latch R holds the register file address, lines WA and WB, at the appropriate codes until the write pulse, GW, occurs. The write command is sent by W and X anytime the bus is enabled (EO lines at pins (25), (26), (27), (28), (67)), and strobes the data into the file selected by the address lines. Delay line S, controlled by switch T, is used to delay the write pulse until the 20-bit data bus is enabled.

7.2.3 SIN/COS Conversion

(Refer to circuit diagram D6, figure 7.18.) As each 20-bit angle appears on the 20-bit bus, it is strobed into latches A, B, C, D, and E by the 'sine latch' instruction, 'SL,' which is decoded from the instruction bus by Q, R, and S and is defined as the logic combination.

Bit 15 AND (NOT Bit 12 AND Bit 11)

The numerical value of the angle is applied to modules F and G for conversion to its sine. Module G uses a fast look-up table algorithm to convert a 16-bit scaled binary angle over the range of 0 to 90 degrees to a 16-bit binary positive number. Module F extends the conversion to all four quadrants by decoding the two most significant bits of the input angle. Once the quadrant is known, the sign of the output is determined, and either the remaining 16-bit binary angle (quadrants 1 & 3) or its complement (quadrants 2 & 4) is applied to G. The output of the combination of the two modules is a 16-bit (magnitude) + sign binary sine function. It is truncated to 15 bits + sign and converted to two's complement format by H, I, J, and K. These are 4-bit adders-subtractors with their 'A' inputs tied to the binary output of G and the 'B' inputs tied low (logical zero). The 'sign' output from F determines whether an addition or subtraction is performed. T is a look-ahead carry generator to speed up the adder function.

Figure 7.18 shows the two's complement conversion circuit. When the sign is positive (quadrants 1 & 2), the output from the adder has its most significant bit equal to zero, followed by the 15 MSBs of the output from G. When the sign is negative (quadrants 3 & 4), the output has the MSB=1, followed by the 15 bits resulting from the operation -G+1. The 16-bit output from the adder is inverted to ground true two's complement format and tied to the 20-bit bus by tri-state inverters L, M, N, and O. The (data-) bus enable 'BU' is decoded from the instruction bus as the logic combination

Bit 15 AND (Bit 12 AND NOT Bit 11)

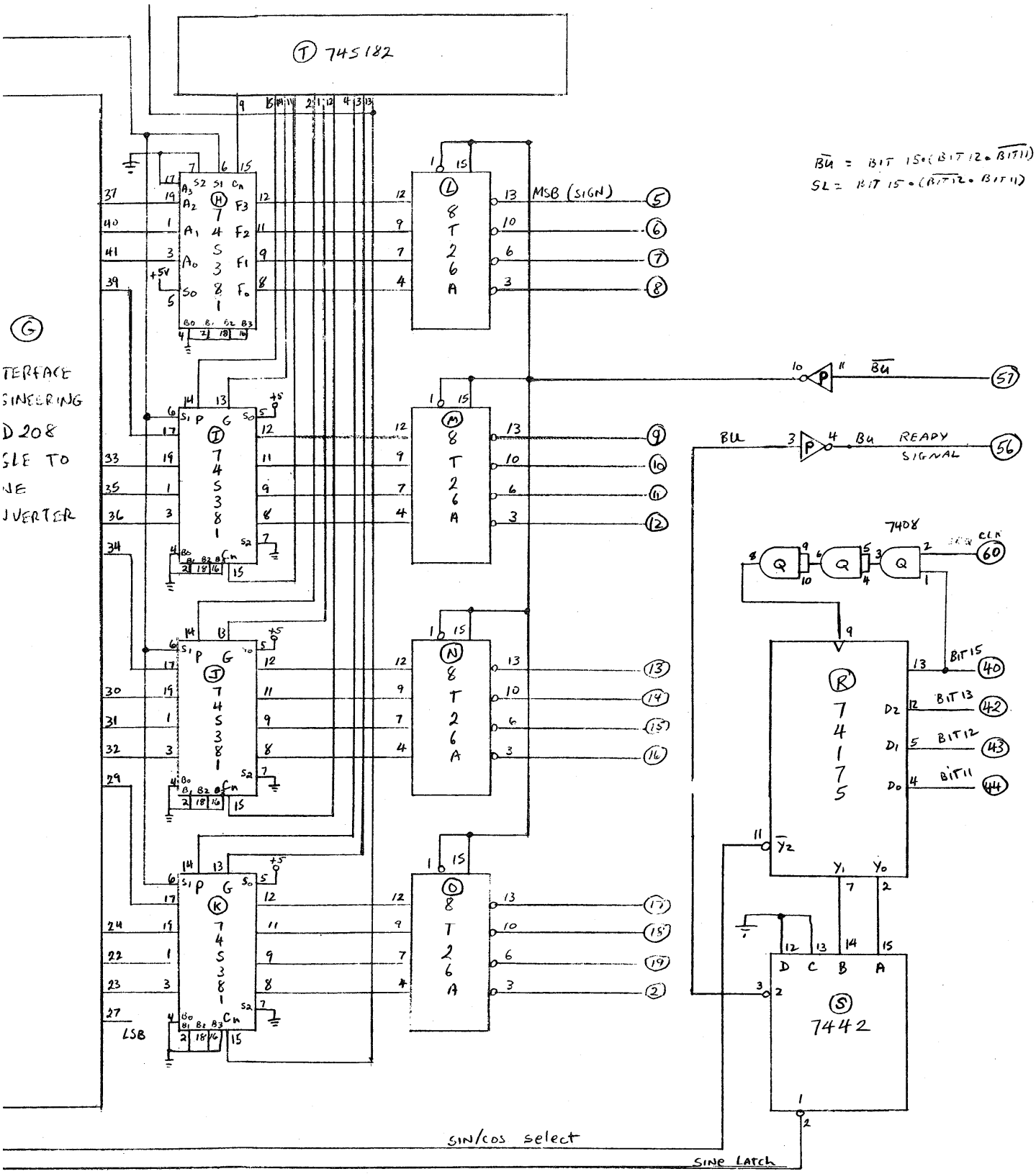
and is sent out through edge connector pin (56) to the priority interrupt circuit on the ALU board D7. Since 'BU' is the highest priority bus instruction, it inhibits all other bus access requests and returns an acknowledge signal through edge connector pin (57) to enable the tri-state inverters during the second half of the system clock cycle during which the 16-bit sine function is placed on the 20-bit bus. (See also figures 5.3 and 5.4.)

7.2.4 Output Registers (Latches)

(Refer to circuit diagram D4, figure 7.19 and timing diagrams 5.3 and 5.4.) As each 16-bit sine function value appears on the bus, it is stored in a set of "D" type latches so that both digital-to-analog converters can be updated simultaneously by the timing pulse, 'TP_1.' The sine value for the 'variable' waveform is strobed into latches M, O, Q, and S by 'VE,' while the 'reference' waveform sine value is strobed into U, W, Y, and AA by 'FE.' The latch circuitry then waits for the timing pulse enable, 'TE' (labeled 'TM' in figures 5.3 and 5.4), which like 'VE' and 'FE' is decoded from the instruction bus. 'TE' is an input to flip-flop F, which produces 'TP_1' on the rising edge of the timing pulse 'TP_1' which comes from the synthesizer board D3 (see figure 7.20,*). 'TP_1' transfers both 'reference' and 'variable' sine values into a second set of edge triggered latches which supply the data directly to the digital-to-analog converters. Once these latches have been updated, the 'OR' bit appears at edge connector pin (68), allowing the high-speed processor to jump out of its wait loop and calculate the next pair of sine values.

Pulses 'VE,' 'FE,' and 'TE' and the trailing edge of 'TP_1' are synchronous with the system clock, while the timing pulse 'TP' and the rising edge of 'TP_1' are asynchronous. The flip-flop in the other half of F and one of the flip-flops in G form a delay circuit which makes sure that the duration of pulse 'TP_1' is at least one system clock period. Retriggerable one-shot H acts as a frequency window comparator and provides a signal at edge connector pin (21) when the repetition frequency of the timing pulse 'TP' is out of range. D is a switch selectable delay line which delays 'VE' and 'FE' to provide data setup time.

*See page 102



SIN/COS Conversion Circuit Dia. D6

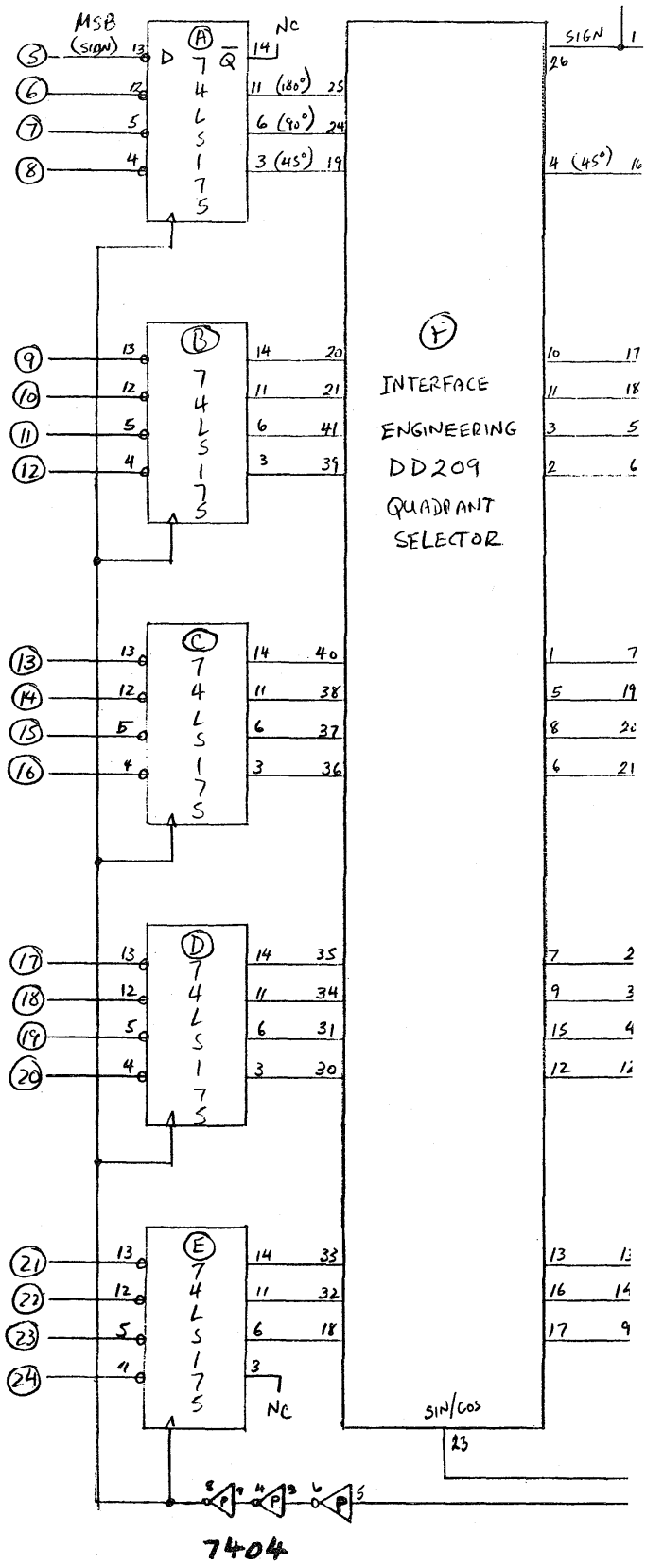

MSB
(SIGN)
NC
SIGN
D
Q
74LS175
INTERFACE
ENGINEERING
DD209
QUADRANT
SELECTOR
SIN/COS
NC
7404

Fig.

7.2.5 Frequency Synthesizer

(Refer to circuit diagram D3, figure 7.21.) Synthesizer E is a commercial board capable of frequency synthesis with 4-digit resolution over a wide frequency range. In normal operation it is used on range '6,' selected by a screwdriver operated hexadecimal switch, between 200 and 400 kHz. The BCD signal, which corresponds to the desired frequency, is loaded onto the 16-bit (low-speed) data bus (from Interface board D10), and is followed by a "synthesizer clock" pulse which appears at edge connector pin (39) and latches the 4-digit frequency value into the inputs of E. A TTL-compatible square wave of the desired frequency appears at edge connector pin (25). This output, however, is only a monitor; the main output timing pulse is fed to system via edge connector pin (24). One-shot G and gates H allow the timing pulse (normally supplied by the synthesizer) to be overridden by an external TTL signal, at edge connector pin (23), if its frequency is greater than 1 kHz.

7.2.6 Digital-to-Analog Converters (DAC)

(Refer to circuit diagram A7 and A9, figure 7.24.) The two 16-bit sine values, latched by 'TP1', are applied to the converter circuits to produce output staircase approximations of the 'reference' and 'variable' sinewaves. Each sinewave is filtered and scaled to the desired voltage using a variable gain, low-voltage amplifier and a fixed gain, high-voltage amplifier as shown in figure 7.22, which is a block diagram of each output channel.

Referring to the circuit diagram of figure 7.24, the 16-bit DAC A supplies a current, proportional to the digitial code, to the summing node of amplifier B which is configured as an infinite gain, multiple feedback, 2-pole Butterworth active filter. Internal resistors in the DAC establish a gain of two for this stage. Amplifier C forms a second 2-pole section with unity gain. The combination is a 4-pole Butterworth filter with a 3 dB frequency of 25 kHz, providing an 80 dB per decade rolloff. The filter output is adjusted to 10.00 V peak (7.07 V rms) and is made available at the coaxial output connector through the relay K by grounding edge connector pin (12). With edge connector pin (12) tied to +5 V, the output amplitude is made programmable, controlled by signals on the 16-bit (low-speed) data bus.

A high-voltage (145-V peak) operational amplifier, I, is configured so that its gain is -20 (see figure 7.23). Table 7.3 gives the digital codes and range bit required to select various output voltages ranging from 0.25 to 100.0 V rms.

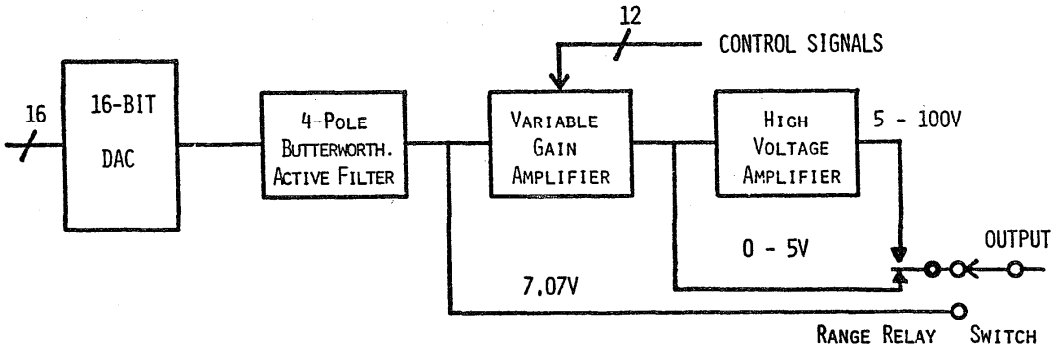


Figure 7.22 Block Diagram of Output Channel

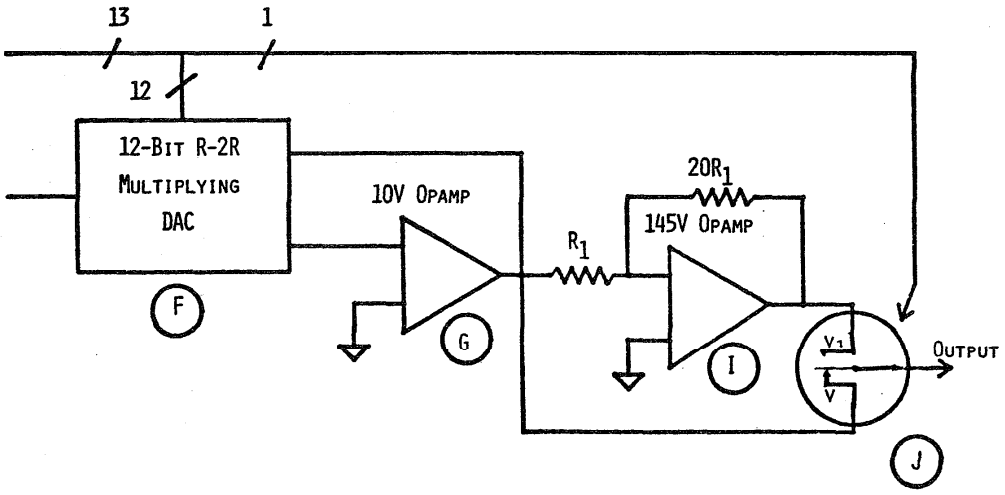
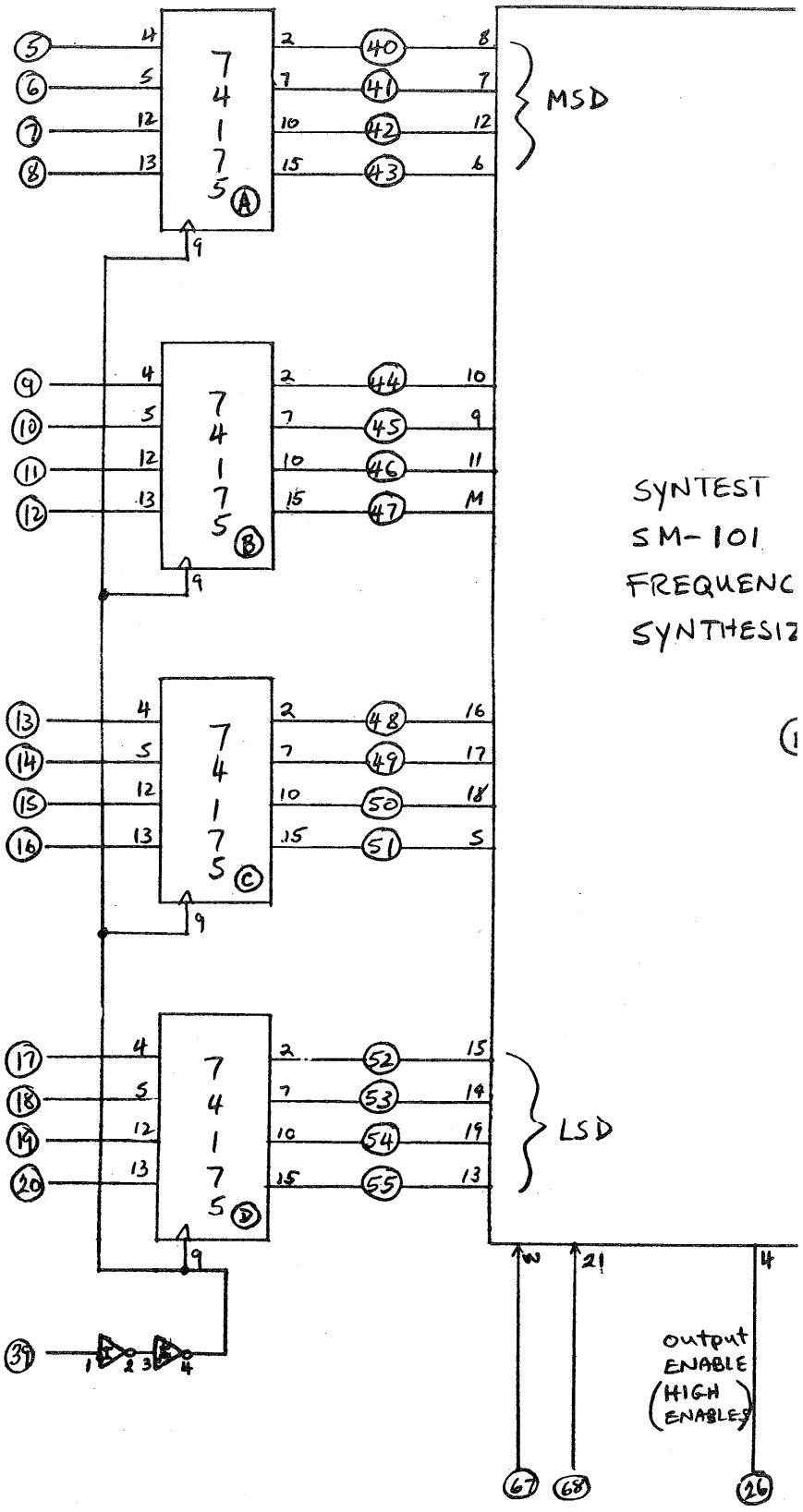
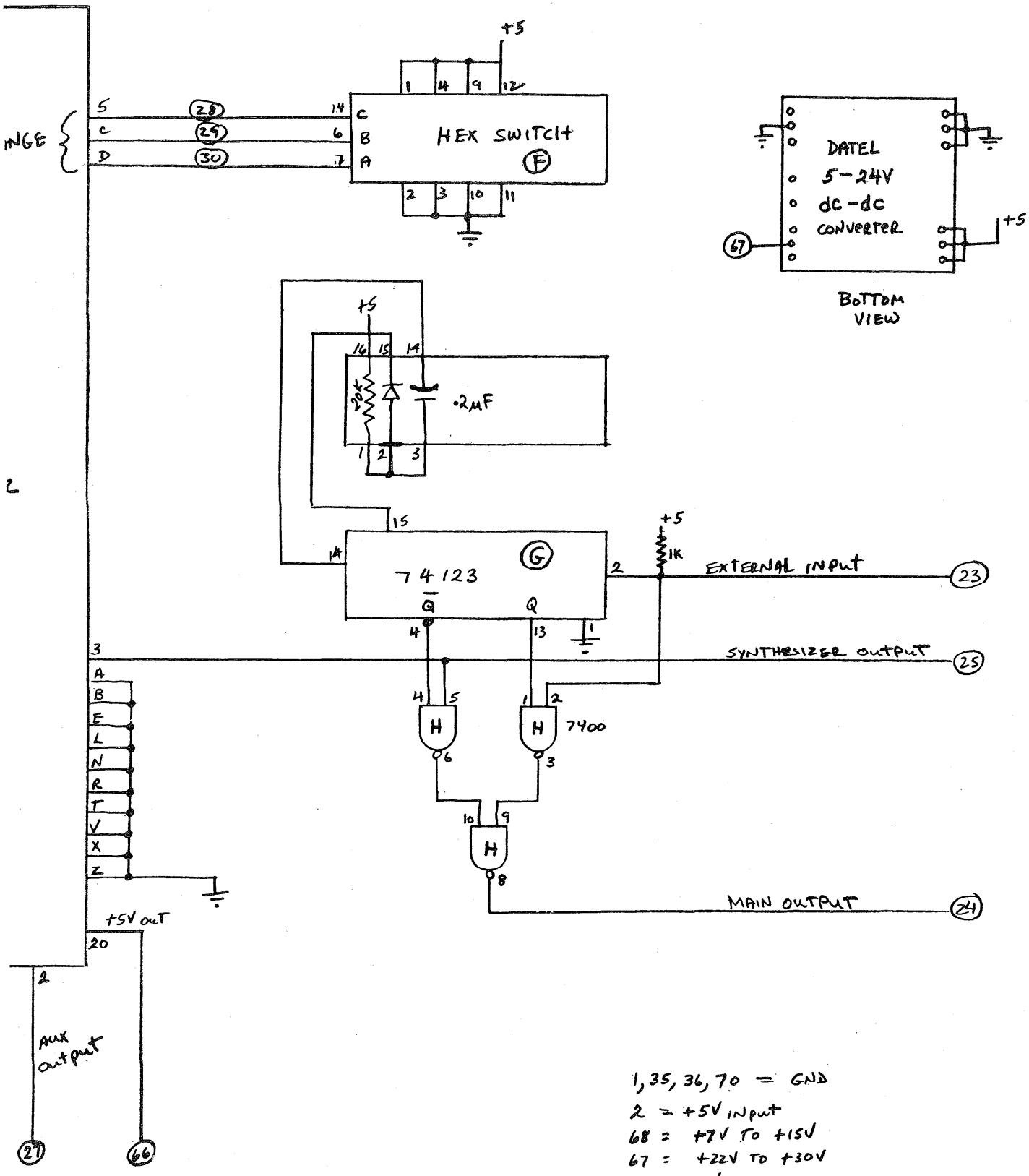


Figure 7.23 Block Diagram of Programmable Output Voltage Circuitry


7417 5 A
7417 5 B
7417 5 C
7417 5 D
MSD
LSD
SYNTEST
SM-101
FREQUENC
SYNTHESIZ
output
ENABLE
(HIGH
ENABLES)



req. Synthesizer Circuit Dia. D3

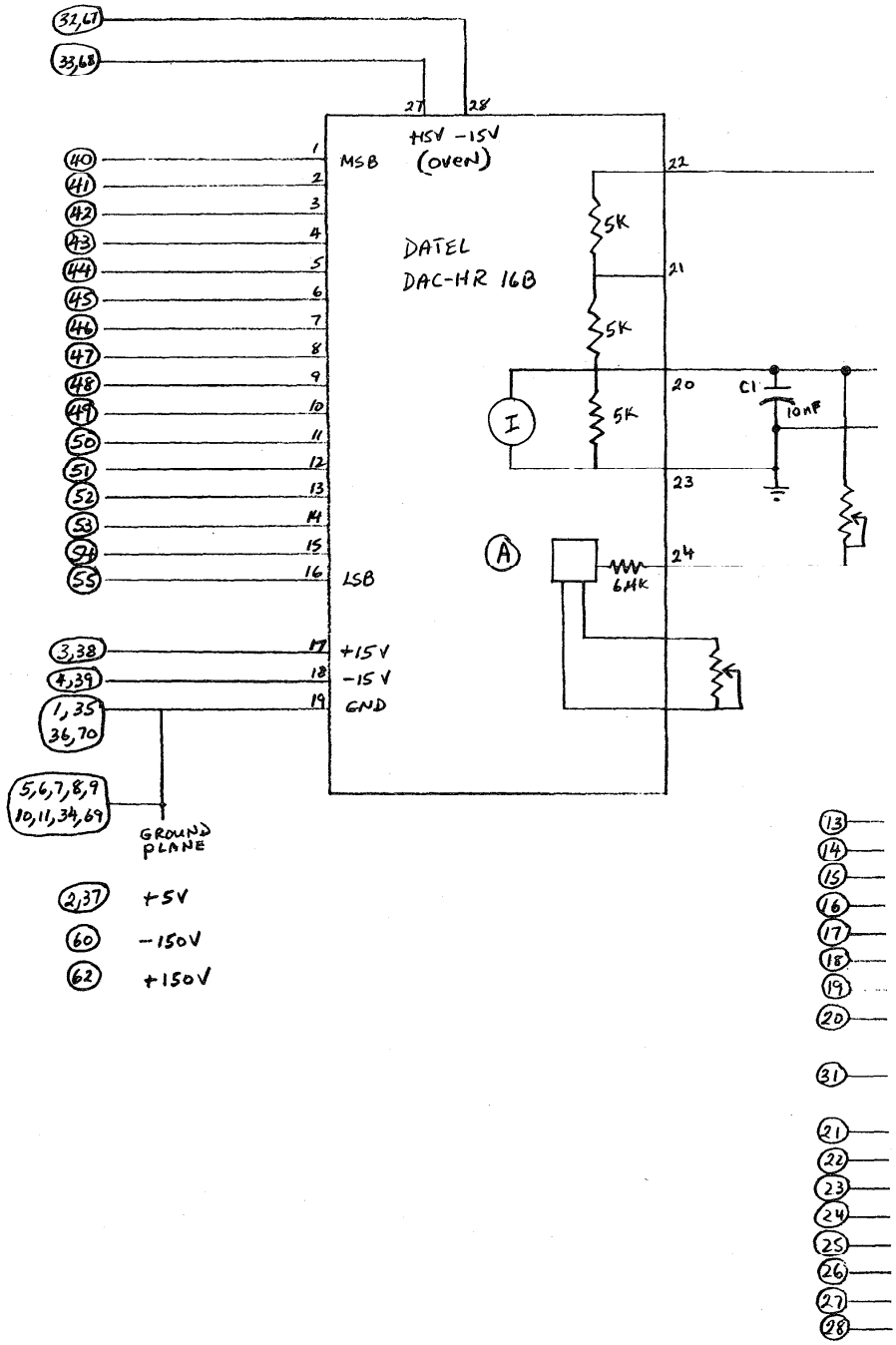
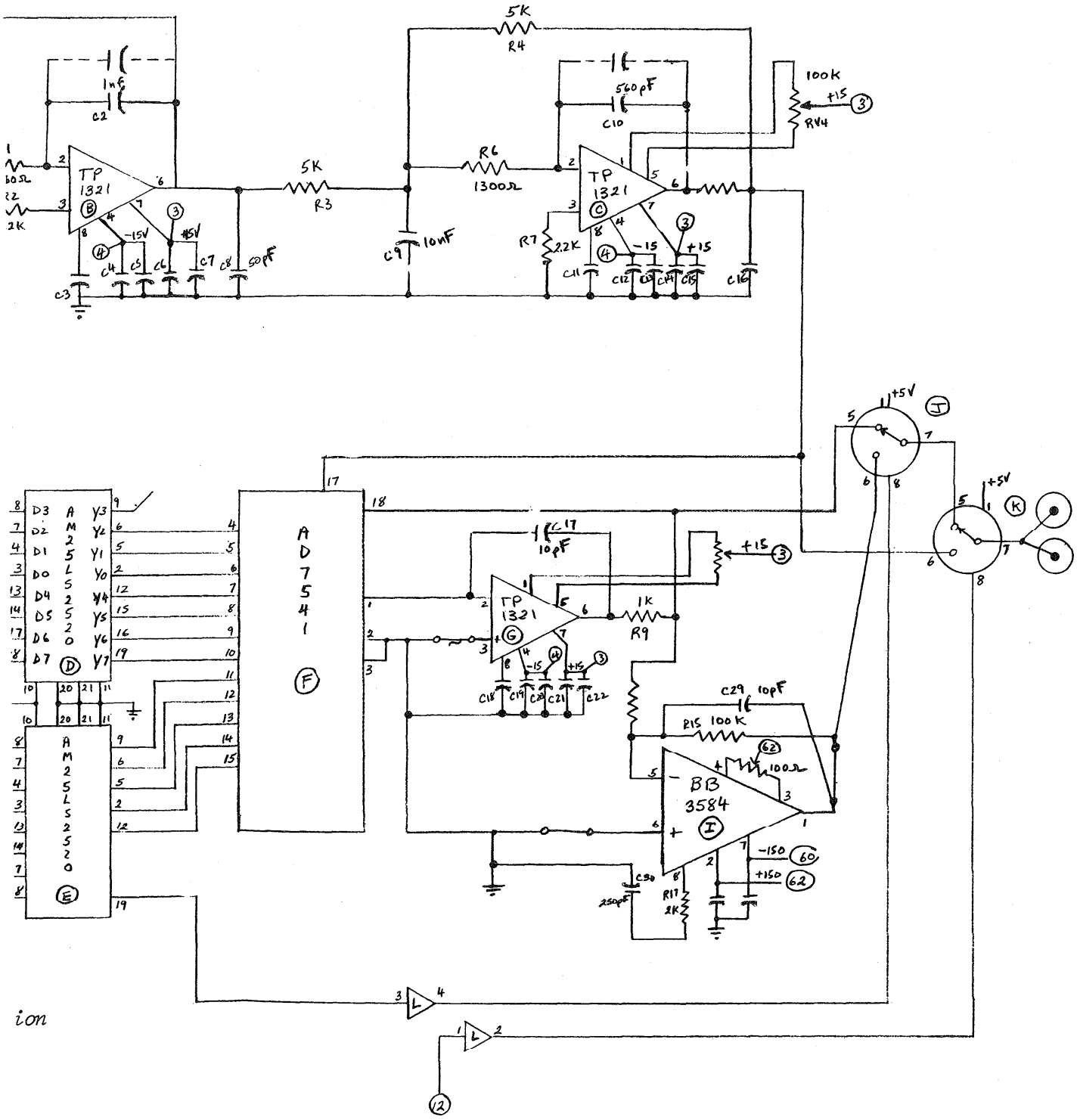
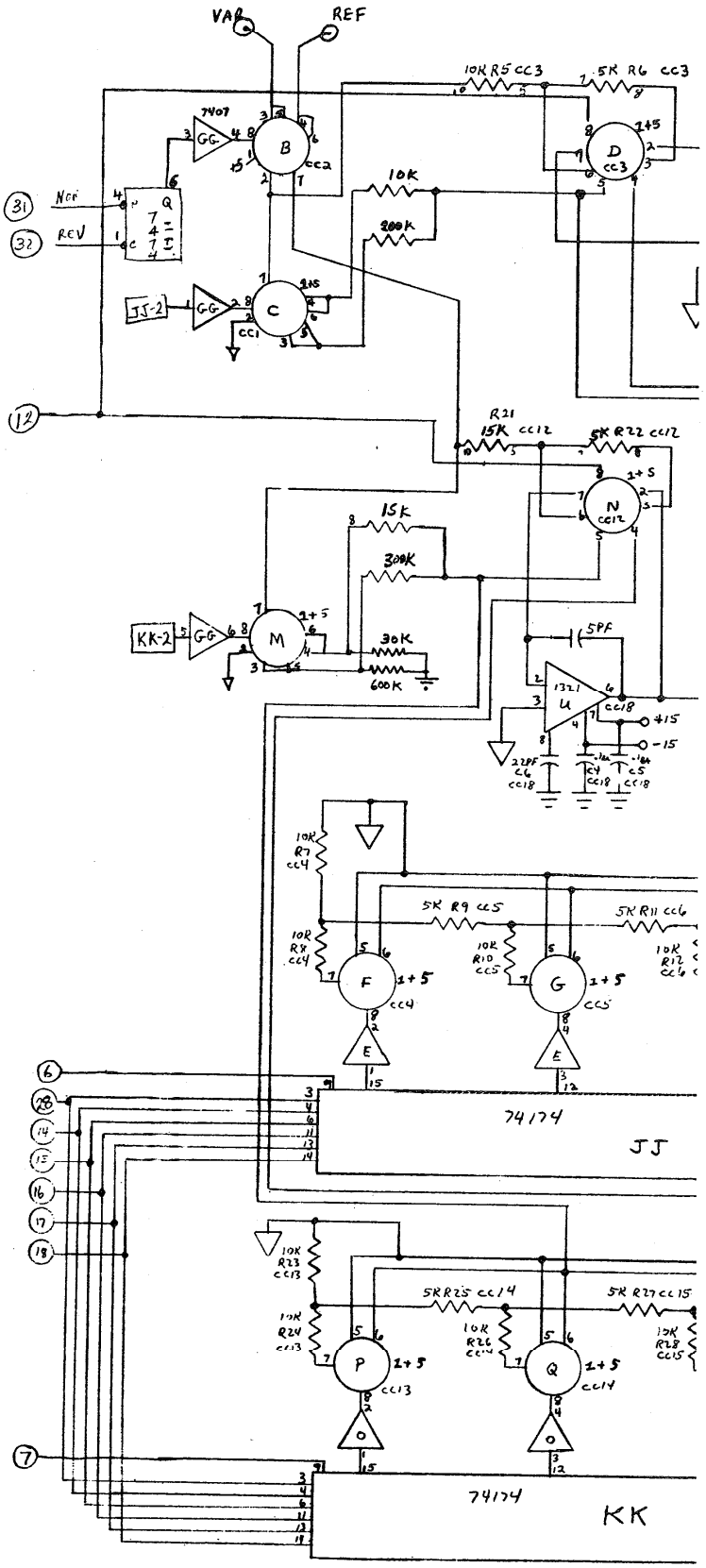


Fig. 7.24 Digital-to-Analog Conve
Circuit Diagram A7 & A8


5K
R4
1nF
C2
560pF
C10
100K
+15
RV4
TP 1321
5K
R3
R6
1300Ω
10nF
C9
R7
2.2K
-15
+15
50pF
C8
C3
C4
C5
C6
C7
C11
C12
C13
C14
C15
C16
+5V
AM25LS2520
ADJ541
C17
10pF
1K
R9
C18
C19
C20
C21
C22
C29
10pF
R15 100K
100Ω
BB 3584
-150
+150
C30
250pF
R17
2K
D3
D2
D1
D0
D4
D5
D6
D7
Y3
Y2
Y1
Y0
Y4
Y5
Y6
Y7
ion


VAR
REF
10K R5 CC3
5K R6 CC3
7407
B
CC2
D
CC3
10K
200K
NOR
REV
7474
JJ-2
C
CC1
R21
15K CC12
5K R22 CC12
N
CC12
15K
300K
KK-2
M
30K
600K
5PF
1321
U
CC18
+15
-15
22PF
C6
CC18
C4
C5
10K R7 CC4
5K R9 CC5
5K R11 CC6
10K R8 CC4
10K R10 CC5
10K R12 CC6
F
CC4
G
CC5
E
74174
JJ
10K R23 CC13
5K R25 CC14
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10K R24 CC13
10K R26 CC14
10K R28 CC15
P
CC13
Q
CC14
O
74174
KK

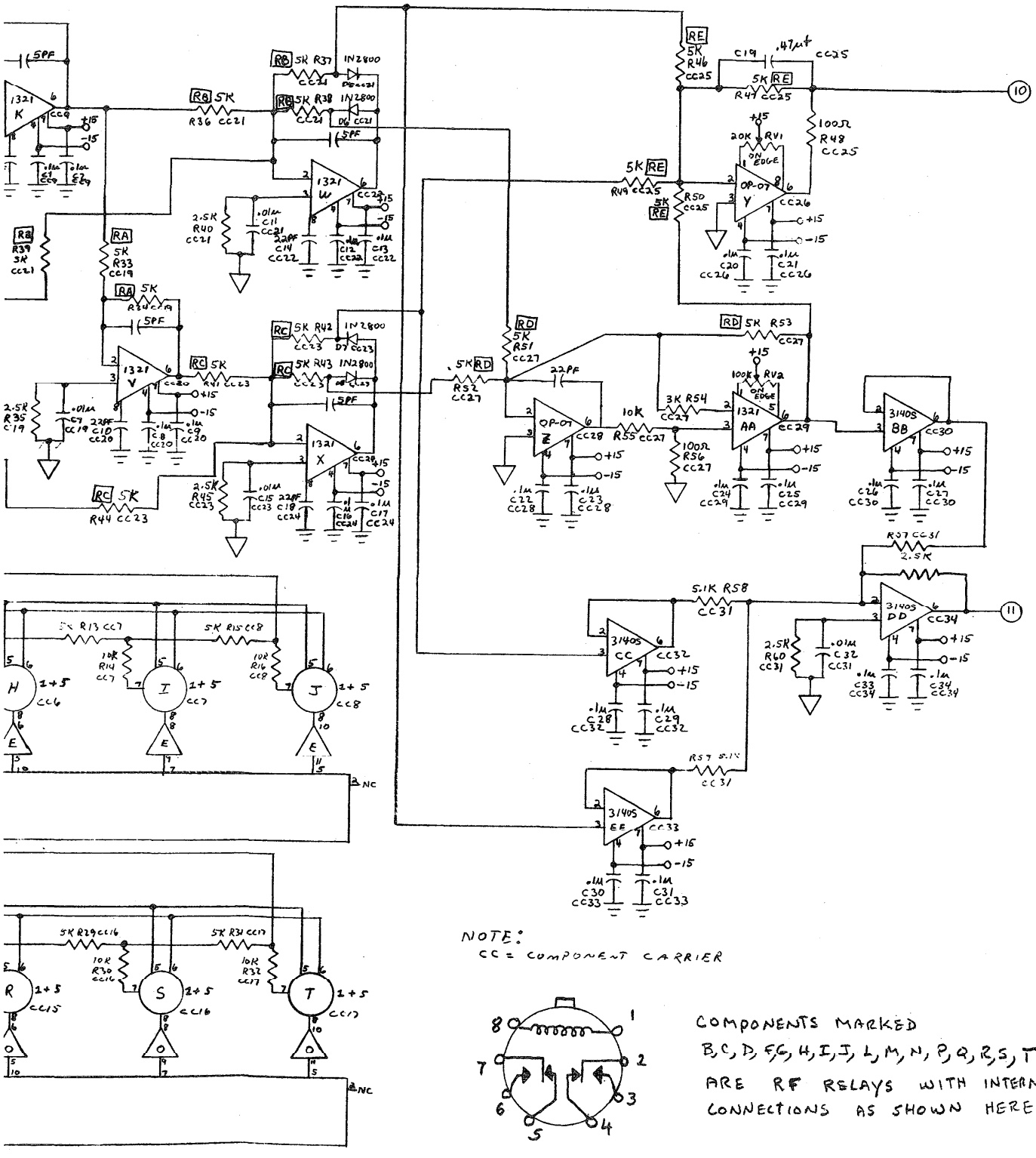


Fig. 7.25 Phase Detector Circuit Diagram A-11

Table 7.3 Amplitude and range codes

Amplitude	Range	Output Voltage
Bus* No. Bit 14--- ---- ---3 ---0 MDAC No. Bit 1--- ---- ---12 Conn.Pin No.(14):::::::::(25) (28)		
0000 1001 0001 xxx1		0.250
0101 1010 1000 xxx1		2.500
0110 0101 0100 xxx1		5.006
0000 1001 0001 xxx0		5.007
0101 1010 1000 xxx0		50.00
0110 0101 0000 xxx0		100.0

*Note: Bit numbering conventions differ between computers and DACs. With DACs, bit '1' is usually designated the most significant bit, and high numbers are assigned to less significant bits. In computer circuits, bit '0' is often the least significant bit, and more significant bits have higher numbers. Pin numbers refer to the edge connector of the board.

Bits 14 through 3 of the low-speed, 16-bit data bus (edge connector pins (14)-(25)) provide the digital settings for the equivalent bits, 1 to 12, of the multiplying digital-to-analog converter (MDAC) F, while bit 15 (edge connector pin (28)) determines the range (set by relay J). Amplitude information is latched from the bus into D and E on the positive transition of a signal at edge connector pin (31) which is generated on the Interface board D10 whenever either 'reference' or 'variable' amplitudes are changed.

The sinusoidal outputs on boards A7 (reference) and A9 (variable) are connected to BNC connectors marked "REF" and "VAR" on the rear panel of the instrument. To the right of these output connectors is a toggle switch labeled "NORMAL" and "7 VOLTS." With the switch in the 'normal' position, edge connector pins (12) on boards A7, A9, and A-11 are tied to the +5-volt dc supply. With this connection the amplitudes of the two output channels are programmable and can be set independently between 0.25 V and 100.0 V from the front panel keyboards. In the '7-volt' position, edge connector pin (12) is tied to ground, and the outputs are supplied directly from the filter circuits at 7.07 V (not programmable).

7.2.7 Phase Detector

(Refer to circuit diagram A11, figure 7.25.) The output filters, although carefully matched, cause slight differential phase shifts between channels. If the instruments were operated strictly at the 7.07 V level, these could be trimmed, and the channels would track to rated

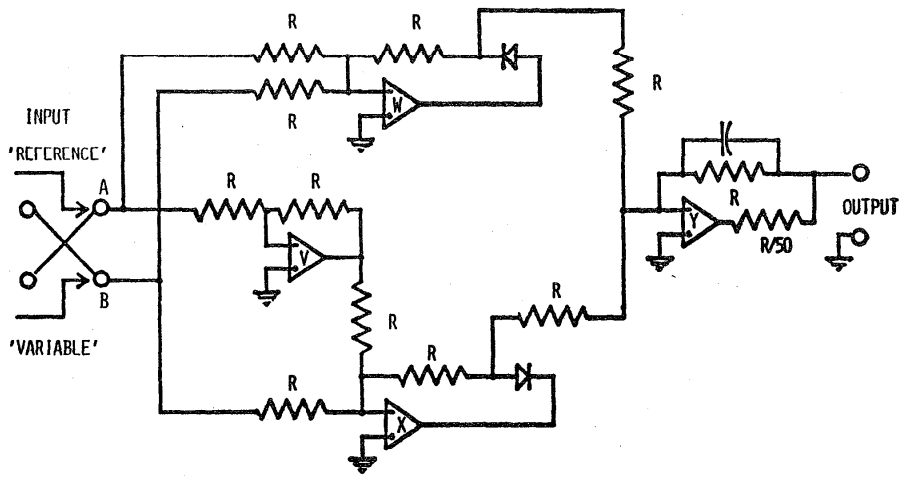


Figure 7.26 Phase Detector Circuit Schematic

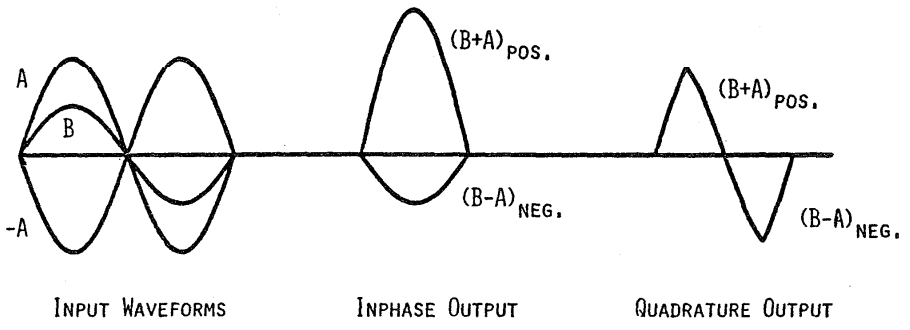


Figure 7.27 Phase Detector Waveforms

accuracy over the full frequency range. However, this type of adjustment would be useful only if long term stability of all analog filter components could be assured. Moreover, if the output amplitudes are not fixed but programmable, the tracking of the differential phase shift between channels can no longer be obtained even with ideal filter components. The phase shift of the programmable gain circuits is a function of the amplitude setting.

To overcome this problem, an 'auto-zero' function is incorporated into the Phase Angle Standard. It checks and corrects differential phase errors between the two channels by measuring the output at (nominal) quadrature. The technique used in this operation is insensitive to component drifts in the detector circuit (see also section 4.6).

Figure 7.26 shows a switching phase detector [2] which can accurately measure phase angles around 90 degrees. It is an operational amplifier implementation of the well known transformer-diode detector which charges the capacitor of an averaging circuit with the positive part of signal components A + B and the negative part of A - B (see figure 7.27). The input and output waveforms are shown in figure 7.27 for the "in-phase" condition, and the output waveform is shown also when the A and B inputs are in quadrature. The resulting voltage applied to amplifier Y is the averaged half-wave sum of these two waveforms which is related to the phase angle (θ) between sinusoidal inputs A and B by:

$$V_{ave} = V_P \frac{\cos \theta}{\pi} \qquad (1)$$

where V_P = peak value of B.

Drifts in amplifier components, which cause changes in the phase and gain of the first three stages, can be compensated by swapping the inputs and averaging the results of the measurements (see also section 4.6).

Figure 7.28 shows the response of the phase detector as a function of the phase angle between the inputs. The output crosses zero when the signals are in quadrature at which point the gain of amplifier Y is not critical.

The actual circuit used has two diodes in each operational rectifier making it full-wave and thereby insensitive to dc offsets in either waveform or stages V, W, and X. This modification requires an additional inverting-summing stage, shown as composite amplifier Z and AA in circuit diagram A-11. Amplifier Z is used to reduce dc drifts in the inverting stage AA even though the measurement procedure of inverting phase angles and swapping inputs virtually eliminates the effects of dc offsets and drifts in this stage, as well as in the output stage Y.

With the rear toggle switch in the '7 volts' position, edge connector pin (12) is tied to ground, and relays D and N apply the 'reference' and 'variable' signal (properly attenuated through K and U) to the phase detector.

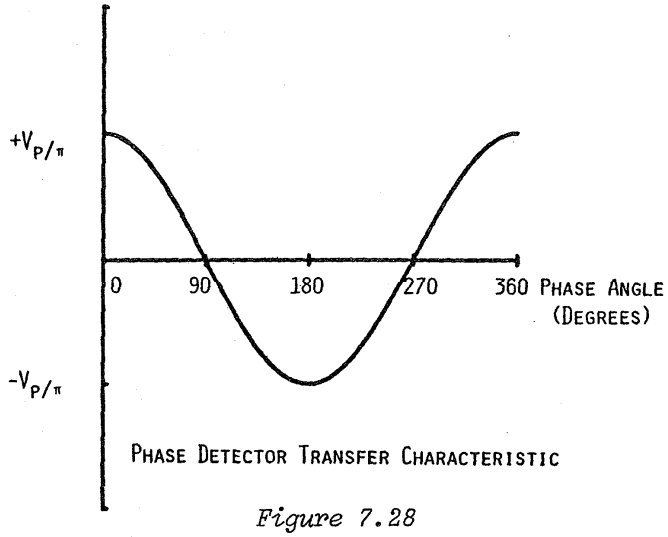


Figure 7.28

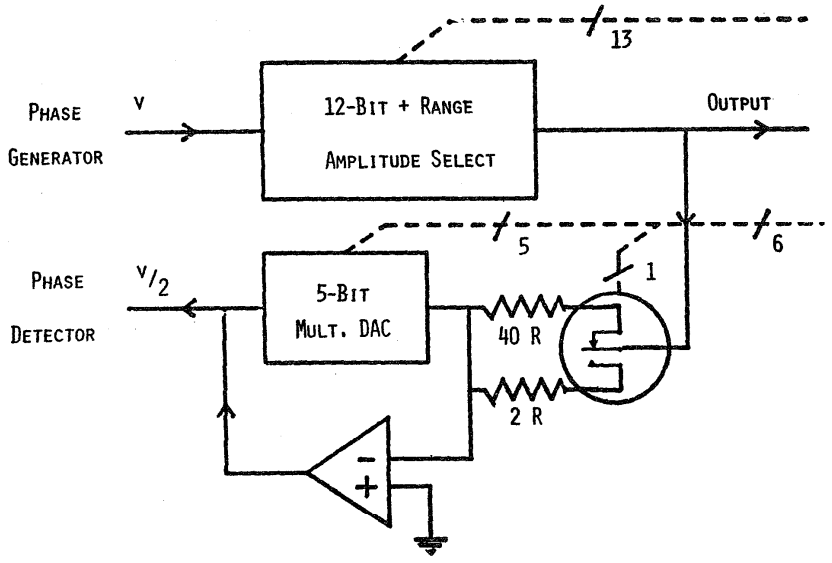


Figure 7.29 Phase Detector Scaling Stage

A sequence of measurements, described in detail in section 6.2.12, determines the correction required to bring the two signals into quadrature. The result is independent of small gain, phase, and offset drifts in any of the circuitry used to measure this correction. The procedure requires a linear scale for settings of the Phase Standard, as it can only correct for fixed differential phase shifts that are independent of phase setting.

The '7 volts' mode is a special case where both channels have equal amplitudes. In the 'normal' mode, the 'reference' and 'variable' amplitudes are independently adjustable from 0.25 V rms to 100.0 V rms, and the amplifiers operated at unequal gains often cause large differential phase shifts. While the phase detector has a dynamic range of 80 dB or more, it has a maximum voltage rating of about 3.5 V rms per channel and optimum sensitivity at this point. The 'reference' and 'variable' signals are therefore scaled appropriately with a second set of variable gain amplifiers.

Figure 7.29 shows the circuit used to provide high-resolution voltage scaling (13 bits) to the output and low-resolution scaling (5 bits) back to the phase detector for the following reasons:

(a) One of the constraints of the phase detector of figure 7.25 is that signal A must be larger than signal B. For this reason the gain of amplifier K (circuit diagram A-11) is 1.5 times the gain of amplifier U. The 5-bit gain control provides sufficient resolution to avoid violating this constraint for all output levels of the Phase Standard.

(b) The phase detector scaling stages are the parts of the instrument vulnerable to component drift - small changes in dc offset and gain will cause negligible effects, but changes in the phase of the output must be avoided. Therefore, the 5-bit multiplying digitial-to-analog converters (MDACs) are constructed of very stable discrete components with relay switching in order to minimize capacitive feed-through. Physical size of the circuitry, therefore, imposes a limitation on the number of bits that can be used for these stages.

(c) Phase shifts at different settings of these scalings are significant, but have good long-term stability; therefore, each setting can be corrected from a software look-up table. Minimizing the number of bits keeps the look-up table small and reduces the calibration time necessary to determine and check the table values.

In addition to the 5-bit MDACs shown in circuit A-11 as consisting of F, G, H, I, J, JJ (for channel A) and P, Q, R, S, T, and KK (for channel B), each channel has a 6th range bit or range switch (C on channel A, and M on channel B). These switches select either input range 0-5 V or 5-100 V. Relay B is the reversing switch controlled by a low level pulse at edge connector pins (31) (normal), and (32) (reverse). 'Normal' is defined as the 'reference' signal into the A channel (amplifier K).

The filtered analog output from the phase detector is available at a coaxial connector on the board. Amplifiers BB, CC, DD, and EE provide a buffered unfiltered version of the output at edge connector pin (11) (a signal which is used in the digitizer board described below).

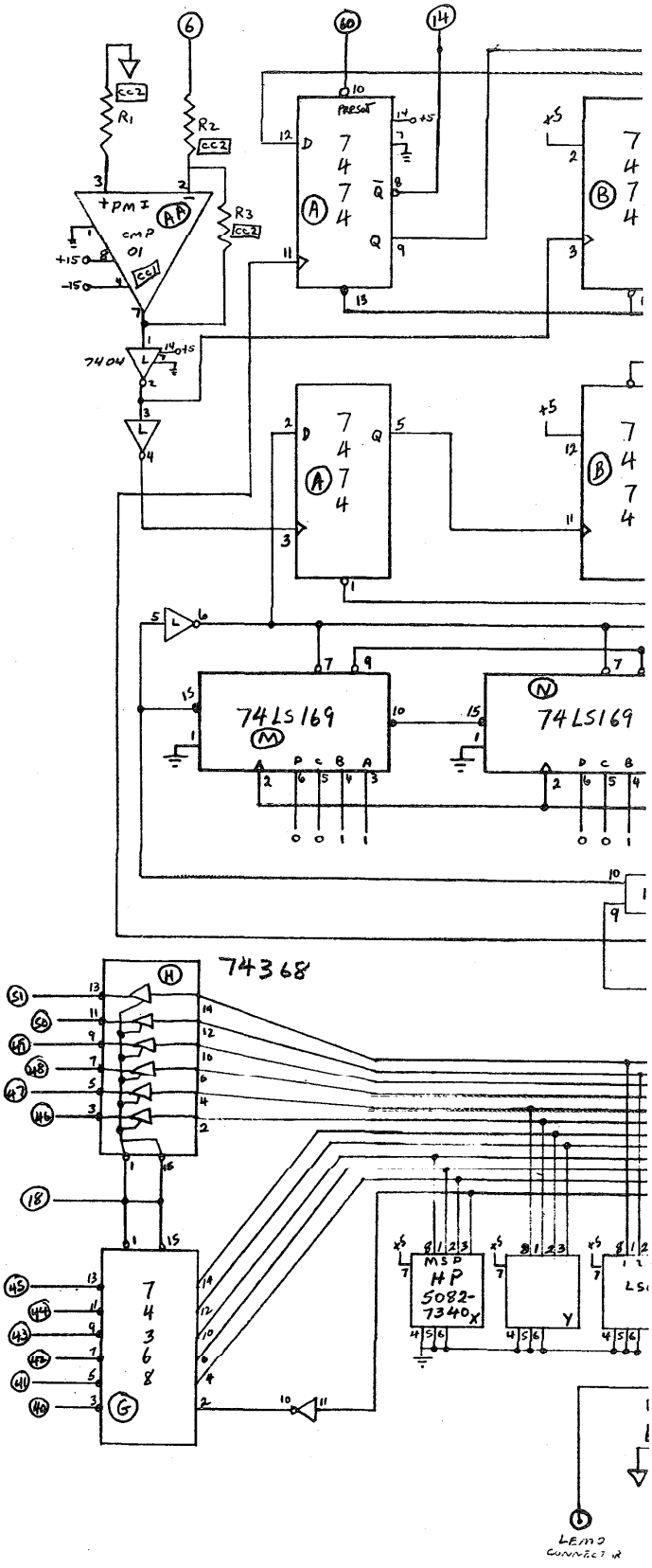
7.2.8 Digitizer (Analog-to-Digital Converter)

(Refer to circuit diagram A13, figure 7.30.) The voltage output of the phase detector is digitized to a resolution of 12 bits (1 part in 4096). The digital code is fed to the microcomputer where it is used in an 'auto-zero' correction loop to eliminate differential phase shifts between the output channels. A difficulty arises in making the analog-to-digital conversion, because the output of the phase detector must average signals with frequencies ranging from 5 kHz down to 1 Hz. At quadrature, the ripple of the signal entering the averager is greater than the peak-to-peak of either input signal. This ripple must be reduced by approximately 80 dB for it to cause negligible effects in a 12-bit conversion. At low frequencies this ripple rejection requires unreasonably long time constants. Therefore, a digitizing method was devised that takes advantage of the fact that, for approximately equal amplitudes A and B, the output ripple, for small angles around 90 degrees is symmetrical.

A fixed conversion time, T, can be used for any frequency by dividin T into two equal conversion times I and II, as shown in figure 7.31. Conversion is accomplished by feeding the scaled and filtered phase detector output into a voltage-to-frequency (V/F) converter. Upon receipt of a 'convert' command from the microprocessor, the counter (figure 7.32) is cleared and the slope detector is armed. The first positive going zero crossing of the input ripple initiates a timer which enables the counter to accumulate the output of the V/F converter for a period of T/2. The count is held until the slope detector recognizes the next negative going zero crossing and enables the counter for a second period of T/2. The V/F converter is offset so that zero input produces a 50-kHz output, providing a bipolar response (able to respond to both positive and negative phase detector outputs). The counter reading is thus proportional to the average value (the shaded areas of figure 7.31 cancel).

Table 7.4 Voltage-to-frequency converter code

V/F Input Voltage	Approx. Angle	Two's Complement Binary Output	V/F Frequency	Conversion Period T
-5	88.6	1000 0000 0000	0 Hz	
0	90.0	0000 0000 0000	50 kHz	40.96 ms
+5	91.4	0111 1111 1111	100 kHz	


74368
74LS169
74LS169
MSP
HP
5082-
7340X
LEMO
CONNECTOR

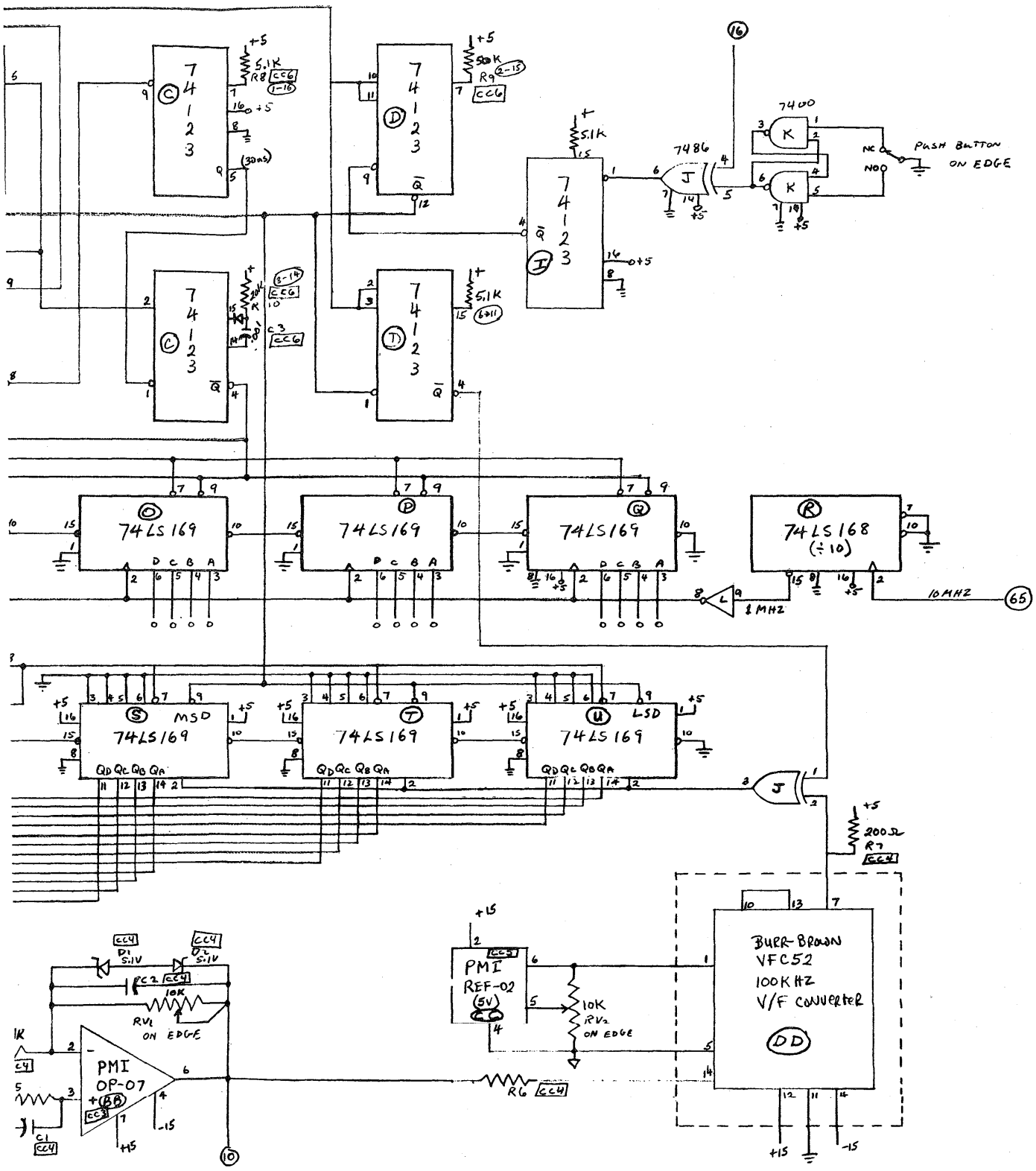


Fig. 7.30 Digitizer Circuit Diagram A13

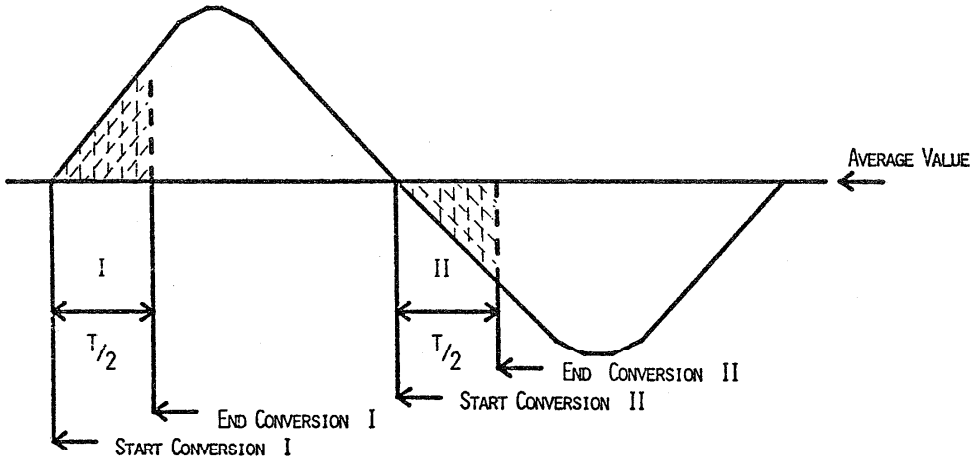


Figure 7.31 Digital Input Ripple

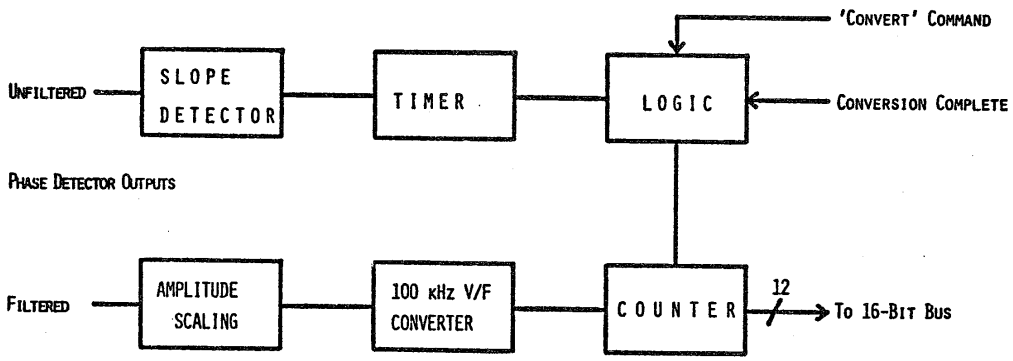


Figure 7.32 Circuit Diagram D-11

It takes 40.96 milliseconds for a 50 kHz signal to accumulate 2^{11} (binary 1000 0000 0000) counts. By setting T=40.96 ms and inverting the most significant bit of the counter output, the measured angle can be scaled to two's complement binary notation. Amplitude scaling is adjusted (see table 7.4) to provide a 1.4 degree range with 1 LSB=0.0007 degrees.

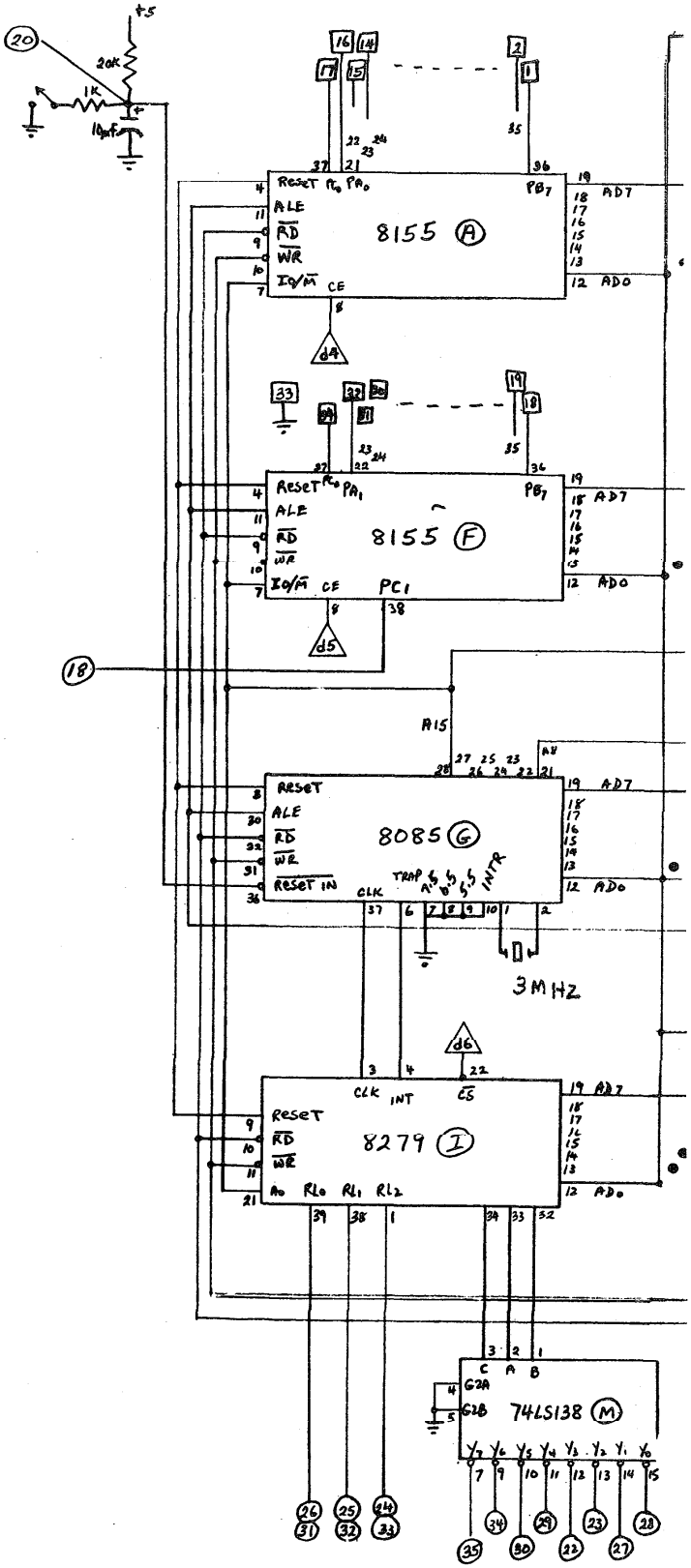
Referring to the circuit diagram A13, the 'convert' command is a low level at edge connector pin (16). This produces pulses at one-shots I, C, and D which initialize timer (M, N, O, P, Q), the counter (S, T, U), and the slope detection circuitry (A, B). The unfiltered phase detector output is applied to edge connector pin (6) where it is converted to a square wave by comparator AA. The filtered phase detector output enters the board through a coaxial connector and is scaled by amplifier BB before it is applied to the V/F converter DD. CC provides the 5-volt offset necessary to make DD bipolar. X, Y, and Z display the counter readings, while G and H provide tri-state buffering for the low-speed, 16-bit data bus. The 'conversion complete' line, edge connector pin (14), is pulled low by the 'convert' command and restored high at the end of the second timing period, II, when the count is complete. Because of the handshake between the microcomputer and the system, once a conversion has started, the digitizer can hang up the system, if the clock (edge connector pin (65)) or the ripple signal (edge connector pir (6)) are removed. A 'low' at edge connector pin (60) resets the digitizer and restores control to the processor (see also section 6.2.10).

As mentioned earlier, this digitizing technique was devised to handle large ripple at low frequencies during the 'auto-zero' loop. It was subsequently discovered that the phase offsets are sufficiently linear with frequency that corrections can be determined by making measurements at only one frequency and calculating corrections for all oth frequencies. To provide high resolution and simple binary manipulation the 'auto-zero' is performed at 4096 Hz, and corrections are scaled for other frequencies. Digitizing at 4096 Hz does not pose serious ripple problems and could probably be satisfactorily accomplished with a commercial 12-bit analog-to-digital converter. It is planned, however, to use this system to calibrate power factor meters and wattmeters (particularly at zero power factor) where one channel will provide voltages up to 240 V rms and the other channel will supply currents up to 10 ampere This capability will require phase angle sensing at the output of auxiliary power amplifiers, and the 'auto-zero' loop will have to operate at frequencies as low as 50 Hz where the gated V/F conversion technique described will be needed.

7.3 Control Circuits

7.3.1 8085 Microprocessor (Microcomputer)

(Refer to circuit diagram D11, figure 7.33.) An 8-bit NMOS microprocessor is used for general control of the system and for the keyboard/display interface. It communicates with the rest of the syst through the 'Interface Unit' D10 (described in section 7.3.2).


+5
20
20K
1K
10μf
8155 (A)
8155 (F)
8085 (G)
8279 (I)
74LS138 (M)
RESET
ALE
RD
WR
IO/M
CE
PC1
RESET IN
CLK
INT
CS
TRAP
INTR
A15
AD7
AD0
3MHz
d4
d5
d6
18
26
25
24
31
32
33
35
34
30
29
23
27
28

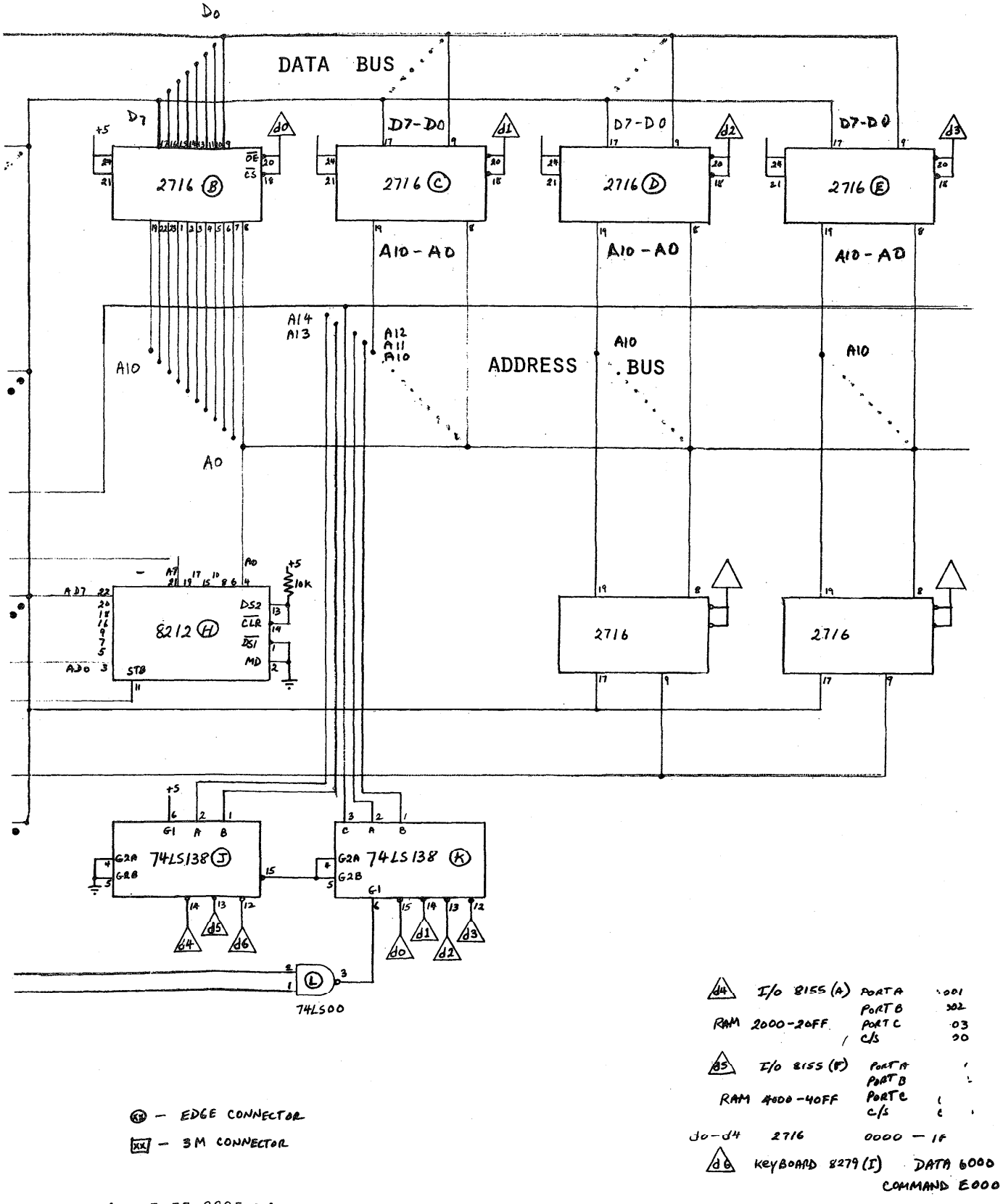


Fig. 7.33 8085 Microcomputer Circuit Dia. D-11

Communication with the front panel keyboard is made through a special purpose interface integrated circuit, I, which sends strobe signals out on the edge connector pins (24)-(26) (number keyboard) and (31)-(33) (function keyboard). The strobed signals are returned on the remaining pins between (22) and (35) where they are encoded in M and fed to I. Keyboard information is sent to the microprocessor G along the data bus. An interrupt line (TRAP) between I and G alerts the processor that a key has been depressed. The 'reset' key has been isolated from the rest of the keyboard circuitry such that it pulls edge connector pin (20) to ground when depressed. This provides the necessary (hardware) reset pulse to G and causes the control software to be re-initialized.

Communication with the interface board, D10, is made through input/output ports on A and F. Data is sent out in 16-bit words on "3M" connector pins (1)-(16). Pin (17) provides a handshaking 'set control' line. Data are brought to the processor from the Interface Unit (15 bit lines) on pins (18)-(32). Pin (33) is the system common and pin (34) is the return handshake line to acknowledge the 'set control' with a 'flag.'

Latch H demultiplexes the data bus, in a standard 8085 configuration, to provide 16 address lines for the erasable, programmable read-only memory (EPROM) B, C, D, and E. J and K decode the address bus to provide chip-enables for the marked chips. In addition to input/output capability, A and F are random-access memories for short-term storage and calculation scratch pad.

7.3.2 Interface Unit

(Refer to circuit diagram D10, figure 7.34.) The system-microcomputer was designed to be substantially independent of the particular type of microprocessor used. The interface communicates with the microcomputer via a 34-line flat cable as outlined in section 7.3.1. Data generated by either the microcomputer or the rest of the system must be separated and decoded at the interface board for transmission on the high-speed, 20-bit bus or transmission on the low-speed, 16-bit data bus (see also section 6.1.3). When a 16-bit word appears at the interface board, the eight MSBs ("3M" connector** pins (1)-(8) are buffered through H as ground-true data; the eight LSBs (pins** (9)-(16)) are buffered through I for decoding in K and J. Table 7.3 outlines the data sent by the microprocessor and their respective destination codes. Depending on the code contained in the eight LSBs, the data in the eight MSBs is latched in either A, B, C, D, or E by the handshake output line 'SC' ('set control' on "3M"** pin (17)).

(a) Data transfer to the 20-bit bus: As described in section 6.1.3, three types of data items are transferred from the 8085 microcomputer

** The "3M" connector pins are indicated on the circuit diagrams by a rectangle, while edge connector pins are circled.

to the high-speed processor via the 20-bit bus. To initiate such a transfer, a bus priority request signal is generated by the Interface Unit by decoding one of the following Interface (instruction) codes (see table 6.1):

10110 Angular Increment Ready	('IR')	'Ready' signals from ALU board
10111 Phase Angle Ready	('PR')	
11000 Offset Angle Ready	('OR')	

'IR,' for example, is latched to the line leading to edge connector pin (19) on the next 'set control' command ('SC'). When the priority circuit on the Angle Computation board (see section 7.2.2) is ready to accept a new 'increment,' a 'low' is sent back through the edge connector pin (58) which enables the tri-state outputs of the 20-bit bus and resets the ready signal flip-flop. Contents of the bus are latched into the Angle Computation board by 'GW' as described in section 7.2.2.

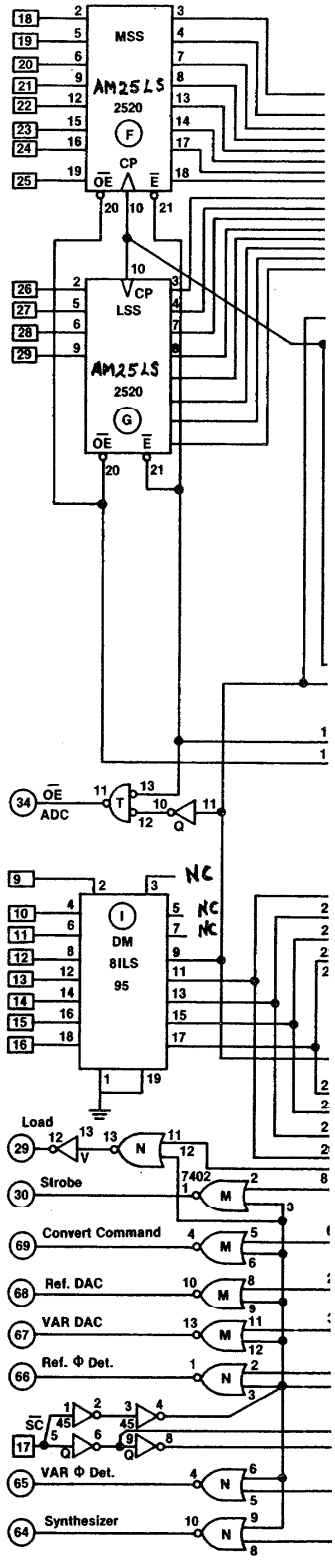
(b) Data transfer to the 16-bit bus is similar in operation to the 20-bit bus, except that it is bidirectional with respect to the interface unit, and the data are positive true instead of ground true (inverted in P and Q). Tri-state latches A and B are enabled whenever "3M" connector pin (12) is low (first 16 codes on table 6.1), allowing data to be transferred to either the MDACs, phase detector, synthesizer, or display. The 16-bit bus is loaded from the microcomputer using Interface Codes (see table 6.1) 10001 and 10010, and information is read off the bus for transmission to the microcomputer with codes 11001 and 11010.

Handshaking between the microcomputer and the interface is carried out through the 'set control' signal, 'SC' ("3M" pin (17)), which is sent from the computer each time new data enters the interface, and the 'flag' ("3M" pin (34)), which is sent back to the computer once the data has been received. For most instructions, the 'flag' is simply delayed for 10 microseconds, however, there are four instructions that can hold up the 'flag.' The three 20-bit bus operations, 'phase,' 'increment,' and 'offset' hold the 'flag' until the data are written into the high-speed register-file (see section 7.2.2). During the 'auto-zero' mode, the 'flag' is also held while the digitizer converts the detector output (see section 7.2.8).

Finally, timer circuit, Y, acts as a pulse stretcher to lengthen the pulse generated by decoding '01111' which activates the buzzer. The pulse has to be lengthened to make the buzzer audible.

7.3.3 Keyboard and Display

The operator can communicate with the 8085 microcomputer through two 12-button matrix keyboards mounted on the front panel (see figures 7.35 and 7.36). The keyboards are connected with a flexible, flat cable to the keyboard/display interface board (in slot number 4 of the upper card cage), which then connects to the microcomputer via the backplane. Details of the interface connection are shown on the backplane wiring


MSS
AM25LS
2520
F
CP
OE
E
LSS
AM25LS
2520
G
ADC
DM
8ILS
95
NC
Load
Strobe
Convert Command
Ref. DAC
VAR DAC
Ref. Φ Det.
VAR Φ Det.
Synthesizer
7402

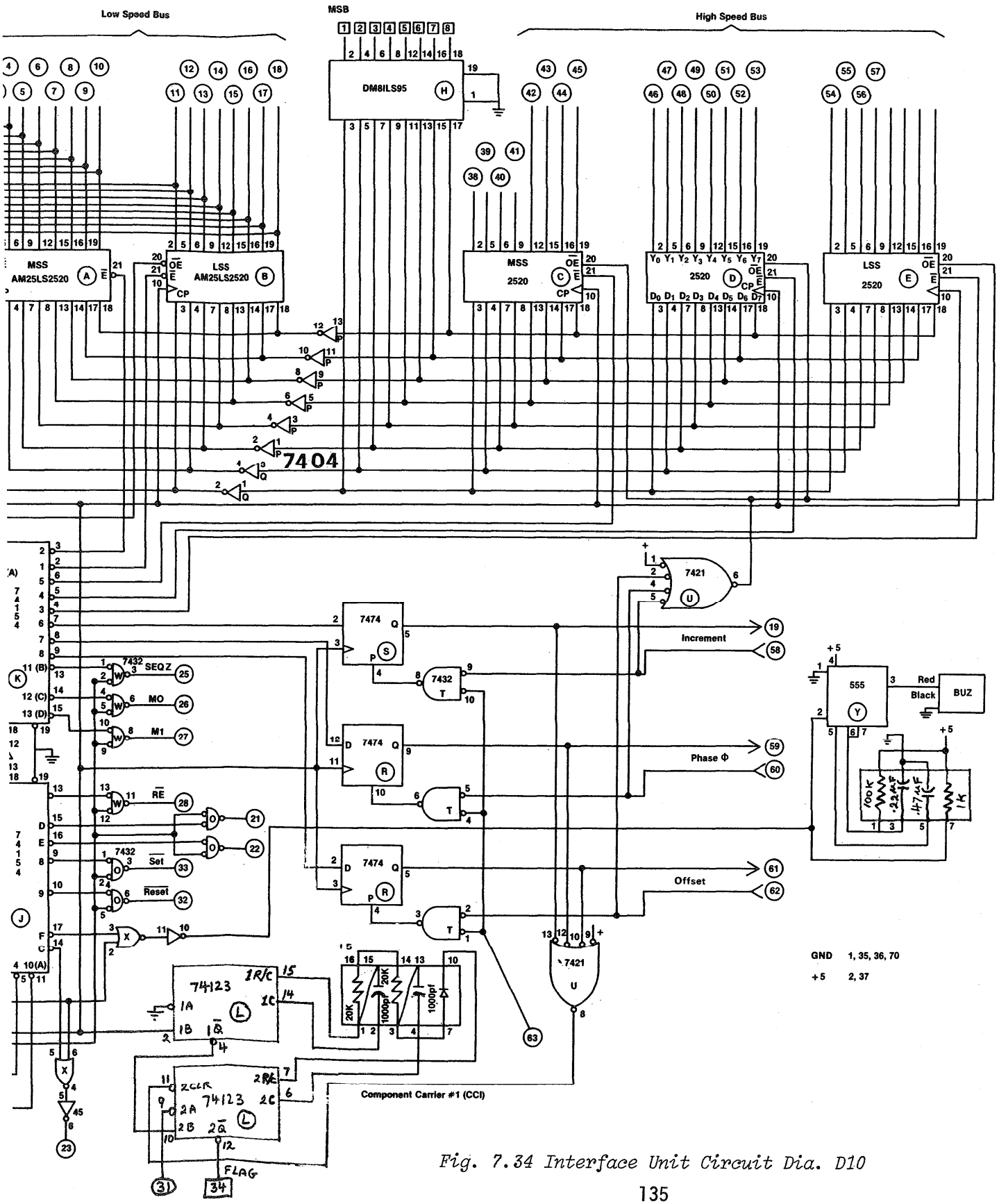


Fig. 7.34 Interface Unit Circuit Dia. D10

diagram for board A4 (figure 7.4). The connector labels in figures 7.35 and 7.36 correspond with those on the left-hand side of figure 7.4. Depressing a key makes a momentary contact between the vertical and horizontal connections shown in figures 7.35 and 7.36.

The display contains 32 alpha-numeric characters arranged in two 16-character lines. It has on-board latches and address lines allowing any part of the display to be updated by the 16-bit, low-speed bus using the 'load' and 'strobe' control lines. Connection to the keyboard/display interface is made by a flexible cable. Details of pin connections are shown on the right-hand side of figure 7.4. Note that the display connector ("IEE") has a different numbering scheme than the cable connector ("3M") which plugs into it.

8. FUNCTIONAL TESTS

8.1 Preliminary Tests

These tests are designed to provide a quick check of the overall performance of the Phase Standard. They will uncover possible gross malfunction rather than calibration errors. The listing is in order of increasing complexity.

8.1.1 Visual Check of Normal Output With Oscilloscope

(a) Turning on the Phase Standard and connecting a dual-trace oscilloscope to the 'variable' and 'reference' phase outputs provides a visual indication of the waveform. The oscilloscope 'sync.' control should be adjusted so that the reference sinewave crosses the zero axis with a positive slope near the left-hand edge of the screen. The 'reference' output can be identified by changing the 'reference' amplitude (channel "0") to 2 volts from its default setting of 1 volt.

Two sinusoidal waveforms with a frequency of 500 Hz should now be displayed. Since the phase angle is initially set to 60 degrees, the 'variable' phase output should have about 7/8 of its positive peak amplitude at the point where the 'reference' waveform crosses the zero axis with a positive slope. By setting the phase angle successively to 90, 270, and 180 degrees, a positive peak, negative peak, and zero (out of phase) amplitude should be obtained at the same point.

(b) This part of the test is designed to check the transition from low to high, and high to low range of the output amplifiers. For this purpose, both amplitudes are first adjusted to 5.000 volts with a phase angle of 60 degrees. The waveforms are then observed on the oscilloscope while first one, then the other amplitude is set to 5.010 volts and back down to 5.000 volts. If the (software) range offset is operating properly, the relative phase angle should remain unchanged irrespective of the amplitude settings in either channel.

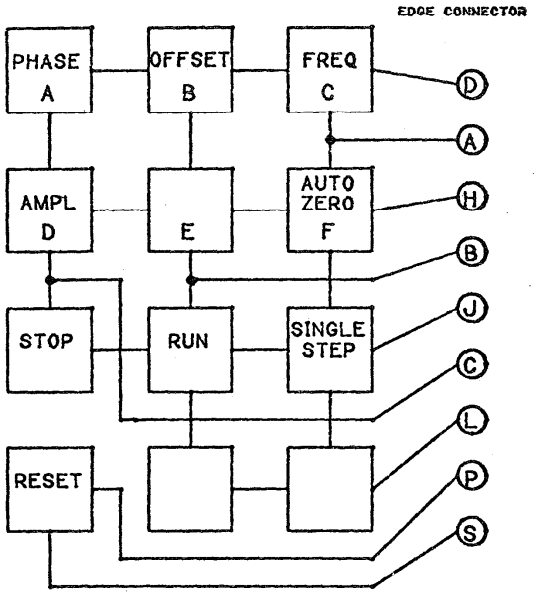


Figure 7.35 Function Keyboard

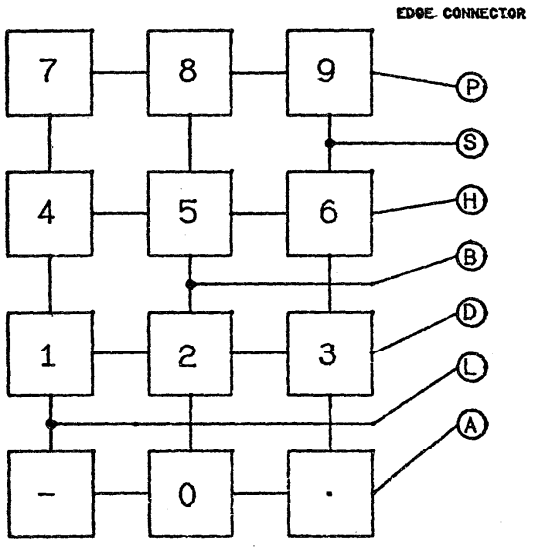


Figure 7.36 Number Keyboard

(c) The Phase Standard output frequency can be checked with a frequency meter or an oscilloscope. Frequencies should be correct to within 0.005 percent.

8.1.2 Waveform Integrity

A gross malfunction of the system can be detected by observing the unfiltered waveform. This can be accomplished without physically removing the filter circuits by slowing down the sampling clock by a factor of 100 (two switch positions in a counter-clockwise direction of the switch on circuit board D3). The slowed down sampling rate shifts the sampling frequency into the pass band of the filter, so that the unfiltered, stepped sinewave can be displayed. This waveform can best be observed by setting the Phase Standard output to "5000" Hz. With this setting, there are only 64 steps per wave, and they can be seen easily. At lower frequency settings, where the number of steps is larger, visual observation is more difficult.

Each 64-step wave is composed of only a small subset of possible output levels of the digital-to-analog converter. By varying the 'phase' and 'offset' settings, different subsets of output levels can be checked. The settings should therefore be changed to several phase angles during this test. Errors in the eight most significant bits can thus be detected and while the tests, in practice, cannot be exhaustive, observable malfunctions are usually detected after a few tries.

The following defects should be looked for:

Missing steps,
steps going to the zero axis,
steps going to full-scale values,
steps changing intermittently.

These types of errors may be due to shorted lines or incorrect timing adjustment of the output latches.

8.1.3 Waveform Analysis

A more careful analysis of the waveshape can be carried out with a wave analyzer or spectrum analyzer. However, the spectral purity of the Phase Standard is such that the dynamic range of most commercial analyzers is not sufficient to detect the harmonic levels without a notch filter to suppress the fundamental. The notch filter should provide at least 30 dB attenuation at the fundamental, and preferably not more than 5 dB at the 2nd harmonic while introducing negligible additional distortion.

The values of the harmonics to be expected is a function of the frequency setting of the Phase Standard and may also vary slightly from one channel to the other. The harmonic content is likely to be highest at frequencies above 3124 Hz, and lowest at the low end of the frequency

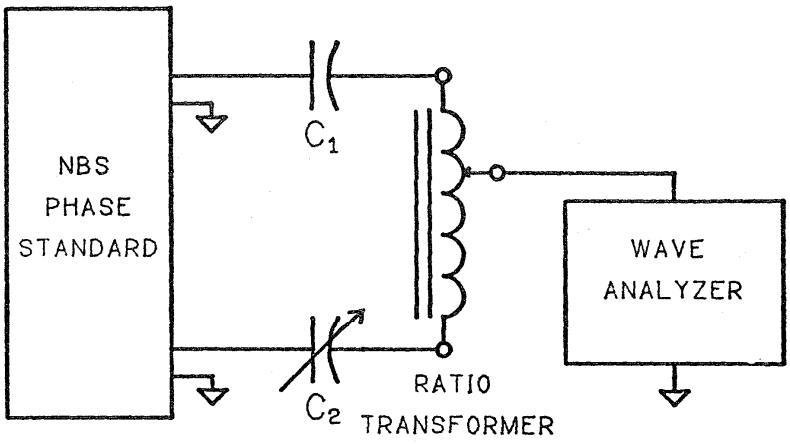


Figure 8.1 Test Circuit

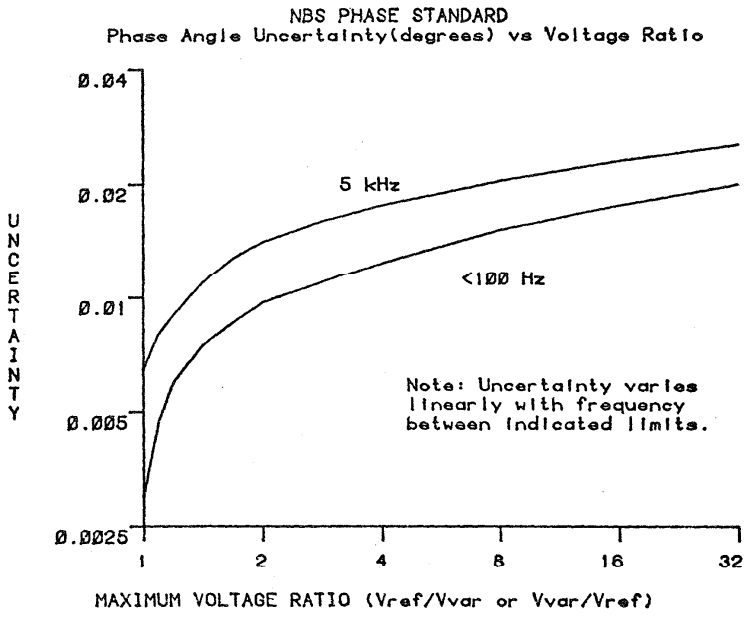


Figure 8.2

range. Typical values of harmonics measured at 500 Hz are shown in table 8.1.

Table 8.1 Harmonic content

Order of Harmonic	Percentage Amplitude (Relative to Fundamental)
1st	100
2nd	0.0056
3rd	0.0011
4th	0.0017
5th	0.0006
...	...
63rd (harmonics due to the sampling process)	----
65th	----

8.2 Accuracy Check

8.2.1 Method for Accuracy Verification

The uncertainty in the accuracy of the Phase Standard has two main components. One is due to deviations from linearity of the angular scale, the other is the result of imprecision in the operation of the auto-zero compensation. The small departure from linearity is inherent in the system design and is not likely to change with time as long as all components are operating properly. The feedback action of the auto-zero compensation can be affected by random disturbances, and may therefore contribute to time dependent drifts. These changes will be small, but are measurable and should be checked at suitable calibration intervals.

The method used to check the accuracy will provide a fixed point on the angular scale, relating the angle displayed on the readout to the actual phase difference of the two output signals. The choice of the point on the scale is arbitrary, and from a theoretical point of view any selected value will do. Experimentally, the 180 degree point is most convenient, and is the one chosen for this test. It has the further advantage, of providing an independent check of the auto-zero correction, since the 180 degree bridge method and the quadrature detector used by the auto-zero procedure are based on different principles.

A diagram of the measuring circuit is shown in figure 8.2. The setup requires a tuned detector (e.g., wave analyzer) with a minimum

full-scale sensitivity of 300 microvolts and a frequency range that includes 4096 Hz. A ratio transformer (inductive divider) with a minimum resolution of 0.00001 and designed for 5 kHz operation is also required. The two capacitors marked C1 and C2 on the diagram should be of good quality (low loss) and at least one of them, but preferably both, should be adjustable to a maximum capacitance of at least 10 or 20 microfarads. None of these components need to be calibrated precisely, though large errors could lead to difficulties in the measurement. The function of the capacitors is to block any direct current from flowing through the inductive divider and thereby saturating its core. The capacitors will introduce undesirable phase shifts, however, and have to be adjusted to make the resultant phase error negligible.

The 'reference' and 'variable' output from the Phase Standard are connected to opposite ends of the inductive divider, and the detector is connected to the adjustable terminal. The divider is therefore floating and its case should be grounded. When the bridge is balanced, the adjustable divider terminal is at, or near, ground, so that each half of the circuit can be considered to be a series R L C circuit connected across one of the outputs of the Phase Standard.

In general, for an R L C circuit, the current will be shifted with respect to the applied voltage by a phase angle 'ϕ' given by

$$\tan \phi = \frac{\omega L}{R} - \frac{1}{\omega RC} \qquad (2)$$

Since the inductance and resistance of part of the divider are proportional to the ratio setting 'α,' we get for equal phase shifts in the two parts of the divider

$$\tan \phi = \frac{\omega L\alpha}{R\alpha} - \frac{1}{\omega R\alpha C_1} \qquad (3)$$

$$= \frac{\omega L(1-\alpha)}{R(1-\alpha)} - \frac{1}{\omega R(1-\alpha)C_2}$$

from this it follows that

$$\frac{C_1}{C_2} = \frac{1-\alpha}{\alpha} \qquad (4)$$

which means that the capacitors have to be adjusted to the inverse ratio of the inductive divider. With typical values for the inductance and effective resistance of a ratio transformer (75 microhenries, 400 kilohms), a 10-microfarad capacitance will produce a phase shift of the order of

5 millidegrees. A 20-microfarad capacitor will come close to resonance conditions where the phase shift is theoretically zero.

8.2.2 Experimental Procedure

The bridge circuit is connected as described above, except that the detector is temporarily disconnected. The outputs of the Phase Standard are then adjusted to the desired voltage levels, and the frequency is set to 4096 Hz. The inductive divider is set to the approximate ratio of the output amplitudes, and the capacitors are adjusted to the approximate inverse ratio.

Next, the AUTO-ZERO key is depressed, and, at the conclusion of this auto-zero action, the readout indicates a phase angle of 0.000 degrees. The 'phase' is then set to 180.000 degrees and the 'offset' to 0.000 degrees. The detector is then connected to the inductive divider and tuned so that it is in phase-lock at the frequency of 4096 Hz. The inductive divider is then adjusted for a minimum reading on the detector. Using the 'offset' adjustment on the Phase Standard and entering positive or negative angular corrections, the bridge is balanced until a minimum reading is obtained. In some cases adjacent millidegree steps will result in the same reading; this is a consequence of the rounding necessary in the conversion from decimal to binary angles inside the Phase Standard. If the angular correction is large, readjustment of the inductive divider may also be necessary. The number displayed as 'offset' on the readout is the deviation of the Phase Standard output from the 180-degree phase angle determined by the bridge.

The 'offset' reading obtained is a function of the voltage ratio of the two output signals. Offsets should be smallest, though probably not zero, for equal amplitudes and are likely to be largest for large ratios. Typical values are shown in figure 8.3.

8.3 Digital-to-Analog Converter (DAC) Tests

8.3.1 Converter Adjustments

The 16-bit digital-to-analog converters used to generate the waveform each have 5 trimmable parameters which should be checked periodically (once or twice a year) to ensure waveform purity and amplitude accuracy. This can be accomplished by the calibration procedure outlined below:

1. With the power off, place the DAC boards (A7 and A9) on extender cards, set the rear panel toggle switch to '7V,' and turn the power on.

2. Push 'RESET' to clear the auto-zero correction register.

3. Push 'STOP' and enter "A0" through the keyboard.

4. Push 'RUN' (This initializes the program starting at PROM address A0; see section 5.4.2.)

5. Connect a dc voltmeter (10 microvolt resolution) to the 'reference' output.

6. Push 'OFFSET' and enter "360.000." Adjust variable resistor P1 (board A7) so that the output reads +10.00000 V. Fine adjustment is available at P3, if necessary.

7. Push 'OFFSET' and enter "-270.001." This turns on all the non-adjustable bits in the DAC (0 to 12). Adjust P2 (board A7) so that the output is +7.50031 V.

8. Push 'OFFSET' and enter "-270.000." This turns off all the non-adjustable bits and turns on bit 13. The output should now read +7.50031 V - 0.00031 V (1 LSB) = 7.50000 V. Adjust DAC trimmer T13 (board A7), if necessary.

9. Push 'OFFSET' and enter "-180.001." This turns on bits 0 to 13. Adjust P2 (board A7) for a reading of 5.00031 V.

10. Push 'OFFSET' and enter "-180.000." This turns on bit 14 and turns all others off. Adjust T14 (board A7) for a reading of 5.00000 V.

11. Push 'OFFSET' and enter "-0.001." This turns on bits 0 to 14. Adjust P2 (board A7) for a reading of +0.00031 V.

12. Push 'OFFSET' and enter "0.000." This turns on bit 15 and all others off. Adjust T15 for a reading of 0.00000 V.

13. Push 'OFFSET' and enter "+359.999." This turns on all bits except the sign bit (+full scale). Adjust P2 (board A7) for a reading of -9.99969 V.

14. Repeat steps 6 through 13 to check for drifts that may have occurred during the calibration.

15. Connect the voltmeter to the 'variable' output, and repeat steps 6 to 14 using the 'PHASE' instead of the 'OFFSET' button, and make adjustments on the 'variable' DAC board A9.

Adjustable resistors P1 (dc offset adjust) and P2 (gain adjust) determine amplitude accuracy, while trimmers T13, T14, and T15 determine the bit weights which affect linearity and waveform distortion.

8.3.2 Output Amplifier Adjustment

In the 'normal' mode the amplitudes are independently adjustable in two ranges. Each range has a different output amplifier and dc offset trimmer. The following outlines the trimming procedure:

1. With the voltmeter connected to the 'variable' output, switch rear panel toggle switch to 'normal.'

2. Initialize PROM program 'A0,' if it is not already running (see steps 2 to 4 in section 8.3.1).

3. Push 'PHASE' and enter "0.000" through the keyboard.

4. Push 'AMP' and then "1," and enter "5.000."

5. Adjust P4 (board A9) for a reading of 0.0000 V.

6. Push 'AMP' and then "1," and enter "100.0."

7. Adjust P5 (board A9) for a reading of 0.0000 V.

8. Push 'AMP' and then "0," and enter "5.000."

9. Push 'AMP' and then "0," and enter "100.0."

10. Connect voltmeter to 'reference' output.

11. Push 'OFFSET' and enter "0.000."

12. Adjust P4 (board A7) for a reading of 0.00000 V.

13. Disconnect voltmeter.

14. Push 'AMP' and then "0," and enter "100.0."

15. Push 'AMP' and then "1," and enter "100.0."

16. Reconnect voltmeter.

17. Adjust P5 (board A7) for a reading of 0.0000 V.

18. Turn power off and replace boards.

9. REFERENCES

[1] Turgel, R. S. and Oldham, N. M. "High-Precision Audio-Frequency Phase Calibration Standard" IEEE Transactions on Instrumentation and Measurement," Vol. IM-27, No. 4, pp. 460-464, December 1978.

[2] Marzetta, L. A. "A High Performance Phase-Sensitive Detector" IEEE Transactions on Instrumentation and Measurement, Vol. IM-20, No. 3, pp. 296-301, November 1971.

[3] 8085 Microcomputer Systems User's Manual, MCS 85, Intel Corporation, March 1977.

APPENDIX

List of Special Components

In order to adequately describe the systems discussed in this report, commercial equipment and parts are identified by manufacturer's name and model number. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

Frequency Synthesizer
Model SM-101, Syntest Corporation

Digital Translator, Binary Angle to Four Quadrant SIN & COS
Model DD208/209, Interface Engineering, Inc.

Digital-to-Analog Converter
Model DAC-HR-16B, Datel Systems, Inc.

Alpha-Numeric Display Sub-System
Model MAX132 3100-02-032N
filter Model MAX132 24505-01
(IEEE. ARGUS) Industrial Electronic Engineers, Inc.

OP Amp
Model 1321, Teledyne Philbrick

Ultra-Low Offset OP Amp
Model OP-07, Precision Monolithics, Inc.

High Voltage OP Amp
Model 3584 JM, Burr Brown Research Corporation

Precision Resistors
Style S102 1%, Vishay Resistor Products

Adjustable Delay Line
Model PTTLDL-7-1, Engineered Components Company

Monolithic Multiplying DAC (12 Bits)
Model AD 7541, Analog Devices, Inc.

Voltage-To-Frequency Converter
Model VCF52BP, Burr Brown

Relay
Model 722-5, Teledyne

Buzzer
Model MMB-01, Star Micronics, Inc.