## **Material Requirements For 3D IC and Packaging**

**Presented by: W. R. Bottoms** 

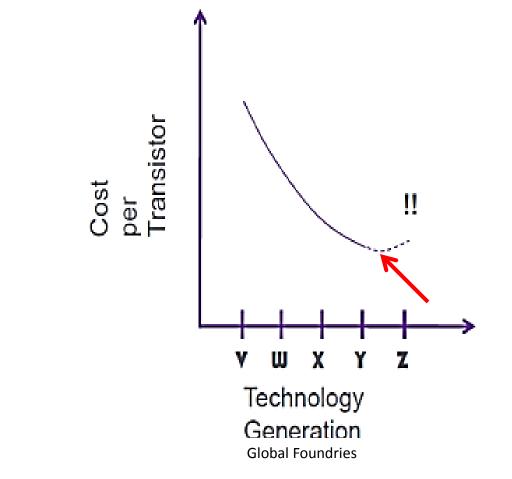
Frontiers of Characterization and Metrology for Nanoelectronics Hilton Dresden April 14-16, 2015

## **Industry Needs Are Changing**

✓ Moore's Law is reaching limits of the physics

- Scaling can no longer support the pace of progress
- Power requirement and performance no longer scale with feature size
- Electronics Industry Drivers have changed
  - Mobile wireless devices, IoT and the Cloud are driving future demand
- Electronics are entering every aspect of our lives
  - Each area has unique requirements

### **Moore's Law Scaling Is Nearing Its End**



# You know it's really "the End" When scaling to the next node increases cost

Frontiers of Characterization & Metrology for Nanoelectronics

### **Moore's Law Scaling Is Nearing Its End**

stor

## Scaling Can help but it cannot be a major component of the solution to these challenges

Y W X I Z

Technology Generation Global Foundries

# You know it's really "the End" When scaling to the next node increases cost

Frontiers of Characterization & Metrology for Nanoelectronics

## New Technology Drivers Are Emerging

Frontiers of Characterization & Metrology for Nanoelectronics

## **Emerging Technology Drivers**

There are 2 market driven trends forcing more fundamental change on the industry as they move into position as the new technology Drivers.

#### ✓ Rise of the Internet of Things

✓ Data, logic and applications moving to the Cloud

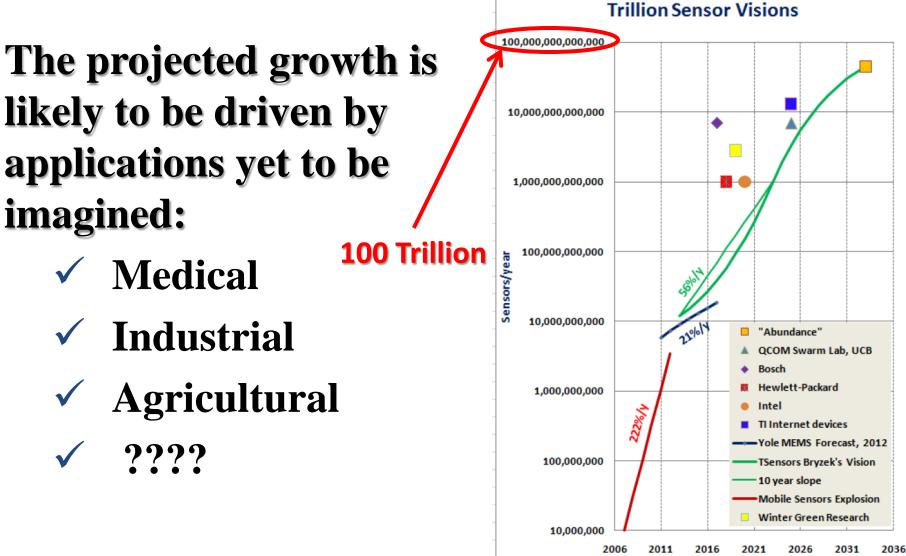
Over the next 15 years almost everything will change including the global network architecture and all the components incorporated in it or attached to it.

## **The Internet of Everything** Driven by Human Communication and Machines



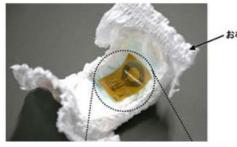
Frontiers of Characterization & Metrology for Nanoelectronics

## IoT With Trillions Internet Connected Sensors



## **New Connected Products Are Coming**

Even diapers will be connected - 40M/day in the US alone



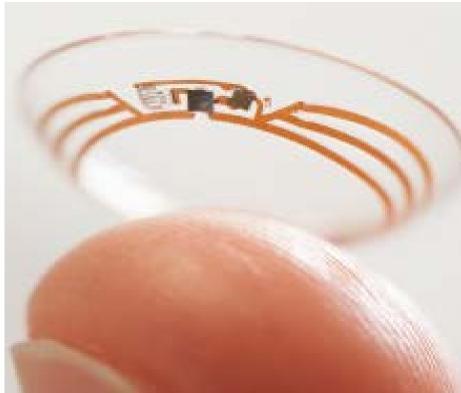


## **IoT Medical Devices**



#### **Next Generation Endoscope**

#### **Contact Lens with intelligence and control**



## What will we have in 15 years?



Source: https://sites.google.com/site/ism6021fall2011/telepresence-is-finally-coming-of-age

Frontiers of Characterization & Metrology for Nanoelectronics

## Migration to the Cloud Data, logic and Applications

## Driving Change in The Global Network

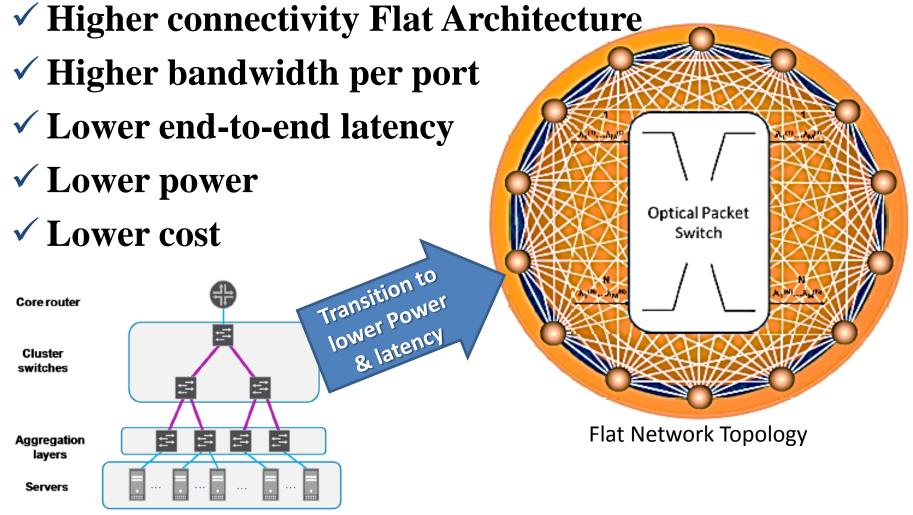
Frontiers of Characterization & Metrology for Nanoelectronics

#### Changes driving data traffic:

- ✓ Global IP traffic will pass <u>1.4 Zettabytes</u> (10<sup>21</sup>) by 2017
- ✓ Wireless traffic will surpass wired traffic by 2016
- ✓ The number of mobile-connected devices first exceeded the number of people on earth this year
- ✓ IoT growth will drive demand for bandwidth
- ✓ Data, Logic and Applications are migrating to the Cloud

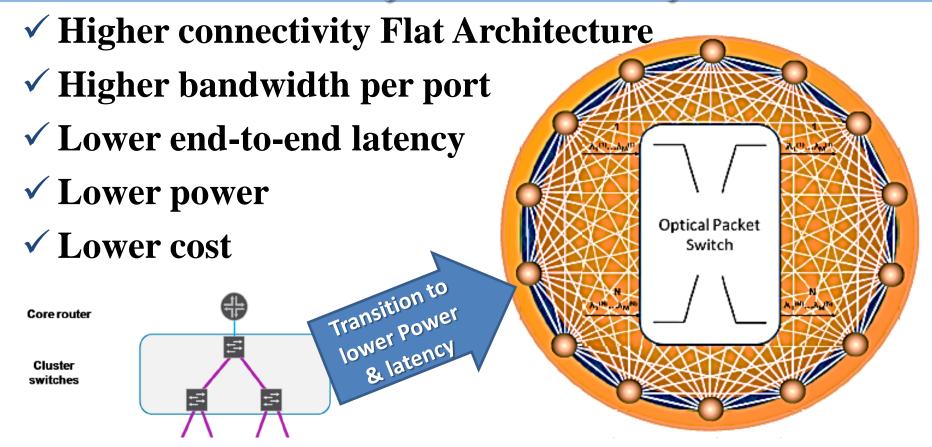
## Today packaging is a limiting factor in cost, performance and size.

## The Network Architecture Must Change Globally and Locally



Traditional Hierarchical Tree Topology

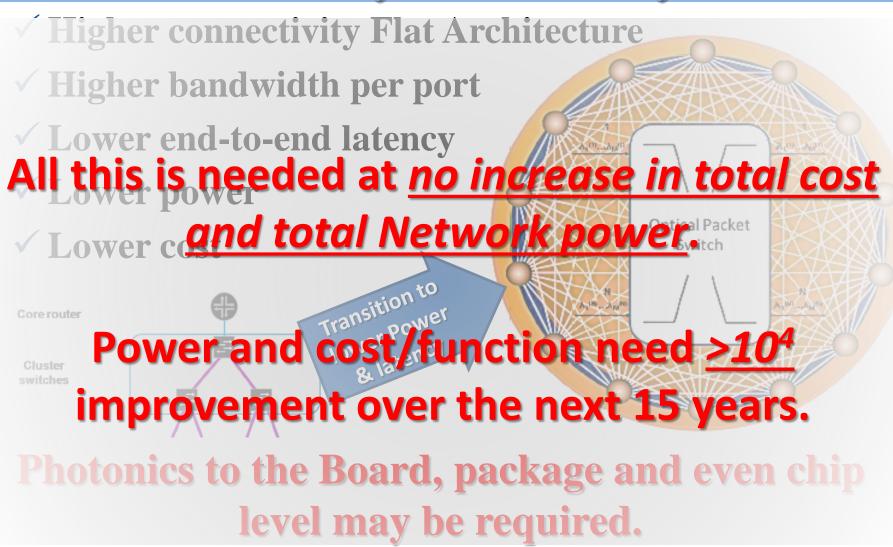
## The Network Architecture Must Change Globally and Locally



# Photonics to the Board, package and even chip level may be required.

Frontiers of Characterization & Metrology for Nanoelectronics

## The Network Architecture Must Change Globally and Locally



Frontiers of Characterization & Metrology for Nanoelectronics

# The Major Challenges to Achieve this vision include:

#### ✓ Power

- Delivery in complex 3D packages
- Integrity at low operating voltage

#### ✓ Latency

 In the package, on the Board, in the global network and everything in between

#### ✓ Thermal management

- At die, package and board level

#### ✓ Bandwidth density

- At the die, in the package and on the board

#### ✓ Cost

 Initial cost, cost of power and cost of reliability in a world where transistors wear out

# The Major Challenges to Achieve this vision include:

#### ✓ Power

- Delivery in complex 3D packages
- Integrity at low operating voltage
- 🗸 T.stenev

## We must move photons closer to the ICs and all other things closer together

- At the die, in the package and on the board

- ✓ Cost
  - Initial cost, cost of power and cost of reliability in a world where transistors wear out

# Only a Revolution in Packaging can satisfy these diverse Needs

#### At the leading edge everything will change. This requires:

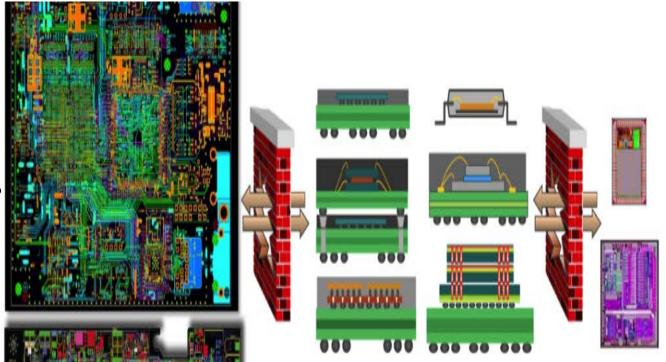
- ✓ New co-design and simulation tools
- $\checkmark \quad Use of the 3^{rd} dimension$
- Heterogeneous Integration
- New materials
- ✓ New device designs and architectures
- New package architectures
- New network architectures
- New manufacturing processes

## **Co-design and Simulation Tools for Packaging are Critical Needs**

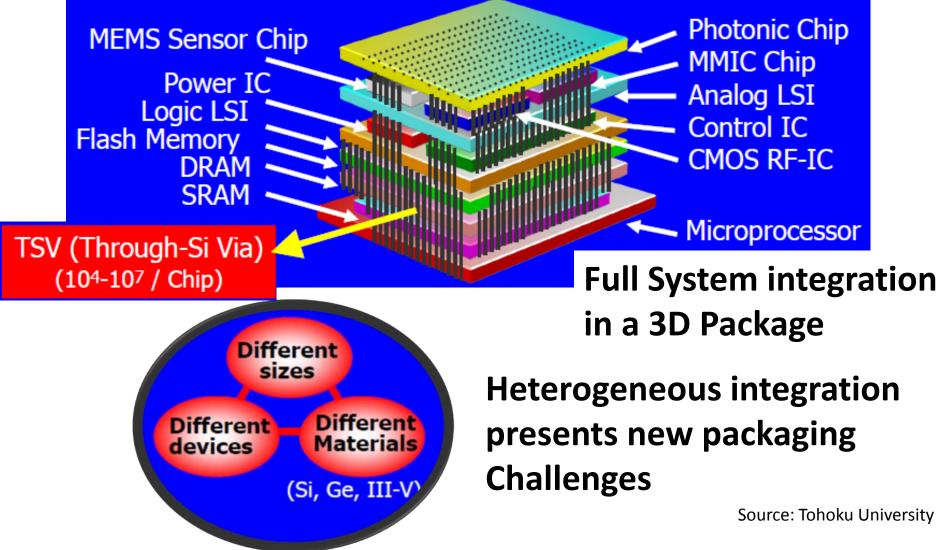
Tools that integrate across the boundaries of device, package, printed circuit board and product will speed the process of migration to higher density (SoC, SiP, 2.5D, 3D, etc.).

This enables:

- ✓ Increased performance and bandwidth
- Decreasing latency, power, size, cost
- Reduced time to market



## **3D Packaging And Heterogeneous Integration Will Be Essential**



**Frontiers of Characterization & Metrology for Nanoelectronics** 

## Heterogeneous Integration by Circuit Fabric Type

#### ✓ Logic

Hots spot locations not predictable, high thermal density, high frequency, unpredictable work load, limited by data bandwidth

#### Memory

Thermal density depends on memory type and thermal density differences drive changes in package architecture and materials

#### ✓ RF

Noise isolation is critical, may require compound semiconductors with different mechanical properties

#### ✓ MEMS

There is a virtually unlimited set of requirements; hermetic, non-hermetic, variable functional density, plumbing, stress control, etc.

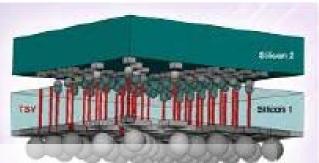
#### Photonics

Extreme sensitivity to thermal changes, O to E and E to O, Optical signal connections, new materials

#### Plasmonics

Requirements are yet to be determined but they will be different from other circuit types

## Other 3D Package Examples of Heterogeneous Integration



## **The Revolution in Packaging**<sup>1009595</sup> **is just beginning**



Micron Dresden April 2015

## New Materials Will Be Required

# Many are in use tod

- ✓ Cu interconnect
- ✓ Ultra Low k digette
- ✓ High k die
- Organic Mic Muctors
  - Høgen free

Gre

vements are needed

## Many are in development

- Nanotubes
- Nano Wirx<sup>®</sup>
- > 2D Repair for Si
  - Macroscules
    - Na Priticles
      - Site materials

New Materials✓Conductors✓Semiconductors✓Dielectrics✓Composites

Frontiers of Characterization & Metrology for Nanoelectronics

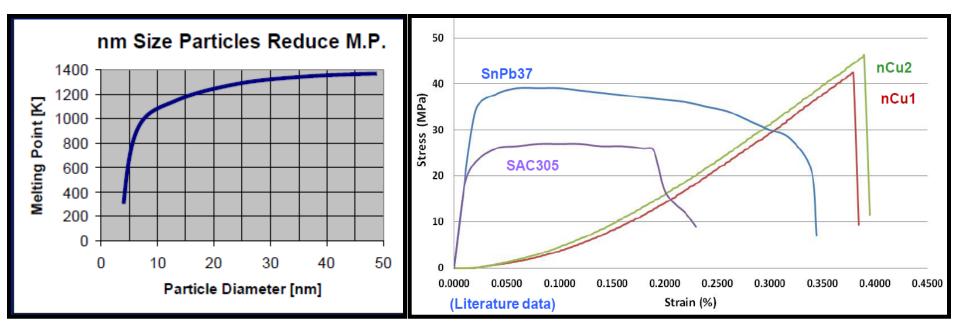
## **Carbon Conductors Look Better Than Cu**

		Cu	CNT	GNR			
	Max current density (A/cm <sup>2</sup> )	~106	> 1x10 <sup>8</sup>	> 1x10 <sup>8</sup>	x10 <sup>2</sup>		
Many questions still to be answered before							
graphene or CNT can be considered as a practical							
interconnect materials. The results so far are							
very promising.							
	Temp. Coefficient of Resistance (10 <sup>-3</sup> /K)	4	<b>&lt; 1.1</b> Kane, et al. Europhys. Lett.,1998	<b>-1.47</b> Shao et al. Appl Phys. Lett., 2008			
	Mean Free Path @ room-T (nm)	40	> <b>1000</b> McEuen, et al. Trans. Nano., 2002	<b>Phys. Rev. Let. 2008</b>	x25		

#### Frontiers of Characterization & Metrology for Nanoelectronics

## Low temp Cu Nano-solder

- ✓ Package assembly at low temp (100C)
- ✓ Reflow solder to PCB <200C
- ✓ Consistent with Direct Interconnect Bonding



Frontiers of Characterization & Metrology for Nanoelectronics

#### Dresden April 2015

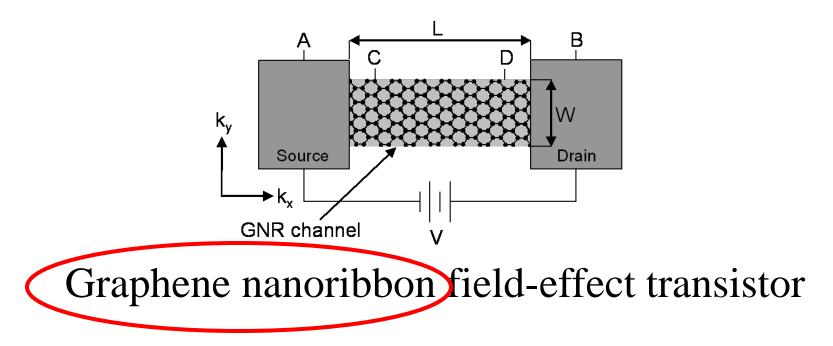
Amorphous Shell

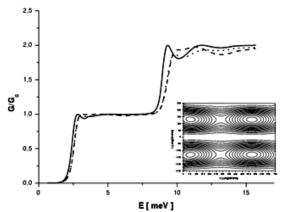
Crystalline

## New Semiconductors 2D Replacements for Si

Frontiers of Characterization & Metrology for Nanoelectronics

## **2D Replacements for Si**



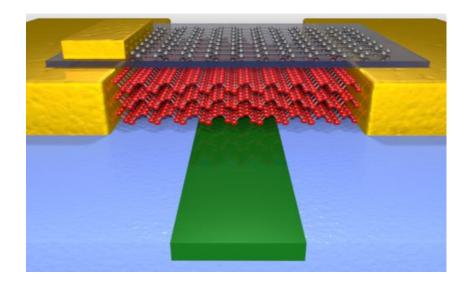


Conductance is function of initial electron energy and on/off ratio is poor. Contacts A and B are at two different Fermi levels.

Source: Brazilian Journal of Physics

Frontiers of Characterization & Metrology for Nanoelectronics

## **2D Replacements for Si**

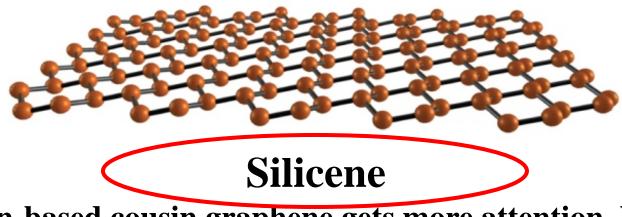




- ✓ Has a band gap for high on/off ratio
- ✓ Compatible with Si making it a good candidate for silicon photonics
- ✓ The bandgap is tunable by varying # of layers on silicon substrate
- $\checkmark$  It is a direct-band semiconductor

Source: EE Times Dresden April 2015

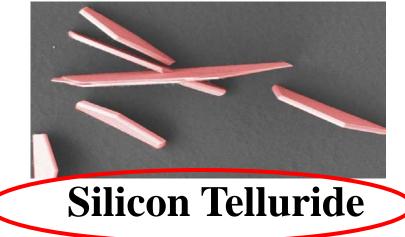
## **2D Replacement for Si**



#### Its carbon-based cousin graphene gets more attention, but silicene is catching up. Unlike graphene, silicene has a band gap and may be a fast follower.

- ✓ 2D crystals of silicon were identified theoretically in 1994
- $\checkmark$  The name 'silicene' is coined in 2007.
- ✓ Fabrication of silicene nanoribbons in 2009
- ✓ First reports of silicene sheets formed on silver in 2012
- ✓ First demonstration of silicene transistor in 2015

## **2D Replacements for Si**



One of a class of 2D chalcogenide semiconductors that have band gaps. Elements can be substituted (Mo, W, S, Se, etc.) to tailor properties.

#### Silicon Telluride is a 2D chalcogenide semiconductor:

- ✓ It is transparent but brilliant red
- $\checkmark$  It is a native p-type semiconductor.
- $\checkmark$  Can be grown as nanoribbons, flat nanoplates or standing nanoplates
- ✓ Can be used as light detectors and light emitters
- High on/off ratios

## **Composite Materials**

#### **Properties not available in Nature**

Frontiers of Characterization & Metrology for Nanoelectronics

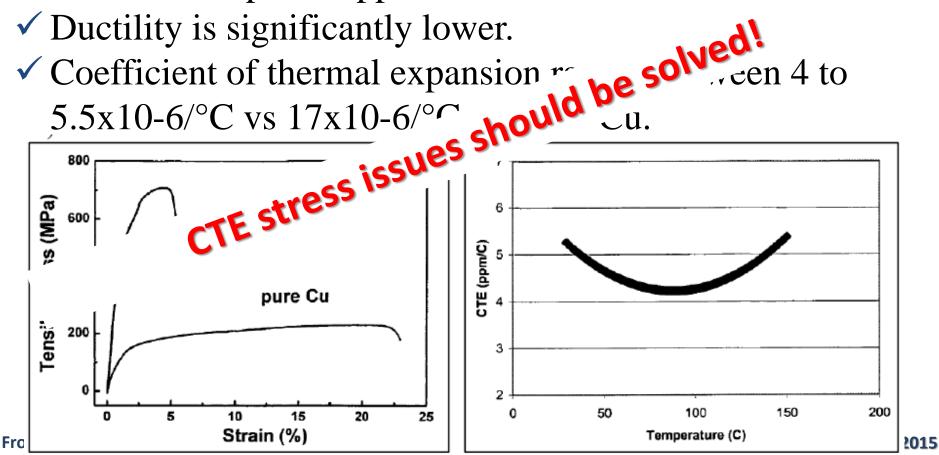
## **Composite Cu Properties**

#### **Measured Properties show:**

✓ The strength of the Cu-SWCNT composite is more than twice that of pure copper

Leen 4 to

- ✓ Ductility is significantly lower.
- $\checkmark$  Coefficient of thermal expansion  $r_{1}$ 5.5x10-6/°C vs 17x10-6/°



## **Conductors Are Changing**

#### **Composite Copper is in evaluation. Current status:**

Measurement	Conventional Copper	TeraCopper®	
Resistivity (Ohm·cm)	1.66 x 10 <sup>-6</sup>	1.26 x 10⁻ <sup>6</sup>	
Conductivity (S/m)	6.02 x 10 <sup>7</sup>	7.94 x 10 <sup>7</sup>	
Increase in Conductivity	N/A	32%	
Avg. Current Capacity(Amps/cm <sup>2</sup> )	3.88 x 10 <sup>4</sup>	5.57 x 10 <sup>4</sup>	
Increase in Current Capacity	N/A	44%	

The first electrical performance improvement in copper since 1913 makes composite copper the most electrically conducting material known at room temperature.

Targets for improvement compared to conventional copper are:

- ✓ 100 % increase in electrical conductivity
- ✓ 100% increase in thermal conductivity
- ✓ 300% increase in tensile strength

Frontiers of Characterization & Metrology for Nanoelectronics

Source: NanoRidge

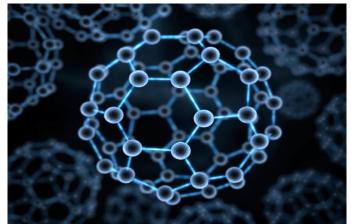
## **Polymer CNT Composites**

### Until recently results were disappointing:

- ✓ Less impact on thermal, mechanical and electrical properties than expected.
- $\checkmark$  Now that is changing rapidly due to:
  - Higher purity
  - Fewer defects
  - Chirality control
  - Reduction in production cost

## **Polymer CNT Composites**

## **Composite Nanomaterials**



## Nano-composites improve high voltage capacity for polymer insulators in high voltages cables.

- ✓ The addition of carbon nanoballs (Buckyballs) to polymer insulated high voltage lines increases voltage capacity by 26%
- $\checkmark$  Theoretically it should be even better with optimization
  - Dispersion of Buckyballs in the polymer
  - Optimal nano-particle loading of polymer
  - Understanding the mechanism

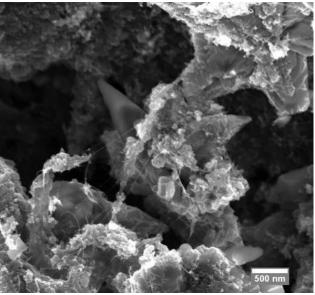
Source: Chalmers University of Technology

Frontiers of Characterization & Metrology for Nanoelectronics

## Nanomaterials are changing Energy Storage

Superior ultracapacitors with an inexpensive composite of graphene flakes mixed with single-wall carbon nanotubes. The great advantage of this hybrid structures design is:

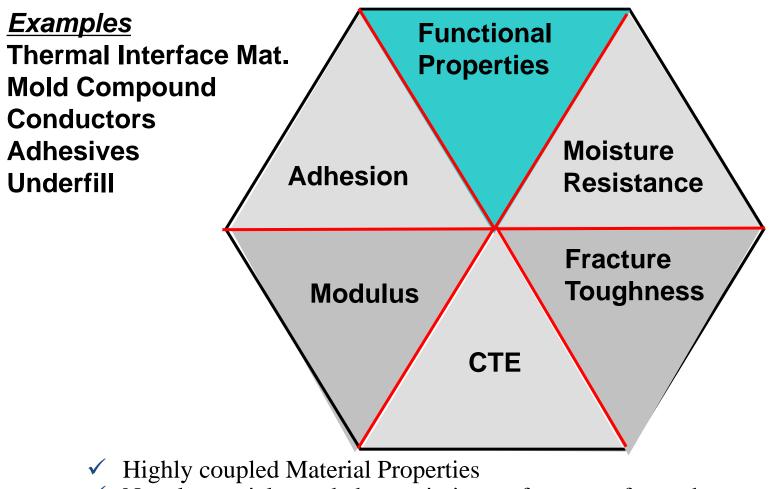
- Graphene provides good conductivity in plane of nanostructures and high surface area for the ultracapacitor.
- Single walled carbon nanotubes connect the structure into a stable, uniform network



SEM image of ultracapacitor's hybrid film with graphene flakes and single-walled carbon nanotubes.

Source: George Washington University

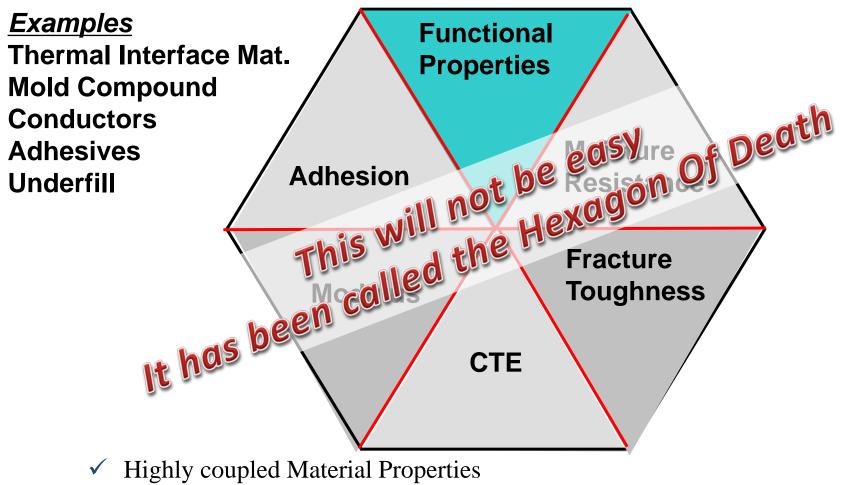
## **Packaging Materials Requirements**



✓ Novel materials needed to optimize performance for each parameter

Frontiers of Characterization & Metrology for Nanoelectronics

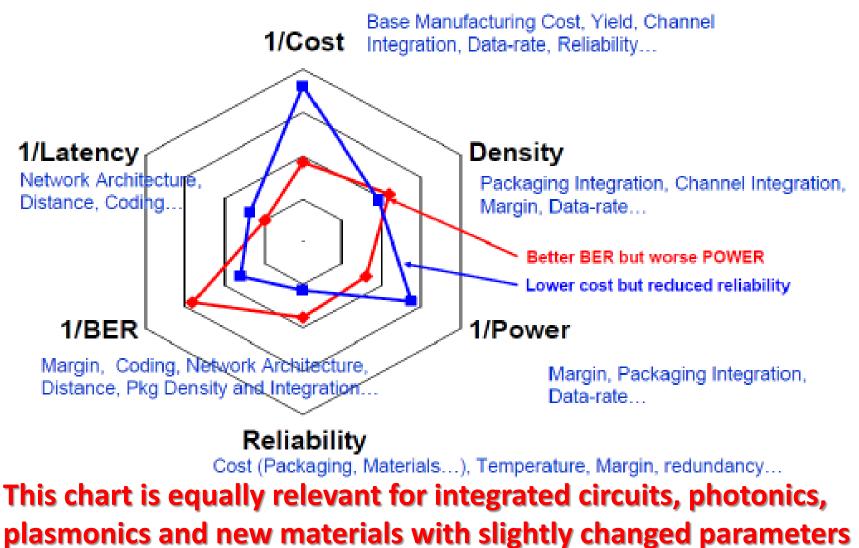
## **Packaging Materials Requirements**



✓ Novel materials needed to optimize performance for each parameter

Frontiers of Characterization & Metrology for Nanoelectronics

## **Trade-offs For Optimization**



Frontiers of Characterization & Metrology for Nanoelectronics

Source: IBM Dresden April 2015

## **Interfaces control Materials Properties**

## **Everything is getting thinner**

- ✓ All layers in a packages
- ✓ All layers in integrated circuits
- ✓ Composite structure interfaces

## In many cases bulk properties no longer matter

- ✓ Metals
- ✓ Insulators
- ✓ Semiconductors
- ✓ Composites

## **Interfaces control Materials Properties**

## **Everything is getting thinner**

- ✓ All layers in a packages
- ✓ All layers in integrated circuits

## We don't yet have metrology to define the interface properties which we must have to optimize a structure

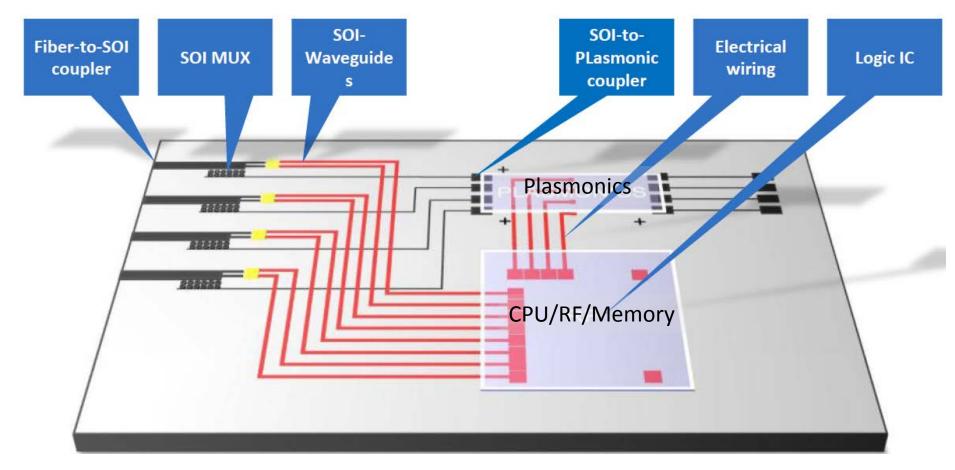
### ✓ Insulators

### ✓ Semiconductors

## ✓ Composites

Frontiers of Characterization & Metrology for Nanoelectronics

## **Co-integration Of Electronics, Photonics And Plasmonics On SOI**



Source: Dr. Nikos Pleros Aristotle University

#### Frontiers of Characterization & Metrology for Nanoelectronics

## **Co-Integration of Technologies**

## Use each technology where it is the best:

- ✓ Electronics
  - Active logic and memory (Processing and routing)
  - Smallest size
- ✓ Photonics
  - High bandwidth
  - Energy efficient
  - Long and intermediate distance
- ✓ Plasmonics (R. Zia et al., "Plasmonics: the next chip-scale technology", Materials Today 9(7-8), 2006)
  - Much smaller than photonic components
  - Potentially seamless interface between Optics and Electronics
  - Low power active functions
  - Sub-wavelength confinement of photon energy

Frontiers of Characterization & Metrology for Nanoelectronics

## Summary

#### **Requirements for IoT/Cloud driven Global Network**

- ✓ Cost and power reduced by >10<sup>4</sup>
- ✓ Flatten the architecture increase ports by >10<sup>6</sup>
- ✓ Reduce latency
- Support software defined networks

Technology identified can deliver 10<sup>3</sup> improvement at most.

A majority of improvement will come from materials & packaging. Innovation is needed but is it practical to find another order of magnitude?

In the first 40 years of Moore's Law scaling every parameter improved by more than one million times.

## Maybe 2 orders of magnitude in 15 years is too conservative

## Conclusion

## New devices and new materials will drive the development of new metrology tools and techniques. Some key issues are:

- $\checkmark$  Interfacial adhesion
- ✓ Nano-particle dispersion
- ✓ Interfacial stress/strain
  - Layer to layer
  - Matrix to nano-particle

✓ Porosity

## Conclusion

New devices and new materials will drive the development of new metrology tools and techniques. Some key issues are: These data sets will be essential to enable optimization of new, engineered materials and processes demanded by the emerging technology drivers 

- Matrix to nano-particle
- ✓ Porosity

# Thank You for Your Attention

Frontiers of Characterization & Metrology for Nanoelectronics