White Paper for TIP Critical National Needs

Nanomaterials/Nanotechnology: Carbon Based Electronics Infrastructure

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TIP Critical National Need: Carbon Based Electronics Infrastructure

Introduction

As the Semiconductor Industry continues scaling into the nano-scale electronic structures, numerous road blocks have become apparent that will most likely limit the scaling of both conventional silicon based CMOS and memory technologies. However, the demand for cost effective nano-scale electronic switches and memories that scale beyond conventional CMOS is as great if not greater than during the days of conventional dimensional and materials scaling. Scaling road blocks in silicon technology generally relate to either excessive power consumption or charge based storage and sensing as devices are scaled, e.g., short channel effect control (SCE) leading to subthreshold leakage and standby power, junction leakage causing higher operating power, gate dielectric thickness scaling leading to high standby current, charge storage and retention limiting memory scaling, and many others that either limit device scaling or require expensive process solutions.

Office of Science and Technology Policy (OSTP) identifies development of next generation manufacturing technology as a critical source of future American jobs and national interest.[1] *Nano-scale technology* falls squarely into this *critical national need area*. Numerous nano-scale silicon and non-silicon based devices have been proposed and extensively studied for both memory and logic devices (as well as Interconnect) including options such as carbon based nano-electronics including applications using carbon nanotubes (CNTs) and graphene ribbons, silicon nanowires, spintronic devices, Phase Change Memories, Metal Oxide Resistance memories, quantum dot or nanocrystals, and organic molecular devices . Many of these devices have been highlighted and discussed in the International Technology Roadmap for Semiconductors (ITRS):2007[2] and its update in 2008[3].

This paper is intended to highlight the National Technology Need for NIST TIP support to further the advancement of *Carbon Based Electronics Infrastructure* technology development in support of carbon nano-electronics as a key alternative or supplement for silicon based nano-electronics. Even though many potential applications have been identified and investigated for carbon based electronics[4] because of their unique properties, significant high risk technical challenges must be overcome, most notably developing the *materials infrastructure*, to successfully bring them to the market place.

[1] OSTP, http://www.ostp.gov/cs/issues/technology
[2] The International Technology Roadmap for Semiconductors:2007, http://www.itrs.net/Links/2007ITRS/Home2007.htm
[3] The International Technology Roadmap for Semiconductors:2008 Update, http://www.itrs.net/Links/2008ITRS/Home2008.htm
[4] R. J. Nicholas, A. Mainwood, and L. Eaves, "Carbon-based electronics: fundamentals and device applications", Phil. Trans. R. Soc., A 2008 **366,** 189-193.

Carbon Based Electronics

Carbon based electronic materials have been extensively studied [5] in several of its allotropic forms such as carbon nanotubes (CNTs), atomic layers of graphite (i.e., graphene), fullerene molecules, and diamond for many years for applications such as resistive memories[6], logic devices, interconnect, biosensors, displays, solar panels, and many others. In the laboratory and to some extent in the commercial environment, the following question has been addressed:

Why Carbon Based Electronics?

Carbon in two of its allotropic forms of carbon nanotubes and graphene (single and multilayer) has demonstrated[7,8] many unique physical and electronic properties that have the potential for extending device scaling and enhance performance.

For *carbon nanotubes,* key properties include high mobility (>50,000 cm^2/V-sec), long ballistic transport (>100 nm) for both device and interconnect applications, high thermal conductivity (>1000 W/m•K), and high mechanical strength to name a few. While there is much interest in their electronic properties, there are many challenges remaining to bring them to main stream electronic applications, none the least of these is the infrastructure to support the quality and quantity needed for commercialization. For electronic applications, chemical vapor deposition (CVD) is the dominant growth technique because of its relative cleanliness, relatively low growth temperature, and quantity that can be grown cost effectively. CNTs can be formed as single-walled nanotubes (SWCNTs) which are either semiconducting or metallic depending on their chirality and multi-walled nanotubes (MWCNTs) which are metallic. Typically CVD grown SWCNTs are found in the ratio of one-third metallic and two-thirds semiconductor which, for FET devices, requires separating the metallic CNTs out of the mix.

Graphene, the only demonstrated 2-D zero bandgap semiconductor and can be thought of as an unrolled single-walled carbon nanotube that also possesses the unique electronic properties of high mechanical strength (200X steel), high thermal conductivity (>3000 W/m•K), and high carrier mobility as high as ~$2x10^6$ cm2/V-sec and practically independent of temperature for a single layer of graphene. In its more graphitic state (multilayer graphene), the 2-D properties are compromised due to the interaction with adjacent layer/s. If production level viable growth techniques are developed that can be integrated into CMOS compatible process, then graphitic materials, such as graphene, either stand-alone or in combination with CNTs have the long-term potential to further enhance carbon-based devices for certain applications by providing other channel technology options for fabricating high mobility planar devices. However as discussed below, graphene or combinations of graphene and CNTs must first catch up with CNT's state-of-the-art for electronic applications since CNTs have solved many of the problems of high purity stable solutions of CNTs such as dispensing of uniform layers using standard semiconductor equipment in standard semiconductor facilities, patterning and etching, and demonstrated

[5] R. H. Baughman, A. A. Zakhidov, and W. A. de Heer, "Carbon Nanotubes – the Route Toward Applications", *Science*, Vol. 297, 2 August, 2002.
[6] T. Rueckes and B. M. Segal "Nanotube Films and Articles", US 6,706,402 (March 16, 2004).
[7] Physical Properties of Carbon Nanotubes, http://www.pa.msu.edu/cmp/csc/ntproperties/
[8] J. S. Bunch, "Mechanical and Electrical Properties of Graphene Sheets", Dissertation Cornell University, May 2008. http://www.lassp.cornell.edu/lassp_data/mceuen/homepage/Publications/bunch_thesis.pdf

compatibility with CMOS in resistive change memories. Since graphene is an "unrolled CNT" and not a "closed tube" as are CNTs, significant issues with passivation of the graphene sheet at the edges (e.g., channel edges for FETs) due to dangling bonds[9] will present significant development challenges and it is not known if the properties of these regions can be controlled and reliably reproduced.

Most interestingly, in addition to these unique properties, these carbon allotropes have the potential to decouple electronic devices from the silicon substrate which would lead to true 3D on-chip integration, i.e., not relying on technologies such as through silicon vias (TSV) to stack chips. Such 3D monolithic integration will advance chip scaling as well as power scaling while increasing performance. Carbon based electronics have the potential for other device applications that require circuit enhancements such as high radiation resistance and high operating temperature that make them attractive for harsh environments such as space, automotive, nuclear environments, and many other critical National Needs.

Issues with Carbon Based Semiconductor Applications

Although graphene is receiving considerable research attention[10, 11] for electronic device applications, as mentioned CNTs have made the most progress toward commercialization due to the significant difficulties in fabricating graphene layers in quantity and quality with conventional fabrication tools such as chemical vapor deposition (CVD), epitaxial growth (EPI), silicon sublimation from SiC, mechanical exfoliation (peeling from graphite), sodium reduction of ethanol, hydrazine reduction, and cutting open CNTs to name a few techniques. Until a breakthrough in larger scale fabrication of electronic grade graphene is discovered, applications of graphene will be limited in electronic applications except where graphitic (multi-layer graphene) materials show promise such as resistive change memories (RCM), biosensors, ultracapacitors, and transparent conducting electrodes to name a few.

CNTs have made good progress in being applied to commercial applications such as improving structural strength (clothes, concrete, high tensile strength fibers, fly wheels, synthetic muscles, etc), electromagnetic devices (field emission displays and X-ray tubes, solar cells, electric motors, ultracapacitors, light bulb filaments, magnets, etc), electroacoustic devices (speakers), chemical and CNT composites (conducting polymers, filtration - water, air pollution, hydrogen storage, biosensors, etc), and mechanical applications (oscillators, membranes, surface friction reduction, actuators, etc).

However the applications of CNTs (or graphene) for electronic circuit applications have suffered major fabrication difficulties limiting their acceptance for electronic circuits as either devices or interconnect, except for a couple of exceptions[12, 13] in the memory and sensor space discussed below. For Carbon Based devices to replace or supplement high performance FETs

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[9] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene", Rev. Mod. Phys., **81**:109, January-March 2009.

[10] *Carbon-Based Electronics: Researchers Develop Foundations for Circuitry and Devices Based on Graphite,* March 14, 2006. http://gtresearchnews.gatech.edu/newsrelease/graphene.htm

[11] T. J. Echtermeyer, M. C. Lemme, M. Baus, B. N. Szafranek, A. K. Geim and H. Kurz, "Nonvolatile Switching in Graphene Field-Effect Devices", IEEE Electron Device Letters **29**: 952. http://arxiv.org/ftp/arxiv/papers/0805/0805.4095.pdf

[12] *Nantero Proves NRAM™ Scalability Successfully Fabricates 22nm Memory Switch,* http://www.design-reuse.com/news/13083/nantero-proves-nram-scalability-fabricates-22nm-memory-switch.html

[13] *Building the nanofuture with carbon tubes,* http://www.aip.org/tip/INPHFA/vol-8/iss-6/p18.pdf

they must meet several basic requirements, i.e., they must be semiconducting and have a reasonable tight distribution of semiconductor bandgaps, be in the desired location (and most likely oriented) between the source and drain connections, have high purity, form controllable n- and p-type materials, incorporate high-permittivity dielectrics for gate control, and have low source/drain contact resistance to not limit the device on-current.

For CNTs to be semiconducting, they must be SWCNTs with the right chirality (n-m $\neq$ 3k). Since the bandgap of semiconducting CNTs is inversely proportional to the CNT's diameter, the bandgap distribution of the semiconducting SWCNTs (s-SWCNTs) will depend on the distribution of CNT diameters. Although these requirements have not been met at the levels needed for high volume manufacturing (HVM), progress, albeit slow, is being made to grow and/or separate CNTs for FET applications, but much high-risk R&D needs to continue to achieve purity levels needed for FET applications as discussed below.

For CNTs, several techniques have been investigated and developed to produce s-SWCNTs for electronic applications. These techniques tend to fall into two broad areas of 1) *in-situ* growth of CNTs in desired locations on the device substrate and 2) *ex-situ* (or off-wafer) techniques that grow the CNTs followed with separation and purification before being incorporated on the device substrate. To date, *in-situ* growth also includes the complicating factors that catalysts (e.g., nickel, iron, etc) needed to initiate the CNT growth and their subsequent removal by chemical means can be very detrimental to FET devices let alone achieving the purity of the CNTs required for VLSI devices; however, they may be tolerated in interconnect applications if the catalyst is limited to the interconnect device layers. Thus to achieve *in-situ* growth, considerable high-risk R&D will be needed to develop the understanding for the design of catalysts and processes that will be needed to enable CNTs for device applications.

Due to the significant challenges to overcome structural defects, metal impurities, and unwanted carbon allotropes with *in-situ* growth, most progress for electronic device applications has been achieved with *ex-situ* growth and purification techniques that have led to initial commercialization activities for non-volatile resistive change memory devices. Although techniques are becoming available to grow SWCNTs only, separation and purification techniques are still needed to separate metallic SWCNTs (m-SWCNTs) from s-SWCNTs to achieve electronic grade CNTs for FET applications even though new growth techniques demonstrating the controlled growth of s-SWCNTs (>90% s-SWCNTs) in the laboratory setting through catalytic compound control[14]. There are several approaches being employed to either separate out the s-SWCNTs from the m-SWCNTs post CNT growth prior to device processing or remove the m-SWCNTs after they are incorporated onto the device wafer using post wafer processing. Post CNT growth separation methods prior to wafer processing showing some promise include selectively reacting and evaporating m-CNTs within a mixed nanotube bundle, hydrogenating m-SWCNTs and selectively etching them away, alternating current dielectrophoresis which takes advantage of the relative dielectric constants of the m-SWCNTs and s-SWCNTs, Agarose Gel electrophoresis, selective functionalization (e.g., Azomethine Ylides), plasma treatment to convert m-CNTs to s-CNTs, and diameter-selective attack of m-SWCNTs from s-SWCNTs with nitronium ions.

An alternative approach to CNT separation is to selectively remove the m-SWCNTs from the s-SWCNTs after they are grown (e.g., CVD) or applied (e.g., by solution) to the device wafer.

[14] *A Recipe For Controlling Carbon Nanotubes*, Science Daily, September 2009, http://www.sciencedaily.com/releases/2009/09/090920204453.htm

A technique that has yielded working level circuits is using selective electrical breakdown of the m-SWCNTs and in recent work[15] converting m-MWCNTs to s-SWCNTs by eliminating the outer conductive layer/s through rapid oxidation of the outermost carbon shells. The approach is to pass high current through the conductive m-CNTs while holding the s-SWCNTs in parallel in a higher resistive state. The s-SWCNTs can be either intrinsically in a higher resistive state or held higher with the application of a suitable applied gate voltage depleting them of their carriers. For m-MWCNTs the outer shell/s will carry the primary current and oxidizes leaving the inner shell which will be either s-SWCNT or m-SWCNT. If it is m-SWCNT, then it will continue to carry a high current and oxidize or electrically break down. Obviously the issue with this technique at the VLSI scale is defects including voids and the circuit requirements needed to perform the removal of the m-CNTs. Other on-wafer process techniques may be possible for separating the s-SWCNTs such as nanotube functionalization followed with selective etch of the m-CNTs, but unfortunately, to date, none has proven effective. Although reasonable progress has been made in the laboratory environment to achieve high-purity (parts per trillion) s-SWCNTs with diameter control, for production grade FETs it will require significant R&D investment and even greater high-risk investment for HVM to be achieved.

As mentioned, numerous applications of CNTs and graphitic electronic devices have been proposed, evaluated, and some carried to initial commercialization; however only a few have succeeded in driving real interest and significant investment in the electronics industry environment. One of these is the resistive change memory (RCM) space as evidenced by the development by Nantero of high purity, semiconductor fabricator-compatible, patterned CNT fabric integrated with CMOS to fabricate nanotube random access memories (NRAM™)[16]. Research work has been performed by Nantero and other work by large independent device manufacturers (IDMs), universities and other research organizations worldwide on the RCM and other CNT or graphitic based FET devices. As with any fundamentally new technology, there are many engineering challenges in bringing carbon based electronics technology to fruition; not the least of these is the *infrastructure* needed for HVM. At the current state of development for memory applications which can be used as a stepping stone to FET and interconnect applications; it is time for R&D and investment to bring the needed *infrastructure* for HVM.

Why Government TIP Funding?

Short Time-frame and High Risk

Although conventional silicon CMOS and memory technologies are continuing to scale into the nanometer device range, albeit more slowly, it is commonly agreed that many roadblocks are on the horizon that will limit or stop their progression due to physical limitations, primarily due to the aforementioned barriers of either excess power or charge based storage and sensing as devices are scaled below 50 nanometers within next few years. Using silicon as an example, development of an *infrastructure* to support a fundamentally new technology can take decades before it is viable and sustainable. Even if the basic carbon based technologies are developed and proven viable, the risks associated with having the *infrastructure* support in place

[15] P. G. Collins, M. S. Arnold, and P. Avouris, "Engineering Carbon Nanotubes and Nanotube Circuits Using Electrical Breakdown", *Science* 27, **292**, no. 5517, pp. 706-709, April 2001.
[16] T. Rueckes, K. Kim, E. Joselevich, G. Y. Tseng, C. Cheung, and C. M. Lieber, "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing", *Science* 7, **289**, pp. 94-97, July 2000.

could severely limit its acceptance by the device manufacturers unless this is rectified. Some of the key high risk *infrastructure* component needs are discussed below.

R&D and Ramp to HVM Costs are too High

For smaller companies where a lot of the initial development and commercialization is taking place and even larger IDMs and others the burden of developing the *infrastructure* for HVM carbon based electronics will be too high. Without external R&D, public and private investment, and supplier development; the full potential of carbon based electronics cannot be fully realized. The transformational benefits envisioned for CNT's (carbon nanotubes) or other graphitic materials depends on creative development of both chemistry and chemical process engineering to manufacture functional nano-structured materials at the HVM scale for high impact applications that are enabled by these nanomaterials.

Although clearly interdependent, the industries responsible for each of these developmental areas do not typically reside in the same business. The complexity and cost associated with each (i.e. material chemistry and application) can result in a stalemate with each side waiting for advances in the other to justify the high risk effort for the development. With TIP funding, the industry could be given a much needed 'kick-start' to provide smaller *infrastructure* technology companies that are well positioned from their initial R&D efforts to positively affect the *infrastructure* problem based on their initial work and knowledge of carbon based materials such as carbon nanotubes and other carbon allotropes. With TIP support for these companies to enhance their capabilities to develop CNT and graphene manufacturing process technologies to support HVM for specialized electronic (and even non-electronic) applications, they will be in the position to provide and support, through licensing, their technology to both high volume nano-material providers and support electronic device application technologies with IDMs and other end users. Without TIP support, the development of the *infrastructure* for HVM will, at best, be a serial event, and thus noticeably delaying the implementation of carbon based electronics.

High Risks

Although there are numerous High Risks associated with the implementation and adoption of carbon based electronics, the intent of this white paper is to focus on the *infrastructure* needed for production level development and to carry the technology to HVM.

Infrastructure Needs for HVM Carbon Based Electronic Applications

Depending on the electronic application whether it be in the area of Displays, Photovoltaics, Sensors, Fuel Cells, Batteries, Devices, or others; the requirements such as chemical purity, allotrope purity, conductivity state, functionalization, and etc for a given application can vary from reasonably lax to very stringent as in the case of FET devices as discussed below for s-SWCNTs.

For many electronic applications including resistive change memory applications, high purity s-SWCNTs only are not required as they are for FET device applications. However many of these large scale applications, e.g., photovoltaics, displays, energy, and others, will require and benefit significantly from a commercial grade of CNT or graphitic material for high purity

films. Many of these applications would benefit from what we would term a "Universal Formulation" of CNTs that would be optimized for both efficient and cost effective CNT manufacture as well as for applicability to a number of these high end targeted applications. The Universal Formulation CNT product directly addresses many of fields in variety of ways. As mentioned the product is suitable for applications such resistive change memories, as transparent electrodes that can be used both in bulk and in thin film photovoltaic cells for solar energy conversion, and many other applications being researched in our universities and other R&D centers today such as solar energy conversion, fuel cell battery membranes, energy efficient high luminescence light sources and others to name a few.

Although availability of research and evaluation level quantities can be acquired from several sources[17], the basic *infrastructure* required to support production development and HVM with the high purity and material properties required for these applications is not in place. It will require significant high risk funding to jump start the development of the large volume processes and other *infrastructure* requirements needed to meet the challenges of carbon based electronics. Some of the large scale *infrastructure* requirements for applications using *ex-situ* growth techniques are 1) high quality and quantity of raw CNTs and/or graphitic material, 2) large scale separation and purification processes to process the raw material into acceptable application quality, 3) delivery system technology including packaging, application tools, transport, etc, and 4) metrology both for processing the materials and for metrology at the wafer or system level; all done at acceptable costs. For CNTs or graphene grown on the wafer, the challenges will be even greater to remove the impurities and unwanted material species. [It is the opinion of this author that, except for a few applications such as interconnects and high luminescence light sources, *in-situ* growth has fundamentally too many challenges to be a viable alternative in the near-and intermediate-term.]

Need for a Scaled Process Solution to HVM

Based on our experience, commercialization is negatively impacted by the non-availability of a large volume multiply sourced and consistent quality of CNTs and other graphitic allotropes that are necessary to carry out the numerous tests necessary for production development and production ramps. Until a reliable supply of cost effective functional carbon based materials becomes available in large volumes to accelerate the development and acceptance of carbon based electronics, the transformational impact of carbon based electronics will not be realized.

These critical applications are underpinned by the need for a robust manufacturing process to reproducibly create highly functional materials with purity consistent with the desired application and at an efficiency that make them economically viable as a material. The focus of *infrastructure* development is the development of the appropriate analytical processes, unit process optimization, final product quality and qualification control that typifies more traditional bulk chemical industry products. However, these *infrastructure* aspects do not currently exist for the processing of raw carbon nanotubes or graphitic materials needed at the commercial scale and there are many formidable high risk challenges to overcome due to the complexity of the materials to achieve the scaling required for HVM. TIP funding will allow smaller materials companies to take a more aggressive experimental position to scaling, rather than scaling through replication of smaller scale-up versions. Along with the aggressive experimental development,

[17] Brewer Science, http://www.brewerscience.com/products/cntrene/

development of accurate process models to bridge the experimental and large scale demonstrations to reduce the time to HVM could be supported with TIP funding.

No Clear Solutions for Producing High Purity Semiconducting Carbon Nanotubes

Although good progress has been made in the development of SWCNTs production level processes, development of a high purity (parts per trillion) s-SWCNT material source is still lacking and no viable solutions at this time are in sight for either a viable off-wafer or on-wafer production process technology. Although some announcements[18, 19] of controlling chirality of CNT growth for either s-SWCNTs or m-SWCNTS have been reported, these efforts are providing better growth mechanism understanding, but are well short of meeting the high purity requirements for FETs. For CNTs or graphitic carbon to be acceptable for many electronic applications such as a viable alternative for the CMOS roadmap, significant high risk investment will be required to develop the necessary process technology and *infrastructure* for high purity s-SWCNT and/or m-SWCNTs to support the continued device development and acceptance of carbon based electronics as an alternative to silicon.

ESH Acceptance

As with any new material technology, ESH (Environmental, Safety, and Health) acceptance by industry is critical and becomes part of the *infrastructure* requirements at both the supplier and end-user. Although initial studies[20, 21] have been conducted on the ESH aspects of carbon nanotubes, comprehensive understanding and regulations are still lacking and must be addressed as part of the *infrastructure* needed for HVM. In some cases, TIP funding may be appropriate to resolve ESH issues in order to accelerate industry acceptance of carbon electronics technology.

High-Reward Science & Technology

The sustainability of the American economy is dependent upon our continuing to drive and lead other countries for the innovation of new products and services. The semiconductor industry provides a highly relevant model for how the advent of advanced materials can alter the landscape of an entire industry. With the core understanding discussed above of the benefits and challenges of carbon nanotubes and graphitic material, Carbon Based Electronics has the potential to alter the electronics landscape and continue **Scaling beyond Silicon CMOS and Memory Technologies** if fully realized and brought to HVM. The markets noted previously that

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[18] A. R. Harutyunyan, G. Chen, T. M. Paronyan, E. M. Pigos, O. A. Kuznetsov, K. Hewaparakrama, S. M. Kim, D. Zakharov, E. A. Stach, and G. U. Sumanasekera, "Preferential Growth of Single-Walled Carbon Nanotubes with Metallic Conductivity", *Science* 2, **326**, no. 5949, pp. 116-120, October 2009.

[19] *Better Control of Carbon Nanotube 'Growth' Promising for Future Electronics*, Science Daily, October 2009, http://www.sciencedaily.com/releases/2009/10/091001163559.htm

[20] T. Brady, D. DePaoli, J. Solomon, T. Wooldridge, S. Brown, "ESH & Nanotechnology: A Joint Study by the Chemical Industry Vision2020 and the Semiconductor Research Corporation," isee, pp.27-31, Proceedings of the 2006 IEEE International Symposium on Electronics and the Environment, 2006., 2006

[21] Diane J. Mundt, PhD., ENVIRON International Corp., July 10, 2007, "Environmental Health and Safety", http://www.internano.org/content/view/27/1/ (includes list of ESH references)

Carbon Based Electronics has the potential to participate exceeds more than **$200 billion**[22, 23, 24] **per annum** not including the spin-off industries that will help the nation lead in the generation of **new high paying jobs**, enhanced **national security**, highly valued **intellectual property**, and development of **trained minds** for the future.

As discussed, **Carbon Based Electronic applications** have many untapped and unique properties that have the potential to not only extend and enhance Silicon Based Electronics, but also the potential to enable newly envisioned nanoscale opportunities that go **beyond silicon limitations**. As noted, one of the most significant opportunities would be the realization of true on chip 3D devices without the limitation of a silicon substrate. However without the carbon materials *infrastructure* including consistent sources of raw materials, processes for large scale materials purification and functionalization, metrology for materials process control and applications, and ESH industry regulations for commercial development and ramps, Carbon Based Electronics will continue its current slow pace and may not be a viable alternative solution when and if silicon reaches insurmountable roadblocks.

[22] Gartner Dataquest, http://www.gartner.com/it/products/research/dataquest.jsp
[23] VLSI Research, https://www.vlsiresearch.com/
[24] IC Insights, http://www.icinsights.com/