

Critical National Need Idea:

**High-performance Si-based Optoelectronic Materials for
National Security and Economic Development**

Keywords: Silicon Materials Optoelectronics, MBE, CdTe

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Background

Semiconducting materials incorporated into electronic devices are generally required to be highly perfect, single crystals to perform their functions. The development of the Si microelectronics industry has virtually perfected the quality of single crystal Si wafers and reduced their cost far below any other single crystalline wafer material. However, many important optoelectronic devices, such as night vision cameras, high-efficiency solar cells, laser diodes, and LEDs require the special properties of other semiconducting materials such as GaN, GaInP, HgCdTe, and InSb. These materials can be costly, in part, because of the high cost of single crystalline wafers such as SiC, GaAs, InP, Ge, CdZnTe, and GaSb, that are used as seed crystals to grow the semiconductor device crystal. Perfecting techniques to grow high-quality optoelectronic materials on Si would open pathways to significant economic development, as well as increasing the availability of critical technologies for healthcare and national security.

Areas of Critical National Need

We will cite a few specific examples where societal needs are met by the availability of lower cost optoelectronic devices:

Night Vision

The US military relies on night vision technology to provide a competitive advantage on the battlefield. HgCdTe-based night vision cameras are the gold standard for high performance in night vision, however at rather high cost. These cameras are used in critical systems, but they cannot be distributed as broadly to soldiers due to the cost. One of the significant cost drivers is the substrate for HgCdTe growth is bulk CdZnTe. CdZnTe is very expensive (> \$200 per square cm) and available in only relatively small sizes (8 cm x 8 cm). Replacing bulk CdZnTe with Si has the ability to dramatically reduce the price of high performance HgCdTe imagers and allow widespread distribution to soldiers.

Infrared Medical Diagnostics

Infrared imaging (thermography) of the human body can sensitively detect abnormal tissue such as tumors in a rapid, non-invasive fashion. For example, thermography is developing into an alternative or complementary procedure to mammography for breast cancer screening. Because it is both non-invasive and painless procedure, it is likely to reduce barriers to patients to obtain screening and promote early detection of cancer. There is also some evidence that thermography can detect changes in tissue earlier than mammography. The cost of high-performance infrared cameras limits its introduction into standard medical practice, where it could have a major impact in diagnosis of a variety of diseases including breast cancer, prostate cancer, skin cancer, and thyroid problems. Availability of lower cost HgCdTe imagers based on Si tailored to this application could help this technology reach the critical mass for widespread adoption.

Energy Independence

The world record for conversion efficiency for photovoltaic (PV) solar cells is held by GaInP/GaInAs/Ge triple junction cells. Such cells require expensive single crystal Ge substrates, which limit their use to space applications (where high cost is accepted) and “concentrator” systems which focus high intensity sunlight onto small, liquid cooled, solar cell chips. Such complex designs are driven by the high material cost of these chips. Development of lower cost, high efficiency solar cells could revolutionize PV electricity generation, reducing US

dependence on fossil fuels. High-quality crystal growth of II-VI compounds such as CdTe or ZnTe on Si substrates could yield such a leap in performance to cost ratio.

Technical Challenge

Crystal growth on lattice mismatched substrates (such as growth of HgCdTe on Si) leads to misfit dislocations at the interface between the substrate and grown layer. These result in threading dislocations (TDs) that can “thread” up to the top surface of the layer. These crystalline defects can have several detrimental effects on an optoelectronic device:

- 1) TDs can provide rapid diffusion pathways for impurities into the material, which can lead to long term reliability issues.
- 2) TDs can create an electrical shorting path through the device, resulting in increased “dark current”, reducing the light detection sensitivity of the device. For a light emitter such as LED or LD, this results in loss of electrical energy as heat, reducing efficiency and possibly causing failure.
- 3) TDs can reduce the minority carrier diffusion length, which is a critical determinant of the light collection efficiency. Essentially, after electron-hole pairs are created by an incident photon, they need to be able to move to the contact layers before they recombine. The TDs act to accelerate this recombination process, resulting in lower performance.

Our Approach

Great progress can be made in high quality crystal growth on mismatched substrates through use of planar optimization techniques, such as the appropriate choice of “buffer” layers, (sometimes with graded composition or superlattice structure), multiple growth rates and temperatures, and stress relaxation anneals. An additional planar approach we investigate is the use of Silicon-on-Insulator (SOI) substrates, consisting of a thin (20 nm) single crystalline silicon layer floating on a 145 nm thick layer of silicon dioxide, attached to a bulk silicon substrate. Such substrates provide an additional mode of strain relaxation via the relatively compliant, non-crystalline silicon dioxide. Our comprehensive strategy for dislocation reduction includes the most effective planar optimizations for a particular material system, and the addition of nanopatterning, to work toward the best possible crystal growth on Si.

Nanoheteroepitaxy (NHE) is a strategy to annihilate threading dislocations before they reach the active volume of the device. The idea is to nucleate the crystal growth on nanoscale islands of material. Stresses generated during growth tend to push TDs toward the edges of the islands, so they will terminate on these edges rather than propagating up to the top portion of the layer. The process of lateral epitaxial overgrowth (LEO) is then used to coalesce the islands into a continuous layer of high crystalline perfection (i.e. low density of TDs). In principle, the technique is quite general, and pioneering work has been done in several optoelectronic material systems, with the underlying goal of reducing TDs that result from crystal growth on lattice mismatched substrates. Growth of InP on off-cut Si(100) was reported¹ in 1996 by Parillaud, et al., using a crystalline GaAs buffer layer and a patterned Si₃N₄ mask layer. LEO was achieved on this structure, resulting in a very low TD density of $< 10^5 \text{ cm}^{-2}$, compared to values around 10^7 cm^{-2} obtained using conventional planar growth methods. During the past decade, one of the present authors contributed to significant progress in the field, including successful

demonstrations of NHE growth of GaAs on Si(100),² GaN on 6H-SiC(001),³ and CdTe on SOI Si(100).^{4,5} Ongoing work at EPIR includes NHE growth of CdTe on Si(211) and HgCdTe/CdTe/Si(211), and has resulted in a US patent application.⁶

Detailed Implementation for HgCdTe Photodetectors

Current state-of-the-art infrared focal plane arrays (IRFPAs) are based on HgCdTe material epitaxially grown on bulk CdZnTe substrates, and use a hybrid technology in which HgCdTe detector arrays and Si readout chips are fabricated separately and connected element by element using indium bumps. The size of these IRFPAs is limited by the size of the available CdZnTe substrates and the thermal mismatch between CdZnTe and the Si readout circuit (thermal expansion coefficients: $4.8 \times 10^{-6} \text{ K}^{-1}$ and $2.3 \times 10^{-6} \text{ K}^{-1}$, respectively), which misaligns the photodiode array with respect to the Si circuit during heating and cooling cycles. Additionally, impurities out-diffusing from the bulk CdZnTe material can degrade system performance, and the overall mechanical strength of the substrates can be a serious concern. Having HgCdTe fabricated on Si-based composite substrates would eliminate the aforementioned drawbacks related to the HgCdTe/CdZnTe system. Indeed, the use of Si-based substrates would also lower detector costs and permit the realization of larger area arrays.

Molecular beam epitaxy (MBE) has emerged in recent years as a flexible manufacturing technology for IRFPA materials and offers the greatest control over crystal growth. The superiority of the MBE technology is further enhanced by the possibility of growing HgCdTe on alternate, robust and inexpensive substrates such as silicon. Over the past decade, several research and development groups, including EPIR Technologies Inc., the Microphysics Laboratory (MPL) at the University of Illinois at Chicago (UIC), the Night Vision Laboratory (NVL), the Army Research Laboratory (ARL), Teledyne, Raytheon Vision Systems (RVS) and Hughes Research Laboratory (HRL), have carried out intensive research on the growth of CdTe on Si by MBE. As a result of this community-wide effort, CdTe/Si has reached a level of maturity to compete with bulk CdZnTe as a substrate for SWIR and MWIR HgCdTe applications. The first MWIR 1024 x 1024 IRFPA using HgCdTe/Si grown at EPIR was fabricated by Rockwell Scientific (now Teledyne) in 1997.

When CdTe/Si(211) is used as a substrate for the MBE growth of $\text{Hg}_{0.78}\text{Cd}_{0.22}\text{Te}$, a lattice mismatch of 0.28% exists between the HgCdTe and CdTe. Such a lattice mismatch, although small, induces dislocations in the HgCdTe layer when the layer thickness is greater than the critical thickness, which in this case is less than 200 nm. This translates into a dislocation density of about 10^9 cm^{-2} at the HgCdTe/CdTe interface, which leads to dislocation densities typically in the 10^6 cm^{-2} range at the top of the HgCdTe surface after growth to a thickness of about 10 μm . It has been a major achievement to reach this level of crystal quality, considering the very large (19%) lattice mismatch in this system, but these dislocation densities fall well short of the $10^4 - 10^5 \text{ cm}^{-2}$ possible using the costly, bulk CdZnTe substrates. Although the dislocation densities achieved for HgCdTe/CdTe/Si have proven satisfactory for many SWIR and MWIR applications, they are unacceptable for LWIR applications involving low temperature and low background conditions, as a direct result of detrimental effects of TDs on electrical performance. We note that long-wave band infrared (LWIR, 8–10 μm) light is strongly emitted

by objects near room temperature, so that sensors of this type are most useful for the night vision and medical diagnostic applications mentioned above.

Our approach is to grow LWIR HgCdTe on CdTe/nanopatterned Si-based alternative substrates. Nanopatterned substrates provide 3-dimensional strain relaxation in contrast with two-dimensional strain relaxation for the case of planar substrates. We propose to grow high quality LWIR HgCdTe material using nanopatterned CdTe buffer layers grown on silicon substrates and CdTe epilayers grown on nanopatterned SOI substrates. Coalescence and novel defect reduction mechanisms are available when the substrate pattern dimensions are reduced to the nanoscale.⁷ The strain energy, which is proportional to the square of the strain in a material system, can be reduced by relaxing the mismatch strain in three dimensions on a nanoscale island, which is superior to the two dimensional strain relaxation that occurs in the case of a planar substrate.

For IRFPA applications, misfit dislocations at the interface with the substrate can be tolerated, provided the material is grown beyond the critical layer thickness for strain relaxation, the dislocations are contained at the interface and that threading defects are inhibited.⁸ However, based on the geometrical requirement that a dislocation must terminate at another dislocation, upon itself, or at a free surface,⁹ preventing threading dislocations is extremely difficult in planar heteroepitaxy.

The threading dislocation density is high in the case of high lattice-mismatch systems such as CdTe/Si because of the high strain at the interface. A reduction in defect density can be obtained by reducing the growth area, which suppresses various sources of misfit dislocations at different scales of patterning. For example, when patterning the growth area down to the 20 to 400 μm scale, misfit dislocation formation attributed to extrinsic nucleation sources present on the starting substrate is reduced proportionally to the growth-area diameter¹⁰ A different type of reduction in misfit dislocation density has also been reported when the growth area is reduced to the sub-micrometer dimension. In this case, the reduction is attributed to intrinsic strain energy considerations and strain relief at the edges of the crystal¹¹ The compliant substrate approach was proposed to mitigate strain in material systems¹² with high lattice mismatch, where the substrate is made thinner than the epilayer to be grown and is attached to a thicker handle substrate. Reductions in defect density in various material systems have been reported¹³ with this approach, but it requires a macroscopic motion that must occur between the compliant layer and the handle substrate¹⁴ as a function of the thermal mismatch.

EPIR Technologies has performed the MBE growth of HgCdTe on patterned CdTe/Si epilayers as part of an internal research and development program with encouraging results, including defect reductions with the reduction of mesa sizes. Circular mesas with diameters ranging from 80 to 320 μm were etched in thick CdTe epilayers grown on silicon substrates to form reduced area templates for subsequent HgCdTe growth. SOI substrates having a compliant (111) silicon layer of thickness 20 nm floating on 145 nm silicon dioxide attached to a handle (100) silicon substrate were used to grow CdTe. Bond x-ray and reciprocal space mapping (RSM) characterization of the grown CdTe epilayers indicate that the strain state of CdTe grown on SOI is different from the strain state of CdTe grown on bulk Si. Specifically, the RSM data indicates

a skew in the distribution of lattice constants towards compression. CdTe grown on SOI is under compressive strain in contrast to past observations of tensile strain in CdTe grown on conventional Si, a consequence of a difference in the thermal contractions of CdTe and Si from the growth temperature to room temperature. It was seen that the strain from the device layer of the SOI substrates decays over a distance of less than 1.5 nm, thus is effectively decoupled from the rest of the substrate.¹⁵ We plan to integrate reduced mesa sizes (to the nanoscale) with compliant substrates to result in the three-dimensional relaxation of strain in the highly lattice mismatched CdTe/Si system. As part of this work, strain partitioning in CdTe/Si was modeled for the growth of CdTe on planar silicon substrates and patterned SOI substrates.

CdTe on nanopatterned SOI substrates are fabricated by interferometric lithography and reactive ion etching. Interferometric lithography is a mask-less and relatively simple method of forming periodic arrays of sub-micron structures on the surface of a substrate that uses interference between coherent laser beams to define a pattern. Two-dimensional pillars in photoresist can be obtained from this process with feature dimensions down to 200 nm. Typical cross-sectional scanning electron microscopy (SEM) images of photoresist nanopillars obtained from the interferometric lithography process are shown in Figure 1.

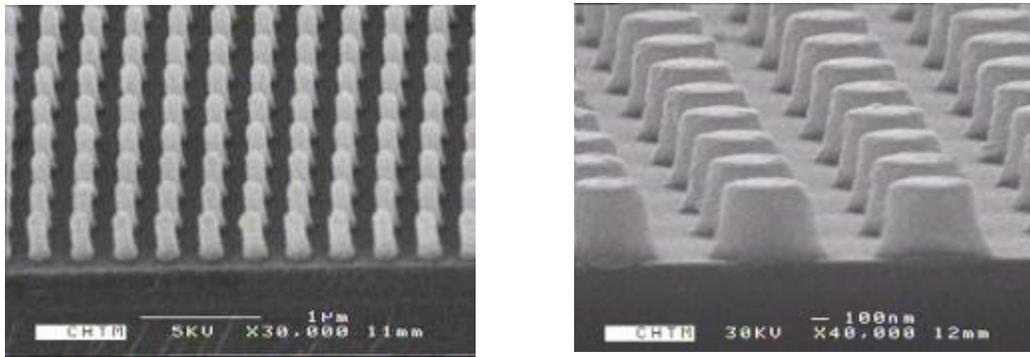


Figure 1: Cross-sectional SEM image of 500 nm pitch grating (left) and 360 nm pitch grating (right)

Following the interferometric lithography process, reactive ion etching was used to transfer the nanoscale patterns into the silicon layer. Strain partitioning in the CdTe/Si material system is effective when CdTe is initially nucleated selectively on the silicon nanoislands to form a 3-D crystal. This is to be followed by a transition from 3-D to 2-D growth to enhance lateral epitaxial overgrowth and leading to coalescence. We successfully grew CdTe selectively on nanopatterned SOI substrates with MBE, the details of which are discussed in this section. A two-step growth process was used to achieve selective CdTe growth, which was characterized by SEM and atomic force microscopy (AFM). Plan view SEM was used as an initial characterization step to observe the selectivity of CdTe on the islands. SEM images of the samples are shown in Figure 2.

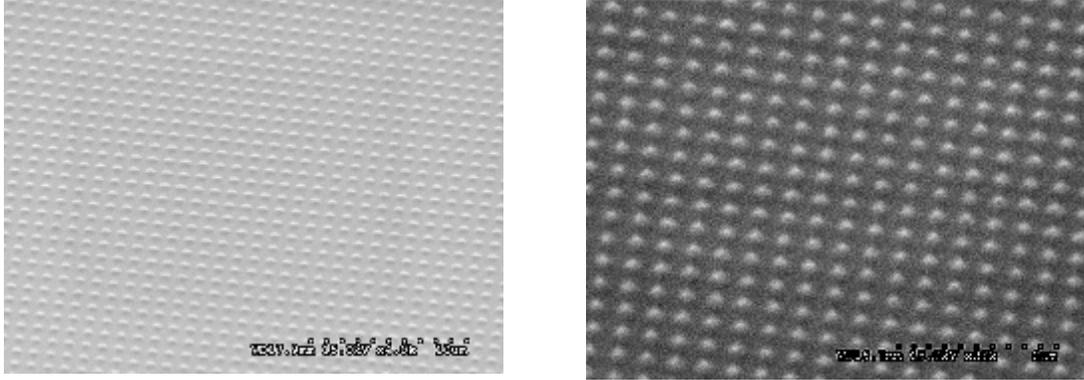


Figure 2: Two plan view SEM images of CdTe selectively grown on nanopatterned SOI substrate

X-ray diffraction (XRD) measurements indicates that the selectively grown CdTe is single crystalline and corresponds to the (111) orientation that is usually found on the Si(100) substrates. These results validate that the MBE growth technique can be used to achieve selective epitaxy of CdTe on patterned substrates and obtain single crystalline epitaxial material.

Lateral epitaxial overgrowth of CdTe on nanopatterned substrates

In the case of nanopatterned substrates, we showed that it is possible to achieve coalescence even with the growth of a thin CdTe epilayer. The coalescence achieved is non homogeneous at this time, as can be seen from the SEM images. Lateral epitaxial overgrowth (LEO) of CdTe and coalescence are shown in SEM images in Figure 3.

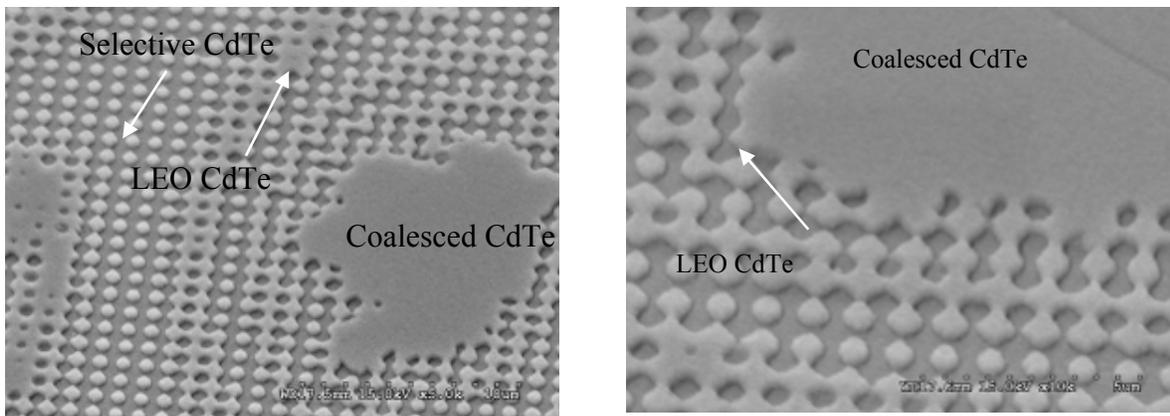


Figure 3: LEO and coalescence of CdTe on nanopatterned SOI substrates.

A similar process was developed to pattern CdTe islands on bulk Si wafers (not SOI). A novel reactive ion etch process was developed to form the nanoscale CdTe islands. We are able to achieve lateral epitaxial overgrowth of CdTe on the nanopatterned CdTe islands with a two-step MBE growth process. The SEM images of Figure 4 show the uniformity in the increase of the CdTe island diameters. It can be seen that some of the islands form nanobridges. We find initial stages of coalescence on some areas of the samples, as shown in Figure 4.

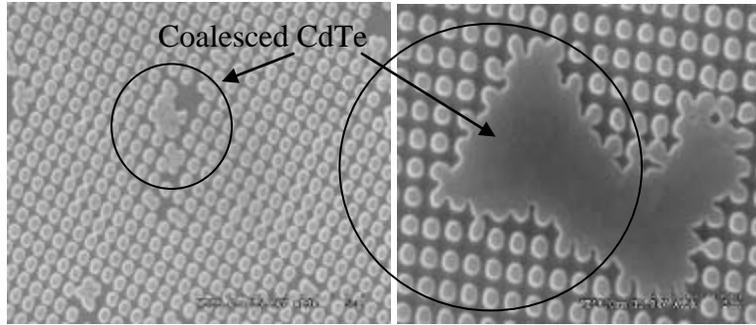


Figure 4: Four SEM images showing areas where CdTe coalesced on a nanopatterned CdTe Sample

High magnification SEM images of regrown CdTe, as seen in Figure 4, show that some regions on the sample have completely coalesced due to the increased dimensions of the nanoislands. The coalesced regions show smooth surface morphologies, indicating the coherence of the coalescence process. No grain boundaries can be seen, which provides evidence of the isotropic nature of the growth on the nanoislands.

Defect characterization was performed on selectively grown CdTe on nanopatterned CdTe buffer layers by cross-sectional TEM measurements. Cross-sectional TEM images of the selective CdTe grown on nanopatterned CdTe buffer layers are shown in Figure 5.

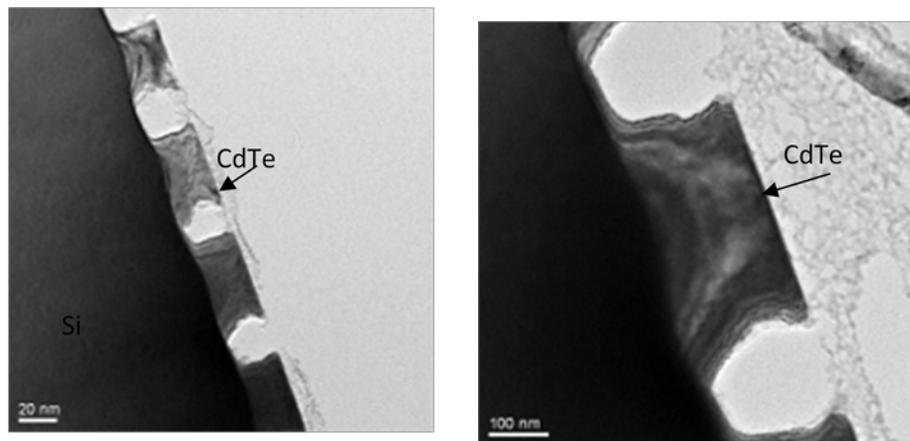


Figure 5: Two low resolution cross-sectional TEM images of CdTe grown on nanopatterned CdTe buffer layers

The TEM images show CdTe islands approximately 200 nm high and 300 nm in diameter with epoxy glue on the top of the islands. The interface between CdTe and the regrown CdTe is not clearly visible. The CdTe islands show no defects. Higher magnification TEM images were taken to characterize a single CdTe island and the corresponding images are shown in Figure 6.

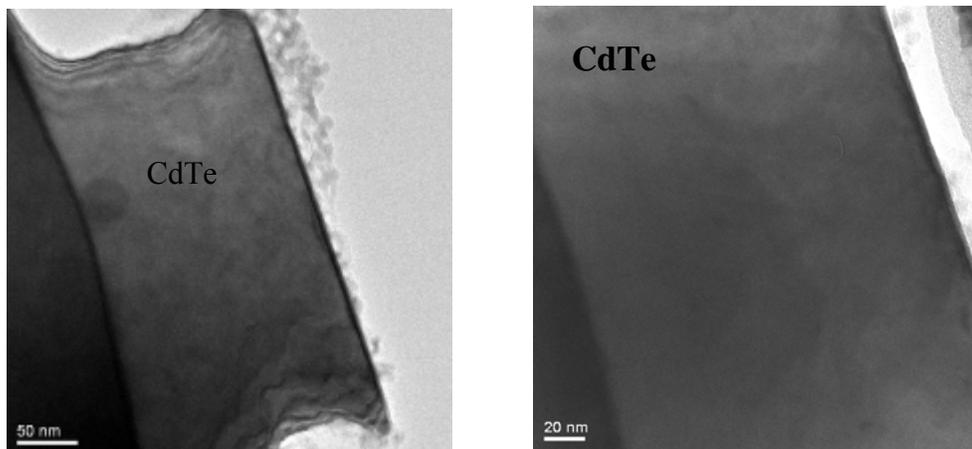


Figure 6: Two high magnification TEM images of CdTe regrown on nanopatterned CdTe buffer layers.

The TEM images in Figure 6 show that there is no evidence of threading dislocations in the CdTe nanoislands. The interface between the CdTe island and the regrown CdTe nanoisland is not clearly visible, which is an indication of the quality of the regrown material. The CdTe epilayer is devoid of any dislocations, which is a consequence of the strain relaxation in 3-dimensions at the nanoscale. This is a major breakthrough in reducing strain-induced mismatch defects in high lattice mismatch systems such as CdTe/Si. We have demonstrated that we can grow essentially defect-free material by using nanopatterned substrates.

Potential Role of the NIST TIP

This technology has the potential to provide a quantum leap in performance vs. cost of optoelectronic devices. Laboratory scale work is going on at various institutions, but none has reached the point of commercialization. Although the NHE process is conceptually straightforward and can be accomplished using established tools, it remains relatively undeveloped compared to conventional planar growth methods. A NIST program could promote synergy between research efforts focused on disparate material systems and applications, and to help the US sustain leadership in developing this new wave of high-performance low-cost optoelectronics.

REFERENCES

- ¹ O. Parillaud, E. Gil-Lafon, B. Gerard, P. Etienne, and D. Pribat, "High quality InP on Si by conformal growth," *Appl. Phys. Lett.* **68**, 2654 (1996).
- ² D.Zubia, S.Zhang, R.Bommena, X.Sun, S.R.J.Brueck and S.D.Hersee "Initial Nanoheteroepitaxial Growth of GaAs on Si (100) by OMVPE", *J. Electron. Mater.*, **30**, 812 (2001).
- ³ X.Sun, R.Bommena, D.Burckel, M.Wrback, S.R.J.Brueck and S.D.Hersee "Defect reduction mechanisms in Nanoheteroepitaxy of GaN", *J. Appl. Phys.* **95**, 1450 (2004).
- ⁴ R. Bommena, T. Seldrum, L. Samain, R. Sporcken, S.R.J. Brueck and S. Sivananthan, "Strain reduction in CdTe grown on nanopatterned SOI substrates", *J. Electron. Mater.* **37**, 1255 (2008).
- ⁵ R. Bommena, C. Fulk, J. Zhao, T.S. Lee and S. Sivananthan, "Cadmium Telluride growth on Patterned Substrates for Mercury Cadmium Telluride Infra-Red Detectors", *J Electron. Mater.* **34**, 704 (2005).
- ⁶ R. Bommena, M. Carmody, S. Sivananthan, "Nanostructures for Dislocation Blocking in Group II-VI Semiconductor Devices," US Patent Application No. 12/331,892 Reference No. 33176.000022.
- ⁷ S. Luryi and E. Suhir, "New approach to the high quality epitaxial growth of lattice-mismatched materials," *Appl. Phys. Lett.* **49**, 140 (1986).
- ⁸ R. Hull and J. C. Bean, "Misfit dislocations in lattice-mismatched epitaxial films," *Critical Reviews in Solid State and Materials Sciences* **17**, 507 (1992).
- ⁹ J. P. Hirth and J. Lothe, *Theory of Dislocations* (John Wiley & Sons, Inc., New York, Ch. 1-7 (1982).
- ¹⁰ E. A. Fitzgerald, G. P. Watson, R. E. Proano, D. G. Ast, P. D. Kirchner, G. D. Pettit, and J. M. Woodall, "Nucleation mechanisms and the elimination of misfit dislocations at mismatched interfaces by reduction in growth area," *J. Appl. Phys.* **65**, 2220 (1989).
- ¹¹ S. Guha, A. Madhukar, and L. Chen, "Defect reduction in strained $\text{In}_x\text{Ga}_{1-x}\text{As}$ via growth on GaAs(100) substrates patterned to submicron dimensions," *Appl. Phys. Lett.* **56**, 2304 (1990)
- ¹² Y. H. Lo, "New approach to grow pseudomorphic structures over the critical thickness," *Appl. Phys. Lett.* **59**, 2311 (1991).
- ¹³ P. D. Moran, D. M. Hansen, R. J. Matyi, J. G. Cederberg, L. J. Mawst, and T. F. Kuech, "InGaAs heteroepitaxy on GaAs compliant substrates: X-ray diffraction evidence of enhanced relaxation and improved structural quality," *Appl. Phys. Lett.* **75**, 1559 (1999).
- ¹⁴ J. S. Speck, A. E. Romanov, P. Chavarkar, S. K. Mathis, A. M. Andrews, L. Zhao, and U. K. Mishra, "Approaches to low threading dislocation density materials and related modeling," presented at the International Conference on Compliant & Alternative Substrate Technology, Orlando Florida, September 19, 1999.
- ¹⁵ A. R. Chowdhuri, D. Jin, C. G. Takoudis, "SiO₂/Si(100) interface characterization using infrared spectroscopy: estimation of substoichiometry and strain," *Thin Solid Films* **457**, 402 (2004).