Project White Paper

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Critical National Need Idea Title:
U.S. Leadership in Process & Capability Development in Advanced Three-Dimensional Packaging

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Critical National Need

Demand for smaller yet higher-performing microelectronic devices is escalating. Until recently the semiconductor industry has relied on device scaling to shrink transistor size and double transistor density more or less every 2 years in accordance with Moore's Law. However, growing limitations with power dissipation, signal latency, and the availability of cost-effective patterning processes have rendered device scaling a much less feasible endeavor. This has led research to move in alternate directions. The prevailing technology pathway seems to be three-dimensional (3D) fabrication. This has led to 3D packaging concepts such as electrical redistribution and 3D vertical integration. In the latter, the 3D through-silicon via (3D-TSV) approach is proving to be the next technological leap in the semiconductor industry. It can offer exceptional benefits for new military microelectronics where size, weight, and power consumption are constant concerns. At the same time, the U.S. military has an extraordinary need for heterogeneous microelectronic systems that integrate a broad array of sensors, microprocessors, actuators, and controls. 3D-TSV provides one of the best frameworks for developing and manufacturing these systems with flexibility and reliability. At this time, most of the manufacturing developments for 3D-TSV technologies are slated for non-U.S.–based companies with locations mainly in the Asia-Pacific region. If this development occurs, the United States will lose technical and manufacturing expertise in a technology that will dominate the semiconductor industry for decades to come. At the same time, a solid 3D-TSV development and manufacturing infrastructure may not even be established domestically to meet future military device packaging needs and maintain technology leadership. Figure 1 shows the current key players in 3D technology. As shown, there are very few U.S. companies working in this area, let alone leading the development. The development of 3D-TSV technology has significant technical hurdles to overcome as well. The formation of a TSV is a multi-step process that utilizes several known processes as well as several processes yet to be developed. There is a national need to further develop the technologies involved and drive the

techniques to a real world solution as quickly as possible to build and secure U.S. leadership.

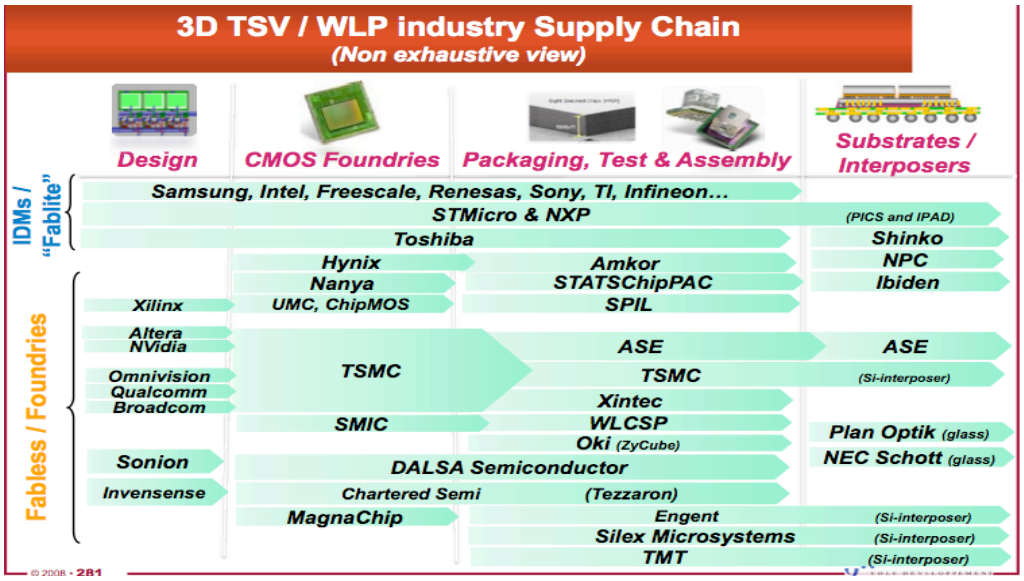

Figure 1. Key players in 3D-TSV technologies.
[Source: Yole Développement, 2008.]

Societal Challenge

As mentioned previously, with the need for alternate solutions for advancement in semiconductor technology, 3D packaging is showing great promise. At the 2006 IEEE International Electron Devices Meeting, Dr. C.-G. Hwang, president and CEO of Samsung Electronics, stated that "*rapid adoption of 3-D integration technology seems to be essential and, thankfully, unavoidable*." 3D integration offers many potential benefits that help to solve many problems with today's technologies. They include:

- Higher system functionality through heterogeneous integration of different device types into one package (microprocessors, memory, MEMS, photonics, etc.)
- Increased data bandwidth and processing speed (shorter chip-to-chip interconnections reduce signal delay and propagation loss versus conventional through-board interconnects or wire bonding)

- Increased system yield and reliability (more devices in one package)
- Smaller form factor (smaller size and lighter weight)
- Reduced power consumption (many resistive losses from long metal interconnections)
- Lower cost (eliminates many individual chip packages).

Many important product advances will be made possible by these technology benefits. Examples of such pivotal advanced products include smart sensors used in military applications and the medical field. These sensors are fabricated by coupling sensors, processors, and communication devices to form mini-computers that can be very small and robust. The major benefits from these types of devices are that they possess extremely advanced capabilities yet are small enough to go places where existing technology cannot. For example, they can be placed in the human body and provide feedback to medical personnel in real time with improved accuracy over standard processes. A recent example of product advancement using 3D packaging in Class I medical devices was demonstrated in smaller, more powerful hearing aides [Dzarnoski, 2008]. Other examples, include more powerful cellular phones, pocket personal computers, global positioning devices, and many more.

One of the key issues in 3D integration is the method of information transfer and the supply of electric power among stacked chips. There are many methods to connect between devices such as wire-bonding, edge connect, capacitive or inductive coupling [Motoyoshi, 2009], and direct contact using TSV technology. TSV is capturing much attention, as it fundamentally solves many of the packaging issues. One of its main technology hurdles, yet to be fully developed, is temporarily supporting the device wafer during the creation of the TSVs. Development of TSVs requires thinning of the device substrate to allow for proper contact dimensions from one side of the substrate to the other. During

this thinning operation, the device substrate becomes very fragile. To accommodate this fragility, temporary bonding of a device wafer to a carrier wafer is the preferred technology. There is a significant challenge to establish a robust technique to accomplish supporting the device wafer. This and other technology development areas are of great importance to enable the U.S. to secure a leadership role in next-generation semiconductor technologies.

Transformational Result

The establishment of full process capability and leadership in the development of 3D-TSV technology will serve as a catalyst for U.S. semiconductor and packaging manufacturers and their suppliers to maintain and advance our role and responsibilities in both the domestic and the world economy. The key outcomes for this activity can be summarized accordingly:

- Shortened “time to market” of 3D-TSV technology and manufacturing
- Creation of a domestic resource for development and integration of advanced semiconductor packaging technologies
- Support for U.S. military and industry 3DP-TSV technology requirements for the next several decades
- Enhanced and sustained 3DP-TSV technology leadership and related critical U.S.-based manufacturing
- Growth in high-tech employment and education opportunities
- Establishment of a pilot line option for U.S. semiconductor and packaging companies
- Support for critical defense-related manufacturing needs for 3D-TSV.

Proposed Solution

The microelectronics industry is turning to 3D packaging technologies to extend Moore’s Law and achieve the processing power and speed benefits that are no

longer attainable through device scaling [Compardo et al., 2009; Carson et al., 2009; Garrou et al., eds., 2008; Ramm and Taklo, 2008; Lu et al., 2007]. 3D packaging utilizes vertical stacking and interconnection of integrated circuits and other single-plane microdevices, such as MEMS, to create microelectronic systems that have smaller form factors, reduced power consumption, and less signal propagation loss. Figure 2 depicts several of today's leading approaches for advanced semiconductor packages. TSV technology, in which devices are connected directly through the chip stack, offers the highest circuit density and presumably the highest reliability because of the near monolithic structure that it enables. The superiority of the TSV approach for different device types is evident from the comparisons of various 3D packaging schemes shown in Table 1.

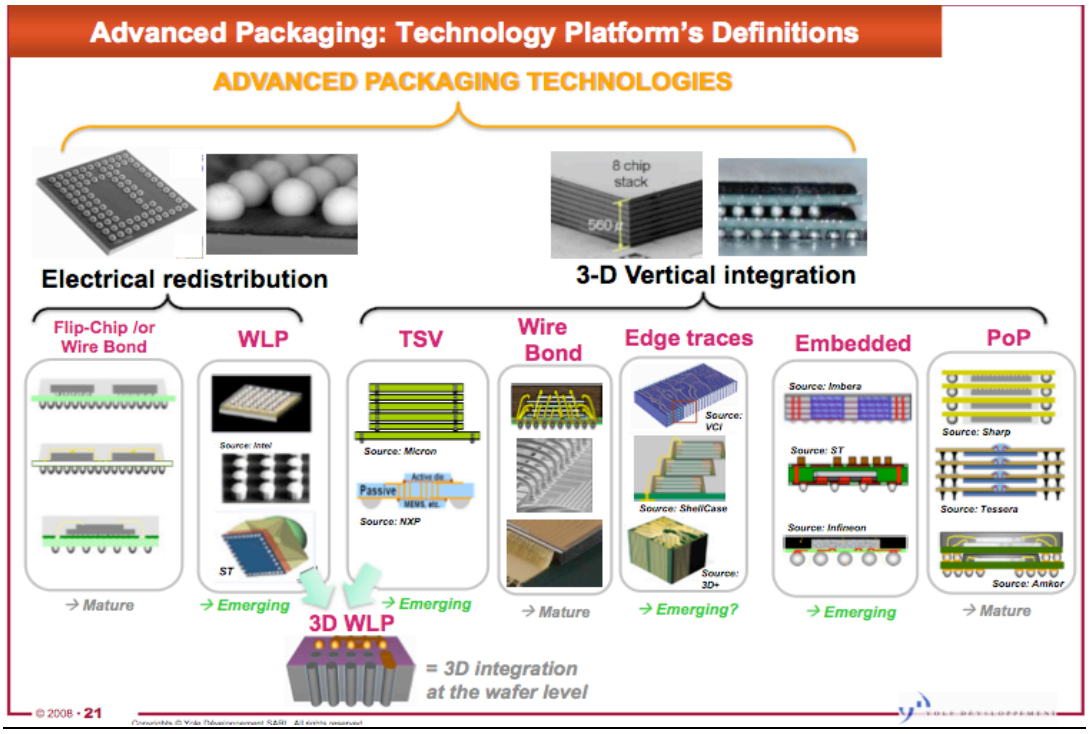

Figure 2. A summary of the leading advanced packaging technologies. [Source: Yole Développement, 2008.]

Table 1. 3D integration technologies and potential applications.
[Source: Yole Développement, 2008.]

The vision presented here is to develop U.S. process leadership and capability in advanced packaging research and development including manufacturing methodology in an integrated solution for 3D-TSV technologies to benefit both the commercial and defense-related device markets. The effort would focus on thin wafer handling as used in TSV processing, specifically associated with supporting the fragile device wafer during and after backgrinding. As mentioned previously, backgrinding or thinning is used to obtain proper thickness of the substrate prior to making connections from one side of the device substrate to the other. In parallel, development of the remaining processes for TSV creation would be studied via alliances with other U.S. government entities, consortia, and private companies. These alliances would allow both full TSV process development as well as U.S. capability development to occur. The ultimate goal is to lead the technological development and build the associated infrastructure required for next-generation semiconductor manufacturing

Entities That May Be Interested in Funding the Proposed Solution(s)

Several Government agencies would benefit greatly by the establishment of the United States as the world leader in 3D-TSV technology. The following agencies may be interested in funding the proposed solution(s):

- U.S. Department of Defense (including U.S. Army, U.S. Air Force, U.S. Navy)
- DARPA
- Missile Defense Agency
- National Science Foundation
- Office of Naval Research
- U.S. Department of Energy

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