Medium Voltage SiC R&D update

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NEXT GENERATION SiC MOSFETS – OVER 5 YEARS IN THE MARKET

Gen 2 DMOS

Commercially released in 2013 as “C2M” product family at 1.2-1.7kV

Gen 3 DMOS

Commercially released in 2015 as “C3M” product family at 900V

Same high reliability DMOS Structure, but optimized to dramatically reduce die size

Smaller pitch

Optimized doping
WOLFSPEED NEXT-GEN SiC DMOS LOWERS SPECIFIC $R_{D\text{SON}}$ DRAMATICALLY


New 900V SiC MOSFET released is 2.3m$\Omega\cdot$cm$^2$
3.3kV, 45mΩ SiC MOSFET CHIP $R_{D_{SON}}$ vs T and $I_{DS}$

- 2.5X increase in $R_{D_{SON}}$ from 25°C to 150°C
- Positive temperature coefficient
- Devices can be readily paralleled

3.3kV, 45mΩ SiC MOSFET CHIP $R_{DSON}$ vs $V_{GS}$

- At temperature, little change in $R_{DSON}$ above $V_{GS}=+14V$
- At 1.8kV, 20A (1/2 rated current), $E_T = 1.1mJ$ (858 uH load)

3.3kV, 45mΩ SiC MOSFET CHIP BODY DIODE

- SiC body diode can eliminate external anti-parallel SiC diode
- Elimination of external anti-parallel diode saves cost and space
- Third quadrant operation of MOSFET possible for additional savings

3.3kV/180A SiC HALF-BRIDGE EVALUATION MODULE

For Quick Evaluation

- Each switch position contains:
  - Four (4) 3.3kV SiC MOSFETs (~45A each) and
  - Four (4) 3.3kV anti-parallel SiC diodes (~45A each)
- 62mm module / No snubber used

3.3kV SiC MOSFET chip

- $V_{DS}$: 3300 V
- $I_D (T_C=90^\circ C)$: 45 A
- $R_{DS}(25^\circ C)$: 45 mΩ

3.3kV SWITCHING LOSS PERFORMANCE @ 25°C
Double Pulse Test

Vlink = 2.2 kV, Rg_ext = 2.5 Ω

Vlink = 2.2 kV, Ids = 250 A

• At 2.2kV, 180A switching event, 45mJ total switching energy
• 3.3kV SiC MOSFETs switching losses are 10-15x lower than 3.3kV Si IGBTs

250A/2.2kV SWITCHING EVENT WITH RG_EXT = 2.5 Ω

Switching speed <150ns; minimal overvoltage (no snubber)

Improved Gen three 3.3kV, 40mΩ SiC MOSFET chip
IMPROVED GEN THREE 3.3kV/40mΩ SiC MOSFET

• 8.5% Reduction in Die Size
• 13.6% Improvement in $R_{DSON}$

Preliminary 3.3kV SiC MOSFET Design
• $R_{DS,ON} = 46.9$ mΩ
• Die Area = 46.7 mm$^2$

Improved 3.3kV SiC MOSFET Design
• $R_{DS,ON} = 40.5$ mΩ
• Die Area = 42.7 mm$^2$
**SiC XHP™ STYLE MODULE - INDUSTRY STANDARD HOUSING**

- Engineering Sample sales
- Up to 12 MOSFETs/switch available
- Ultra-Fast Switching, Low Inductance (<20 nH V+ to V-)
- Companion gate driver
  - Desaturation protection, temperature sensing, programmable UVLO with hysteresis, galvanic signal isolation, & on-board isolated power supplies.

**3.3 kV SiC HALF-BRIDGE POWER MODULE**

- **N-Channel MOSFET**

**FEATURES**
- High Voltage: $V_{DS} = 3.3$ kV, $T_{j(\max)} = 175$ °C
- AS9100C: Rev. C-Certified Manufacturing,
- Traceable Throughout Value Chain
- Ultra-Fast Switching, Low Inductance
- Enables High System Efficiency
- "XHP" Style Half-Bridge Power Module

**APPLICATIONS**
- Solid-State Transformers
- Medium Voltage Drives
- Solid-State Circuit Breakers
- Smart Grid / Grid-Tie Distributed Generation
- Energy Storage Systems

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**Power Module Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition(s)</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DSS}$</td>
<td>Drain-Source Voltage</td>
<td></td>
<td>3300</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GSS}$</td>
<td>Gate-Source Voltage</td>
<td></td>
<td>-8/+19</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Continuous Drain Current</td>
<td>$T_C = 25$ °C, $T_J = 175$ °C</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Maximum Power Dissipated</td>
<td>$T_C = 25$ °C, $T_J = 175$ °C</td>
<td>2586</td>
<td>W</td>
</tr>
<tr>
<td>$T_{J(\max)}$</td>
<td>Maximum Junction Temperature</td>
<td></td>
<td>175</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature Range</td>
<td></td>
<td>-55 to 175</td>
<td>°C</td>
</tr>
</tbody>
</table>
Gen three 6.5kV, 100mΩ SiC MOSFET chip
• Nominally a 30A SiC MOSFET
• $R_{DS\text{ON}_{\text{max}}}$ at room temp $\sim 100\,\text{m}\Omega$
• $R_{DS\text{ON}_{\text{max}}}$ at 90 °C $\sim 171\,\text{m}\Omega$
  — all parameters subject to change without notice
Improved Gen three 10kV, 350mΩ SiC MOSFET chip
Measured I-V Characteristics at 150°C of Enhanced Short Circuit Capability and Baseline Gen3 10 kV/350 mOhm SiC MOSFETs

- Very Small Difference in On-Resistance ($R_{DS,on}$) at 150 °C
- Enhanced Short Circuit 10 kV SiC MOSFET has Higher Threshold Voltage
Short Circuit Simulation/Test of Gen 3 10 kV/350 mOhm SiC MOSFETs With Enhanced Short Circuit Capability

- Demonstrated Gen3 10 kV/350 mOhm SiC MOSFETs Capable of Sustaining Short Circuit Current For > 13 µsec at 5000V
- Measurement and Simulation Courtesy of Al Hefner at NIST
Conduction/Switching Measurements and Model of Enhanced Short Circuit Capability Gen3 10 kV/350 mOhm SiC MOSFETs

200 W/cm² @ 10A

Area: 0.312 cm²
125 °C

- - - Measured
— — Simulated

Drain Current (A) vs. Drain-Source Voltage (V)

Drain Current (A) vs. Time (µs)

Voltage = 8 kV

Area: 0.312 cm²
25 °C

- - - Measured
— — Simulated

• Measurement and Model
  Courtesy of Al Hefner at NIST
10kV Switching Measurements

A. ½ Bridge Configured Measured Switching Energies and Waveforms
B. Boost Configured Switching Energies
½ BRIDGE CONFIGURED MEASURED SWITCHING ENERGIES AND WAVEFORMS

\[ E_{TS} = 21 \text{mJ} \text{ at } 7\text{kV}, 15\text{A}, \]

½ bridge configuration used for switching measurements of a 10kV, 345mΩ SiC MOSFET in both the high position and low positions.

• New R&D 10kV SiC MOSFETs > 40X lower switching losses than 6.5 kV Si IGBT in boost configuration
  • Peak switching voltage set by overshoot and cosmic ray FIT – potentially much less de-rating in SiC vs Si

10 kV BODY DIODE STATIC CHARACTERISTICS

- 10 kV body diode is bipolar – lower resistance than a 10 kV JBS diode at high temperatures
- Reverse conducting antiparallel JBS diode can be eliminated

10 kV BODY DIODE REVERSE RECOVERY

- 10 kV body diodes show low reverse recovery

10kV SiC MOSFET XHV-6 POWER MODULE

Key Features

- 10 kV / 240 A, half-bridge power module
- 18 10 kV / 350 mΩ MOSFETs per position
- Low inductance power (~ 16 nH) and gate (~ 10 nH) loops
- Low Rjc (0.026 °C/W per half-bridge switch position)
- Can be configured as a 3-phase module
- Reworkable submodules
- Meets UL 840 and IEC 60664-1 creepage/clearance for a 15 kV module
- Mounts to standard 3x EconoDUAL footprint coldplate

Funded by ONR
PM: Lynn Petersen

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PROTOTYPE GATE DRIVER WITH TARGET >100 kV/μs CAPABILITY

Gate Driver output with custom totem pole. Max peak current >70 A

Non-Isolated DC/DC regulation
Unregulated 10-30V to +20/-5V, or +15/-4V

Fiber-optic control signals, non-isolated side would be on a separate board in final implementation

HV unregulated Isolated (>10kV) Power Supply 20-30V input to 15-30V output
SUMMARY

- SiC MOSFETs released over 5 years ago
- Gen 3 SiC MOSFETs released beginning in 2015 at 900V;
- Gen 3 SiC MOSFETs engineering samples at 1.7kV, 3.3kV, 6.5kV and 10kV
- Modules available
  - Companion gate drivers/power supplies for all modules available
  - 1.7kV modules using Econodual™ based design
  - 3.3-6.5 kV module
    - (Infineon XHP™ standard footprint)
    - Internal design is customized to enable SiC high switching frequency operation with low loop inductance <20 nH
  - 10kV SiC MOSFET XHV-6 Power Module
    - Up to 240A, half-bridge topology