SIC MANUFACTURING IN THE FOUNDRY MODEL
SEPTEMBER 2014
Company History

**SiC Research**
Launched by Rutgers University

- **1999**
  - **Prototypes** DC-DC Converters, High Frequency Power Switch, SiC Modules for DOD, DOE

- **2002**
  - Prototypes of SiC Schottky Diodes, MOSFETs, JFETs

- **2005**
  - **ACQUIRED BY DOLCE MGMT TEAM**

- **2009**
  - New HQ Established
    - Built in-house 4”FAB

- **2010**
  - **Fab-Lite model**
    - On-Line With Foundry Partner To Increase Capacity

- **2012**
  - Q1: Production Release xR
    - 1200V & 650V JBS Diode Series
      - 1200V Normally-on JFETs

- **2014**
  - Q4: Production Release
    - 1200V Cascode Series

Princeton, NJ
“Einstein’s Alley”
<table>
<thead>
<tr>
<th>JBS</th>
<th>JFET</th>
<th>MOSFET</th>
<th>IC</th>
</tr>
</thead>
<tbody>
<tr>
<td>![Diode Icon]</td>
<td>![JFET Icon]</td>
<td>![MOSFET Icon]</td>
<td>![IC Icon]</td>
</tr>
<tr>
<td><strong>650V – 16kV</strong></td>
<td><strong>650V-6.5kV</strong></td>
<td><strong>1200V – 10kV</strong></td>
<td><strong>50V</strong></td>
</tr>
<tr>
<td>Low $V_F$ &lt;br&gt;Zero $Q_{RR/\text{TR}}$ &lt;br&gt;175°C package &lt;br&gt;250°C die</td>
<td>Normally On &amp; Off &lt;br&gt;Ultra low FOM &lt;br&gt;Minimal $E_{ON}$ &amp; $E_{OFF}$ &lt;br&gt;175°C package &lt;br&gt;250°C die</td>
<td>Low $R_{DS(ON)}$ &lt;br&gt;Low $Q_{GD, G}$ &lt;br&gt;150°C</td>
<td>500°C $T_{J(\text{MAX})}$</td>
</tr>
</tbody>
</table>
6.5KV N-off JFETs

- **Rdson** = 350 mΩ

6.5KV JBS Diodes

- **Ir < 500 μA**
- **VDS = 6500V**
History of the foundry model in power devices

1970s-1990s
Power Discretes use custom processes and architectures. Fabs work with previous generation CMOS equipment.
Top suppliers own their FABs (5in-6in)

Late 90s-2000s
8inch Foundry model appears for low voltage MOSFETs – while most incumbents are still at 6inch

2005-2008
8inch Foundry model applied to FS-IGBTs and Superjunction technologies. Top suppliers still operate in-house FABs.

2008-today
Expansion to 12inch limited. New FAB investments small - most suppliers trying to exploit overcapacity at 8inch.
Outsourcing older tech to meet demand.

Outsourcing older tech to meet demand.
The foundry model in SiC

**PROS**

- Silicon foundries bring a lot of established baseline expertise and manufacturing discipline
- High uniformity and high throughput processing equipment
- Foundries of sufficient scale with a solid (non-SiC) base business can offer reduced process costs
- By aggregating the SiC business from multiple companies, they can generate more economies of scale
- Capital efficient for ramping volume production

**CONS**

- Most foundries need consigned equipment to enable a SiC process
- Concerns about IP protection – exclusivity can defeat the cost benefit from volume aggregation.
- Speed of technology development
- Volume projections in the near term 2-3 years are still too low to justify large investments
- Capacity and engineering resource allocation
## Economics of 6inch foundry process costs

<table>
<thead>
<tr>
<th>Fab size</th>
<th>Fab Outs/mo</th>
<th>Monthly Running costs</th>
<th>Cost/Wafer at 80% utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small</td>
<td>1000</td>
<td>$1,000,000</td>
<td>$1,250</td>
</tr>
<tr>
<td>Small</td>
<td>10000</td>
<td>$2,000,000</td>
<td>$250</td>
</tr>
<tr>
<td>Medium</td>
<td>30000</td>
<td>$3,000,000</td>
<td>$125</td>
</tr>
<tr>
<td>Large</td>
<td>60000</td>
<td>$4,000,000</td>
<td>$83</td>
</tr>
</tbody>
</table>

- Total fab volume and utilization drive costs – must find SiC volume drivers, or share the factory with other volume contributors
- High cost tools with limited throughput drive up costs – SiC has several such bottlenecks in epi, implant, backgrind, saw. These are being rapidly improved.
Epi cost dominates present day SiC high voltage costs – area needing rapid improvement in throughput without worsening quality

For pure unipolar devices (JBS Schottky, MOSFET, JFET), several large chips needed for meet the current requirements.
• Unipolar device costs always increase with voltage rating since $R_{dsA} \propto BV^{2.5}$
• Flattening the epi cost curve can drive down costs substantially
• Long term: need to get bipolar options to flatten the $R_{dsA} – BV$ relationship
• The foundry model brings down wafer FAB costs, allow volume ramp with targeted capital expenditures, and brings Si high volume manufacturing capability to SiC.

• This translates both to stable high yields, as well as the ability to quickly deliver large volumes.

• Technological progress is needed and ongoing to drive down epitaxy costs for >3300V devices.

• Insertion of medium voltage diodes into IGBT modules can bring benefits in efficiency and improved operating lifetimes from lower operating temperatures.

• HV transistor solutions have a lot of promise, and initial products must be seeded to allow engineers to work on all the system issues with fast switching at 5-10KV.
Thank You!

USCi Welcomes Your Questions

United Silicon Carbide
732-355-0550