

Georgia Research Tech Institute

# Microfabricated Symmetric Ion Trap for Quantum Information Processing\*

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### **Objective**

Design, fabricate and test scalable microfabricated ion traps based on the needs of the experiment for quantum computation and simulation

- Ion traps are to contain 20-100 ions in linear, equally spaced ion chains, stable for times required for the quantum simulations (~>seconds)
- Optical access to the traps are to be consistent with the Raman control and cooling laser beams.

#### **Current trap design**

- Symmetric trapping potentials
- Deep trap (~1eV for Yb) stable, long lifetime ion chains
- Control of compensation and principal axis orientation
- Through wafer optical access with angle etch
- Reduced laser scattering and oxide charging



### Design

Most current designs of the microfabricated ion traps are planar and ions are trapped above the surface. While these designs are scalable they suffer the challenges of shallower trap depths and light scattering due to roughness of the surface. This novel multilevel design provides much deeper trap depth and optical access combined with the scalability that microfabricated traps offer.

#### **Dimensions criteria**

- Optimum electrode width (60um) to minimize equal ion spacing
- Slot width (125 um) chosen to be large enough for optical access and to minimize light scattering but small enough to
- keep the RF and DC voltages in a manageable range Inter-electrode gaps chosen to maximize the critical dimension
- tolerance avoiding vapor arching emissions.







### Linear chain optimization

Linear chain optimization code, developed at GTRI, is used to

- Find the control voltages
- Space ions equally and associated errors
- Optimize electrode widths while minimizing the equal spacing errors



## **Fabrication**

•Fabrication in progress in Nanotechnology Research Center at Georgia Tech

- \*Developed Processes:
- \*Low stress PECVD oxide and LPCVD nitride depositions \*Uniform and repeatable metal deposition using RF sputtering \*Feature definition via plasma RIE and ICP etching and wet
- Feature definition via plasma RIE and ICP etching and wet etching using EGBOE
- •Contact lithography for electrode, loading slot, via and recessed wire bonding pad patterning

Carlo Carlos

•KOH back side wet etch is developed





SEM micrographs of device at different steps of the buildup

### Structure buildup



#### 20 ions with uniform 10µm spacing, $^{171}\text{Yb}^{*},\,\Omega_{\text{RF}}$ = 60 MHz, $V_{\text{RF}}$ = 250 V peak

## **Closely coupled design, fabrication and testing**

### **GTRI facilities**

•Traps are fabricated at Georgia Tech's Nanotechnology Research Center (NRC)

•40Ca+ trapping with flexible data acquisition system

•Multiple chambers for rapid turnaround of devices under test (up to 98 connections)



Iultiple Vacuum Chambe



Gen 2

#### **Future work**

- Optimize ion chain lifetimes and lengths
- Understand chain lifetime vs. chain length, e.g. collision models
- Photo-emitted electrons associated with high intensity laser pulses could disrupt ion chains
- Understand quantum simulation errors associated with trap parameters.



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