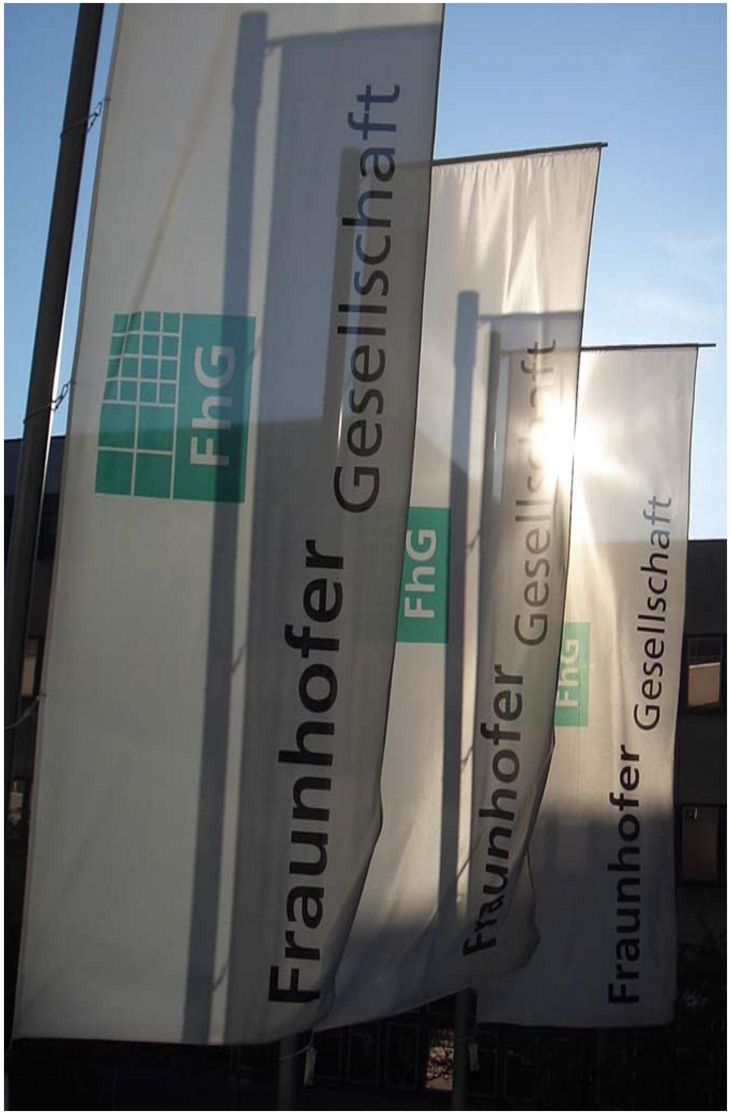
Metrology and Failure Analysis for 3D IC Integration



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Fraunhofer IZFP Dresden
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CNSE at the University at Albany/NY, USA

Grenoble, 26 May 2011

www.nanoanalysis.fraunhofer.de

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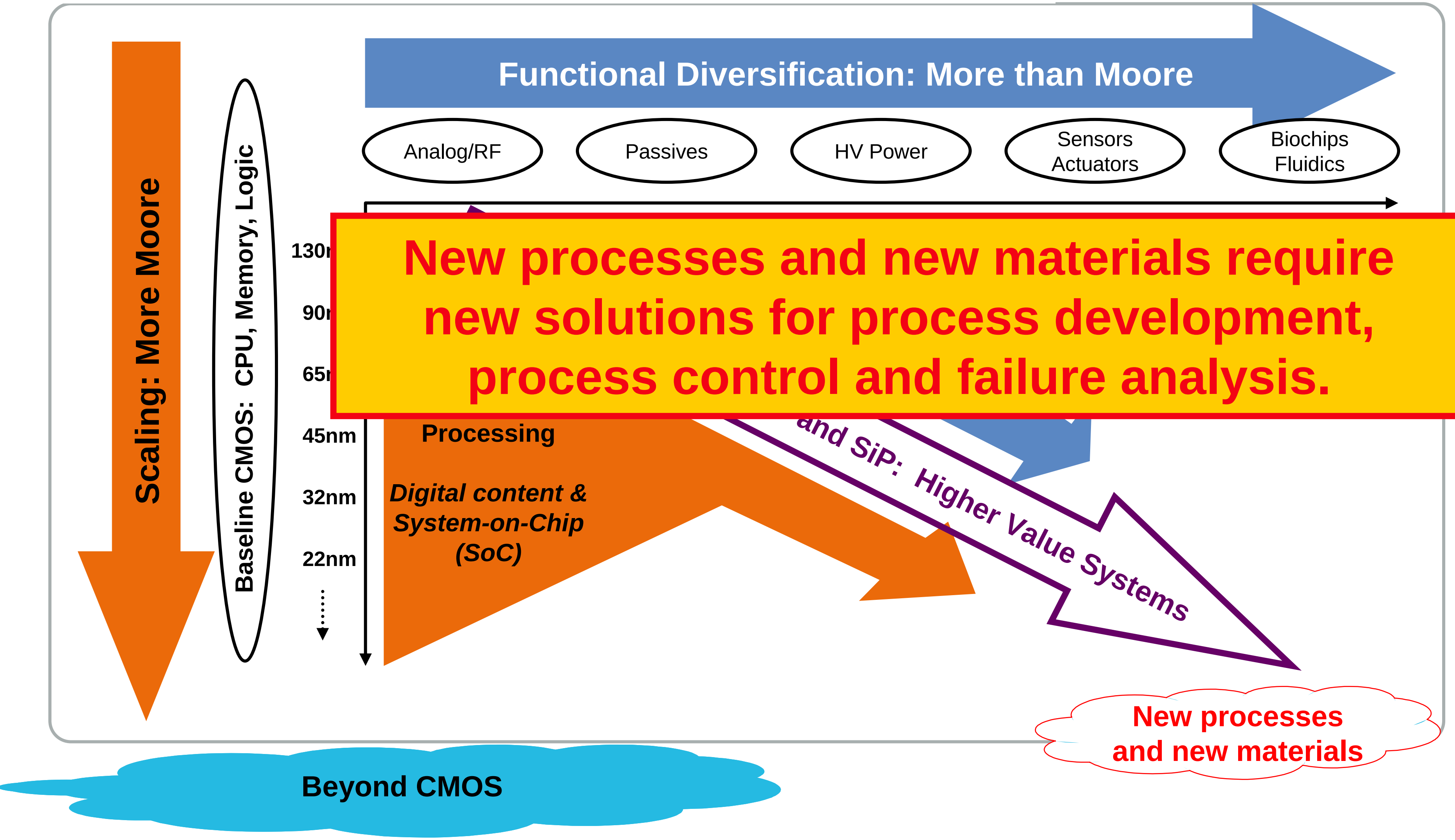
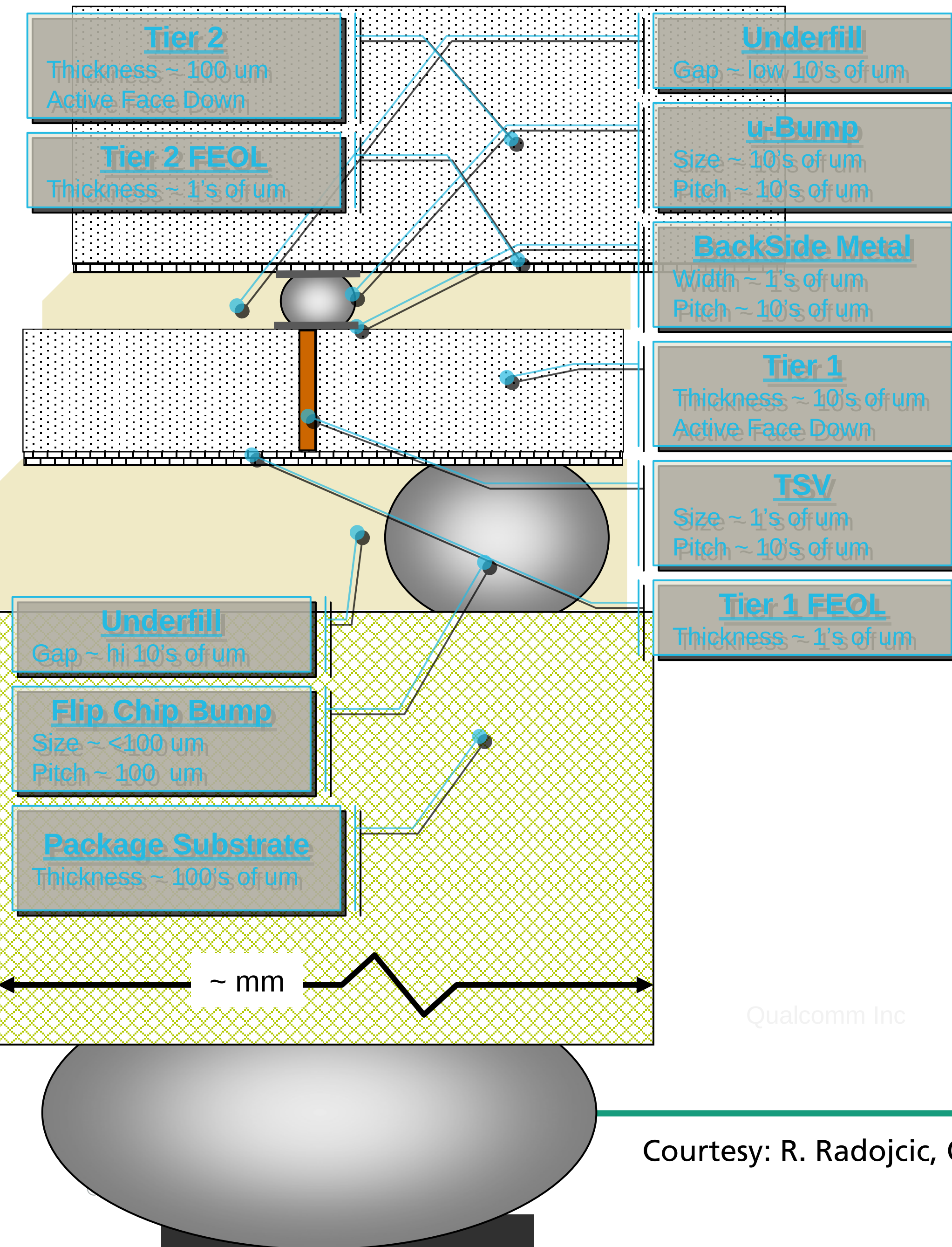
3D IC integration – Process control and failure analysis

From International Technology Roadmap for Semiconductors: http://www.itrs.net



3D TSV scheme



Integrated Heterogeneous 2-Die Stack

- **Tier 1 : CMOS Logic SoC**
  - TSV (connect frontside to backside)
  - Very thin Wafer (manage TSV aspect ratio)
  - Active face down
- **Interface µ-Bump**
  - Backside RDL Metal (interface to µBump and/or routing to allow offset of µBump vs TSV)
  - µ-Bump (Tier to Tier interconnect)
  - Very thin underfill
- **Tier 2 : Commercial Die**
  - Memory or Analog die, or…
  - Frontside Metal (interface to µBump)
  - Active face down & Pretty Thin
- **Flip Chip (C4) Bump**
  - Regular flip chip bump
  - Regular underfill
- **Package**
  - Regular PCB substrate
  - Regular plastic molding
  - Regular Package BGA Bump

Courtesy: R. Radojcic, Qualcomm

Contents

- Process control / Metrology
- Quality control / Failure analysis
- Stress engineering

Contents

- Process control / Metrology
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- Stress engineering

3D IC Integration: Process control/metrology needs (1)

TSV process

- TSV pitch and TSV CD (top & bottom)
- TSV depth: within wafer and wafer-to-wafer uniformity
- TSV etch profile: sidewall angle (top and bottom), via bottom profile (curvature)
- Sidewall oxide liner thickness
- Metal barrier dep: thickness uniformity, step coverage
- Cu ECD fill (filling defects: voids)
- Cu ECD overburden
- post-CMP topography

Microbump process

- Microbump quality

3D IC Integration: Process control/metrology needs (2)

Wafer bonding

- Wafer thickness
- Wafer bonding quality: bond strenght, voids/micro-voids, hermeticity, …
- Overlay metrology: wafer-to-wafer alignment, bond alignment

Defects

- Defects: critical vs. non-critical defects (etch defects, wafer edge defects, particles, scratches, …)
- Delamination
- …

Analytical techniques for process control

Requirements

- Full-wafer (for wafer-level 3D IC)
- Nondestructive
- No particle generation
- High throughput
- High technique reliability and tool uptime
- Easy to use (operators, no physicists!)
- …

Analytical techniques for process control

In-line techniques (nondestructive)

- Scanning acoustic microscopy
- IR microscopy
- …

Lab-based techniques

- X-sectioning of samples (e. g. FIB) + SEM imaging
- Scanning acoustic microscopy

Analytical techniques for process control

In-line techniques (nondestructive)

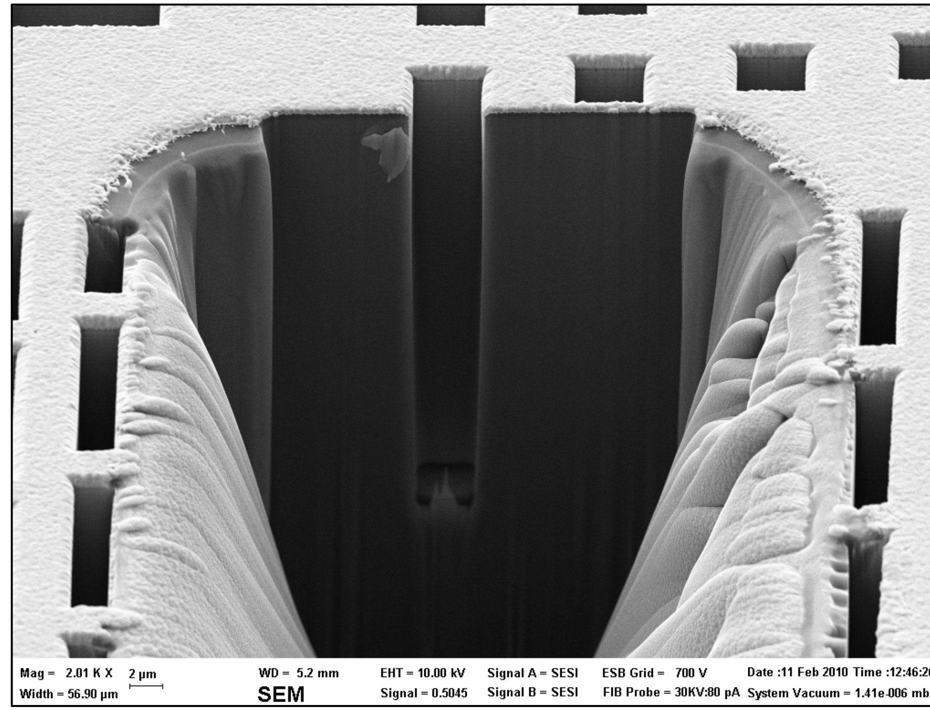
- Scanning acoustic microscopy
- IR microscopy
- …
- ➔ Talks Alain Diebold (Tue + Wed)

Lab-based techniques

- X-sectioning of samples (e. g. FIB) + SEM imaging
- Scanning acoustic microscopy
- ➔ Today

3D TSV process control: Target sample preparation

Focused Ion Beam is the method of choice for site specific preparation



Restrictions of standard FIB :

- large quantities of materials to be milled
- precise, but too slow (> 2…10 hours depending on geometry)

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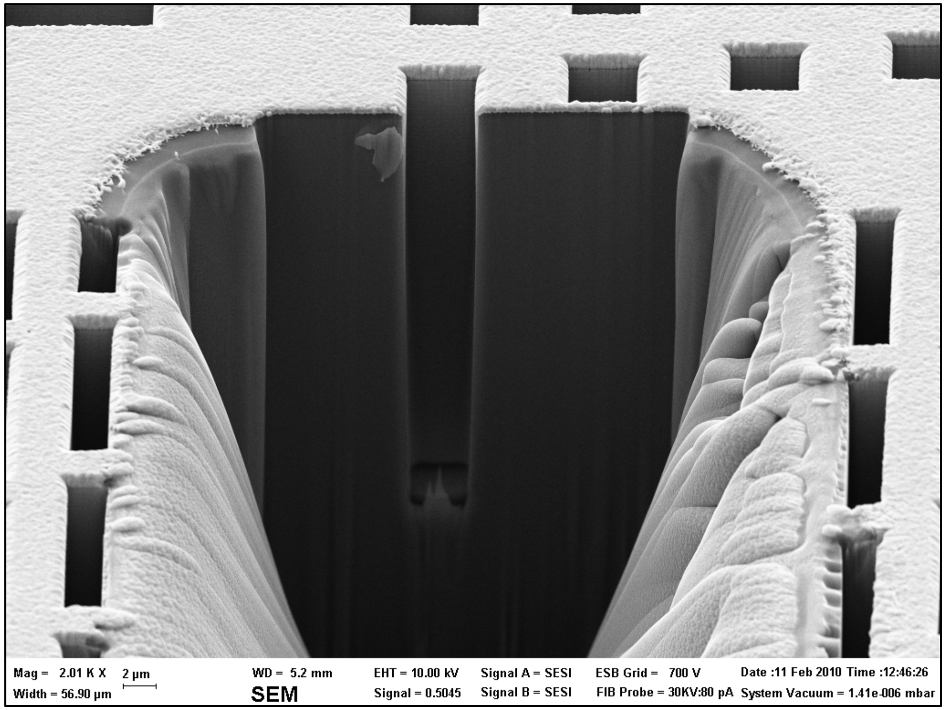
3D TSV process control: Fast sample preparation (work in progress)

Approaches for rapid X-sectioning:

1. increase of milling rate using chemical enhancement (for Si removal) and high current FIB
2. new plasma sources for FIB milling
3. laser ablation prior to high-rate FIB polishing



Reduction of preparation time (approaches 2 and 3):
~ 5 hours ➔ ~ 0.5 hours

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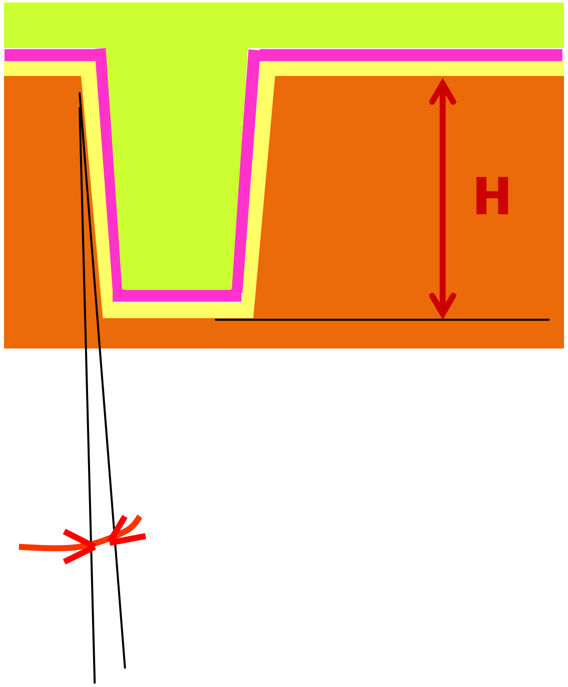
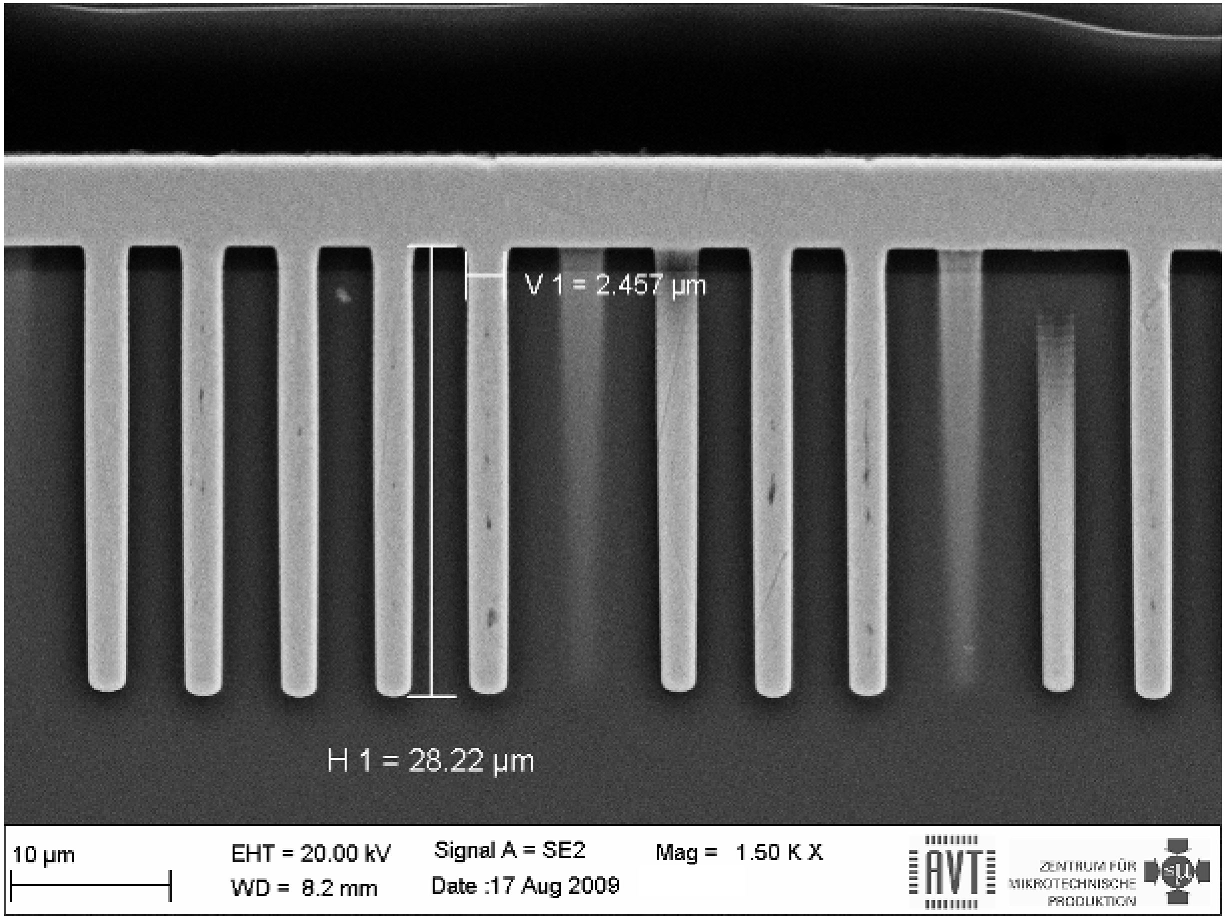
Selected TSV Process Control Requirements

Monitoring of via etch process (depth, taper, ...)





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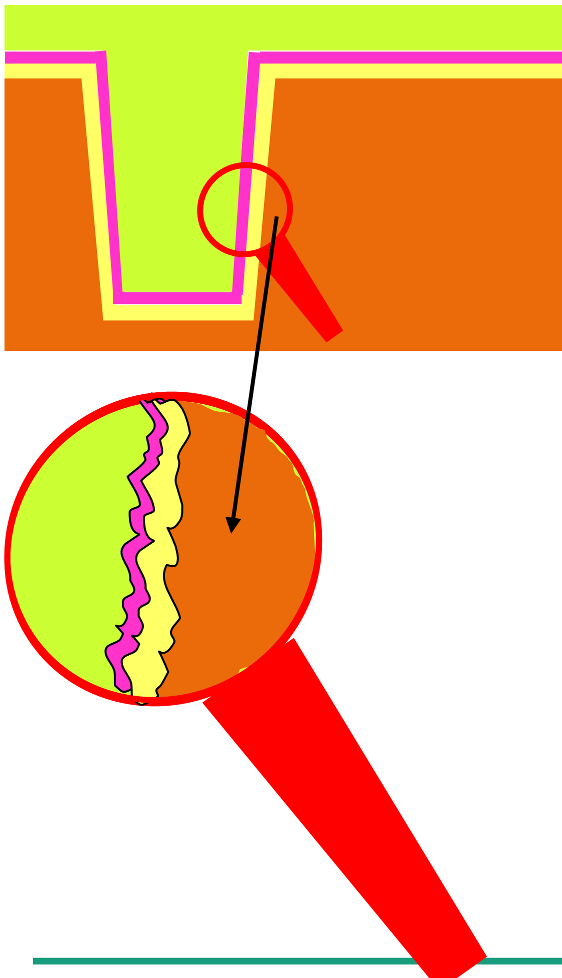
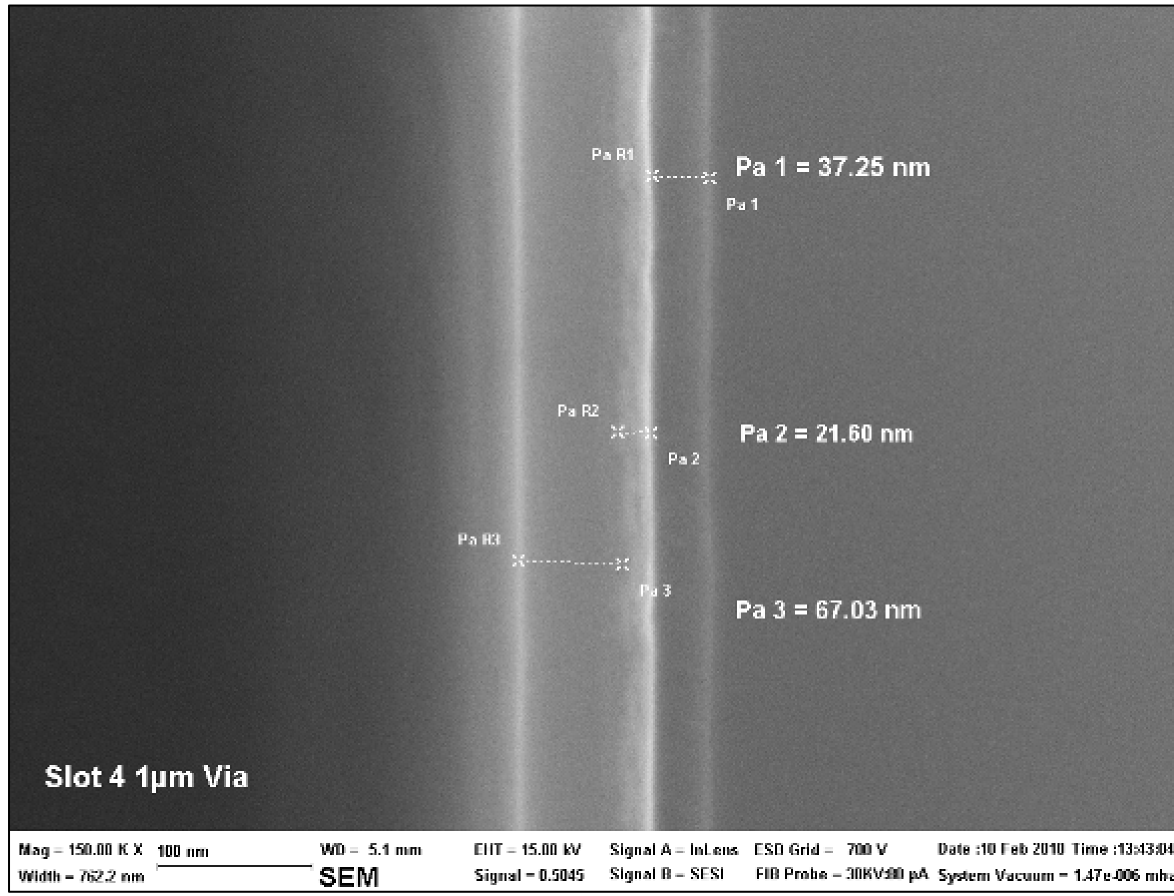
Selected TSV Process Control Requirements

Monitoring of sidewall and bottom oxide/barrier (thickness, uniformity,...)





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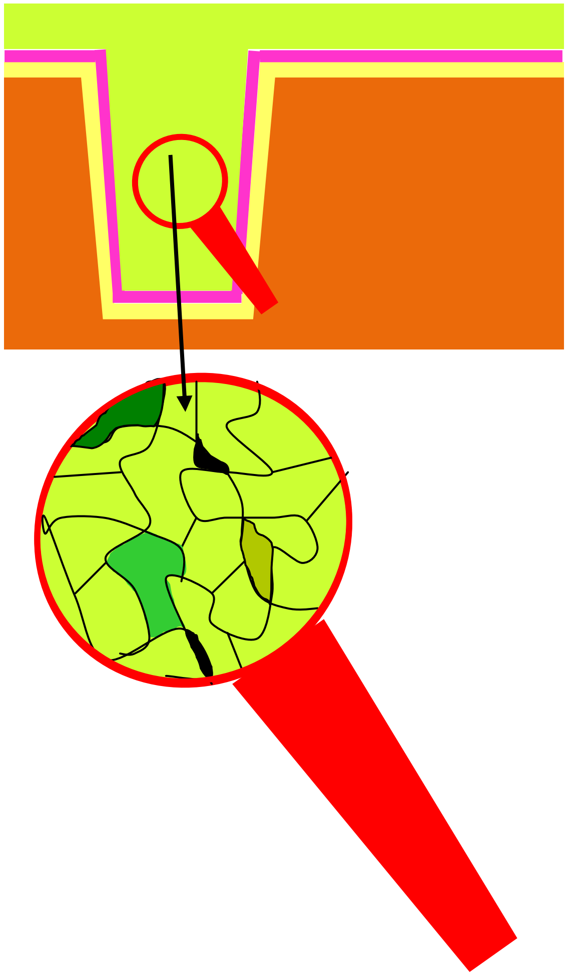
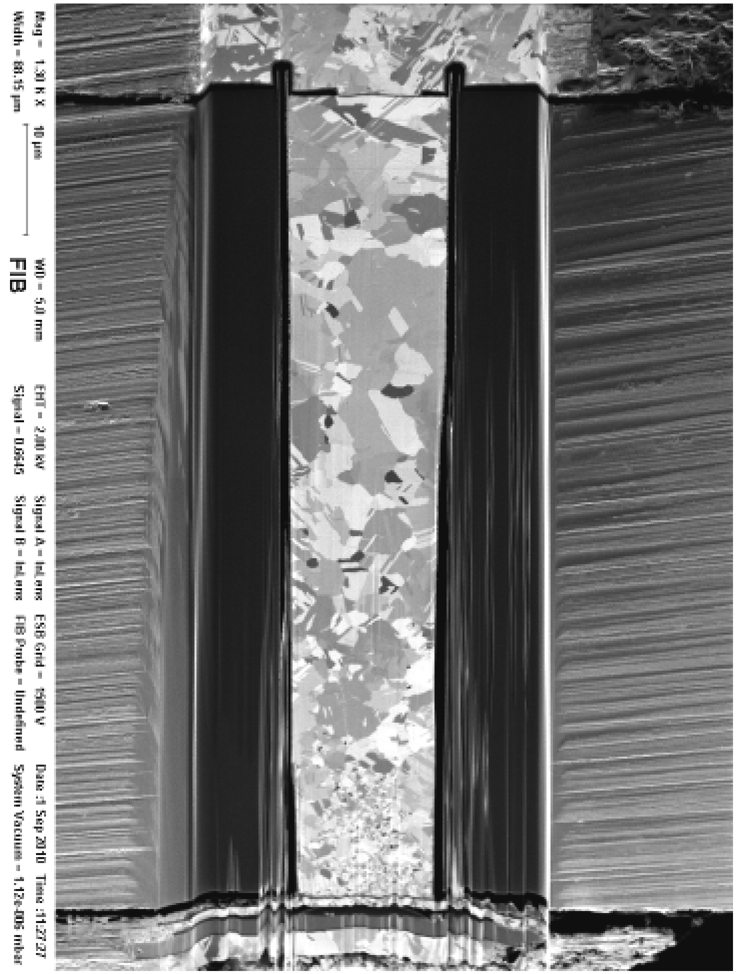
Selected TSV Process Control Requirements

Monitoring of fill material (voids, grain structure, impurities ....)

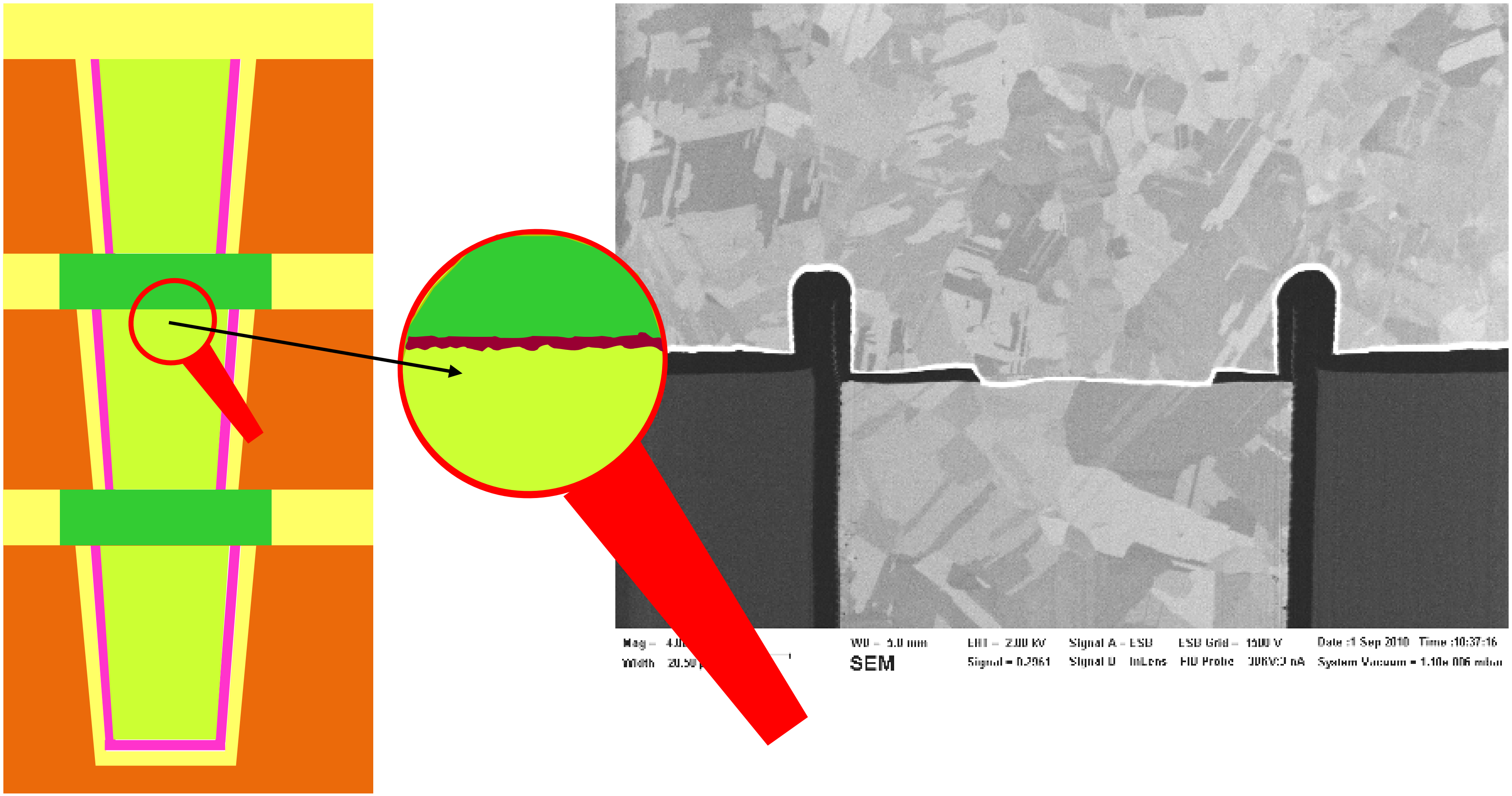




FIB Channeling Contrast

Selected TSV Process Control Requirements

Monitoring of via-via-interconnections (IMC formation and distribution)



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Contents

- **Process control / Metrology**
- **Quality control / Failure analysis**
- **Stress engineering**

3D IC Integration: Quality engineering / failure analysis needs

- Liner/barrier coverage/homogeneity (➔ leakage)
- TSV incomplete fill / voids
- Adhesion/delamination
- Stress (➔ CPI, Si cracks, Cu extrusion/„pop-up“)

Analytical techniques for failure analysis

Requirements

- Full-wafer or samples
- Non-destructive or destructive
- Reasonable throughput
- Reasonable technique reliability and tool uptime
- …

Analytical technique for failure analysis

In-line techniques (nondestructive)

- Scanning acoustic microscopy
- IR microscopy (?)
- …

Lab-based techniques

- Nano-XCT + subsequent X-sectioning (z. B. FIB) + SEM imaging
- …

Analytical technique for failure analysis

In-line techniques (nondestructive)

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Lab-based techniques

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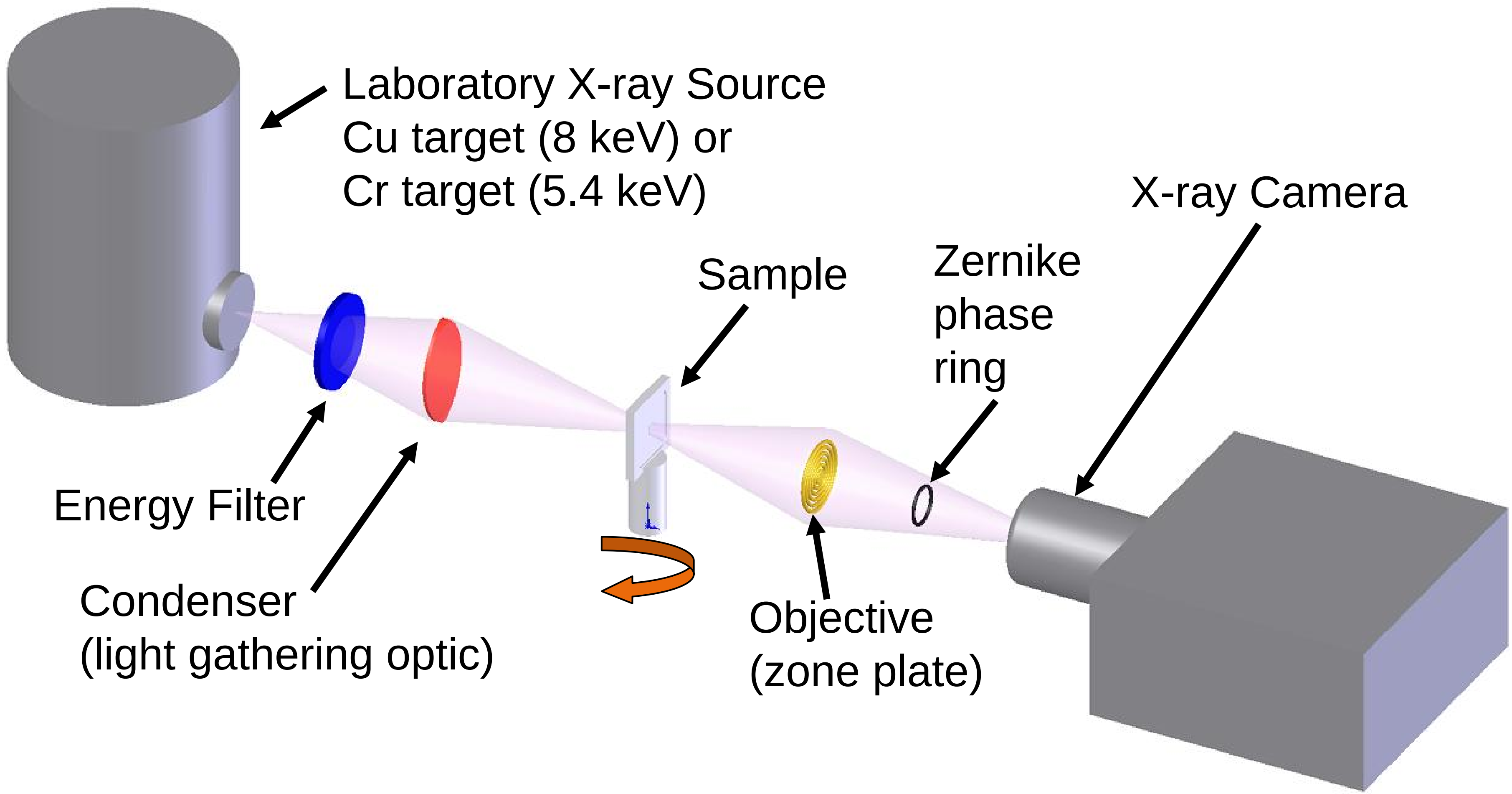
- …
- ➔ Today

Xradia NanoXCT: Lab based X-ray microscopy



Courtesy: Xradia Inc.

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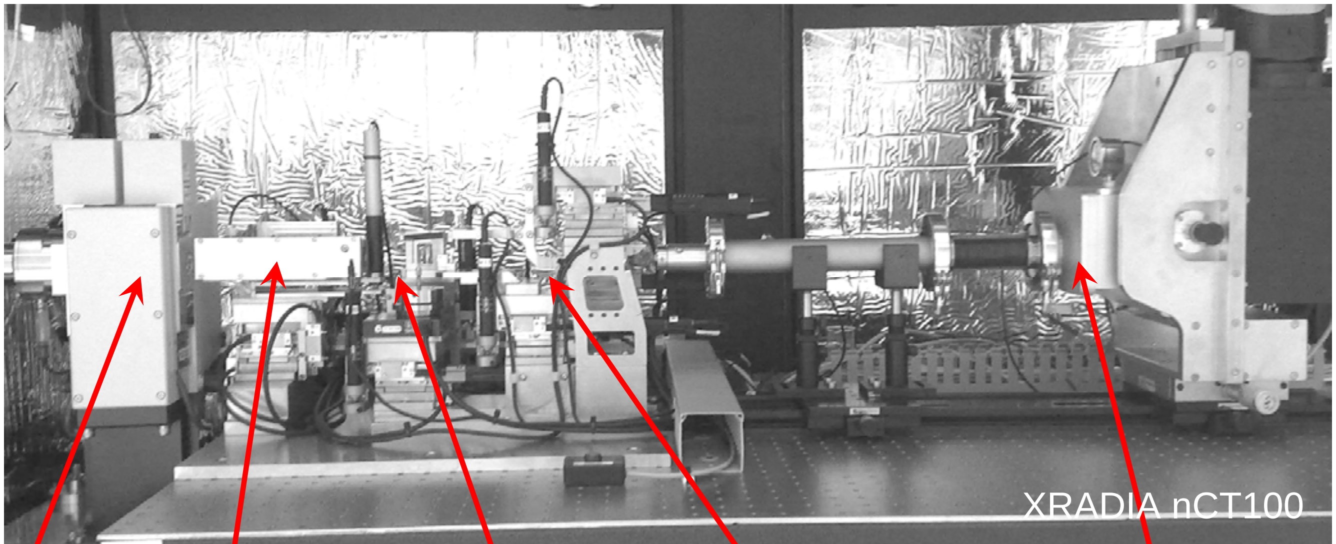
Xradia nanoXCT @ Fraunhofer IZFP Dresden



X-ray tube

Collimator

specimen

lens

imaging system

about 30 motors

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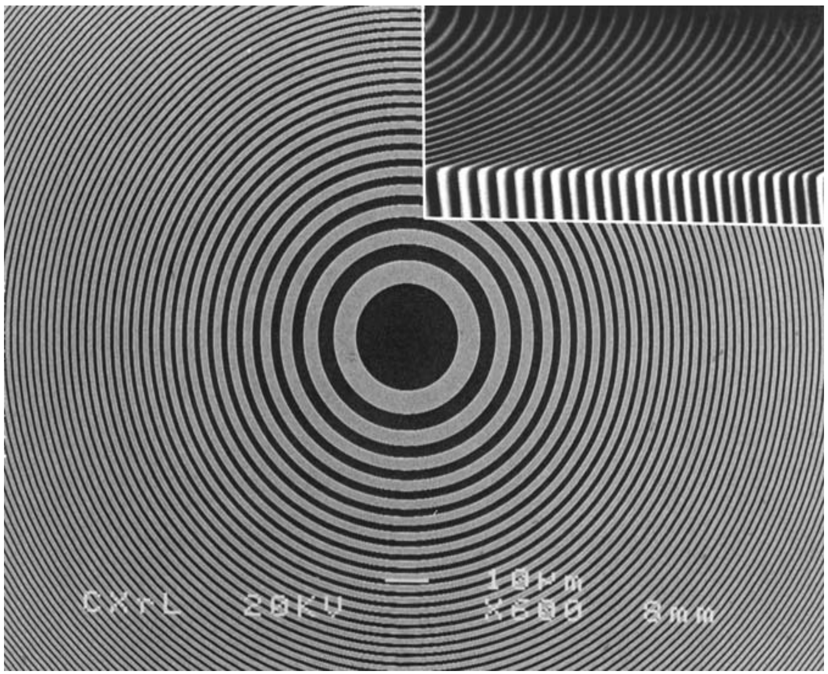
Zone plate's key parameters

Zone plate (X-ray lense) consists of concentric rings (zones) with zone width decreasing with radius



SEM image of a zone plate and its zone profile

Interference principle of Huygens and Fresnel: Delay of the light in different regions, strong chromatic aberration.

Number of zones > 100 required for good focusing

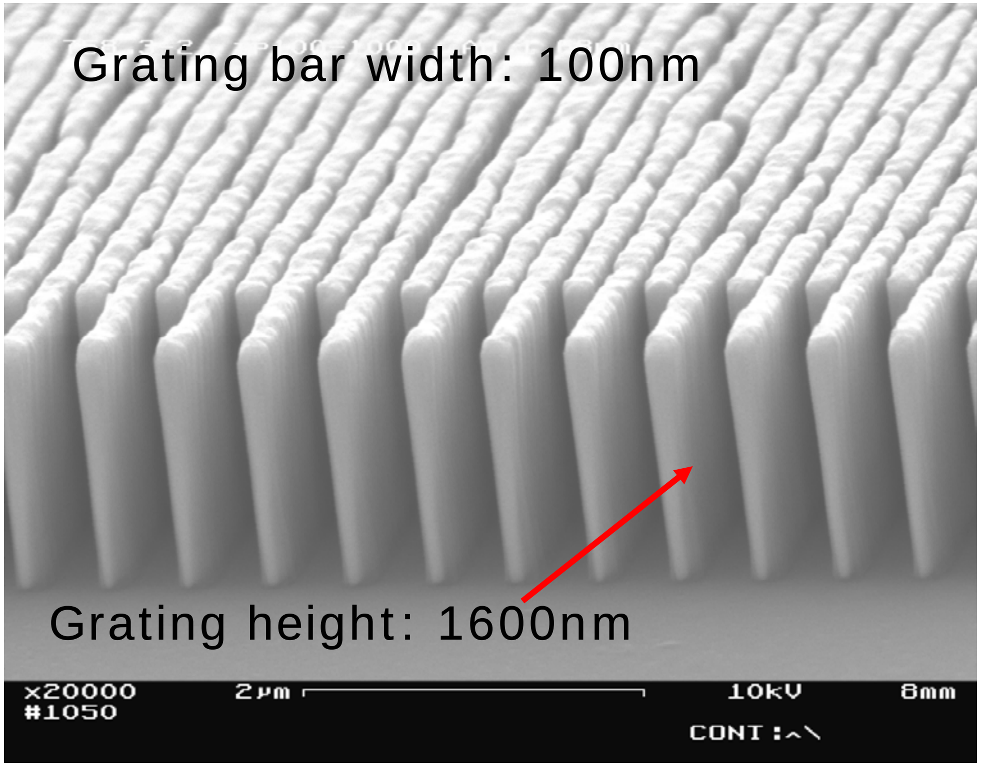
Resolution is proportional to the width of the outermost (smallest) zone.

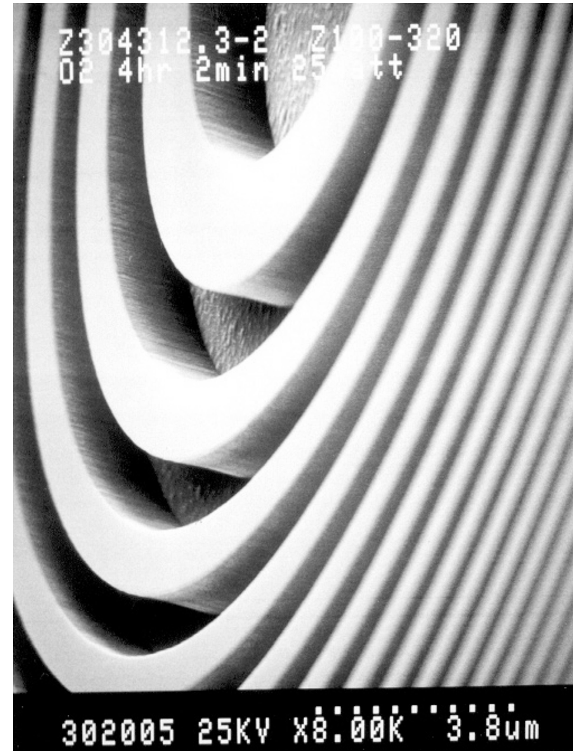
Outermost (smallest) zone width determines resolution and NA

(current limit: ~ 30nm, A/R ~ 30)

E. Zschech, W. Yun, G. Schneider, Appl. Phys. A 92, 423 – 429 (2008)
Courtesy: Xradia Inc.

Limits of zone plates: ~ 30 nm structures





Zone plates are fabricated out of high-Z (typically gold) material using electron beam lithography, reactive ion etching and electroplating.

Focusing efficiencies 10-30% currently achievable (depends on A/R).

E. Zschech, W. Yun, G. Schneider, Appl. Phys. A 92, 423 – 429 (2008)
Courtesy: Xradia Inc.

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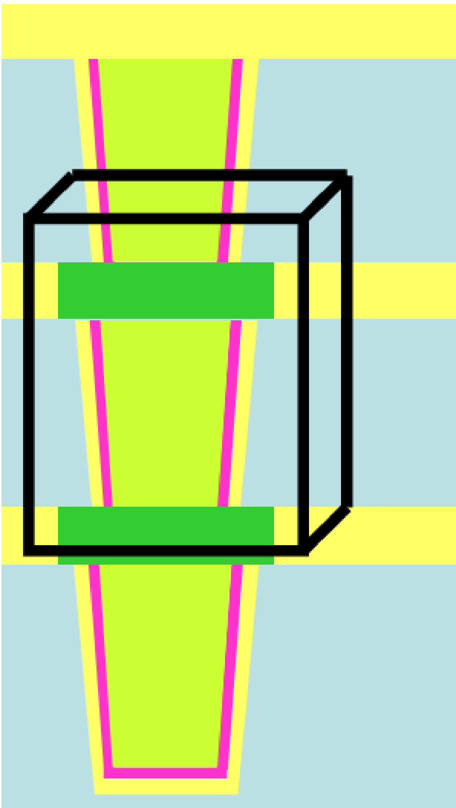
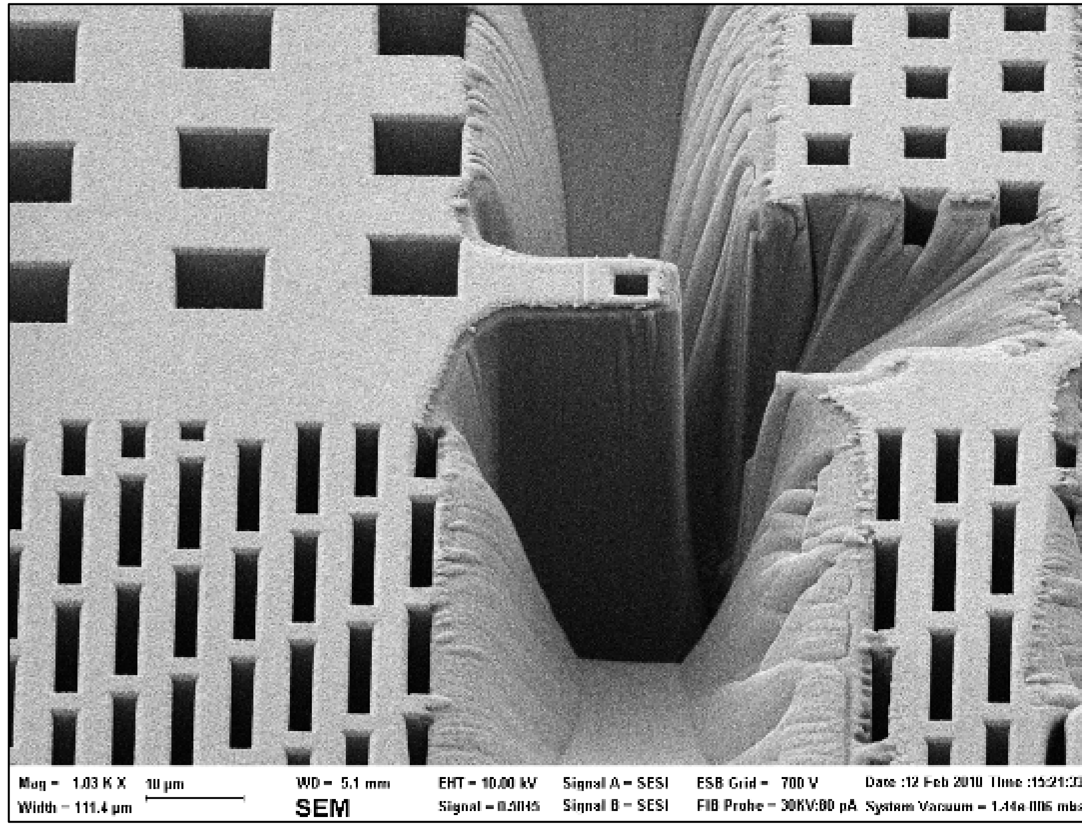
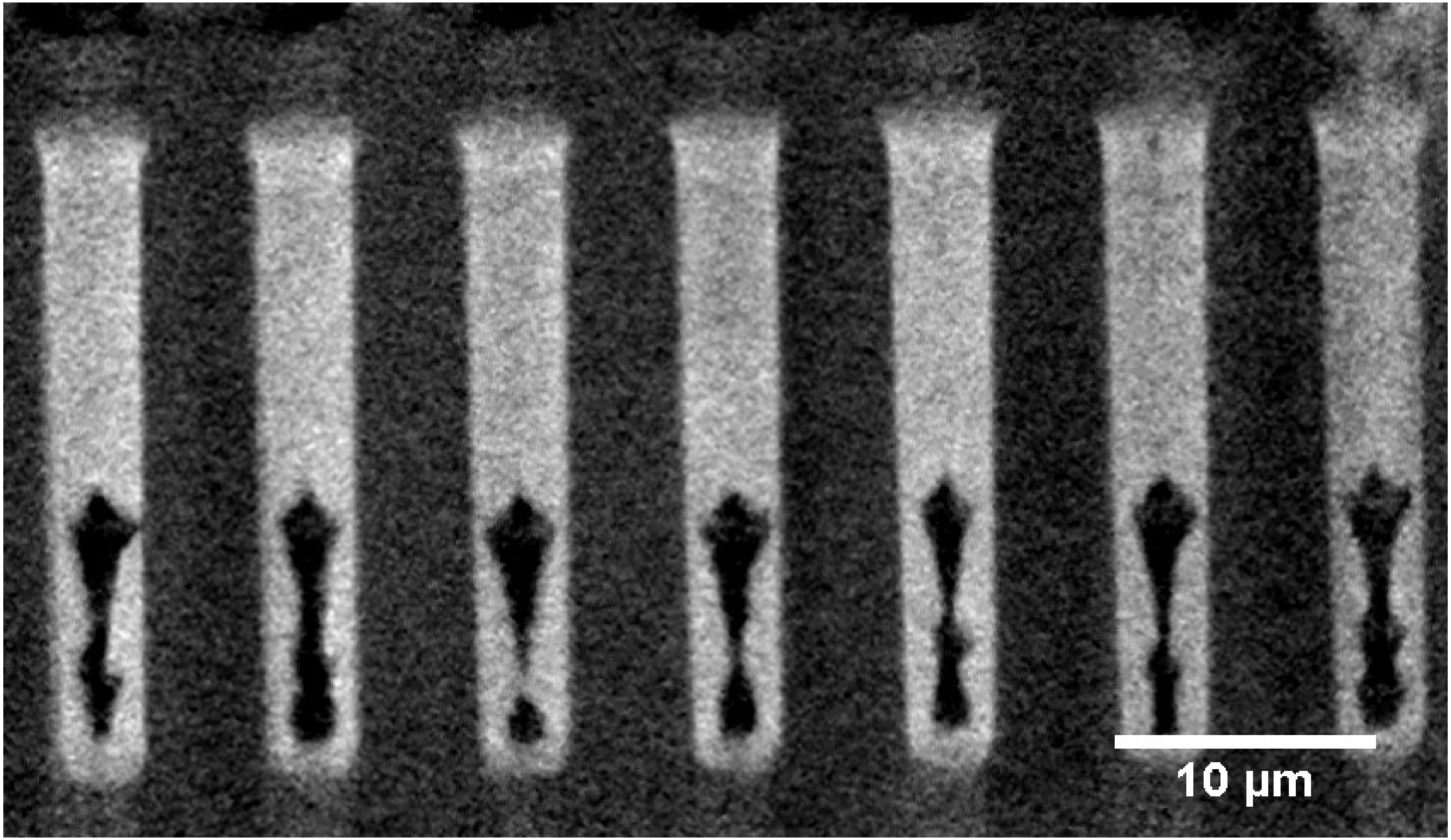
TSV sample preparation for nano X-ray tomography





Prepreparation (e. g. with laser ablation) + Focused Ion Beam

Process development: nanoXCT analysis of TSVs



Failure localization in TSVs: Large filling defects

Cooperation with Lay Wai Kong, College of Nanoscale Science and Engineering at the University at Albany / NY

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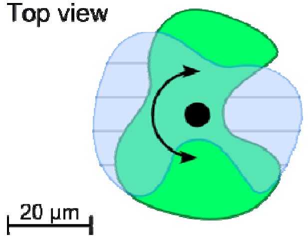
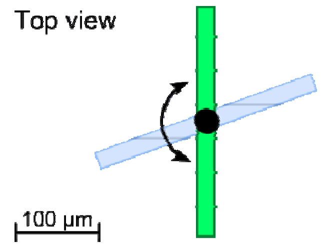
Flat samples: Laminography with tilted axis

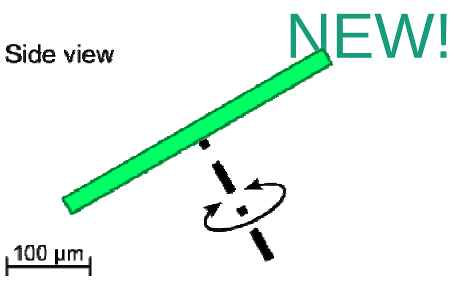
- Johann Radon
  - Back projection possible based on projections of different angles
- Rotation of sample or X-ray source
- Reconstruction of 3D data, e.g. by filtered back projection
- Acquisition geometry depends on sample shape
  - cylindrical samples: normal CT
  - flat samples: Laminography, typical artifacts



CT



Limited angle CL

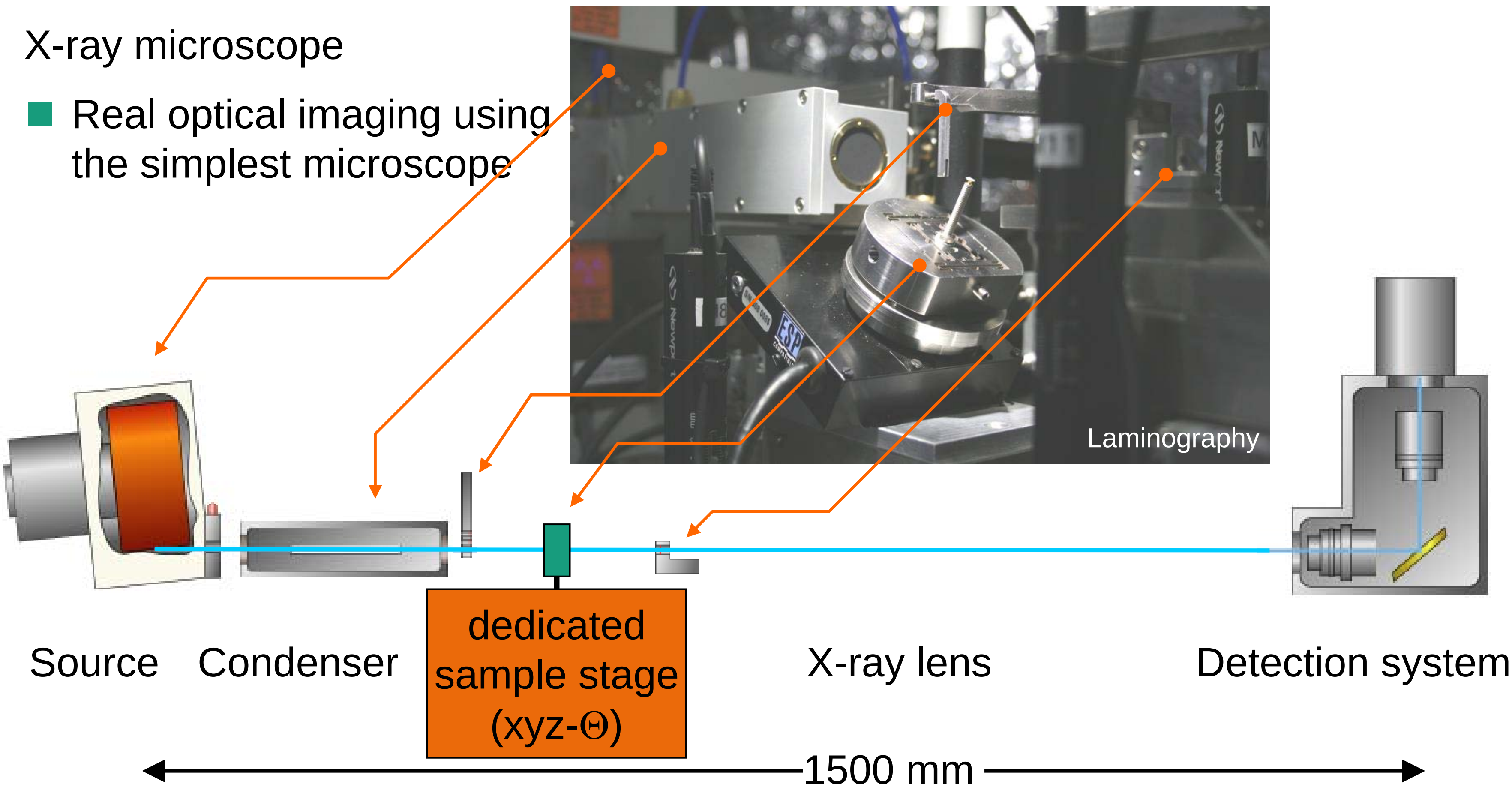


CL with tilted axis

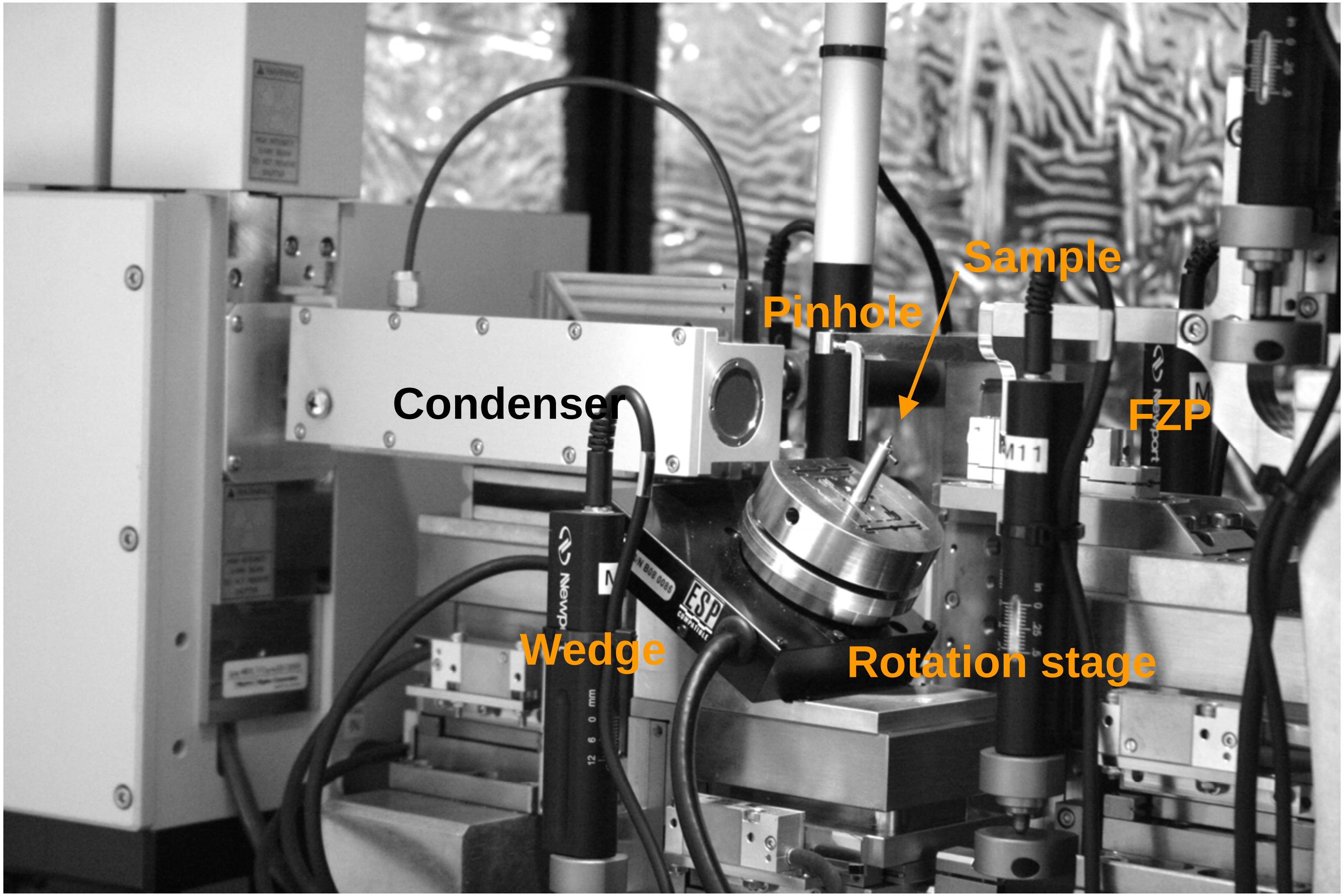
X-ray microscope – setup

X-ray microscope

- Real optical imaging using the simplest microscope



Sample tilt



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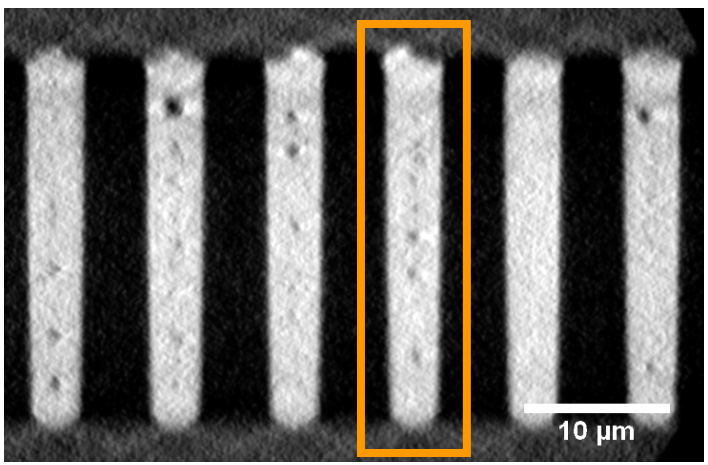
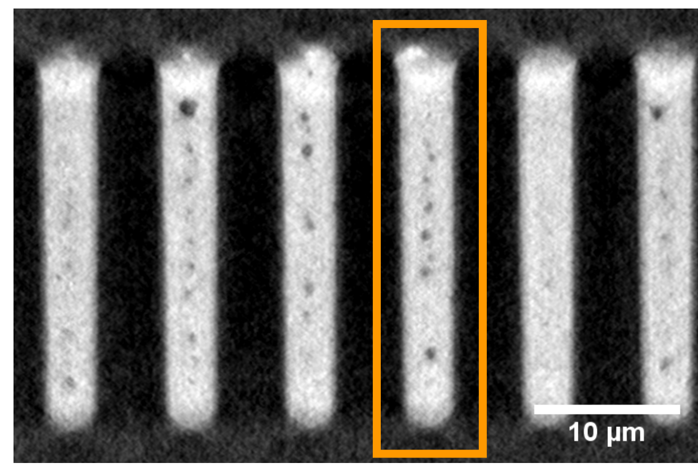
X-ray computed laminography study of TSVs

Comparison for equal measurement time

- Limited Angle CT



- CT with tilted rotational axis



➔ Better image quality (contrast)

➔ Less artifacts at the bottom of the TSV

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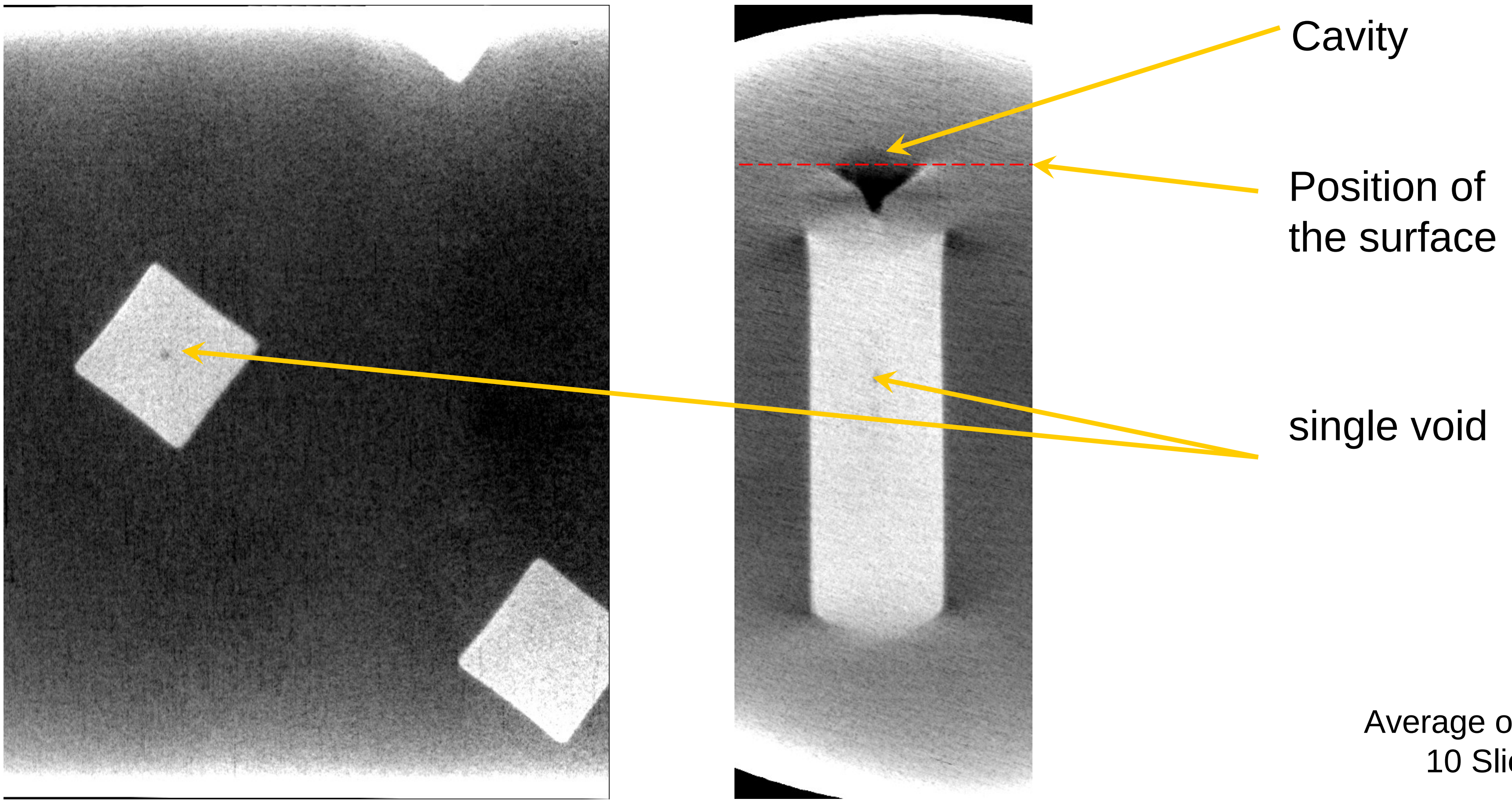
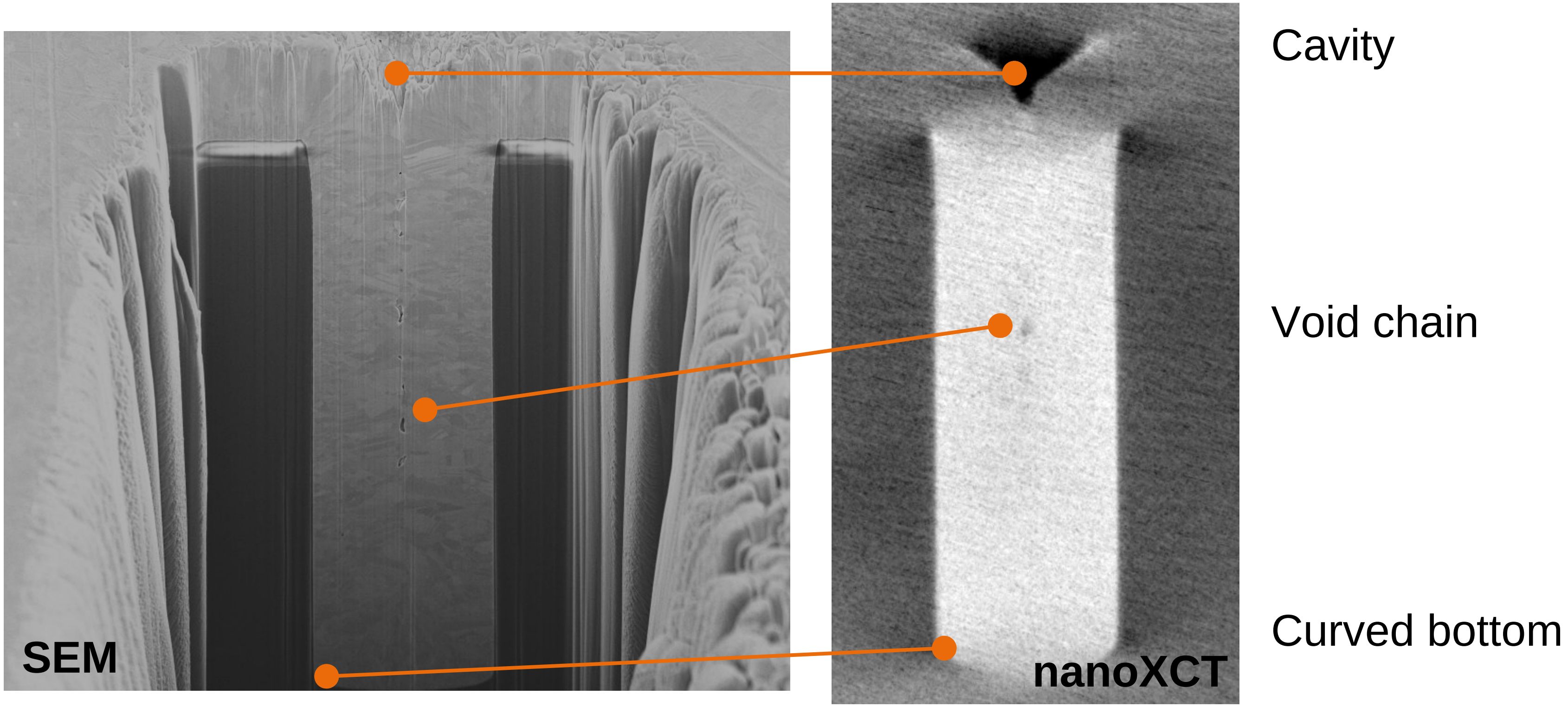
Xray tomography at TSV sample: < 100nm voids visible



Average over
10 Slices

FIB X-section of TSV after XCT study



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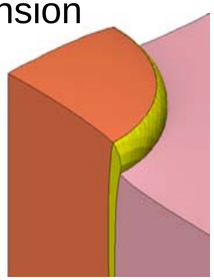
TSV performance and reliability risks

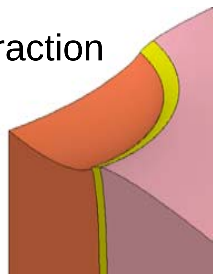
• **Reliability**

Expansion

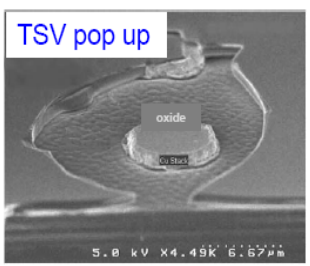


ΔT > 0

Contraction



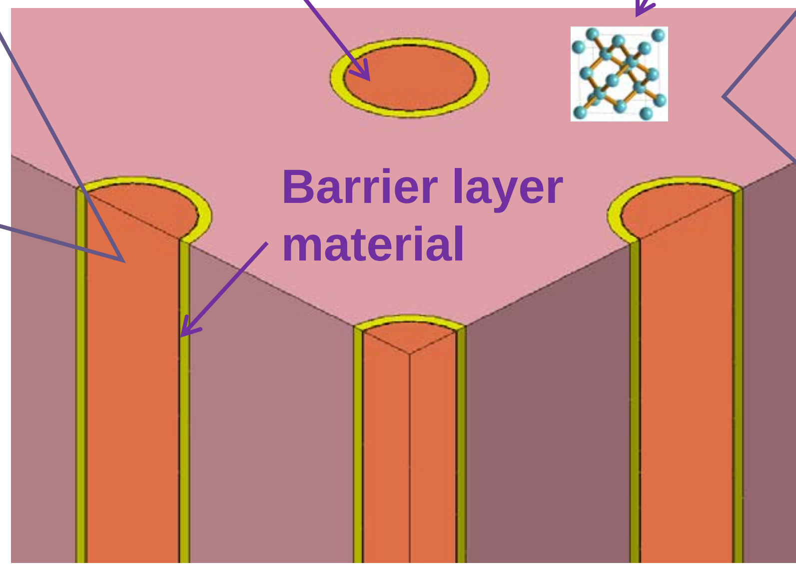
ΔT < 0



TSV extrusion and de-lamination
- P. Ho, RTI 3D Symposium 2009

Via material, diameter

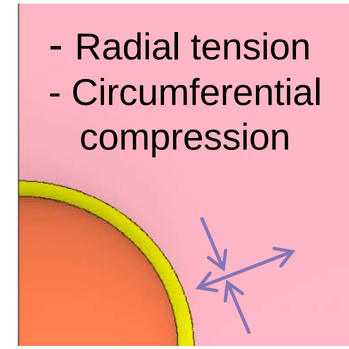
Silicon crystal orientation, P/N

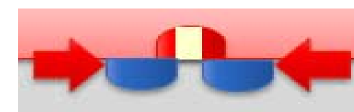


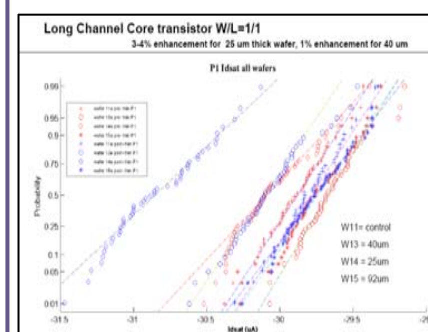
Insulation liner material and thickness

TSV array pitch, height

• **Mobility change**







Performance shifting after wafer thinning
- QCT/IMEC, DATE 2009

Courtesy: Xiaopeng Xu, Synopsys

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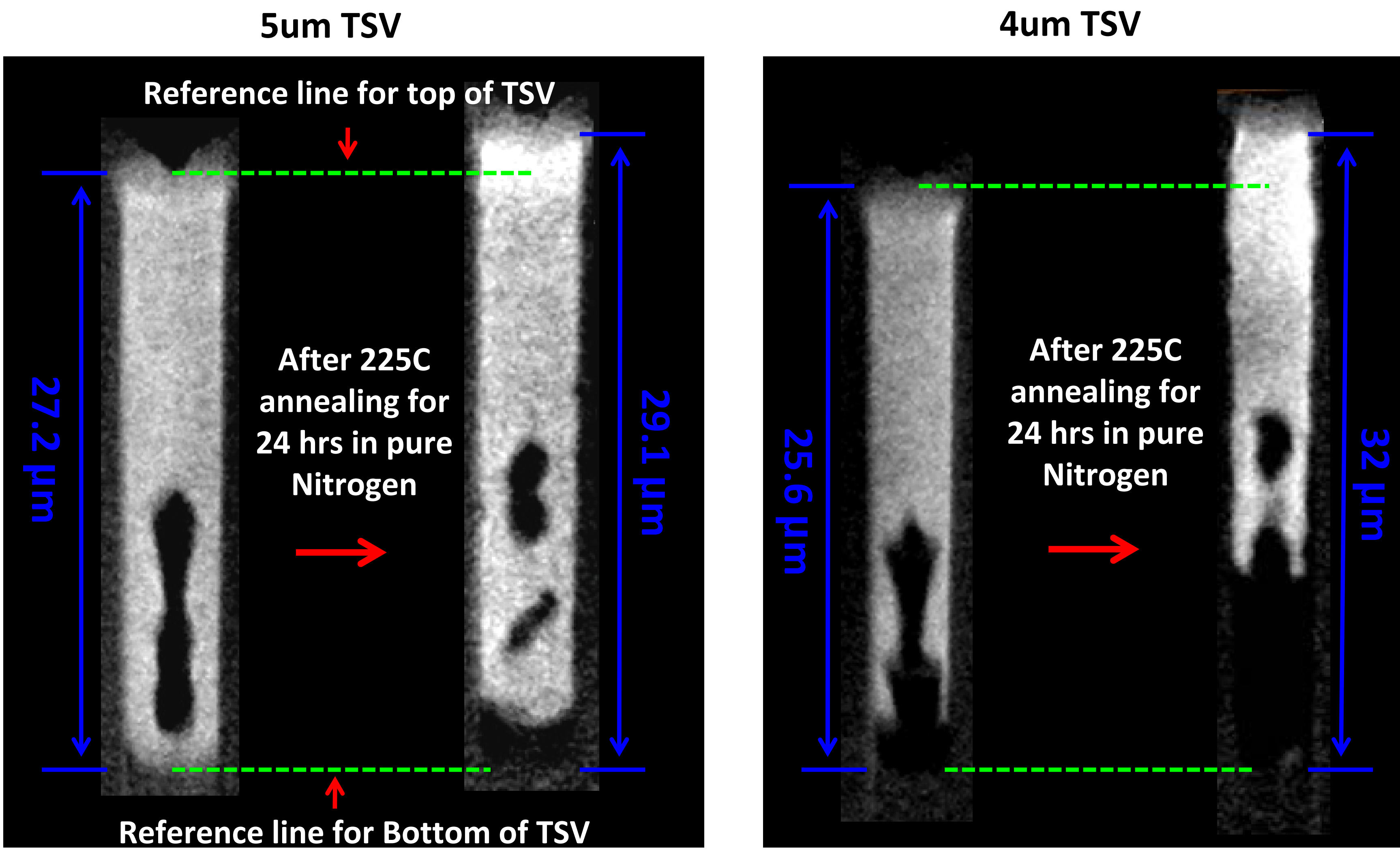
Cu TSV extrusions – Quantitative analysis



Both 4 and 5um TSV show Copper is extruded and with de-lamination at the wall

Cooperation with Lay Wai Kong, College of Nanoscale Science and Engineering at the University at Albany / NY

Stress-induced reliability-limiting effects

Example: Cu extrusion / “pop-up”

- Reasons:
  - Shear stress (depends on geometry, process flow (thermal cycles) and materials (E, CTE values)
  - Adhesion (sidewall)

- Nano-XCT is a potential technique to study this effect nondestructively (region of interest not destroyed)

  ➔ Systematic quantitative analysis possible

Summary

3D TSV integration (new processes and materials) requires

- advanced techniques for **process control / metrology**

  ➔ Time-to-data has to be reduced for X-sectioning techniques

  Plasma FIB, Laser ablation + FIB, …

- advanced techniques for **quality control / failure analysis**

  ➔ Time-to-data has to be reduced for nanoXCT

  Improved X-ray sources, optics and detectors

  Improved data analysis strategies (➔ Discrete tomography)

Acknowledgement

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Lay Wai Kong

Xradia Inc., Concord/CA

Kevin Fahey, Jeff Gelb

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