Silicidation and Strain Analysis of Silicon Nanowires


NaMLab, DCN– TU Dresden, Fraunhofer IKTS-MD, CfAED

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Towards nanowire electronics & nanometer scale silicidesc
Aim of scaling is to **increase value** each generation
The **scaling path** requires new geometries to reduce short channel effects

**Planar metal gate / high-k**
![Chipworks / IBM (45nm)]

**SOI-FET**
![EECS Berkeley]

**Trigate finFET**
![Intel Corp. 22 nm]

**Omega / multi-gate**
![Rustagi, EDL 28, 2007]

**Nanowire FET**

**Metal silicidesc** are contact materials to source, drain and gate
![Source: Bit-tech.net]

**Source:** IBM
Silicidation and Strain Analysis of Silicon Nanowires

Outline

- Metal / silicon nanowire heterostructures
- Strained nanowires
- Transistor applications
- Summary
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Nanowire and SOI systems employed

Top down

D. Deb, A. Erbe, M. Grube, W. Weber
NANONET-HZDR & namlab

• SOI (10nm $d_{Si}$ on 100nm BOX)
• Defined by lithography & RIE
• Front-end process up to 200 mm wafers
• Prone to surface roughness

Bottom up

Catalyst particle

• Diameter down to 5nm defined by seed size
• Controlled crystal orientation: $<110>$, $<112>$, $<111>$ Si NW
  $<110>$, $<111>$ Ge NW
• Low surface roughness
• Transfer to test-chip needed
• Simple test vehicle for demonstrators

Si nanowires

J. Trommer
Namlab

W. Weber, M. Grube
namlab

SiO$_x$ hardmask

10 nm SOI

BOX

W. Weber, M. Grube
namlab

20 nm

1 µm

Ge nanowires

J. Trommer
Namlab

Catalyst particle

200nm
Basic nanowire growth mechanism

**Growth:** Vapor-Liquid-Solid (VLS) mechanism

Wagner, R.S.; Ellis W.C. Appl. Phys. Lett. 4, 89 (1964)

SiH$_4$ (g) → Si-nanowire (s) → Au/Si (l)

Si supersaturation

Au/Si eutectic diagram

- Size of clusters define the nanowire's thickness

W. Weber
Intrinsic Si-nanowires (NW) Growth on amorphous SiO$_2$

- $d_{\text{Au}} = 0.5$ nm
- $p_{\text{SiH}_4} = 5$ Torr
- $T = 450^\circ$C
- $g \sim 7\mu$m / min

T. Mikolajick, RRL 7, 793 2014
Intrinsic $<110>$ Si-nanowires

Growth on crystalline-Si (100)

$\Rightarrow$ 0.5 nm Au

$\Rightarrow$ Oriented growth in $<110>$

Ge Nanowire growth

⇒ Nominally intrinsic Ge NWs on Ge / Si substrates
⇒ Pick & place w. manipulator, cross section preparation in ultra-low voltage FIB
⇒ <111> axis w. 6-fold sidewall facetting
Longitudinal silicidation:
Deposition of Ni reservoir

- Contact NWs with Ni reservoirs (plated or deposition)
- Diffusion from an unexhaustible Ni reservoir
Longitudinal Ni-silicidation over long range

First observation of:

- Longitudinal intrusion of Ni over long distances ~ 1µm Ni-diffusion length
- Formation of sharp interfaces
- Different phase formation in different NWs

![Image of Ni-silicidation](image)

Anisotropic Ni silicidation in nanowires

Case 1. - <110> Si nanowires

**Process**
- RTP at 480°C with inexhaustible Ni source.
- <110> Si nanowire diameter.

**Properties:**
- Direct NiSi₂ formation without intermediate phases
- Single crystal cubic CaF₂ structure of NiSi₂ grown epitaxially on <110> Si
- Sharp NiSi₂ / Si interface
- - 0.4 % lattice mismatch to Si <111>

**Reaction kinetics from in-situ TEM at ~420°C**

**Volume interstitial diffusion of Ni**

A) Long range >> 1μm length, **diffusion limited:** \( d \sim \sqrt{t} \)

B) Short range < 1μm length, **reaction limited:** \( d \sim t \)

Case 2: Ni silicidation of <112> Si nanowires

Elongation of NWs by ~ 30% Sequential evolution of 3 different phases

⇒ Different segments are formed
⇒ Apparently NiSi₂ forms first, followed by two other phases
⇒ A sequence of phases form, similar to that of bulk and thin films

⇒ However: In flash anneal no evident formation of different phases

W. Weber
Ni silicidation of bulk Si with inexhaustible Ni source
Anneal at 480°C

D. Deb, M. Grube, A. Erbe, M. Helm Nanonet

B) NiSi₂ zone axis (1-10)
A) Ni₃₇Si₂₃ complex zone axis (1-10)

S. Banerjee, E. Zschech, M. Löffler DCN TU-Dresden

Nickel silicide reactions in Si nanowires w. radial compressive strain

**Process:**

Thermally grown SiO₂ prior to silicidation (875°C).

Oxidation induces radially compressive strain $\sim 1.3$ GPa into Si core

Case 1. - $<110>$ nanowires

- **NiSi₂** formation, no fracturing of shell even for long $> 1\mu m$ silicide length

Case 2. - $<112>$ nanowires

- Cracking of oxide shell near the Ni pad

$=>$ Follows similar phase behavior than without shell
Summary – NixSi_y nanowire heterostructures

• Phase formation dependent on crystal orientation:

  \(<110>\)  --> Direct cubic NiSi_2 lattice matched nucleation
  - \(0.4\%\) lattice mismatch to Si \(<111>\)

  \(<112>\)  --> Sequence: Ni_2Si / NiSi / NiSi_2


-> Phase formation and kinetics of silicidation given by crystal orientation and related facets of outer walls

Adapted from K.N. Tu
Nickel germanide reactions in Ge nanowires

**Process:**

\(<111>\) Ge nanowires
RTP at different temperatures 300-400°C

- **Uncapped Ge nanowire**
  - Strong surface diffusion on Ge nanowires results in void formation

- **Capped Ge nanowire**
  - Capping in ALD Al₂O₃ or Si prevents surface diffusion: no voids formed

Jens Trommer
Ni$_2$Ge nanowire segments at the Si junction

TEM EDX profile on longitudinal lift-out lamella
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Influence of Strain on Electronic properties of $<$110$>$Si NWs

$<$110$>$ highly sensitive to strain
Radial compressive strain by oxidation
Ec: lowering of light $\Gamma$ valleys ($\sim 50$ meV)
Split $\Delta z$ $m^*$ drops from 0.19 to $\sim 0.076$ $m_0^*$


Population of low mass $\Gamma$ valley

André Heinzig
Strain mapping of \(<112>\) Si nanowire

Strain extracted from lattice spacing at different positions for different illuminations. Strain relaxation in the nanowire center. Strongest compressive strain at nanowire surface.

Analysis: Sayanti Banerjee, Sample: André Heinzig
Cross-section analysis oxidized $<110>$ Si nanowires

- Oxidation converts part of the nanowire to $\text{SiO}_2$
- Resulting crystalline nanowire diameter is reduced
- Typically, this leads to compressive strain
- Size has to be known for device modeling due to size effects

S. Banerjee, M. Löffler  DCN

Analysis: Sayanti Banerjee, Sample: André Heinzig
Outlook: mechanical in-situ testing in the TEM

Using the Hysitron PI95 Indenter holder with push-to-pull MEMS chips

- Sample preparation with micromanipulation in the (FIB)SEM
- Measure strain-dependent bandgap and maximum tolerable strain
Radial compressive strain in Si nanowires

- Process simulation

(100) \( t_{ox} = 6 \) nm

(111) \( t_{ox} = 8 \) nm

- Same trend in strain distribution between HRTEM vs. process simulations
- Relaxation in nanowire center, highest compressive strain @ nanowire top surface
- Mean stress extracted from microRaman: -1.3 GPa (radial compressive)
Silicidation and Strain Analysis of Silicon Nanowires

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Metal / silicon nanowire heterostructures

Strained nanowires

Transistor applications

Summary
What we use silicide and strain for: Reconfigurable Transistors

Doping free silicon technology, giving unipolar p- and n-FET behavior from the same device as programmed electrically.

Conventional CMOS inverter

- Doping profiles needed
- Different width
- Different stressors for p- and n-FET
- STI needed to isolate p- n-FETs

Reconfigurable FET inverter

- No doping needed
- Single stressor
- Identical device for p- and n-FET
- No STI needed
- Two gates per device needed (self-aligned)

Adapted from TU Wien / Selberherr

A. Heinzig
Working principle Schottky FETs

- Intrinsic-Si: depletion / accumulation
- Field induced band bending at junctions
- Injection of both electrons and holes -> ambipolar behavior

Reference: bulk NiSi<sub>2</sub>/Si

\[ e\Phi_B \text{ holes} = 0.39 - 0.48 \text{ eV} \]
\[ e\Phi_B \text{ electrons} = 0.66 - 0.75 \text{ eV} \]

How can we manipulate electron and hole injection?
Transport alteration in metal / Si / metal nanowires

- Turn device on with electron tunnel current
- Enhance on-current by flushing holes at drain
- Non-volatile program through charge trapping

In contrast to a MOSFET a point potential selectively controls electron / hole transport

Reconfigurable Si nanowire FETs

- Same FETs provide p- and n-type transport: leaner complexity
- Higher device functionality -> reprogrammable logic

\[
I_{on} / I_{off} > 5 \times 10^7 \quad ; \quad J_{on} = 6 \times 10^5 \text{ A/cm}^2 \quad @ \quad V_d=1\text{V} \quad ; \quad g_m = 130 \mu S/\mu \text{m}
\]

Strain to adjust tunneling currents

\[ T \propto e \]

\[ -4w \frac{2m^*_{n,p}}{3qhV} \phi_{n,p}^{3/2} \]

- \( V_{PG} \) filters undesired carriers in intrinsic channel; \( V_{CG} \) acts as regular gate

- Full symmetry, \( I_{on} \), \( V_t \) by strain engineering

Complementary inverters integrated in 1-D

- Complementary operation with single $V_{dd}$
- Switching at $V_{dd}/2$
- n/p fully exchangable
- Capable of driving next stage -> Ultralow capacitances $C_L = 0.03 \text{ fF}$ -> 78 ps delay

Mixed mode simul.
Benefit of reconfigurability at circuit level

Reduction of transistor count and delay for main boolean functions

Example: 1bit full adder (needed for calculations and address decoders)

In CMOS 28 T needed

6T NAND / NOR

XOR/XNOR parity function

Basic 1 D cell

\[ \text{CMOS CARRY} \]

\[ \text{RFET CARRY} \]

\[ \text{CMOS SUM} \]

\[ \text{RFET SUM} \]

\[ \text{-> 1-bit full adder with 14-T and up to 50\% reduced structural delay} \]

J. Trommer, A. Heinzig


**Summary**

**Formation of metal / silicon nanowire heterostructures**

Reactions depend on size and crystal direction

**Strain analysis in nanowires**

Strain distribution is uneven along nanowire cross section and length

**Transport properties**

*carrier type* injected controlled by point potential

**Reconfigurable electronics**

*p- and n-type behavior on the same devices*

NAND $\rightarrow$ NOR reconfigurable circuit string