Techno-Economic Pressures and the case for Innovation

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OUTLINE

- <u>Semiconductor Market Trends</u>
- Eco-system Challenges
- Technology Innovations
- Implications to Characterization and Metrology

Mega Trends That Will Drive the Economy, Technology and Semiconductors

Coverage and insatiable bandwidth needs will drive **Next-Gen Wireless**

Mobile computing will continue to converge functions and drive compute power

Platform Owners rapidly growing semi skills – changing customer relationship model

Internet of Things will drive mobile processing at low power with ubiquitous RF

Increasing **Security** concerns at all levels: government, enterprise and personal

Networks and Storage focus on hardware and more on Applications-Centric Infrastructure

Mobility Drives the Wave of Computing Evolution

→ Are we now at another inflection point?

	1970's	80's	90's	00's	10's	20's
	wired	wireless	wired	wireless	wireless	
Bandwidth	28kbps	10kbps	100kbps	1Mbps	10Mbps	
Unit Shipments	~1M	~10M	~100M	~1B	~100B	

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Market Segments Characteristics

- High performance multi-core multi-processor
- Thermal Limited in Performance
- High speed on and off chip interfaces
- Large embedded memories

Data Centers
Networking
Specialty

Mobile, Consumer
Automotive* & Industrial

Performance

IoT devices*
(Medical, Wearable)

- Ultra-low-power SoC
- ULV Digital(0.6V)
- ULV RF (<0.6V)

- Energy- efficient SoC:
- Multiple Modes of Operation
- Blend of Power and Performance
- RF Integration

Power

* Embedded Non-Volatile Memory Required

Internet of Things (IoT) is More Than Just Hype

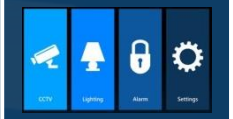
Compelling Market Drivers

- Energy efficiency
- Manufacturing competitiveness
- Vehicle traffic management
- Climate change
- Health care costs
- Global Security

- Buildings
- Manufacturing lines
- Vehicles
- Forests, oceans, farms
- Vital signs
- Activity

Need to monitor 10's of billions of systems to facilitate real-time decision making and system optimization

Layers of Opportunities in IoT

	Wearables/ Medical	Smart Meters	Smart Home	Factory Automation
Analytics/ Apps	Fitness Tracker App	Billing, PEV Charging scheduling	Lighting, security HVAC	Inventory JIT Scheduling Historian
Data Centers/ Servers	iCloud	Utility Servers	iCloud (Secure)	Enterprise, Factory Servers
Wide Area Connectivity	LTE/4G/3G Cable/Fiber	ZigBee NAN SubGHz RF G3/Prime, LTE	LTE/4G/3G Cable/Fiber	Wi-Fi 802.11 Ethernet
Gateways	Smart Phone	Electricity Smart Meter	ISP, home Gateway, Smart phone	SCADA Distribution Access Switch
Local Area Connectivity	Wi-Fi 802.11 Bluetooth 4.0	SEP2.0/15.4 M-Wireless, WiSUN	Wi-Fi 802.11 BT Smart ZigBee/15.4	6TiSCH/15.4, ProfiBus/ 802.3/802.11
Edge Nodes				

Aggregation Layers

Breakthrough innovation is required at the edge

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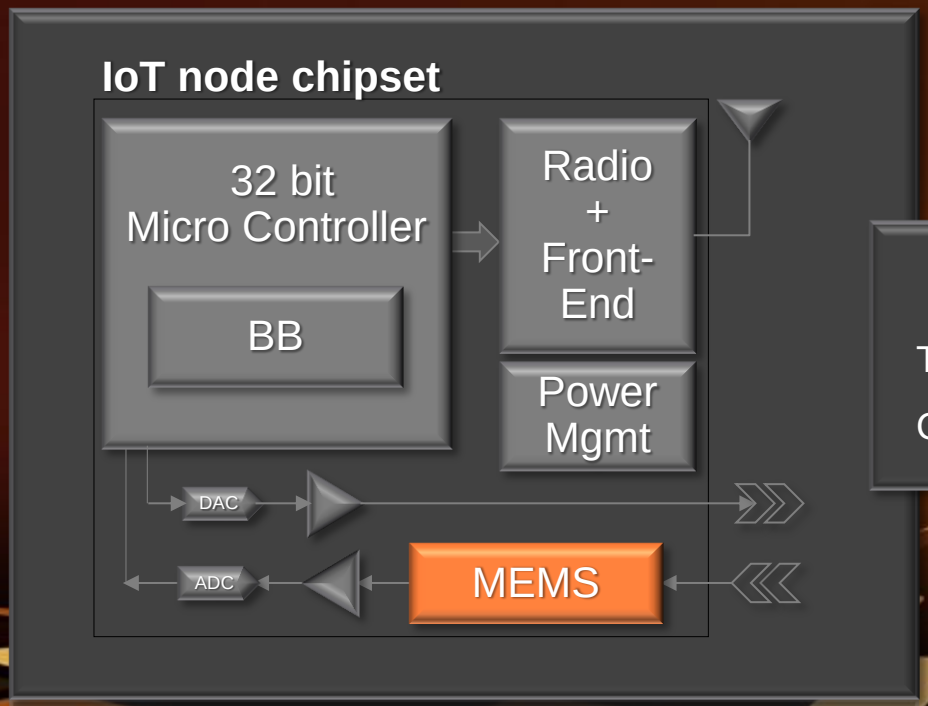
IoT: Extremely challenging design requirements



	Past	Future
Time to Market	<3-4yr	<1-2yr
Cost of end chipset	>> $1	<< $1

Design Constraints

1. Signal Chain → as complicated as a cell phone
2. Cost → < 1/100th of a cell phone
3. Size → < 1/1000th of a cell phone
4. Power Consumption → < 1/1000th of a cell phone

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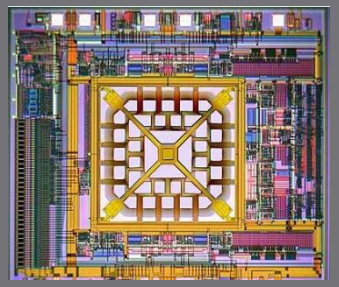
Opportunities for Innovation Abound!

Sensors

Platform Technology

Integration with Si

Packaging



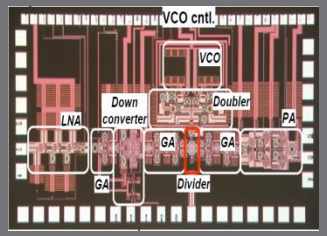
RF

RF Power

Power Consumption

Bandwidth

Integration



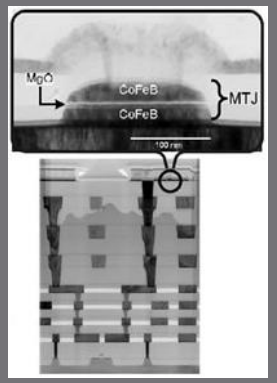
eNVM

Power

Scaling

Reliability

Integration

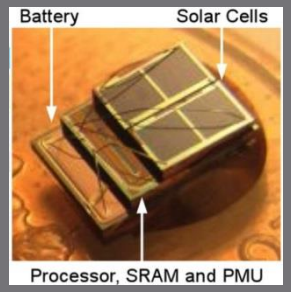


Packaging

Cost Effectiveness

Flexibility

Alternative scaling opportunities (2.5/3D)



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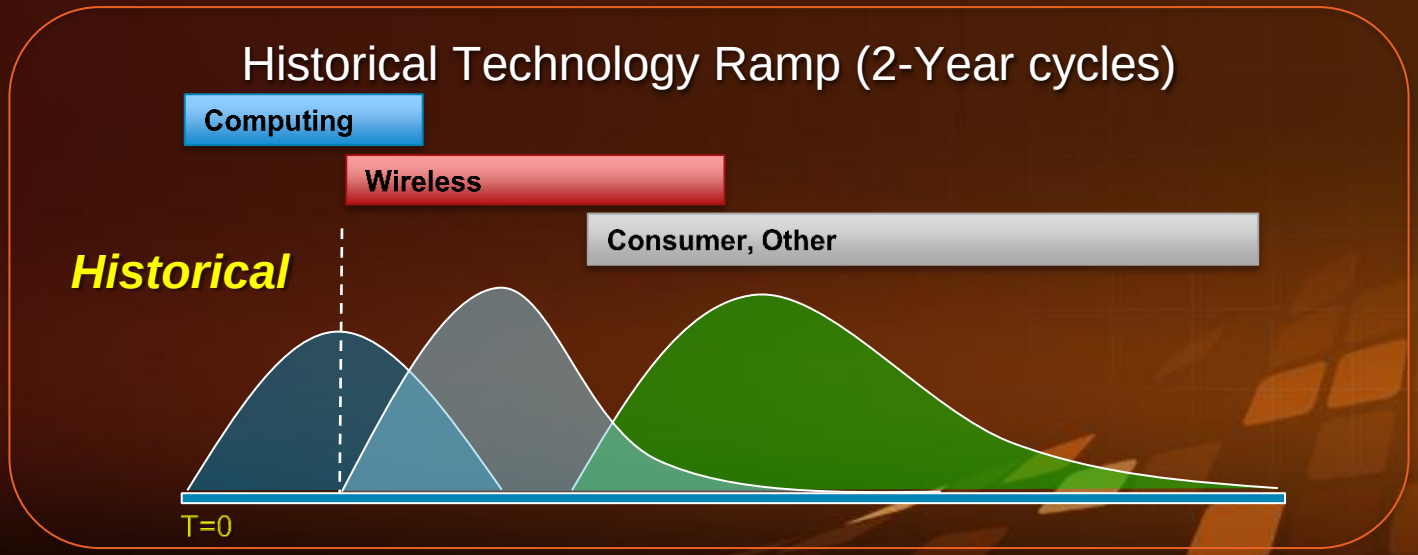
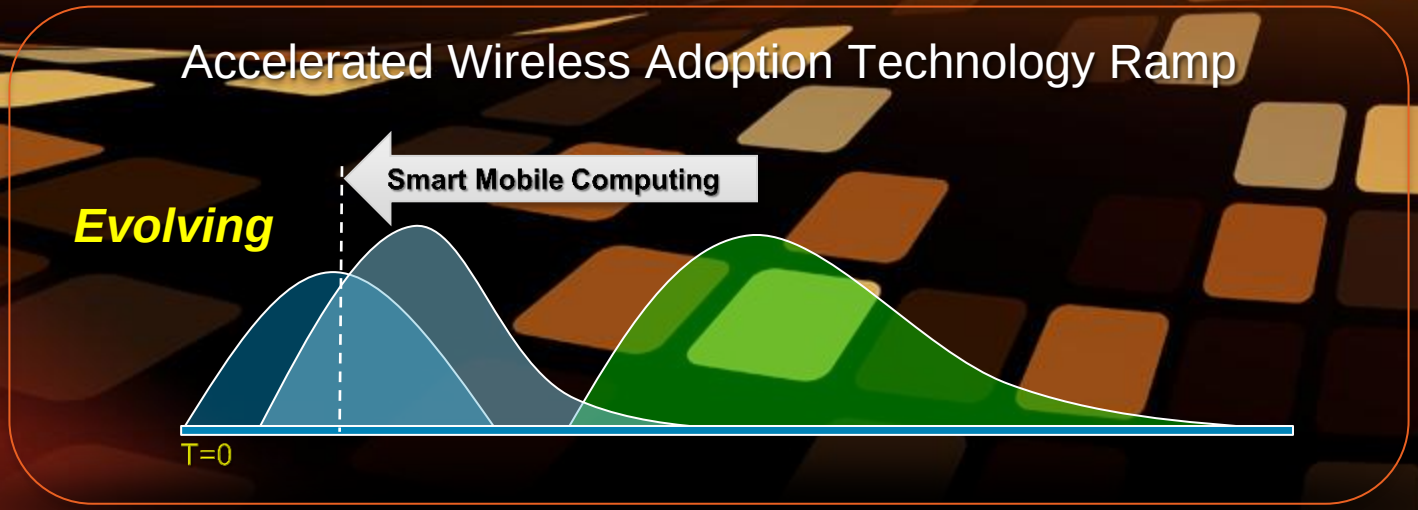
Evolving Industry Landscape

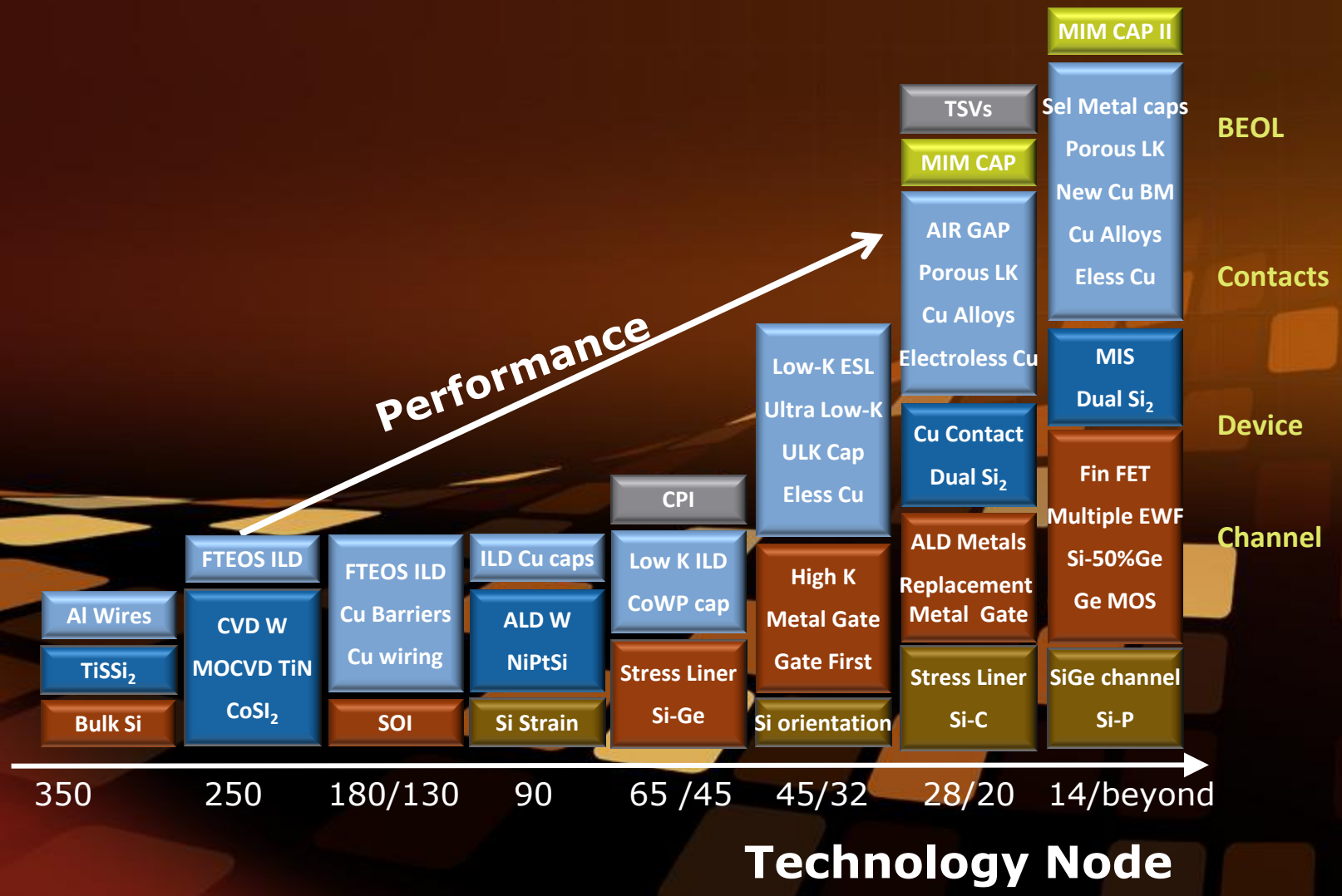
PC to mobility transition	▪ Foundry, Qualcomm and ARM winners in mobility ▪ Mobility: Low-end driving growth; high-end driving profits – 2017: 1.8bn mobile devices (smartphone and tablet) ▪ PCs (x86 base): Declining (~300mm units in 2013)
Customer consolidation	▪ 5 companies drive >60% of total industry wafer demand ▪ System companies designing directly to fabs/foundry
Supplier consolidation	▪ Over $20B of M&A during the past three years
Industry cyclicality	▪ Semiconductor industry remains cyclical (4-yr forecast CAGR of ~6%) ▪ Mobility CAGR ~10%, foundry CAGR 6-8%
Technology scaling	▪ Capex and development costs increasing ▪ Only a few 14nm fabs in the world with $3-5bn revenue / year each ▪ 28nm and 14/10nm likely to be long-lived nodes

Accelerated Leading-Edge Adoption Profile:
Drives Greater Cost and Complexity





Process innovations required for each successive technology is exploding exponentially



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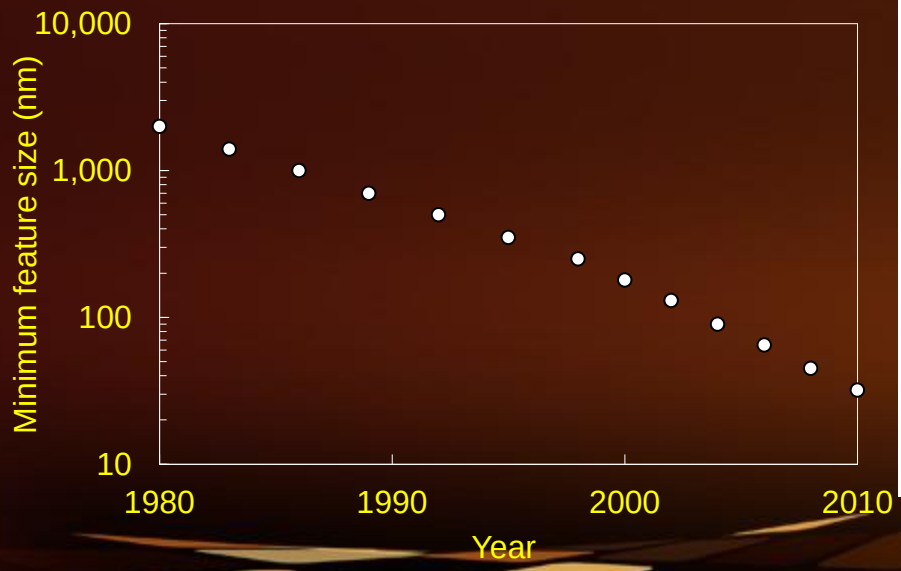
Two ways of looking at Moore's Law

Minimum feature size



Cost per transistor

No Exponential is Forever: But "Forever" Can Be Delayed!

Gordon Moore, ISSCC, 2003

The era in which shrinking features automatically ensured cheaper transistors is over!

The economic foundation on which the semiconductor industry has functioned for 4 decades – a steady decline in prices – is not very solid.

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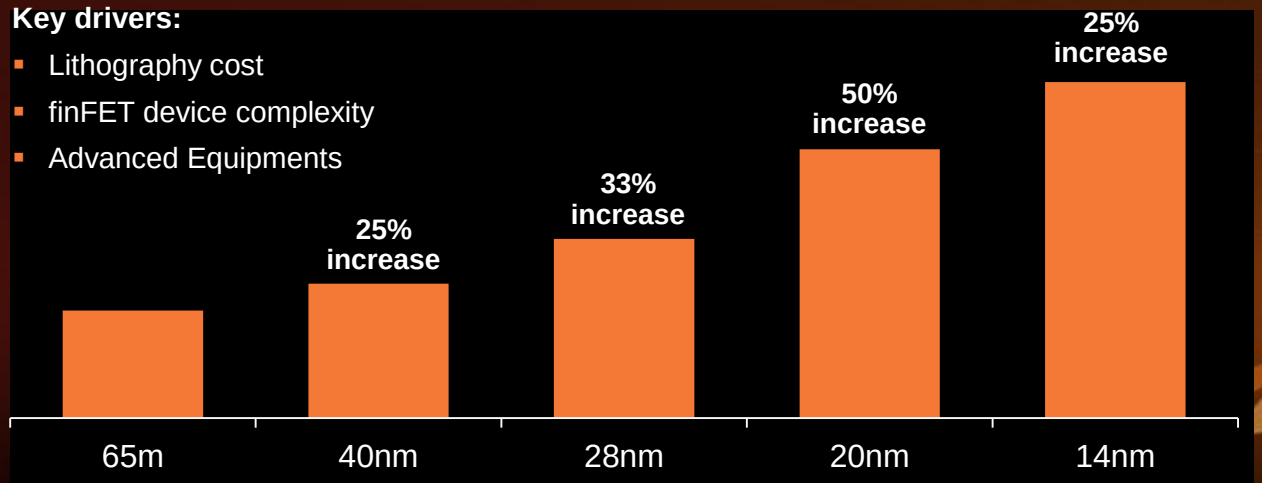
Capex Challenge: Semiconductor Scaling May be Approaching an End at 7nm

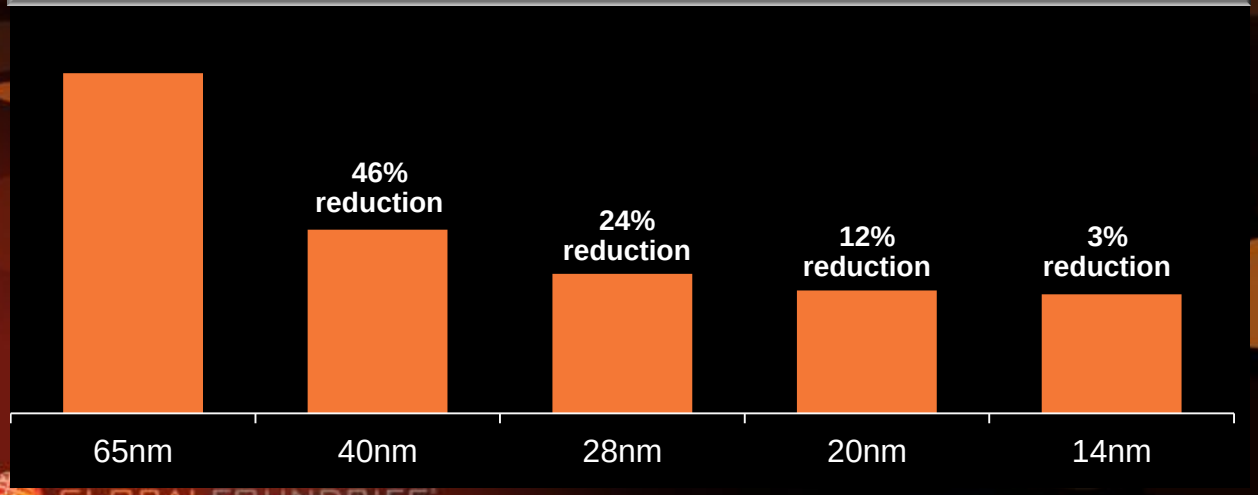
Capex per kwpm of installed capacity ($mm)1

Key drivers:

- Lithography cost
- finFET device complexity
- Advanced Equipments



Cost per transistor reduction (indexed to 65nm)



- At 20nm and below:
  - Lower cost reduction per transistor
  - Performance / Power improvements
- Only customers requiring density, Performance or Lower power consumption will migrate
  - 28nm likely a “long node”
  - Next long-lived node may be 14/10nm, **lengthening investment capture period**
- Cost of building leading-edge fab now >$10bn

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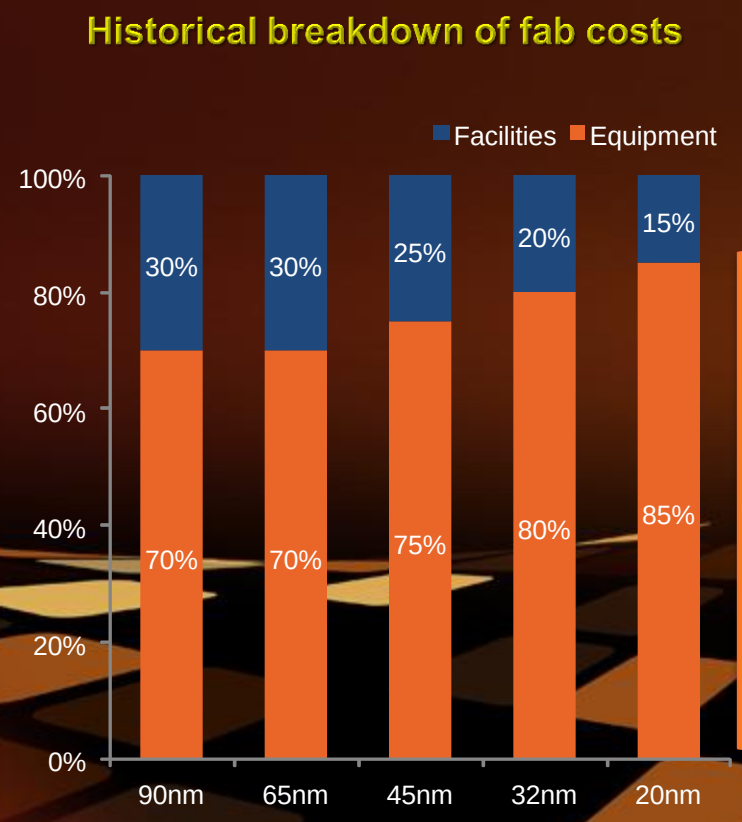
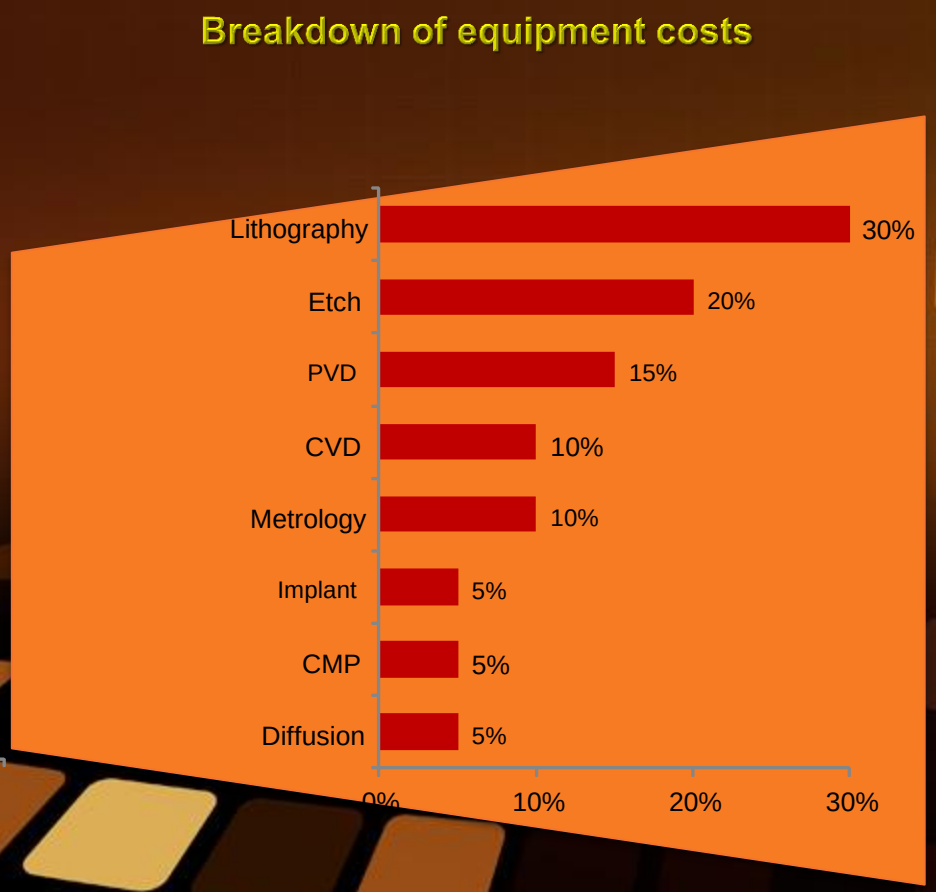
Source: GLOBALFOUNDRIES, Sanford Bernstein, February 2014

[1] Includes equipment and building

Equipment is a greater proportion of overall Fab Costs





Rising technology complexity is driving significant increase in equipment costs

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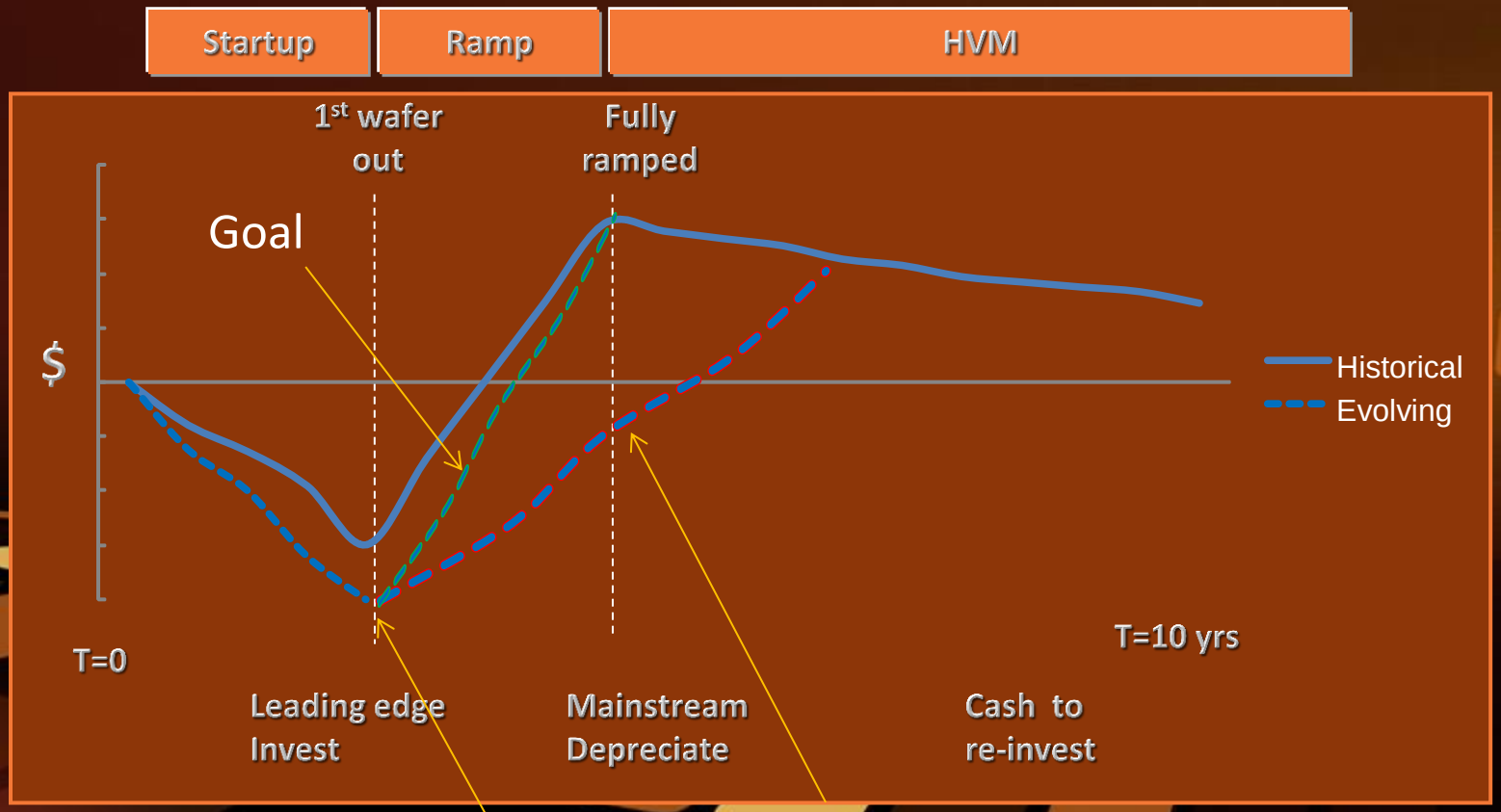
SOURCE: VLSI

ROI Delayed due to increased investment and slower time-to-volume (TTV)



Slower TTV (Higher level of Integration, New yield ramp challenges)

Increased Investment

2015 and Beyond: The Industry Transformation Continues

- The economics of innovation are changing our industry
  - Smart mobile devices redefining personal computing
  - High volume, low cost and globally pervasive
- Advanced technology innovation will provide the path forward
  - Lithography and material inflection points
  - Packaging comes to the forefront
- Collaborative innovation is becoming the norm
  - A shared model for R&D and manufacturing
  - Collaboration from product definition to production

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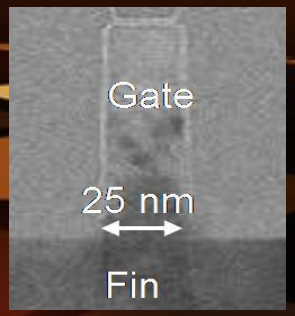
The “Big Five” Opportunities / Challenges

Device Architectures/ Materials

- FDSOI
- FinFETs
- NanoWires
- III-V

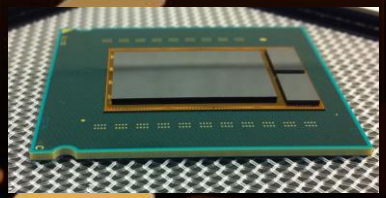


Litho/EUV

- Cost
- Multi-pattern immersion
- EUV Source power
- Tool availability

Packaging

- ‘Normal economics’ are dead
- Value proposition shifting toward PPC
- Alternative scaling opportunities (2.5/3D)



450mm

- Pilot lines and HVM timing driven by 193i and EUV lithography
- G450

COST and Time to Everything

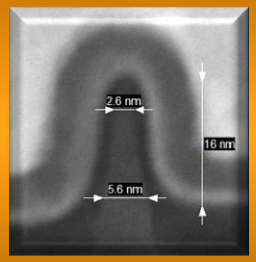
Device Architecture is Poised for Tectonic Shifts

Over one decade IC technology will likely experience major shifts in:

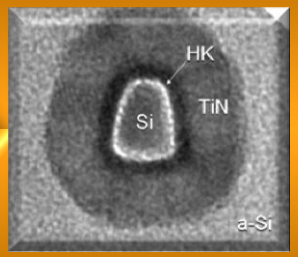
Architecture …

PLANAR

FinFET

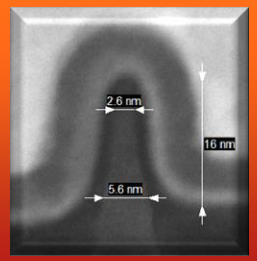


Nanowire



And Materials …

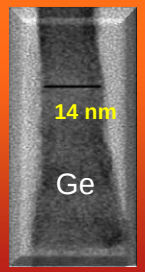
Si



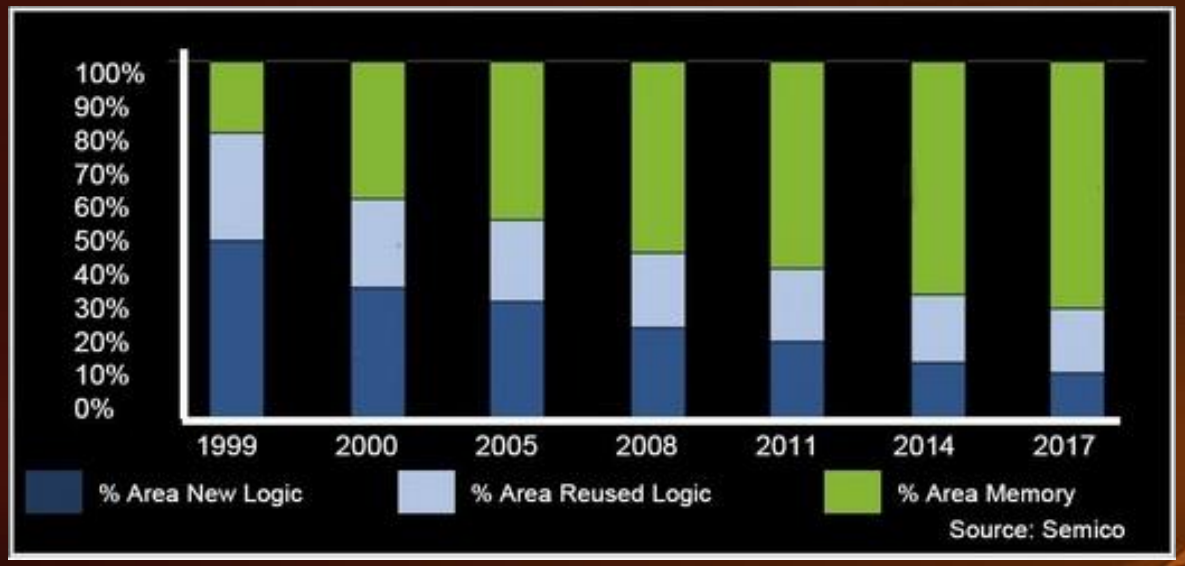
Si/SiGe

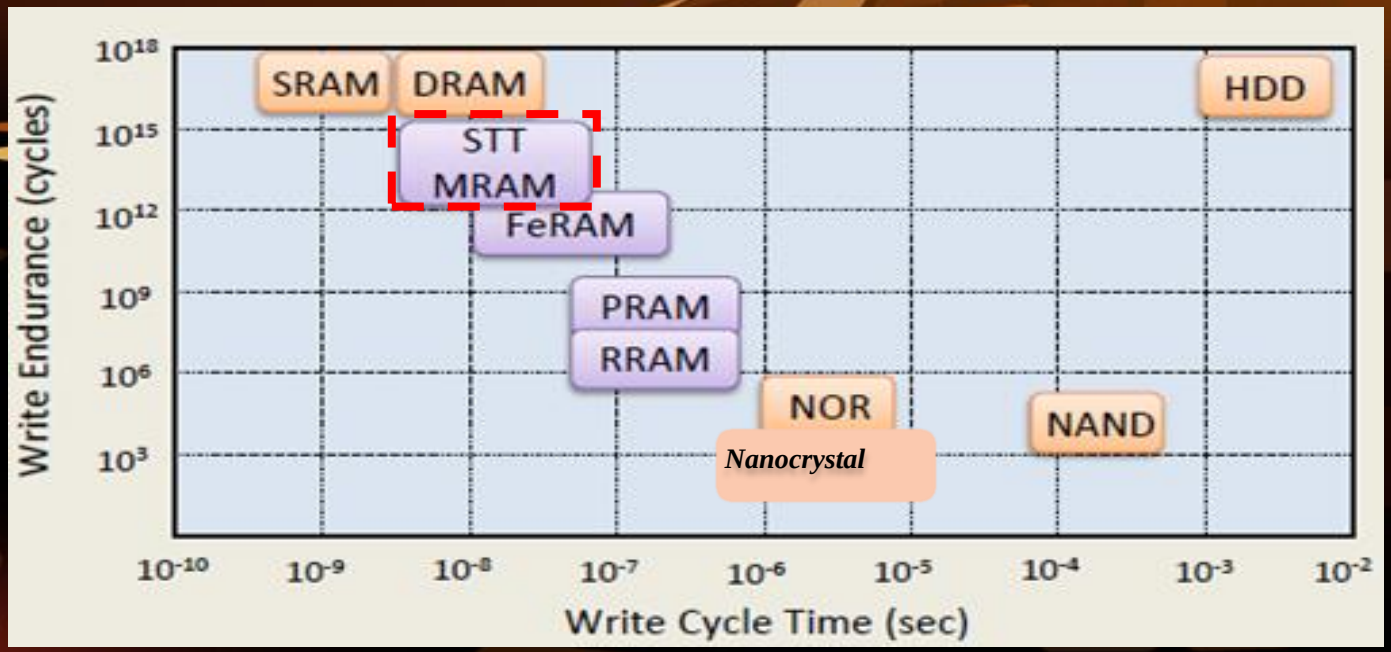
SiGe

Ge/III-V



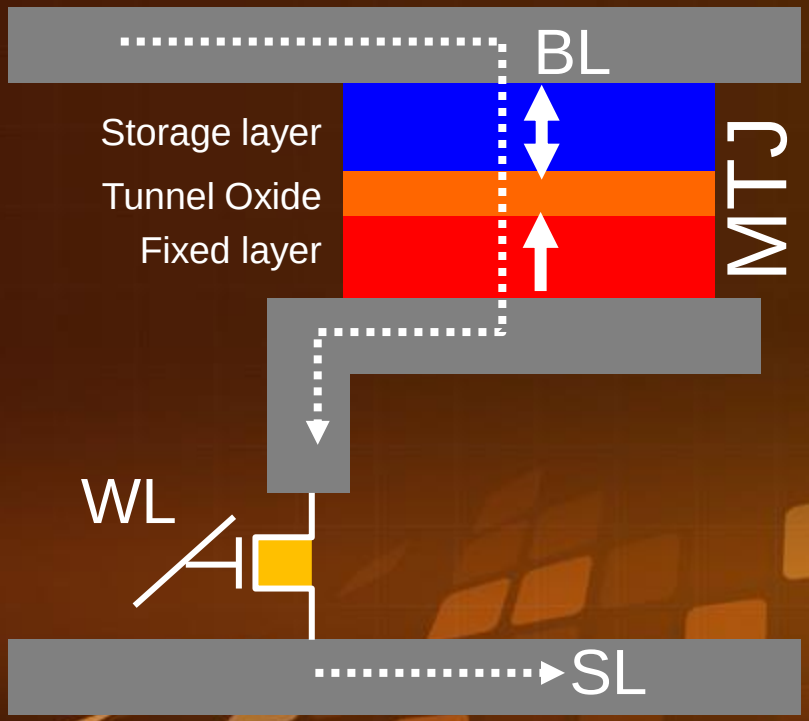
SoC Memory Usage growing…

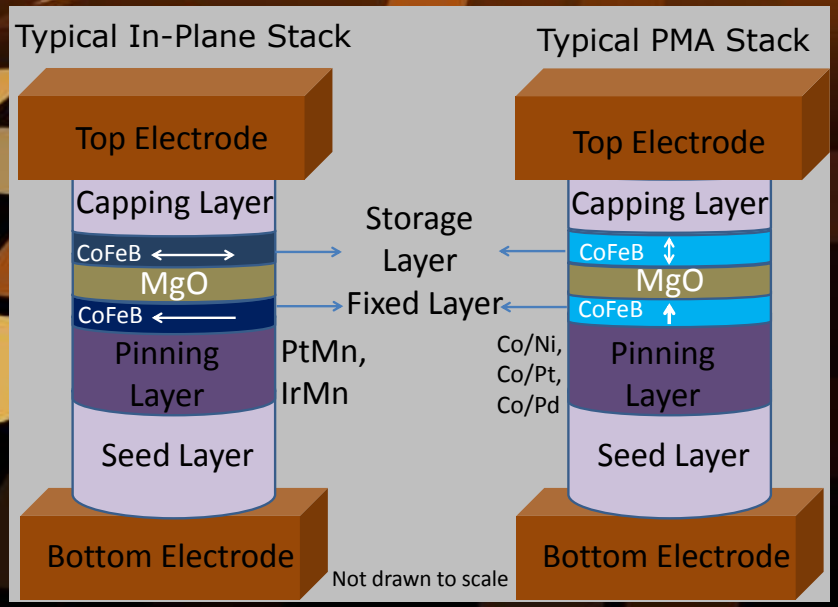




STT-MRAM

- BEOL based memory utilizing magnetic orientation to store bits
- 1 FET 1 MTJ architecture @ 20-40F^2
- Low voltage (~1V) operation – no HV need
- Broad range of applications from retention, endurance, speed and low power characteristics
  - NVM
  - Non Volatile Cache
- Two MTJ types:
  - In-plane: more mature; not seen as scalable beyond 28nm
  - Perpendicular: in-development; similar materials, lower current, faster, smaller MTJ area, scalable





EUV lithography

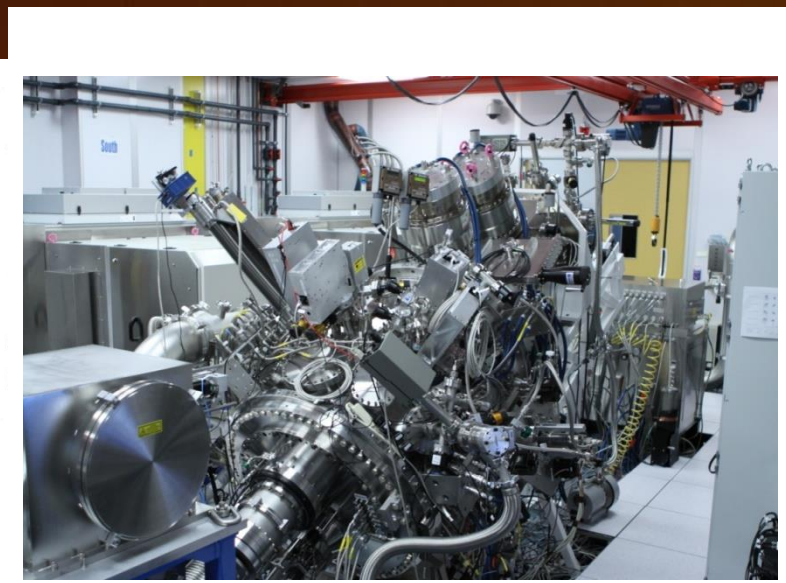
- Semiconductor lithography has always been practiced at wavelengths where there are intense, narrow-band sources of light.

Mercury g-line and i-line

(Image courtesy of Ushio)

KrF and ArF excimer lasers

(Image courtesy of Cymer Inc.)



EUV lithography is practiced at wavelengths where there are multilayer coatings with reasonably high reflectance.

Changes from immersion to EUV lithography

Fundamental changes		
Factor	**Immersion lithography**	**EUV lithography**
Light source	ArF excimer laser	Laser-produced plasma
Mask	Transmission	Reflection
Pellicle	Fluoropolymer	None
OPC	Mature algorithms	New 3D effects
Exposure tool	In air	Vacuum

Changes due to scaling	
Factor	**Major concerns**
Resists	Resolution, line-edge roughness (LER), and sensitivity
Metrology	CD < 20 nm, overlay < 4 nm
Device	Contact resistance, transistor

It has been demonstrated that integrated devices can be fabricated and yielded using EUV

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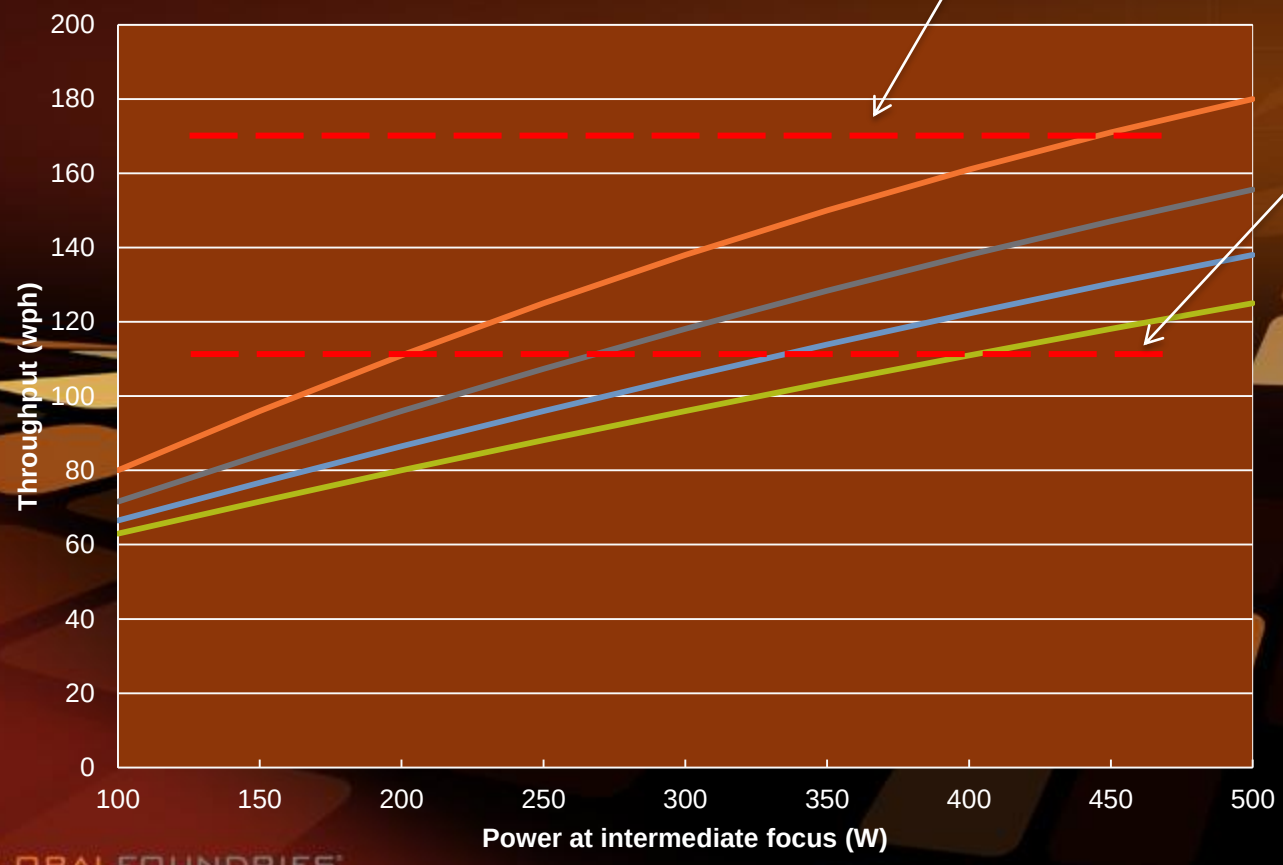
Can we make money using EUV lithography?

EUV: CoO is a strong function of source power

Today, the best sources integrated with exposure tools are < 100 W

Cost equivalence to immersion double patterning

Cost equivalence to triple patterning



Resist sensitivity

15 mJ/cm2
20 mJ/cm2
25 mJ/cm2
30 mJ/cm2

>500 W sources likely needed to make EUV cost effective

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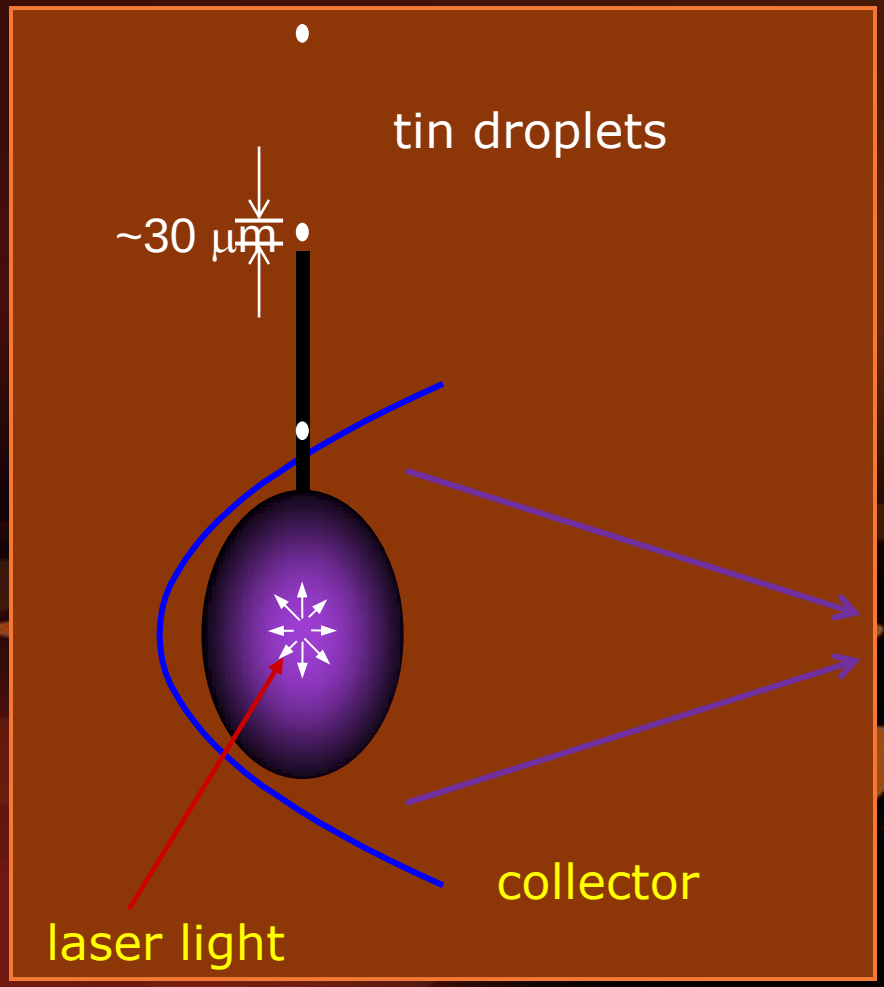
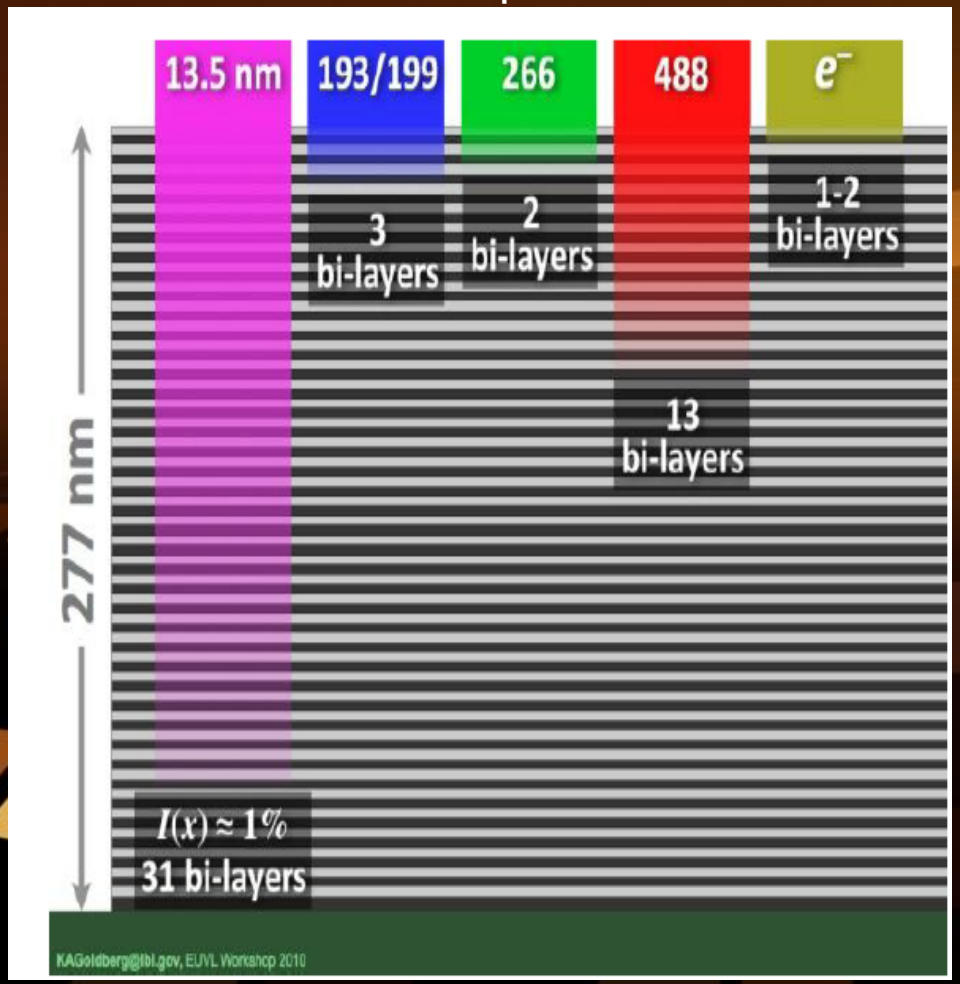
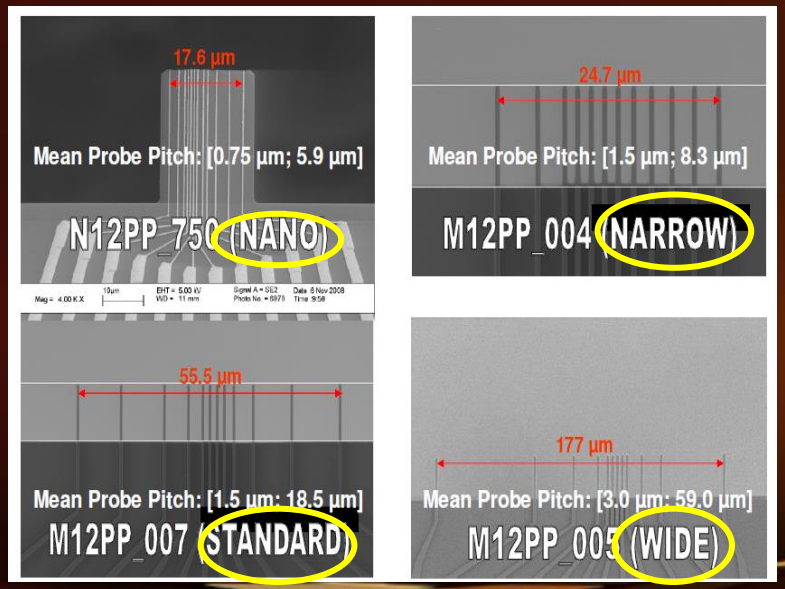
EUV light source and masks

New capabilities will be needed for mask defect inspection.





Metrology challenges for MRAM:
MTJ stack (blanket film)

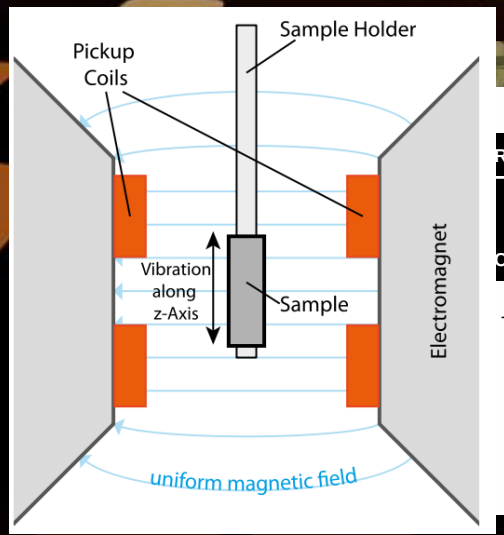


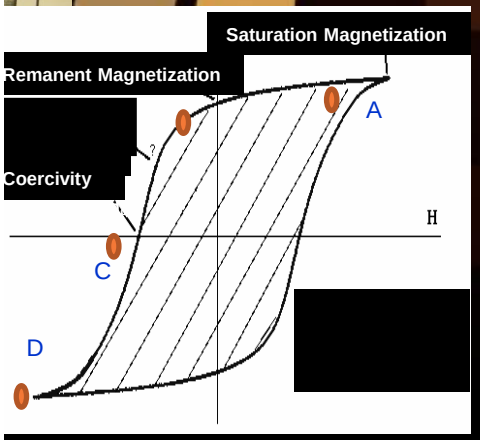
Current in-plane Tunneling (CIPT)

- **In order to measure tunneling magnetoresistance (TMR) signal and resistance areal (RA) product (from MgO tunnel barrier).**
- **Expensive metrology: Probe cost~1500 USD for 100 touch down!**
- **Not considered in-line monitoring tool.**

Challenges on MRAM magnetic wafers measurements
VSM is offline monitoring _low sensitivity

- **Samples need to be diced to small pieces (4mm x 4mm size).**
- **This is not in-line monitoring tool.**





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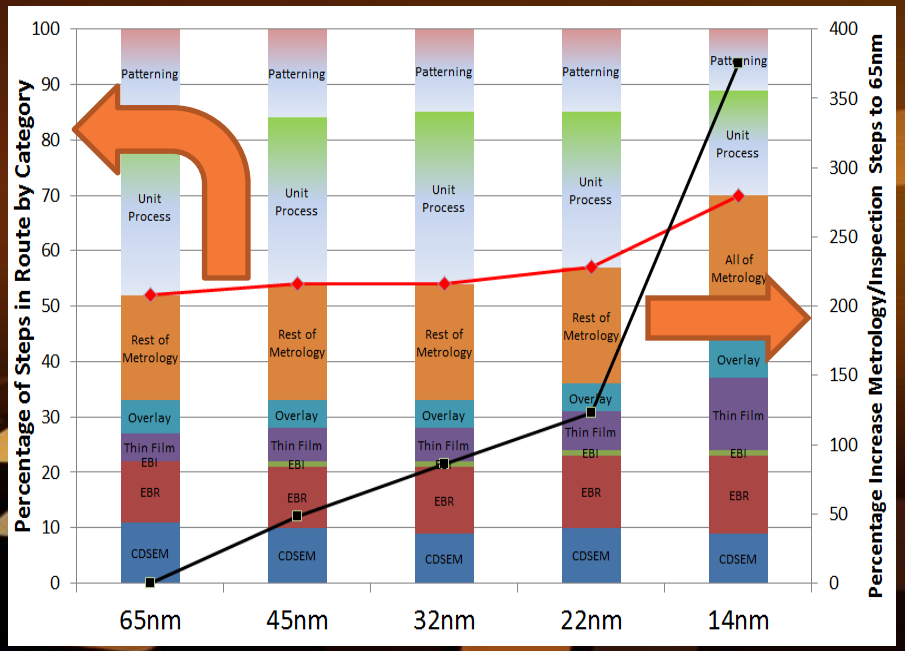
Pervasiveness of Metrology

- State of the art chip manufacturing technology nodes are approaching 2000 steps
- Metrology and inspection steps consume a large share of these steps
  - ~50% of all steps and generally growing
- ~25% to 33% of all the tools in the fab are metrology/defects toolsets
- Significant fab floor space is needed for just metrology/inspection
- CDSEM/film thickness toolsets are typically the most numerous tools in all fabs



- ***Metrology has a significant impact on the Semiconductor Ecosystem Challenges***

Trends in IC Impacting Metrology

1. Shrink puts pressure on Measurement Uncertainty (see ITRS Roadmap)
   - Atomic level accuracy, matching and precision challenge

2. Complex integration, new materials (undercuts, multi-layer SiGe): 3D & Patterning

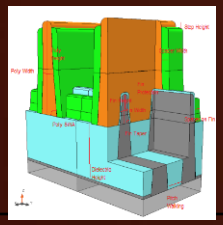
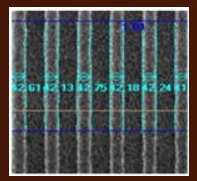
3. Advanced Patterning aspects due to lack of EUV

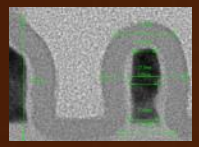
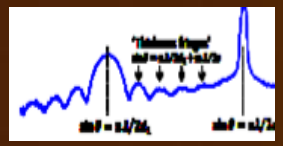
4. How to leverage the best value from Metrology
   - Are we measuring just for the sake of measuring -> need to create value, MTTD

5. Sources of Variation & process control
   - Variability (lot, wfr, die)
   - Need in-die metrology?

Tech Node	65nm	45nm	32nm	22nm	14nm	10nm	7nm
	CDSEM	CDSEM	CDSEM	CDSEM	CDSEM	CDSEM	CDSEM
	Optical Overlay	Optical Overlay	Optical Overlay	Optical Overlay	Optical Overlay	Optical Overlay	Optical Overlay
	Film Thickness – SE and R	Film Thickness – SE and R	Film Thickness – SE and R	Film Thickness – SE and R	Film Thickness – SE and R	Film Thickness – SE and R	Film Thickness – SE and R
		OCD – SE and R	OCD – SE and R	OCD – SE and R	OCD – SE and R	OCD – SE and R	OCD – SE and R
		AFM	AFM	AFM	AFM	AFM	AFM
			MBIR	MBIR	MBIR	MBIR	MBIR
			XPS	XPS	XPS	XPS	XPS
			LEXES	LEXES	LEXES	LEXES	LEXES
				XRR	XRR	XRR	XRR
				XRF	XRF	XRF	XRF
				HRXRD	HRXRD	HRXRD	HRXRD
					Hybrid	Hybrid	Hybrid
							Speculation?

3D Metrology – Technology overview

Attributes:	OCD	CD-SEM	AFM	TEM/XSEM	X-Ray
What to measure	CD, profile, other	CD, roughness	CD, profile	CD, profile, other	Ultrathin films, composition
Where to measure	Periodic grating	Any	Any	Any	Mostly Unpatterned
Time to solution	Days to weeks	Minutes	Minutes	Hours to days	Minutes
Destructive	Negligible	Minor (resist)	Mostly none	Yes	Mostly none
Time to measure	Seconds	Seconds	Minutes to hours	Days	Minutes to hours
Summary: strengths	- Fast measure - Most profile info - High Precision	- Quick setup and fast measure - Anywhere	- Most profile info - High accuracy	- Full profile info - High accuracy	- Ultra-thin films and composition - Synergistic to OCD
Assumptions and limitations	- Model assumptions - Accuracy & precision trade-off - Requires grating	- Constant and uniform profile - Limited profile info - Affected by profile	- Tip wear and characterization - Needs Large space - Low throughput	- Process-dependent resolution - Limited statistics - Expensive & destructive	- Complete correlation volume / composition (needs hybrid)
Typical Fab usage	"workhorse" for CD and profile	"workhorse" for CD	Reference, partial in-line	Absolute reference	Composition

Difficult for a single metrology technique to measure all critical parameters sufficiently on 3D -> ***Hybrid Metrology*** emerging to fill-in gaps where individual techniques are lagging

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In Summary, Eco-system challenges abound, but …

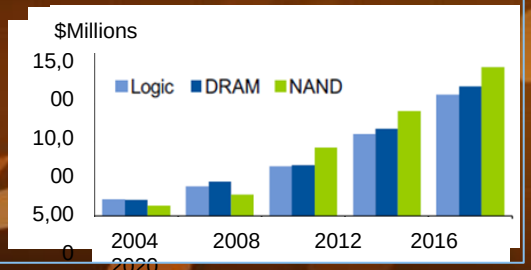
4Xnm → Increasing the need for process control → 1Xnm

Time to Market

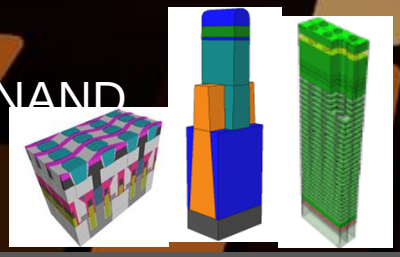
The 'mobile era' has shortened the time between technology nodes

Cost Economics

Major increase in fab construction cost and in process R&D cost in advanced tech nodes



Complex 3D structures: FinFET, 3D-NAND
Double / Quad patterning
Novel materials: HKMG, eSiGe, III-V



Process Complexity

…. Innovation and Engineering have always triumphed

And will drive economical scaling for several more nodes !!

Thank you

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