

Studies of Impurity Redistribution in Copper Ultrafine Lines in BEOL Structures

H. Parvaneh*, S. Novak, K. Dunn, M. Rizzolo and E. Lifshin**

College of Nanoscale Science and Engineering, University at Albany, 251 Fuller Road, Albany, NY 12203

**Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy NY 12180*

*** Corresponding Author*

Abstract

Ultrafine line interconnects in BEOL structures are currently formed by electroplating copper into narrow trenches with a width 40 nm or less. The plating is done over a PVD copper seed deposited on a thin layer of Ta/ TaN that makes contact with the dielectric above the FEOL structures. The total thickness of liner and seed must be as thin as possible to ensure that most of the trench is filled with high purity copper as free of defects and impurities as possible to maintain high conductivity as well as to minimize potential problems that could arise from electromigration. While it would be most desirable to have the copper consist of a single crystal, “bamboo” structure of large grained material whose grain boundaries are perpendicular to electric current flow is considered satisfactory. As deposited copper is usually fine grained, however, and an annealing step is required to promote grain growth needed to attain the bamboo structure. For lines greater than 100 nm in width such annealing procedures usually give satisfactory results, but once the lines are narrower, fine grain structures can persist leading to the possibility of degraded performance. In the current study a variety of analytic techniques have been used to determine the distribution of plating solution components in copper both as a function of solution composition and with and without annealing. Figure 1. Illustrates results obtained by time of flight secondary ion mass spectrometry (ToF-SIMS). Measurements were also made by an SEM/EDS x-ray analysis to obtain higher lateral resolution.

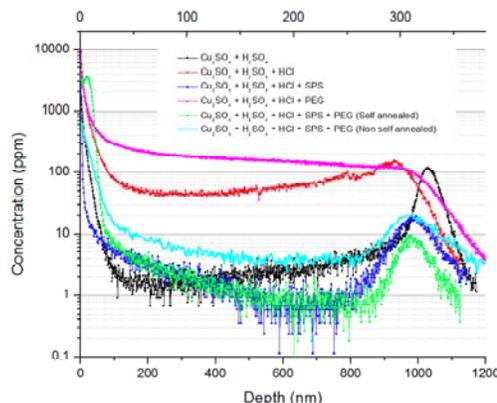


Figure 1. ToF-SIMS Depth Profiles for Chlorine for the Different Plating Conditions