FIB/SEM Structural Analysis Of Through-Silicon-Vias

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ABSTRACT

3D integration of electronic circuits allows to overcome the interconnect performance limitations and to introduce heterogeneous integration of various device technologies. In the 3D stacked IC’s the connection between the dies is made with Cu filled ‘through silicon vias’ (TSV's). Typical dimensions are 25-50 µm depth and 5 µm diameter. For the development of the TSV processing a control of the filling quality is necessary, while for stacked dies the major interest shifts to the study of the bonding quality. Dual beam focused ion beam / scanning electron microscopy is an important method for the structural characterization (Cu filling, Cu grain size, bonding) of TSVs. Due to the large dimensions, the analysis time is however very long.

Different milling strategies that can be applied to optimize the milling conditions will be discussed. To keep the total analysis time acceptable, relatively high beam currents need to be used, generally also in the final milling steps. Due to the large milling depth and the differences in milling rate of the various materials (Cu, Si, SiO₂ liner, TaN barrier, voids) curtaining artifacts can be severe under these conditions and in particular at the bottom of the TSVs the curtaining can complicate the interpretation of the images. Ways to minimize these artifacts or to move the artifacts to positions where they are less harmful for the interpretation of the images will be discussed.

FIGURE 1. SEM images of the bottom of 50 µm deep TSVs a) milled with the standard procedure resulting in strong curtaining artifacts, b) final milled under an angle relative to the TSV axis, and c) milled orthogonal to the TSV axis so that the curtaining lines are strongly suppressed.