IR-Drop Based Electromigration Assessment Materials Data and Characterization Requirements

Valeriy Sukharev¹, Jun-Ho Choy¹, Armen Kteyan², and Xin Huang³

¹Mentor Graphics, Fremont, CA, USA
²Mentor Graphics, Armenia
³UCR, Riverside, CA, USA
Outline

- Introduction and motivations
- Chip design verification for sign-off EM assessment
  - On-chip interconnect elemental unit for EM reliability vs. standard test-structures
  - A role of interconnect redundancy in the resistance degradation
  - Power/ground grid vs. signal nets
- A role of residual stress and temperature in EM-induced degradation
- Methodology of across-interconnect residual stress assessment
- Methodology of across-interconnect temperature assessment
- Voiding-induced IR-drop degradation – parametric failure
- Multi-scale materials data as input for the simulation
- Characterization techniques for models/methodology validation
Reliability vs. Performance

- Current assessment of chip reliability kills chip performance!

**Question:**
How can one predict an IR-drop degradation for a particular chip design?

**Answer:**
- Accurate physics
- Solid models
- Fast and clever algorithm

- Reduction of the operation frequency or voltage at the instance in time when IR drop degradation (increase) exceeds a projected value is killing the chip performance while not affecting the chip EM reliability.
Electromigration Basics

- Material depletion and accumulation occurring at the sites of atomic flux divergence results the localized tensile and compressive stresses.
- Resulting stress gradient creates a backflow atomic flux.
- If the electron-wind and back-stress forces balance each other before the critical stresses needed for void nucleation or metal extrusion are developed the interconnect segment will be immortal.
General Physical Model

If atom an flux divergences somewhere inside metal line then accumulation or depletion of atoms is happening there:

\[ \frac{\partial N_A}{\partial t} + \nabla \cdot J_A = 0 \quad \Rightarrow \quad \frac{\partial \sigma_{Hyd}}{\partial t} = \frac{\partial}{\partial x} \left( \frac{eZj}{\Omega} + \frac{\partial \sigma_{Hyd}}{\partial x} \right) \]

Solution of Korhonen’s equation:

\[ \sigma(x,t) = \sigma_{res} - \frac{eZj}{\Omega} \left( x + 4L \sum_{n=0}^{\infty} \cos \left( \frac{m_n}{2} + \frac{x}{L} \right) \right) \]

Condition for the stable void formation:

\[ \sigma_{crit} = \sigma_{res} - \frac{eZj}{\Omega} \left( x + 4L \sum_{n=0}^{\infty} \cos \left( \frac{m_n}{2} + \frac{x}{L} \right) \right) \]

Nucleation time for stable, growing void:

\[ t_{nuc} \approx \frac{L^2}{2D_0 \Omega B} \frac{E_v + E_{ab} - \Omega \sigma_{crit} - eZjL/2}{k_B T} \ln \left( \frac{eZjL}{2\Omega \sigma_{crit} + eZjL/2 - \sigma_{crit}} \right) \]

Evolution of the hydrostatic stress (a) along the metal line loaded with DC current, and at the cathode end of line, (b) \( j = 5 \times 10^9 \text{A/m}^2, T = 400K \).

Black’s equation based MTTF

EM accelerated test: $T_{\text{accel}}$ and $j_{\text{accel}}$

- TTF averaged with the accepted distribution function provides mean time to failure (MTTF).
- A set of calculated MTTF obtained for different $T_{\text{accel}}$ and $j_{\text{accel}}$ is used for extraction of the current density exponent $n$ and apparent activation energy $E$ used in the Black’s equation:
  $MTTF = \frac{A}{j^n} \exp\left(\frac{E}{kT}\right)$
- Assuming an “universal” character of the extracted $n$ and $E$, the MTTF at the used conditions is:
  $MTTF_{\text{use}} = MTTF_{\text{accel}} \left(\frac{j_{\text{accel}}}{j_{\text{use}}}\right)^n \exp\left(\frac{E}{k \left(\frac{1}{T_{\text{use}}} - \frac{1}{T_{\text{accel}}}\right)}\right)$

Different lines characterizing by different microstructures reveal different times to failure (TTF)

Experiments demonstrates that $n$ and $E$ by themselves are the functions of $j$ and $T$

M. Hauschildt, C. Hennesthal, G. Talut, et al. (GF & Fraunhofer), 2C.1.1, IRPS 2013
EM Assessment – PROBLEM!

- Stress and temperature dependency of the current density exponent,
- Current density and temperature dependency of the activation energy
- Across-interconnect temperature and residual stress variation

ALL THESE FACTORS MAKE QUESTIONABLE USING BLACK EQUATION and BLECH LIMIT (CRITICAL PRODUCT) FOR ACCURATE EM ASSESSMENT!

\[ t_{\text{nucl}} = \frac{A(\bar{r}, \sigma_{\text{res}})}{j n(T, \sigma_{\text{res}})} \exp\left( \frac{E(j, T)}{kT} \right) \]

\[ (j \times L)_{\text{crit}} = \frac{\Omega(\sigma_{\text{EM}} \pm \sigma_{\text{res}}(\bar{r}, T))}{eZ\rho} \]

EM assessment requires:
- Current density assessment
- Temperature assessment
- Residual stress assessment

Chip-scale EM assessment

Interconnect functionality

- interconnectivity for signal propagation
  - bidirectional pulsed currents
- voltage delivery
  - unidirectional current
  - power grids, more susceptible to EM effect

Traditional segment-based EM assessment

- single segment based stress analysis
  - assume individual segment is confined by diffusion barriers
  - however, in power grids, atoms can diffuse in the interconnect tree, stress redistribution
- EM induced failure rate of the individual segment

EM induced degradation in power grids

- high level of redundancy
- Failure: loss of performance, parametric failure
  - cannot deliver needed voltage to any point of the circuitry

New methodology for EM assessment:

- IR drop based assessment
- physics based models for void initiation and evolution
STRESS ASSESSMENT
IC Problem

- Consumer demand is driving the need for thinned substrates, introduction of new connectivity structures (e.g. 3D stacking, TSVs, C4- and u-bumps) that cause unexpected device performance

Mechanical stress caused by IC architecture and packaging impacting MOSFET characteristics/performance – **Chip-Package-Interaction (CPI)**
What is 3D TSS (Through Si Stacking) Technology

- **Value Proposition**
  - Small form factor (in X-Y & Z)
  - Improved Performance
  - Heterogeneous Integration

- **Typical Implementation**
  - e.g. Memory-on-Logic
    - stacking orientation: F2B
    - TSV via diameter ~ 5μm
    - wafer thickness ~ 50 μm
  - e.g. Die on (Active) Interposer
    - stacking orientation: F2F
    - TSV via diameter ~ 10μm
    - wafer thickness ~ 100 μm
  - ~20 μm ~100 um ~20 um

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Multiscale methodology for calculation of device-to-device variation of stress: Stress Exchange Format

**Package-scale simulation (FEA)**
**Input:** geometry; material properties; smeared mechanical properties for RDLs, Silicon/TSV bulk, interconnect.
**Output:** field of displacement components on the die faces.

**Die-scale simulation (FEA)**
**Input:** geometry; field of displacements on the die faces; coordinate-dependent mechanical properties for RDLs, Silicon/TSV bulk, interconnect.
**Output:** Distribution of the strain components across device layer.

**Layout-scale with feature-scale resolution:**
**Input:** GDS.
**Output:** distribution of the stress components across interconnect metal layer.

**Package scale**
- Package tech file
- Package simulations (FEA)

**Die scale**
- Bump effect (compact model)
- TSV induced stress (compact model)
- CPI stress/strain (FEA)

**Feature scale**
- Composite interconnect layers (compact model)
- Transistors layout effect (compact model)
- Design (GDSII, OASIS Design tech file)

Stress and strain components (per transistor); mobility shift
Effective mechanical properties of BEoL, BRDL interconnects and Si/TSV bulk layer

- Theory of the mechanical properties of anisotropic composites is employed.
- Required input: (a) Thermo-mechanical properties of each material – metal, dielectric: CTE, Young’s moduli, Poisson factors; (b) fraction of dispersed phase; (c) routing direction of the metal layer.
- For each bin of each layer of interconnect, depending on routing direction: for example the Young’s modulus:

\[
E_{\parallel}^{i,j} = E_M \rho_{M}^{i,j} + E_D \left(1 - \rho_{M}^{i,j}\right)
\]

\[
E_{\perp}^{i,j} = \frac{E_M E_D}{E_D \rho_{M}^{i,j} + E_M \left(1 - \rho_{M}^{i,j}\right)}
\]

Young’s modulus components for M1 layer

- \(E_x\) for bulk Si/TSVs: bin size 20 (left) and 100nm (right), TSV 6nm, spacing 40nm.


FCMN2015, Dresden
Supported Compact Models

1. Package-scale: Warpage-Induced Stress

2. Compact Model for Bump-Induced Displacements

3. Effect of Non-Uniform Interconnect

4. Compact Model for TSV-Induced Stress:

Residual stress in on-chip interconnect

Interconnect face warpage

Hydrostatic stress in M1 layer

Residual (hydrostatic) stress distribution across M1 layer with the overlaid C4 bumps, (left) and u-bumps (right).

Interconnect tree is an elemental EM reliability unit representing a continuously connected, highly conductive metal (Cu) lines within one layer of metallization, terminated by diffusion barriers.
TEMPERATURE ASSESSMENT
Major components

- MGC’s effective thermal properties extractor.
  - Each interconnect layer is considered as a composite: a mixture of metal fibers included in a dielectric matrix.
  - Calculates the effective thermal conductivity \( k_i, i=x,y,z \), specific heat of each interconnect layer as a function of local metal density \( \rho_M \).
  - Lateral components \( K_{x,y} \) inside each metal layer are determined by a routing direction:
    - Parallel to the routing direction:
      \[
      k_{ll} = \rho_M k_M + (1 - \rho_M)k_{ILD}
      \]
    - Normal to the routing direction:
      \[
      k_\perp = k_{ILD} \left[ 1 + \frac{\rho_M}{k_{ILD}/(k_M - k_{ILD}) + (1 - \rho_M)/2} \right]
      \]
    - A vertical component:
      \[
      k_z = \rho_M k_M + (1 - \rho_M)k_{ILD}
      \]

- Thermal Netlist Builder.
  - A die is represented by a 3D array of cuboidal thermal cells. Each cell contains a thermal node, and is characterized by local effective thermal properties \( (R_{th}, C_{th}) \).
  - The array transforms into a thermal netlist.

- SPICE simulator.
  - Calculates transistor power consumption.
  - Solves for temperature for each thermal node.
From effective thermal props to thermal netlist

- Construct an array of cuboidal cells of dimension, LxLxt: “L” is user-supplied binSize.
- For each cell, MGC’s engine uses Calibre to extract local metal density, and calculates effective thermal properties.
- Thermal netlist builder transforms effective thermal properties into $R_{th}$ and $C_{th}$.

$$
R_{top/bottom,i} = \frac{1}{k_z,i} \frac{t_{M6}}{L^2}; \ R_{north/south,i} = \frac{1}{k_{y,i}} \frac{L/2}{t_{M6}L}; \ R_{east/west,i} = \frac{1}{k_{x,i}} \frac{L/2}{t_{M6}L}
$$

$$C_{cell,i} = S_i \cdot (L \cdot L \cdot t_{M6})$$

- The array transforms into a thermal netlist.
- Consideration on boundaries
  - Fixed T with V source & R=0; Insulation with large R.
INTERCONNECT SCALE EM MODELING
Chip-scale EM assessment

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Interconnect segment vs. wire

Closed-form analytical solution for stress evolution in the multi-branched interconnect tree

Evolution of the stress distribution along the segment of the shown T-shaped tree; (a) line 1, (b) line 2, and (c) line 3.

If we disassemble these branches a standard stress evolution will take place in each of them:

Steady state distribution of the hydrostatic stress inside interconnect tree in void-less regime

- Assume (just for a moment) that the void less steady state was achieved in the tree.
  
  For the steady state: \[ \sigma_{\text{cathod}} - \sigma_{\text{anode}} = \Delta \sigma_{ij} = \frac{eZ\rho(j_iL_{ij})}{\Omega} \]

- Consider the redistribution of the atoms between sub-segments due to unblocked sub-segment ends:
  
  \[
  \sum_{i=1}^{j} \left( \sigma_i - \frac{B}{3} \left( \frac{R}{\delta} \right) e^{\frac{E_v}{kT_{25}}} + \frac{eZ\rho(j_iL_{ij})}{2\Omega} \right) \right]L_{ij} = 0
  \]

- Previously, we use uniform temperature distribution:
  The shortest void nucleation time is characterized by the biggest steady state stress \( \sigma_m(j_1, j_2, \ldots, j_n) \),
  
  \[
  t_{\text{nuc}}^m \approx \frac{L_{\text{max/min}}^2}{2D_0} e^{\frac{E_v+E_D}{kT}} kT \exp \left\{ -f\Omega \sigma_m(j_1, j_2, \ldots, j_n) \frac{kT}{\Omega B} \cdot \ln \left\{ \frac{\sigma_m(j_1, j_2, \ldots, j_n) - \sigma_{\text{Res}}}{\sigma_m(j_1, j_2, \ldots, j_n) - \sigma_{\text{crit}}} \right\} \right\}
  \]

- With temperature variation: Void nucleation time is affected by both T and hydrostatic stress. Consider both factors to find the first nucleated void (min\{t_{\text{nuc}}^m\})
Voiding

When void is nucleated the stress at the void surface is zero. The solution of the stress kinetics equation with the zero-flux condition at the downstream (anode) end of the line is [J. He and Z. Suo, AIP Conf. Proceedings, vol. 741, 2004]:

$$\sigma(x,t) = -\frac{eZ\rho jL}{\Omega} \left( \frac{x}{L} + \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n-1)^2} \sin \left( \frac{(2n-1)\pi x}{2L} \right) \exp \left( -\left( \frac{2n-1}{2} \right)^2 \frac{t}{\tau} \right) \right)$$

Here,

$$\tau = L^2 \frac{\kappa}{k_B T DB \Omega}$$

Once the stress field is solved, the void volume is calculated from the volume of atoms drifted into the line:

$$V = -A \int_0^L \Omega N_p dx = -A \int_0^L \Omega \left( \frac{\sigma}{B} \right) dx = -A \int_0^L \left( \frac{\sigma}{B} \right) dx = \frac{eZ\rho jL^2 A}{2\Omega B} \left( 1 + \frac{32}{\pi^3} \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n-1)^2} \exp \left( -\left( \frac{2n-1}{2} \right)^2 \frac{t}{\tau} \right) \right)$$

There are two limiting cases for volume void:

1. Short time; stress in the line is small, so

$$\Gamma(\bar{r}) = \frac{D}{\Omega k_B T} eZ\rho j \text{ and } V = \Omega \Gamma A t = \frac{eZ\rho jDA t}{k_B T}$$

2. Steady state was reached; the atomic flux vanishes, void volume is saturated:

$$\sigma(x) = -\frac{eZ\rho j x}{\Omega} \text{ and } V_{sat} = -A \int_0^L \left( \frac{\sigma}{B} \right) dx = \frac{eZ\rho jL^2 A}{2\Omega B}$$
Void growth-induced line resistance change

Once V(t) is known the kinetics of line resistance can be easily calculated.
For a void volume at an instance in time t we have:

\[ V_{\text{void}}(t) = \vartheta \star (t - t_{\text{nuc}}) HW \]
\[ \vartheta = \frac{DeZ \rho j}{kT} \]

Or, when current density depends on time:

\[ V_{\text{void}}(t) = HW \frac{DeZ \rho}{kT} \int_{t_{\text{nuc}}}^{t} j(t) dt \]

For the corresponding change in the line resistance we can write:

\[ \Delta R = R_{\text{Ta}}^{\text{Void}} - R_{\text{Cu}}^{\text{Void}} \]
\[ \frac{1}{R_{\text{Ta}}^{\text{void}}} = \frac{1}{R_{\text{Ta}}^{\text{void, wall}}} + \frac{1}{R_{\text{Ta}}^{\text{void, wall}}} + \frac{1}{R_{\text{Ta}}^{\text{void, bottom}}} \]

\[ R_{\text{Ta}}^{\text{void, wall}} = \rho_{\text{Ta}} \frac{\vartheta \star (t - t_{\text{nuc}})}{hH} ; R_{\text{Ta}}^{\text{void, bottom}} = \rho_{\text{Ta}} \frac{\vartheta \star (t - t_{\text{nuc}})}{hW} ; R_{\text{Cu}}^{\text{void}} = \rho_{\text{Ta}} \frac{\vartheta \star (t - t_{\text{nuc}})}{HW} \]

\[ \Delta R(t) = \vartheta \star (t - t_{\text{nuc}}) \left[ \frac{\rho_{\text{Ta}}}{h(H + 2W)} - \frac{\rho_{\text{Cu}}}{HW} \right] \approx \vartheta \star (t - t_{\text{nuc}}) \frac{\rho_{\text{Ta}}}{h(H + 2W)} = \frac{V_{\text{void}}(t) \rho_{\text{Ta}}}{h(H + 2W)HW} \]
Void nucleation time and void growth time as the functions of the current density and test temperature

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<td>2.56E+08</td>
<td>1.54E+07</td>
<td>9.21E+05</td>
<td>8.71E+04</td>
<td>1.22E+04</td>
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</tbody>
</table>

Critical product as a function of temperature.

Extracted dependencies of $n$ on $T_{test}$ (a), and $E_a$ on $j$ (b) for Sim. 1 ($T_{ZS}=653$ K, $S_{crit}=500$MPa) and Sim. 2 ($T_{ZS}=723$ K, $S_{crit}=600$MPa) vs. experimental data.

Extraction of the current density exponent, (a), and the apparent activation energy, (b), based on the calculated $t_{nuc}$.
EM-induced supply voltage degradation

- Nucleated void
- Growing void
- Saturated void

EM Assessment Results in IBM Benchmarks

- Current source values are modified to ensure initial IR drop of any node is smaller than the threshold value.

<table>
<thead>
<tr>
<th>Power Grid</th>
<th>Time to Failure (yrs)</th>
<th>CPU time of Our Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Nodes</td>
<td>Black's Equation</td>
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<tr>
<td>IBMPG2</td>
<td>61797</td>
<td>7.82</td>
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<td>12.58</td>
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<td>IBMPG5</td>
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<td>IBMPG6</td>
<td>807825</td>
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<tr>
<td>IBMPGNEW2</td>
<td>715022</td>
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</tr>
</tbody>
</table>

- Both Black's equation based series and Mesh models lead to pessimistic predictions.

- EM effect is sensitive to temperature
  - TTF exponentially relates to temperature (the same as Black's equation)

- Reducing chip temperature/temperature gradient could extend TTF

In this work, the first failure is most likely to happen at the nodes where the initial hydrostatic stress is large.

(a) Voltage drop (V) distribution and (b) Initial steady state hydrostatic stress (Pa) distribution predicted by initial current density in IBMPG2.

EXAMPLE OF IR-DROP EM ASSESSMENT
CHIP-SCALE EM ASSESSMENT CONSIDERING THE IMPACT OF TEMPERATURE AND CPI STRESS VARIATIONS
Layout

- Design:
- 7-metal layer
- 32nm
- Dimension: 184um × 184um

<table>
<thead>
<tr>
<th>Layer number</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Contact</td>
</tr>
<tr>
<td>4</td>
<td>M1</td>
</tr>
<tr>
<td>5</td>
<td>V1</td>
</tr>
<tr>
<td>6</td>
<td>M2</td>
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<td>11</td>
<td>V4</td>
</tr>
<tr>
<td>12</td>
<td>M5</td>
</tr>
<tr>
<td>13</td>
<td>YX(V5)</td>
</tr>
<tr>
<td>14</td>
<td>IA(M6 wide)</td>
</tr>
<tr>
<td>15</td>
<td>XA(V6)</td>
</tr>
<tr>
<td>16</td>
<td>IB(M7 wide)</td>
</tr>
</tbody>
</table>
Initial current density and initial IR-drop
-power net, M1 layer

FCMN2015, Dresden
Initial hydrostatic stress
-power net, M1 layer

$suspicious$ to EM failure

$\sigma_{crit} = 500$ Mpa
Temperature distribution

Metal 1 layer


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EM induced IR drop change
- power net

- Significant IR drop changes in M1 layer
EM induced IR drop change
- power net

Branches with voids
- power net

Voids mainly locate in M1 layer, some voids locate in M3 layer

EM induced IR drop change
- power net

Chip fails when the maximum IR drop > threshold level

FCMN2015, Dresden
How to calibrate/validate verification tools?

• **Both types of tools predicting the effect of CPI on chip performance and chip reliability need as inputs:**
  - Measured foundry and process dependent thermal-mechanical properties of the involved materials.
  - Calibrated compact models employed for calculation of the stresses and temperature across a device layer and across the whole chip.
  - Calibrated models for calculating effective thermal-mechanical properties of all composite layers (BEoL and RDL interconnects, underfill with C4 and u-bumps, silicon bulk with TSVs, etc.).

• **Both types of tools need to be validated by a direct comparison between the predicted characteristics and measured:**
  - Comparing the measured characteristics of individual transistors and predicted by verification tools is a validation of the CPI effect on chip performance.
  - **What kind of test-structures should be used to validate the effect of CPI on chip reliability (EM as an example)?**
Calibration of the models for effective thermal-mechanical properties

- New approach to determine CTE for Cu/ULK for a partially de-processed 3DIC, by combination of FIB cutting and SEM (heating stage holder).
  - isolate a bar
  - separate into two bars of same length, and measure the gap in the middle as a function of temperature up to 250°C
- Layout file (GDSII & Oasis) allows to calculate all three components of the effective CTE for different bin sizes.
- Following FEA simulation could allow to calibrate the effective CTE model.

- Similar approach can be employed for calibration of the models for effective Young’s modulus and Poisson factor.
- There is a need in experimental methodology for calibrating the models for thermal properties of on-chip interconnects and other composite layers.

Proof Electrical vs. Mechanical

**MECHANICAL DOMAIN**

H-Bar – TEM Lamella

Distance to TSV

**TEMP CBED measurement of strain**

Reconstructive FEA simulation

After FIB processing

Before FIB processing

**ELECTRICAL DOMAIN**

Calibrating $\varepsilon_{th}$:

$$\sigma_x = -\sigma_y = \frac{E_s \varepsilon_{th}}{1 - 2\nu_s} \frac{D_{TSV}^2}{4r^2} \cos 2\theta$$

Strain distribution in lamella

Calibrating $\varepsilon_{th}$:

$$\Delta I_{\text{simul}} = \left(\pi_x' \sigma_x + \pi_y' \sigma_y + \pi_z' \sigma_z\right)^{\text{SPICE}}$$

Good fit between simulated and measured electrical characteristics of transistors located at different distances from TSV allows to calibrate the developed tool with relatively easy accessible electrical data.

Validation with the Foundry calibrated Model

Calibration was performed on ~100 gates
Prediction was made for all (~4000) gates

Test-chip segment

Die Corner Array: Test-chip 28nm node

Schematics of the test structures used for model calibration: die corner

Validation related tasks

• How can we validate the predicted stress distribution inside the interconnect metal of the die stacked by 3D IC technology?
• How can we validate the distribution of the EM- or SM-induced voids inside BEOl interconnect?
• How can we monitor the accelerated kinetics of IR-drop degradation? What kind of test-structures should be developed?
• Test-chips with the temperature sensors?
• Itc., etc.
CONCLUSIONS

A NOVEL METHODOLOGY FOR FULL-CHIP POWER/GROUND NETS REDUNDANCY-AWARE EM ASSESSMENT BASED ON IR-DROP ANALYSIS WAS DEVELOPED.

PHYSICS-BASED MODEL FOR TEMPERATURE- AND RESIDUAL STRESS-AWARE VOID NUCLEATION AND GROWTH WAS DEVELOPED AND IMPLEMENTED IN THE FLOW.

A DEVELOPED TECHNIQUE FOR CALCULATING THE HYDROSTATIC STRESS DISTRIBUTION INSIDE A MULTI BRANCH INTERCONNECT TREE ALLOWS TO AVOID OVER OPTIMISTIC PREDICTION OF THE TIME TO FAILURE MADE WITH THE BLECH-BLACK ANALYSIS OF INDIVIDUAL BRANCHES OF INTERCONNECT SEGMENT.