2015 INTERNATIONAL CONFERENCE ON FRONTIERS OF CHARACTERIZATION AND METROLOGY FOR NANOELECTRONICS
THE 10TH CONFERENCE IN THE SERIES!

APRIL 14-16, 2015
DRESDEN, GERMANY

DAVID G. SEILER, FCMN CO-CHAIR
CHIEF, SEMICONDUCTOR AND DIMENSIONAL METROLOGY DIVISION,
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY, GAITHERSBURG, MD
I AM DELIGHTED TO BE IN DRESDEN!
FCMN LOCATIONS

• 2003: J.J. Pickle Research Campus, Univ. of Texas, Austin, TX
• 2005: Univ. of Texas at Dallas, Richardson, TX
• 2009: College of Nanoscale Science and Engineering, SUNY, Albany, NY
• 2011: MINATEC Campus, Grenoble, France (CEA-Leti)
• 2015: Dresden, Germany (Fraunhofer)
FCMN COMMITTEE

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  • Bob McDonald, formerly of Intel (Treasurer)
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  • Alain Diebold, College of Nanoscale Science and Engineering, SUNY Albany

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  • Victor Vartanian, ISMI
  • Wilfried Vandervorst, IMEC
  • Usha Varshney, NSF
FOCAL POINT FOR FRONTIERS OF SEMICONDUCTOR NANOELECTRONICS METROLOGY

Some Keynote Speakers

Craig Barrett, formerly President, Intel
Mark Melliar-Smith, formerly President and CEO of SEMATECH
Dennis Buss, VP, Silicon Tech. Development, Texas Instruments
Bob Helms, formerly President and CEO of SEMATECH
Michael Polcari, President and CEO of SEMATECH
Mark Durcan, COO of Micron
Tze-Chiang (T.C.) Chen, IBM Fellow and VP, Science & Technology
Michel Brilhacq, Senior Advisor, CEA-LETI
Mike Mayberry, VP, Intel
Frontiers of Characterization and Metrology for Nanoelectronics 2015

April 14-16, 2015
Dresden, Germany

Editors:
E.M. Secula
D.G. Seller

www.nist.gov/pml/div883/conference/

Hubert Lakner,
Executive Director,
Fraunhofer Institute
for Photonic
Microsystems

Suresh Venkatesan,
Senior VP,
Technology
Development,
Global Foundries

Klaus von Klitzing,
Max-Planck-Institut
FKF
ARCHIVED PAPERS AND TALKS FREE ON-LINE!

• Proceedings papers from 1998-2009 are available free of charge, thanks to an agreement between the National Institute of Standards and Technology (NIST) and the American Institute of Physics (AIP)

• Presentation slides from most of the invited talks from 2000-2013 are available

• Most posters from the 2013 conference are available

• www.nist.gov/pml/div683/conference/archives.cfm
SNAPSHOT FROM THE CONFERENCE SERIES

• “Transistor Scaling will continue to be an important Technology Driver in the Internet Era. But it will no longer be the sole driver: SOC Integration will be increasingly important.”
  • “Technology in the Internet Era,” Dennis Buss, Texas Instruments, 2000 FCMN

• “CMOS Extension and Beyond CMOS both require characterization and metrology at the nanoscale.”

• “Interfacial measurement is increasing in difficulty & importance.”
  • “The Impact of Nano-Sized Dimensions on Characterization and Metrology,” Alain Diebold, SEMATECH, 2007 FCMN

• “3D Technology integration is a family of technologies enabling vertical stacking of semiconductor chips and other components. It is the next revolution in Semiconductor technology roadmap and is fundamental to staying on the path of performance improvement … The integration of 3D technology will enable performance, form factor, power savings, and cost requirements of the next generation of electronic devices.”
  • “Research Challenges for CMOS Scaling: Industry Directions,” T.C. Chen, IBM, 2009 FCMN
SNAPSHOT FROM THE CONFERENCE SERIES

• “Novel materials in complex 3D structures are here now and will be increasingly prevalent going into the future.”
• “Metrology and characterization are vital to develop, improve, and control advanced manufacturing processes.”
  • “Pushing Beyond the Frontiers of Technology,” Mike Mayberry, VP and Director of Component Research, Intel, 2013 FCMN

• “Emerging memory technologies present significant challenges in the area of materials and structural characterization.”
• “The very act of measuring many of the emerging memory materials can change them.”
  • “Characterization and Metrology Challenges for Emerging Memory Technology Landscape,” Naga Chandrasekaran (VP of Process R&D, Micron) and Shifeng Lu (Micron), 2013 FCMN
Our World is Filling with Devices – and their Big Data

<table>
<thead>
<tr>
<th>Item</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rice grains grown each year</td>
<td>1,000,000,000,000,000,000 (1 quadrillion)</td>
</tr>
<tr>
<td>Ants crawling the earth</td>
<td>100,000,000,000,000,000,000 (100 quadrillion)</td>
</tr>
<tr>
<td>Devices produced each year</td>
<td>10,000,000,000,000,000,000,000 (10 quintillion)</td>
</tr>
</tbody>
</table>

From: Eric-Mark Huitema, IBM, ISS
Europe, Feb. 24, 2014

More than 1 billion devices for every one of us
SO WHAT IS THE CHALLENGE?
SCIENCE AND ENGINEERING AT THE ATOMIC AND MOLECULAR LEVEL

• **Nanoscale Science and Technology Involves the Atomic and Molecular Level**
  • fundamental understanding of phenomena and materials at the nanoscale
  • creation and use of structures, devices, and systems that have novel properties and functions because of their small size
  • control of matter and processes at the atomic and molecular level
  • Integration of nanoscale materials and structures into larger materials components, systems, and architectures
  • 3D becomes critical
Metrology is Enabling

- **Metrology:**
  - Empowers engineers with the information needed to make transistors smaller
  - while systematically eliminating
    - The causes of yield losses
    - Performance sapping variability at the transistor level
- **At the semiconductor and electronics levels**
  - Metrology creates demand using Moore’s Law to lower the cost of chips and computers
  - The macroeconomic result is greater productivity, lower inflation, and job creation
The Value of Metrology is delivered in many forms

- Return on Investment
- Increased Revenues
- Faster Time to Money
- Greater Profits
- Loss Prevention
- Business Continuity
  – Brand value
For finFETs and stacked die to become mainstream, advances are needed in metrology.

So what’s the big problem? Metrology, the science of measuring and characterizing tiny structures and materials, is becoming more complex and expensive at each node.

And specifically for 3D NAND and finFETs, there are a multitude of gaps in metrology. Today’s metrology tools are capable of measuring structures in two dimensions, and in three dimensions to a limited degree, but that’s not nearly enough for the wave of new chip architectures and materials in the market.

“At some point of time, especially at the 5nm node or less, you are going to want to know where every atom is in 3D,” said John Allgair, director of product development at Nanometrics. “You will want to know what type of atom exists and what are its electrical properties.”
FRONTIERS OF NANOMETROLOGY

• Studying features and phenomena at the nanoscale requires instruments capable of resolutions at the nano-, subnano-, and even pico-levels.

• Developing new experimental and analytical tools with a broader range of capabilities at the nanoscale (e.g., chemical analysis, surface and sub-surface defects, sub-surface properties, charge transport, spectroscopy), but these tools must also work in situ, real-time, non-intrusively or destructively, and under the variable conditions seen in processing (e.g., temperature, pressure, electrical and magnetic fields).

• Developing new methods of calibration and standardization and in concert, affordable calibration standards, to ensure the accurate interpretation of results.

• Working at nanometer accuracy and precision.
KEYNOTE SESSION

Session Chair: David Seiler, NIST

• 9:00
  Characterization Challenges In The 28 nm Technology Node
  Hubert Lakner, Executive Director, Fraunhofer Institute for Photonic Microsystems

• 9:45
  Techno-Economics Pressure In Semiconductor Value Chain May Impact Consumers And Global Economy – What Is Our Solution?
  Suresh Venkatesan, Senior Vice President, Technology Development, Global Foundries

• 10:30
  Coffee Break and Poster Viewing

• 11:00
  Nanoelectronics for Metrology
  Klaus von Klitzing, Max-Planck-Institut FKF