2009 International Conference

Frontiers of Characterization and Metrology for Nanoelectronics

Final Program and Abstracts

May 11-14, 2009

Albany, New York

College of Nanoscale Science and Engineering

University at Albany

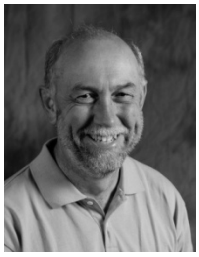
www.eeel.nist.gov/812/conference/

2009 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

D. Seiler

A. Diebold

R. McDonald



M. Garner

D. Herr

R. Khosla

2009 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

Welcome to the 2009 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics! Our goal is to bring together scientists and engineers interested in all aspects of the characterization technology needed for nanoelectronic materials and device research, development, and manufacturing. All approaches are covered in this conference: chemical, physical, electrical, optical, in-situ, and real-time control and monitoring. The conference summarizes major issues and provides critical reviews of important semiconductor techniques needed as the semiconductor industry moves to silicon nanoelectronics and beyond. It is hoped that the invited talks, contributed poster papers, and informal discussions will be a stimulus to provide practical perspectives, breakthrough ideas for research and development, and a chance to explore collaborations and interactions.

We are pleased to have T.C. Chen, IBM; Hans Stork, Applied Materials; Gisele Roesems-Kerremans, European Commission; and Koji Kuroda, Dai Nippon Printing, as keynote speakers. Alain Kaloyeros, College of Nanoscale Science and Engineering, Univ. at Albany, will be the keynote speaker at our banquet on Tuesday evening.

Thirty other invited talks will offer overviews in the sessions that follow. Poster papers will supplement these overviews with the latest metrology-based research results. These poster papers represent significant contributions to the latest developments in characterization and metrology technology, especially at the nanoscale.

The 2009 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics is the seventh in a series that began in 1995. It emphasizes the frontiers and innovation in characterization and metrology of nanoelectronics. The proceedings for all six previous conferences were published as hardcover volumes by the American Institute of Physics, New York. The most recent proceedings, Frontiers of Characterization and Metrology for Nanoelectronics: 2007, was published in September 2007.

With best wishes from the Committee Co-Chairs,

David Seiler, NIST; Alain Diebold, CNSE, SUNY Albany; Robert McDonald, Technology Associates; Mike Garner, Intel; Dan Herr, SRC; and Rajinder Khosla, NSF

Sponsors

- National Institute of Standards and Technology
- College of Nanoscale Science & Engineering, University at Albany
- Semiconductor Equipment and Materials International
- Semiconductor Research Corporation
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- American Physical Society
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Exhibitor

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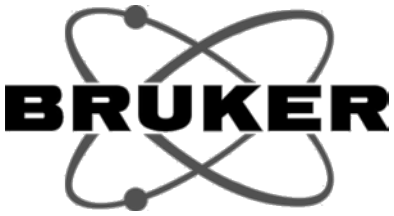

- Omicron NanoTechnology USA

Purpose and Goals

We bring together scientists and engineers interested in all aspects of the characterization technology needed for nanoelectronic materials and device research, development, and manufacturing. All approaches are welcome: chemical, physical, electrical, optical, in-situ, and real-time control and monitoring. The conference summarizes major issues and provides critical reviews of important semiconductor techniques needed as the semiconductor industry moves to silicon nanoelectronics and beyond.

Contributed Poster Papers

One of the major emphases of this conference is on the contributed poster papers. The poster papers selected by the committee represent significant contributions to frontier, state-of-the-art materials and device characterization and metrology

Authors must be present at the conference for their papers to be accepted for publication in the conference proceedings. Specifically, authors are responsible for setting up their displays, being present for posters sessions, and removing their displays at the end of the day.

Proceedings

After being formally reviewed, accepted manuscripts will be published in a hardback book by the American Institute of Physics. If your manuscript has not already been submitted, it must be submitted in the prescribed camera-ready format by e-mail (erik.secula@nist.gov) by May 21, 2009, in order to be included in the proceedings. The book and CD-ROM are expected to be available in the fall of 2009.

Banquet

The Conference Banquet will be held on campus at the College of Nanoscale Science and Engineering (CNSE) on Tuesday, May 12th. The banquet attendees will be addressed by Alain Kaloyeros, Senior VP and CEO, CNSE, Univ. at Albany, who will give a talk entitled "The "Business" of Nanotechnology. Translating Innovation into Real Technological Breakthroughs."

Poster Sessions

Poster sessions with complimentary wine and beer are scheduled for the end of Tuesday, Wednesday, and Thursday at the CNSE. Thursday's session will also include cheese and heavy hors d'oeuvres.

Best Paper Awards

The Best Paper Awards will be presented at the evening barbecue on Wednesday. The papers were judged by committee members and other technically qualified persons based on the following criteria:

- new, innovative ideas and breakthroughs in metrology presented (40%)
- strong potential impact of the research presented (40%)
- ideas written in a clear and organized manner with good writing style and grammar (20%)

The first place ($2500) and second place ($750) awards will be given to the lead contacts for the papers chosen. The winning authors need to be present at the conference in order to claim the awards.

Barbecue

An evening barbecue is planned at the CNSE on Wednesday, May 13th.

Program at a Glance

	MORNING	AM SESSION	PM SESSION	EVENING
Monday, May 11			Check-in at hotel **1:00 pm – 5:00 pm** Short Course at CNSE	**6:30 pm** Reception with registration at the Hilton Garden Inn
Tuesday, May 12	**7:30 am** Registration/ Attendee Check-in	**8:45 am** Conference Opening **9:00 am** Session 1: Keynote Talks	**1:50 pm** Session 2: Technology Overview for Nanoelectronics and Metrology **3:50 pm** Session 3: Electrical Measurements at Nano Dimensions **4:50 pm** Poster Session	**6:00 pm** Banquet at CNSE
Wednesday, May 13	**7:30 am** Registration/ Attendee Check-in	**8:00 am** Session 4: Metrology for CMOS Extension **10:30 am** Session 5: Metrology for Beyond CMOS and Extreme CMOS Devices	**1:50 pm** Session 6: Interconnects **3:50 pm** Session 7: Characterization Methods **5:20 pm** Poster Session	**6:30 pm** Barbecue at CNSE
Thursday, May 14	**7:30 am** Registration/ Attendee Check-in	**8:00 am** Session 8: Microscopy for Nanoelectronics	**12:50 pm** Session 9: Theory, Modeling, and Simulation **2:20 pm** Session 10: Metrology for Patterning **3:50 pm** Poster Session (with wine and cheese)	

Conference Program

Monday, May 11

1:00 PM

Sort Course at CNSE

High Resolution X-ray Scattering Methods for Nanostructure Characterization and Metrology
Instructor: Richard Matyi, Univ. at Albany

6:30 PM

Reception with registration at the Hilton Garden Inn

Tuesday, May 12

7:30 AM

Registration/Attendee Check-in, Coffee

Conference Opening

8:45 AM

Conference Opening
David Seiler, NIST, Conference Chair

Session 1: Keynote Talks

Session Chair: Robert Doering, Texas Instruments

9:00 AM

Research Challenges for CMOS Scaling: Industry Directions
T.C. Chen, IBM

9:45 AM

Topic TBD
Hans Stork, AMAT

10:30 AM

Coffee Break and Poster Viewing

11:00 AM

Nanoelectronics Landscape in Europe: New Opportunities for Research and Innovation

Gisele Roesems-Kerremans, European Commission, Information Society and Media / Nanoelectronics

11:45 AM

Globalized Innovation in Electronics - The 4th Factor of Production: Innovation

Dan Hutcheson, VLSI Research, Inc.

12:30 PM

Lunch and Poster Viewing

Session 2: Technology Overview for Nanoelectronics and Metrology

Session Chair: C.Y. Sung, IBM T.J. Watson Research Center

1:50 PM

Overview of the Nanoelectronics Research Initiative: An Industry-Government-University Innovation Partnership

Jeffrey Welser, Director, SRC Nanoelectronics Research Initiative

2:20 PM

Metrology for Emerging Materials, Devices, and Structures

Alain Diebold, College of Nanoscale Science and Engineering, SUNY Albany

2:50 PM

Characterization of Integrated Nano Materials

Amal Chabli, CEA-DRT-LETI

3:20 PM

Coffee Break and Poster Viewing

Session 3: Electrical Measurements at Nano Dimensions

Session Chair: Lori Nye, Brewer Science

3:50 PM

Boron Nanowires for Flexible Electronics and Field Emission
H.J. Gao, Chinese Academy of Sciences

4:20 PM

Nanoscale Measurement Methods for Novel Material Characterization
Alex Liddle, NIST

4:50 PM – 5:50 PM

Poster Session

6:00 PM

Banquet

The "Business" of Nanotechnology. Translating Innovation into Real Technological Breakthroughs
Alain Kaloyeros, Senior VP and CEO, College of Nanoscale Science and Engineering, Univ. at Albany

Tuesday Poster Paper Session

TU-001

Wave Front Sensor for Highly Accurate Characterization of Flatness on Wafer Surfaces
A. Nutsch,[1] I. Lazareva,[1] L. Pfitzner,[1] T. Grandin,[2] and S. Bucourt[2]
[1]Fraunhofer IISB, Erlangen, Germany
[2]Imagine Optic, Orsay, France

TU-002

VOC & Metallic Contaminant Control For SOI Process Monitoring
R. Brun,[1] C. Moulin,[1] C. Girard,[1] B. Usry,[2] and R. Newcomb[2]
[1]Soitec, Crolles, Cedex France
[2]Qcept Technologies, Atlanta, GA, USA

TU-003

Nanoscale Characterization of Ultra-Thin Dielectrics Using Scanning Capacitance Microscopy
O. Ligor, A. Descamps, D. Albertini, L. Militaru, N. Baboux, and B. Gautier
Lyon Institute of Nanotechnology (INL), Villeurbanne, France

TU-004

Reference-Free Characterisation of Semiconductor Surface Contamination and Nanolayers by X-Ray Spectrometry

B. Beckhoff, R. Fliegauf, P. Hönicke, M. Kolbe, M. Müller, B. Pollakowski, F. Reinhardt, J. Weser, and G. Ulm

Physikalisch-Technische Bundesanstalt, Berlin, Germany

TU-005

Polarized Optical Scattering Measurements of Metallic Nanoparticles on a Thin Film Silicon Wafer

C.-Y. Liu, T.-A. Liu, and W.-E. Fu

Center for Measurement Standards, Industrial Technology Research Institute, Hsinchu, Taiwan

TU-006

Fundamental SIMS Metrology Development and Considerations for Molecular Depth Profiling of Photoresist Materials on Silicon

C. Szakal,[1] S. Hues,[2] J. Bennett,[3] and G. Gillen[1]

[1]National Institute of Standards and Technology, Gaithersburg, MD, USA

[2]Micron Technology, Inc., Biose, ID, USA

[3]SVTC Technologies, Austin, TX, USA

TU-007

Withdrawn

TU-008

Built-In Self Test Capability for MEMS Microhotplate Temperature Sensors

M. Y. Afridi, C. B. Montgomery, E. Copper-Balis, S. Semancik, K. G. Kreider, and J. Geist

Semiconductor Electronics Division and Process, Measurements Divisions, National Institute of Standards and Technology, Gaithersburg MD, USA

TU-009

Enhanced Spatial Resolution Scanning Kelvin Force Microscopy Using Conductive Carbon Nanotube Tips

J. J. Kopanski,[1] P. McClure,[2] and Vladimir Mancerski[2]

[1]Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD, USA

[2]Xidex Corporation, Austin, TX, USA

TU-010

Application of Micro-thermal Analysis for Metal, Oxide, and Non-oxide Thin Film Materials

N. Carlie, J. Massera, L. Petit, and K. Richardson

Clemson University School of Materials Science and Engineering / COMSET, Clemson University, Clemson, SC, USA

TU-011

Work Function Measurements in Kelvin Force Microscopy: Analytical Understandings of Experimental Parameters Effects

K. Kaja, N. Chevalier, D. Mariolle, G. Feuillet, F. Bertin, and A. Chabli

CEA, LETI, MINATEC, Grenoble, France

TU-012

Contact Resistance Measurements of Metal on HOPG and Graphene Stacks

A. Venugopal,[1] A. Pirkle,[2] R. M. Wallace,[2] L. Colombo,[3] and E. M. Vogel[1]

[1]Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX, USA

[2]Department of Materials Science and Engineering, University of Texas at Dallas, Richardson, TX, USA

[3]Texas Instruments Inc., Dallas, TX, USA

TU-013

Sub-Surface Nano-Metrology of Buried Patterns and Structures in EUVL and DUV Masks Using Ultrasound

G. Shekhawat,[1] A. Srivastava,[2] and V. Dravid[1,2]

[1]Institute for Nanotechnology, Northwestern University, Evanston, IL, USA

[2]Department of Material Science and Engineering, Northwestern University, Evanston, IL, USA

TU-014

Advanced Capacitance Metrology for Nanoelectronic Device Characterization

C. A. Richter,[1] J. J. Kopanski,[1] C. Jiang,[1] Y. Wang,[2] M. Y. Afridi,[1] X. Zhu,[3] D. E. Ioannou,[3] and Q. Li[3]

[1]Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD, USA

[2]Quantum Electrical Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD, USA

[3]Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA, USA

TU-015

The Effect of Surface Conditioning on Silicon Wafer Resistivity Monitoring

E. Tsidilkovski and A. Bertuch

Semilab USA, Burlington, MA, USA

TU-016

Variable Temperature Measurements in Cryogenic Probe Stations

J. Lindemuth

Lake Shore Cryotronics, Westerville, OH, USA

TU-017

Inline 90nm Technology Gate Oxide Nitrogen Monitoring with Non Contact Electrical Technique

N. Pic,[1] G. Polisski,[2] E. Paire,[1] V. Rizzo,[1] C. Grosjean,[1] B. Bortolotti,[1]and J. Damico[3]

[1]STMicroelectronics, Rousset Cedex, France

[2]Applied Materials GmbH, Feldkirchen, Germany

[3]Semiconductor Diagnostics Inc., Tampa, FL, USA

TU-018

Compact X-Ray Tool For Critical-Dimension Metrology

B. Yokhin,[1] A. Krokhmal,[1] A. Dikopoltsev,[1] D. Berman,[1] I. Mazor,[1] B.-H. Lee,[2] D.-C. Ihm,[2] and K. H. Kim[2]

[1]Jordan Valley Semiconductors Ltd., Migdal Haemek, Israel

[2]Samsung Electronics, Hwasung-City, Gyeonggi-Do, Korea

TU-019

Porous SiOCH Post Plasma Damage Characterization Using Ellipsometric Porosimetry

C. Licitra,[1] R. Bouyssou,[2] T. Chevolleau,[2] N. Rochat,[1] and F. Bertin[1]

[1]CEA, LETI, MINATEC, Grenoble, France

[2]LTM/CNRS (CEA, LETI, MINATEC), Grenoble, France

TU-020

EBSD Analysis of Narrow Damascene Copper Lines

R. H. Geiss,[1] D. T. Read,[1] G. B. Alers,[2] and R. L. Graham[2]

[1]Materials Reliability Division, National Institute of Standards and Technology, Boulder, CO, USA

[2]Physics Department, University of California at Santa Cruz, Santa Cruz, CA, USA

TU-021

Characterization of Electrodeposited Copper Films with Time-of-Flight SIMS

H. Demers,[1] E. Lifshin,[1] and A. C. West[2]

[1]College of Nanoscale Science and Engineering, University at Albany, Albany, NY, USA

[2]Department of Chemical Engineering, Columbia University, New York, NY, USA

TU-022

Analysis and Metrology with Back Scattered Helium

S. Sijbrandij, J. Notte, and C. Sanford

Carl Zeiss SMT, Peabody, MA, USA

TU-023

Scanning Acoustic Microscopy of 3D-Interconnect

L. Kong,[1] A. Rudack,[2] S. Arkalgud,[2] and A. C. Diebold[1]

[1]College of Nanoscale Science and Engineering, University at Albany, Albany, NY, USA

[2]International SEMATECH, Albany, NY, USA

TU-024

Withdrawn

TU-025

A Critical Comparison of X-Ray Scattering Methods for Porosity Metrology of Low-k Thin Films

C. M. Settens,[1] R. J. Matyi,[1] V. K. Kamineni,[1] A. C. Diebold,[1] G. A. Antonelli,[2] and A. Grill[3]

[1]College of Nanoscale Science and Engineering, SUNY – University at Albany, Albany, NY, USA

[2]Novellus Systems, Inc., Tualatin, OR, USA

[3]IBM T.J. Watson Research Center, Yorktown Heights, NY, USA

TU-026

Spectroscopic Ellipsometry of Porous Low-κ Dielectric Thin Films

V. Kamineni,[1] A. Grill,[2] A. Antonelli,[3] C. Settens,[1] R. Matyi,[1] and A. Diebold[1]

[1]College of Nanoscale Science and Engineering, University at Albany, Albany, NY, USA

[2]IBM T.J. Watson Research Center, Yorktown Heights, NY, USA

[3]Novellus, Tualatin, OR, USA

TU-027

Electron Transport Metrology: Ballistic Electron Emission Microscopy Studies of Hot Electron Scattering in Copper

J. J. Garramone,[1] J. R. Abel,[1] I. L. Sitnitsky,[1] L. Zhao,[2] I. Appelbaum,[2] and V. P. LaBella[1]

[1]College of Nanoscale Science and Engineering, University at Albany, SUNY, Albany, NY, USA

[2]Department of Electrical and Computer Engineering, University of Delaware, Neward, DE, USA

TU-028

Controlled Oxidation of Silicon Nanowires

S. Krylyuk, A. Davydov, I. Levin, A. Motayed, and M. D. Vaudin

Material Science and Engineering Laboratory, National Institute of Standards and Technology, Gaithersburg, MD, USA

TU-029

Gate Stack Interfaces in Post-Si Nanoelectronics

T. Feng, H. D. Lee, L. Goncharova, S. Rangan, E. Bersch, O. Celik, C.-L. Hsueh, A. Wan, L. Yu, L. Feldman, T. Gustafsson, R. Bartynski, and E. Garfunkel

Rutgers University, Piscataway, NJ, USA

TU-030

Surface, Sub-surface and Interface Characterization and Analysis of Semiconductor Nanofilms

R. G. Krishnan

*A*STAR Institute of Microelectronics, Agency for Science, Technology and Research, Science Park II, Singapore*

TU-031

Atomic Force Microscopy Measures Single Electron Charges on Quantum Dots in Ambient Conditions

R. Olac-vaw,[1] N. Guz,[2] M. Dokukin,2 V. Mitin,[1] and I. Sokolov[2]

[1]Dept. Of Electrical Engineering, University of Buffalo, The State University of New York, Buffalo, NY, USA

[2]Dept. Of Physics, Clarkson University, Potsdam, NY, USA

TU-032

Thermal Conductivity and Thermal Rectification in Graphene Nanoribbons: a Molecular Dynamics Study

J. Hu,[1] X. Ruan,[2] Z. Jiang,[3] and Y. P. Chen[4]

[1]School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN, USA

[2]School of Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN, USA

[3]School of Physics, Georgia Institute of Technology, Atlanta, GA, USA

[4]Department of Physics, School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN, USA

TU-033

Raman-Based Graphene Thickness and Defect Metrology

G. Rao, S. McTaggart, J. U. Lee, and R. E. Geer

College of Nanoscale Science and Engineering, University at Albany, SUNY, Albany, NY, USA

TU-034

New Methods for Nanoscale Characterization and Functionalization of Templated Ge(Si) Quantum Dot Arrays

J. Thorp,[1] J. F. Graham,[1] and R. Hull[2]

[1]University of Virginia, Dept. of Materials Sci. and Eng., Charlottesville, VA, USA

[2]Rensselaer Polytechnic Institute, Troy, NY, USA

Wednesday, May 13, 2009

Session 4: Metrology for CMOS Extension

Session Chair: Gert Leusink, Tokyo Electron USA

8:00 AM

Evolution of the Ultimate Nano-Transistor

Bruce Doris, IBM

8:30 AM

Nanoscale Strain Metrology of Microelectronic Devices by Dark-Field Electron Holography

Martin Hytch, CNRS, Université de Toulouse

9:00 AM

FINFET Doping: Fabrication and Metrology Challenges

Wilfried Vandervorst, IMEC

9:30 AM

A 3D Stacked Nanowire Technology: Applications in Advanced CMOS and Beyond

Thomas Ernst, CEA-LETI, MINATEC

10:00 AM

Coffee Break and Poster Viewing

Session 5: Metrology for Beyond CMOS and Extreme CMOS Devices

Session Chair: Bruce Doris, IBM

10:30 AM

Overview of Carbon-Based Nanoelectronics

Ji Ung Lee, CNSE

11:00 AM

Scanning Single Electron Transistor Microscopy on Graphene
Jens Martin, Weizman Institute, Israel

11:30 AM

Spin Torque Transfer Nonvolatile Devices for CMOS Integrated Circuits
Hideo Ohno, Tohoku University

12:00 PM

Lunch and Poster Viewing

1:20 PM

Scaling Effects on Ferro-Electrics: Application in Nanoelectronics and Characterization
Bertrand Vilquin and Brice Gautier, Nanotechnology Institute of Lyon, France

Session 6: Interconnects

Session Chair: Greg Hughes, University at Albany

1:50 PM

Overview of 3D Interconnect Requirements
Sitaram Arkalgud, SEMATECH

2:20 PM

Cross Sectional Characterization of Planar and Non-planar Nanostructures using X-ray Scattering
Wen-li Wu, NIST

2:50 PM

X-ray Microscopy for Interconnect Characterization
Wenbing Yun, Xradia Inc. Concord/CA

3:20 PM

Coffee Break and Poster Viewing

Session 7: Characterization Methods

Session Chair: Eric Garfunkel, Rutgers Univ.

3:50 PM

Facts and Artifacts in Atom Probe Tomography
Francois Vurpillot, Univ. Rouen

4:20 PM

Synchrotron-Based Nanocharacterization
Pierre Bleuet, ESRF

4:50 PM

Application of TOF-SIMS and LEIS for the Characterization of Ultra-Thin Films
Thomas Grehl, ION-TOF GmbH

5:20 PM – 6:20 PM

Poster Session

6:30 PM

Barbecue

Wednesday Poster Paper Session

WE-001

Three-Dimensional Compositional & Structrual Characterization of Semiconducting Materials with Sub-NM Resolution
A. Shariq,[1] K. Wedderhoff,[1] and S. Teichert[2]
[1]Fraunhofer Center for Nanoelectronic Technologies, Koenigsbruecker Strasse, Dresden, Germany
[2]Qimonda Dresden GmBH & Co. OGH, Koenigsbruecker Strasse, Dresden, Germany

WE-002

Effect of Substrate Engineering of AlN/Si(111) Substrates on Overgrown GaN Films
M. Tungare, N. Tripathi, V. Jindal, G. Rao, R. Geer, and F. Shahedipour-Sandvik
College of Nanoscale Science and Engineering, University at Albany - State University of New York, Albany, NY, USA

WE-003

Characterization of Organic Contamination During Semiconductor Manufacturing Processing
A. Nutsch,[1] B. Beckhoff,[2] G. Bedana,[3] G. Borionetti,[3] D. Codegoni,[4] S. Grasso,[4] G. Guerinoni,[3] A. Leibold,[1] M. Muller,[2] M. Otto,[1] L. Pfitzner,[1] M.-L. Polignano,[4] D. De Simone,[4] and L. Frey[1]
[1]Fraunhofer IISB, Erlangen, Germany
[2]Physikalisch-Technische Bundesanstalt, Berlin, Germany

[3]*MEMC Electronic Materials SpA, Novara, Italy*
[4]*Numonyx, Milan, Italy*

WE-004

GIXRF in the Soft X-Ray Range Used for the Characterization of Ultra Shallow Junctions

B. Beckhoff,[1] P. Hoenicke,[1] D. Giubertoni,[2] G. Pepponi,[2] and M. Bersani[1]
[1]*Physikalisch-Technische Bundesanstalt, Berlin, Germany*
[2]*Fondazione Bruno Kessler, Povo, Trento, Italy*

WE-005

Ultra-Thin AlOx and LaOx Metrology – WD-XRF Techniques Development

C. C. Wang, A. Bello, M. Ye, R. Wang, D. Liu, Y. Cao, X. Tang, Y. Uritsky, and S. Gandikota
Defect and Thin Films Characterization Laboratory, Applied Materials, Inc., Santa Clara, CA, USA

WE-006

On the Use of Synchrotron Radiation for the Characterization of "TiN/HfO_2" Gate Stack

C. Gaumera,[1] E. Martinezb,[2] S. Lhostis,[1] F. Fillot,[2] P. Gergaud,[2] B. Detlefs,[3] J. Roy,[3] Y. Mi,[3] J. Zegenhagen,[3] and A. Chabli[2]
[1]*STMicroelectronics, Crolles, France*
[2]*CEA, LETI, MINATEC, Grenoble, France*
[3]*European Synchrotron Radiation Facitiliy, Grenoble, France*

WE-007

Designing an X-Ray Reflectometry Standard Reference Material: an Inverse Problem for an Inverse Problem

D. L. Gil and D. Windover
Ceramics Division, MSEL, National Institute of Standards and Technology, Gaithersburg, MD, USA

WE-008

Multi-Technique Characterization of Arsenic Ultra Shallow Junctions in Silicon Within the ANNA Consortium

D. Giubertoni,[1] G. Pepponi,[1] B. Beckhoff,[2] P. Hoenicke,[2] S. Gennaro,[1] F. Meirer,[3] D. Ingerle,[3] G. Steinhauser,[3] M. Fried,[4] P. Petrik,[4] A. Parisini,[5] M. A. Reading,[6] C. Streli,[3] J. A. van den Berg,[6] and M. Bersani[1]
[1]*Fondazione Bruno Kessler, Povo, Trento, Italy*
[2]*Physialisch-Technishe Bundesanstalt, Berlin, Germany*
[3]*Atominstitut der Oesterreixhischen Universiteaeten, Wien, Austria*
[4]*MFA-KFKI, Budapest, Hungary*
[5]*CNR-IMM, Bologna, Italy*
[6]*School of Computing, Science and Engineering and Institute of Materials Research – University of Salford, Salford, UK*

WE-009

NIST High Resolution X-Ray Diffraction Standard Reference Material: SRM 2000

D. Windover, D. L. Gil, A. Henins, and J. P. Cline
Ceramics Division, MSEL, National Institute of Standards and Technology, Gaithersburg, MD, USA

WE-010

Characterization of HfO_2, Hafnium Silicate and Nitrided Hafnium Silicate Films on SiO_2/Si

E. Bersch,[1] M. Di,[1] J. LaRose,[1] M. B. Huang,[1] S. Consiglio,[2] R. D. Clark,[2] G. J. Leusink,[2] and A. C. Diebold[1]

[1]College of Nanoscale Science and Engineering, University at Albany, Albany, NY, USA

[2]TEL Technology Center, Albany, NY, USA

WE-011

Non-Traditional Spectroscopy for Analysis of Semiconductor and Photovoltaic Thin Films Materials

F. Li and S. Anderson

Air Liquide Electronics - Balazs NanoAnalysi, Fremont, CA, USA

WE-012

An Investigation on Airborne Particular & Molecular Condensation Through Liquid Nitrogen Assisted Cooling

R. G. Krishnan[1] and G. Y. Raaj[2]

*[1]A*STAR Institute of Microelectronics, Agency for Science, Technology and Research, Science Park II, Singapore*

[2]Raffles Junior College, Singapore

WE-013

Detection of Metal Contamination on Silicon Wafer Backside and Edge by New TXRF Methods

H. Kohno,[1] M. Yamagami,[1] J. Formica,[2] and L. Shen[2]

[1]Thin-film Analysis Group, Rigaku Corporation, Takatsuki-shi, Osaka, Japan

[2]Semiconductor Fab Products, Rigaku Americas Corporation, The Woodlands, TX, USA

WE-014

In Situ Real Time Gas Phase Absorption Measurements During Atomic Layer Deposition

J. E. Maslar, W. A. Kimes, J. T. Hodges, B. Sperling, D. R. Burgess, and E. F. Moore

National Institute of Standards and Technology, Gaithersburg, MD 20899

WE-015

Vacuum-Ultraviolet Reflectometry of Ultra-Thin HfO_2 Films

J. Hurst[1] and V. Vartanian[2]

[1]Metrosol Inc., Austin, TX, USA

[2]ISMI, Albany, NY, USA

WE-016

Stress Measurement In Microstructures by Raman Microscopy

B. Uhlig,[1] J.-H. Zollondz,[2] M. Goldbach,[2] H. Bloeß,[2] and P. Kücher[3]

[1]Fraunhofer -Institut für Keramische Technologien und Systeme, Dresden, Germany

[2]Qimonda Dresden GmbH & Co. OHG, Dresden, Germany

[3]Center of Competence CoC Metrology/Analytic, Fraunhofer-Center Nanoelektronische Technologien CNT, Dresden, Germany

WE-017

Application of the SPV-Based Surface Lifetime Technique to In-Line Monitoring of Surface Cu Contamination

J. D'Amico,[1] A. Savtchouk,[1] M. Wilson,[1] C. H. Kim,[2] H. W. Yoo,[2] C. H. Lee,[2] T. K. Kim,[2] and S. H. Son[2]

[1]Semiconductor Diagnostics, Inc., Tampa, FL, USA

[2]Hynix Semiconductor, Inc., Kyoungki-do, Korea

WE-018

High-Resolution Rutherford Backscattering Analysis of Nanoscale Thin Films

J. LaRose and M. Huang

SUNY-Albany, Albany, NY, USA

WE-019

Ion Channeling Study of Activated Boron and Disordered Si Atoms in Silicon Ultra-Shallow Junctions

L. Vanamurthy,[1] M. Huang,[1] H. Bakrhu,[1]T. Furukawa,[2] N. Berliner,[2] J. Herman,[2] Z. Zhu,[2] P. Ronsheim,[2] B. Doris,[2] M. Li,[3] P. Banks,[3] and S. Felch[4]

[1]College of Nanoscale Science and engineering, University at Albany-SUNY, Albany NY, USA

[2]IBM Corporation, Albany, NY, USA

[3]AMAT, Albany, NY, USA

[4]Spantion Inc., Sunnyvale, CA, USA

WE-020

Evaluation of Experimental Techniques for In-line Ion Implantation Characterization

L. Vignoud,[1] F. Milesi,[1] E. Nolot,[1] A. Danel,[1] and S. Favier[2]

[1]CEA-LETI MINATEC, Grenoble Cedex 9, France

[2]ST Microelectronics, Crolles Cedex, France

WE-021

High Temperature X-Ray Diffraction for the Determination of Thin Film Phase Diagrams of High-k Dielectrics

L. Wilde,[1] S. Teichert,[2] P. Reinig,[2] S. Schmidt,[3] W. Weinreich,[1] and P. Kücher[1]

[1]Fraunhofer Center Nanoelectronic Technologies, Dresden, Germany

[2]Qimonda Dresden GmbH & Co. OHG, Dresden, Germany

[3]Westachsische Hochschule Zwickau, Zwickau, Germany

WE-022

Advanced Gate and Stack Dielectric Characterization with FastGate® Technology

R. J. Hillard,[1] L. Tan,[1] and K. G. Reid[2]

[1]Solid State Measurements, Inc. Pittsburgh, PA, USA

[2]Tokyo Electron America, Austin, TX, USA

WE-023

Nanocalorimetry of Thin Film Solidification and Nickel Silicide Formation

D. A. LaVan,[1] F. Yi,[1] R. K. Kummamuru,[1,2] L. De La Rama,[2] L. Hu,[2] M. D. Vaudin,[1] and L. H. Allen[2]

[1]Ceramics Division, Materials Science and Engineering Laboratory, National Institute of Standards and Technology, Gaithersburg, MD, USA

[2]Department of Materials Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL, USA

WE-024

Towards Routine Backside SIMS Sample Preparation for Efficient Support of Advanced IC Process Development

M. J. P. Hopstaken,[1] C. Cabral Jr.,[1] D. Pfeiffer,[1] C. Molella,[2] and P. Ronsheim[2]

[1]IBM T.J. Watson Research Center, Yorktown Heights, NY, USA

[2]IBM East Fishkill, Hopewell Junction, NY, USA

WE-025

X-Ray Photoelectron Spectromicroscopy of Doped Silicon Patterns

N. Barrett,[1] M. Lavayssière,[2] O. Renault,[2] L. F. Zagonel,[1] and A. Bailly[2]

[1]CEA DSM/IRAMIS/SPCSI, CEA Saclay, Gif sur Yvette, France

[2]CEA, LETI, MINATEC, Grenoble, France

WE-026

Spectroscopic Ellipsometry Characterization of High-k Films on SiO_2/Si

M. Di,[1] E. Bersch,[1] S. Consiglio,[2] R. Clark,[2] G. Leusink,[2] A. Srivatsa,[3] and A. C. Diebold[1]

[1]College of Nanoscale Science and Engineering, University at Albany, Albany, NY, USA

[2]TEL Technology Center America, Albany, NY

[3]KLA-Tencor Corp., Milpitas, CA, USA

WE-027

Withdrawn

WE-028

Quantitative Analysis of Stress Components in Si Device Structures Using UV Raman Spectroscopy

T. Tada, V. Poborchii, and T. Kanayama

MIRAI, Nanodevice Innovation Research Center (NIRC), National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Ibaraki, Japan

WE-029

Photoreflectance Spectroscopic Characterizations of Charge States in High-k Dielectric Layers

T. Zhang,[1] M. Di,[1] E. J. Bersch,[1] H. Chouaib,[2] A. Salnik,[2] L. Nicolaides,[2] S. Consiglio,[3] R. D. Clark,[3] and A. C. Diebold[1]

[1]College of Nanoscale Science and Engineering, State University of New York, Albany, NY, USA

[2]KLA-Tencor Corp., San Jose, CA, USA

[3]TEL Technology Center America, Albany, NY, USA

WE-030

Quantification of Hafnium in Hafnium Oxide Film for Reference Materials

T. Takatsuka,[1] I. Kojima,[1] Y. Kobayashi,[1] K. Hirata,[1] N. Nonose,[1] T.i Ohchi,[2] C. Ichihara,[3] H. Matsue,[4] M. Morita,[5] H. Takahara,[6] and T. Asano[7]

[1]National Metrology Institute of Japan, National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki, Japan

[2]NTT-AT-Nanofabrication Co.

[3]Kobe Steel, Ltd.

[4]Quantum Beam Science Directorate, Japan Atomic Energy Agency

[5]Graduate School of Engineering, Osaka University

[6]Technos CO., Ltd.

[7]Ibaraki Prefectural Industrial Technology Center

WE-031

Process Tool Contamination - From Starting Material to On-Wafer

V. K. F. Chia

Balazs NanoAnalysis, Fremont, CA, USA

WE-032

Thickness Measurement of Thin Metal Films by Optical Metrology

V. Kamineni,[1] M. Raymond,[2] E. Bersch,[1] B. Doris,[3] and A. Diebold[1]

[1]College of Nanoscale Science and Engineering, University at Albany, Albany, NY, USA

[2]AMD, Albany, NY, USA

[3]IBM, Albany, NY, USA

WE-033

Post-Deposition Annealing Analysis for HfO_2 Thin Films Using GIXRR/GIXRD

W.-E. Fu, E. Chang, and Y.-C. Chen

Center for Measurement Standards, Industrial Technology Research Institute, Hsinchu, Taiwan

Thursday, May 14, 2009

Session 8: Microscopy for Nanoelectronics

Session Chair: Robert Hull, RPI

8:00 AM

Progress Towards Low Vacuum Critical Dimension Metrology

Brad Thiel, University at Albany - SUNY

8:30 AM

Nanotechnology: An Overview and Impact on Metrology

Meyya Meyyapan, Director, Center for Nanotechnology, NASA

9:00 AM

Aberration-corrected TEM for Nanoelectronics Applications
Christian Kisielowski, NCEM/LBNL

9:30 AM

Coffee Break and Poster Viewing

10:00 AM

Corrected Electron Optics - Improved Resolution and New Analysis Capabilities
Michael Steigerwald, Carl Zeiss Oberkochen, Germany

10:30 AM

Energy Filtered PhotoElectron Microscopy
Konrad Winkler, Omicron NanoTechnology GmbH

11:00 AM

Understanding the Imaging and Metrology Using the Helium Ion Microscopy
Michael Postek, NIST

11:30 AM

Lunch and Poster Viewing

Session 9: Theory, Modeling, and Simulation

Session Chair: David Kyser, AMAT

12:50 PM

Simulations of Scatterometry Down to 22 nm Structure Sizes and Beyond
Wolfgang Osten, ITO Stuttgart (Institute of Technical Optics)

1:20 PM

Challenges and Opportunities for Modeling and Simulation
Mark Lundstrom, Purdue

1:50 PM

Coffee Break and Poster Viewing

Session 10: Metrology for Patterning

Session Chair: Sitaram Arkalgud, SEMATECH

2:20 PM

Pushing Resists to Their Limits: Creating New Targets for Metrology
Chris Ober, Cornell

2:50 PM

Metrology for Advanced Patterning and Overlay
Bart Rijpers, ASML

3:20 PM

Mask Metrology – Current and Future Challenges
Greg Hughes, SEMATECH

3:50 PM – 4:50 PM

Poster Viewing (with cheese and heavy hors d'oeuvres)

Thursday Poster Paper Session

TH-001

Thermal Diffusivity and Boundary Resistance Analyses in Resistance Random Access Memory (ReRAM)
H. Akinaga and H. Shima
National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Ibaraki, Japan

TH-002

Lithography with Helium Ions
D. Winston,[1] B. M. Cord,[1] B. Ming,[2] D. C. Bell,[3] W. F. DiNatale,[4] L. A. Stern,[4] A. E. Vladar,[2] M. T. Postek,[2] M. K. Mondol,[1] and K. K. Berggren[1]
[1]Massachusetts Institute of Technology, Cambridge, MA, USA
[2]National Institute of Standards and Technology, Gaithersburg, MD, USA
[3]Harvard University, Cambridge, MA, USA
[4]Carl Zeiss SMT Inc., Peabody, MA, USA

TH-003

Withdrawn

TH-004

Predicting Overlay Distortions on a Litho-Scanner
K. T. Turner[1] and J. Sinha[2]
[1]Department of Mechanical Engineering, University of Wisconsin, Madison, WI, USA
[2]Wafer Inspection Group, KLA Tencor, Milpitas, CA, USA

TH-005

A Comparison of Linewidth Measurements on Sub-20 nm Graphene Nanostructures

J. J. Peterson,[1] M. A. Rodriguez,[2] V. Tileli,[2] M. Sprinkle,[3] C. Berger,[3] B. L. Thiel,[2] and W. A. de Heer[3]

[1]Intel Corporation Assignee to INDEX, Albany, NY, USA

[2]University at Albany-SUNY, Albany, NY, USA

[3]School of Physics, Georgia Institute of Technology, Atlanta, GA, USA

TH-006

Integrated ODP Metrology Matching to Reference Metrology for Lithography Process Control

P. Kearney,[1] J. Uchida,[1] S. Egret,[1] H. Weichert,[1] D. Likhavchev,[2] and G. Fleischer[3]

[1]Tokyo Electron Europ Limited, German Branch, Dresden, Germany

[2]Timbre Technologies, Inc., Santa Clara, CA, USA

[3]Qimonda Dresden GmbH & Co. OHG, Dresden, Germany

TH-007

A High Resolution X-Ray Reflectometry Study of Extreme Ultraviolet Photoresists

R. J. Matyi and R. L. Brainard

College of Nanoscale Science and Engineering, University at Albany, Albany, NY, USA

TH-008

Re-Calibration of the SRM $20^{5}9$ Master Standard Using Traceable Atomic Force Microscope Dimensional Metrology

R. Dixson, J. Potzick, and N. Orji

Precision Engineering Division, National Institute of Standards and Technology, Gaithersburg, MD, USA

TH-009

Measurements of Sub-30 nm Structures Over Large Areas Using Grazing Incidence Small Angle X-Ray Scattering

R. L. Jones,[1] K. Yager,[1] C. Wang,[1] K.-W. Choi,[2] E. K. Lin,[1] and W.-l. Wu[1]

[1]Polymers Division, National Institute of Standards and Technology, Gaithersburg, MD, USA

[2]Intel Corporation, Santa Clara, CA, USA

TH-010

A Novel Wafer-Plane Dosimeter for EUV Lithography

S. Grantham and C. Tarrio

National Institute of Standards and Technology, Gaithersburg, MD, USA

TH-011

Cross Sectional Characterization of Sub-50 nm Structures Using CD-SAXS

C. Wang,[1] R. L. Jones,[1] K.-W. Choi,[2] D. Ho,[1] E. K. Lin,[1] W.-l. Wu,[1] J. S. Clarke,[3] J. S. Villarrubia,[4] and B. Bunday[5]

[1]Polymers Division, National Institute of Standards and Technology, Gaithersburg, MD, USA

[2]Intel Corporation, Santa Clara, CA, USA

[3]Intel Corporation, Hillsboro, OR, USA

[4]Precision Engineering Division, National Institute of Standards and Technology, Gaithersburg, MD, USA

[5]International SEMATECH Manufacturing Initiative (ISMI), Austin, TX, USA

TH-012

Interference Microscopy for Semiconductor Backend Patterning Metrology

X. Colonna de Lega,[1] P. de Groot,[1] M. Fay,[1] R. Kruse,[1] D. Grigg,[1] and J. Barnak[2]

[1]Zygo Corporation, Middlefield, CT, USA

[2]Zygo Corporation, Hillsboro, OR, USA

TH-013

Spectroscopic Scatterfield Microscopy

B. M. Barnes,[1] H. Zhou,[1] N. A. Heckert,[2] and R. M. Silver[2]

[1]KT Consulting, Inc., Antioch, CA, USA

[2]National Institute of Standards and Technology, Gaithersburg, MD, USA

TH-014

Understanding the Phase Images from FIB Prepared Semiconductor Devices

D. Cooper, J.-M. Hartmann, P. Rivallin, and A. Chabli

CEA, Leti, Minatec, Grenoble, France

TH-015

Simulation Study of Transmission Electron Microscopy Imaging of Graphene Stacking

F. Nelson,[1] R. Hull,[2] and A. C. Diebold[1]

[1]College of Nanoscale Science and Engineering, University at Albany, Albany, NY, USA

[2]Rensselaer Polytechnic Institute (RPI), Troy, NY, USA

TH-016

Scanning Tunneling Spectroscopies of Graphene

G. M. Rutter,[1] D. L. Miller,[2] K. D. Kubista,[2] M. Ruan,[2] W. A. de Heer,[2] P. N. First,[2] and J. A. Stroscio[1]

[1]Center for Nanoscale Science and Technology, National Institute of Standards and Technology, Gaithersburg, MD, USA

[2]School of Physics, Georgia Institute of Technology, Atlanta, GA, USA

TH-017

Enhanced TEM Sample Preparation Using In-situ Low Energy Argon Ion Milling

H. Stegmann,[1] Y. Ritz,[2] D. Utess,[2] and E. Zschech[2]

[1]Carl Zeiss NTS GmbH, Oberkochen, Germany

[2]AMD Fab 36 LLC & Co. KG, Dresden, Germany

TH-018

TEM Spectral Imaging and Tomography for Chemical Imaging of Three-Dimensional Nanoelectronic Devices

I. M. Anderson and A. A. Herzing

Surface and Microanalysis Science Division, National Institute of Standards and Technology, Gaithersburg, MD, USA

TH-019

Hysteresis Correction of SPM Image by Moving Window Correlation Method

J. Fu, W. Chu, R. Dixson, G. Orji, and T. Vorburger

National Institute of Standards and Technology, Gaithersburg, MD, USA

TH-020

Electrical Measurements by Scanning Spreading Resistance Microscopy: Application to Carbon Nanofibers and Si Nanowires

N. Chevalier,[1] D. Mariolle,[1] L. Fourdrinier,[2] C. Celle,[2] C. Mouchet,[2] S. Poncet,[2] J. P. Simonato,[2] H. Le Poche,[2] E. Rouviere,[2] F. Bertin,[1] and A. Chabli[1]

[1]CEA, LETI, MINATEC, Grenoble, France

[2]CEA-LITEN/Hybrid Components Laboratory, Grenoble, France

TH-021

A Study of Gate-All-Around Transistors by Electron Tomography

P. D. Cherns,[1] F. Lorut,[2] C. Dupré,[1] K.Tachi,[1] D.Cooper,[1] A.Chabli,[1] and T. Ernst[1]

[1]CEA, LETI, MINATEC, Grenoble, France

[2]ST Microelectronics, Crolles, France

TH-022

Quantifying and Enforcing the Two-Dimensional Symmetry of Scanning Probe Microscopy Images of Periodic Objects

P. Moeck,[1] B. Moon Jr.,[1] E. Sánches,[1] M. Abdel-Hafiez,[2] and M. Hietschold[2]

[1]Department of Physics, Nano-Crystallography Group, Portland State University, Portland, OR, USA

[2]Institute of Physics, Solid Surfaces Analysis Group & Electron Microscopy Laboratory, Chemnitz University of Technology, Germany

TH-023

Structural Fingerprinting of Nanocrystals in the Transmission Electron Microscope

P. Moeck,[1] S. Rouvimov,[1] and S. Nicolopoulos[2]

[1]Nano-Crystallography Group, Department of Physics, Portland State University, Portland, OR, USA

[2]NanoMEGAS SPRL, Brussels, Belgium

TH-024

Automated Crystal Orientation and Phase Mapping of Iron Oxide Nano-Crystals in a Transmission Electron Microscope

S. Rouvimov,[1] E. F. Rauch,[2] P. Moeck,[1] and S. Nicolopoulos[3]

[1]Nano-Crystallography Group, Department of Physics, Portland State University, Portland, OR, USA

[2]SIMAP/GPM2 Laboratory, CNRS-Grenoble, France

[3]NanoMEGAS SPRL, Brussels, Belgium

TH-025

Helium Ion Beam Microscopy for Copper Grain Identification in BEOL Structures

R. J. J. van den Boom,[1] H. Parvaneh,[1] D. Voci,[2] D. Ferranti,[2] C. Huynh,[2] K. A. Dunn,[1] and E. Lifshin[1]

[1]State University of New York, University at Albany, Albany NY, USA

[2]Carl Zeiss SMT Inc., Peabody, MA, USA

TH-026

Edge Structure of Suspended Graphene Confirmed by HRTEM

S. Y. Park, Y. J. Suh, and M. J. Kim

Department of Material Science and Engineering, The University of Texas at Dallas, Richardson, TX, USA

TH-027

Withdrawn

TH-028

Spectroscopic Polarimetry of Light Scattered by Surface Roughness and Textured Films in Nanotechnologies

F. Ferrieu

STMicroelectronics, Crolles Cedex, France

TH-029

Density Functional Theory Studies of Defects in Graphene

E. Cockayne

Ceramics Division, Materials Science and Engineering Laboratory, National Institute of Standards and Technology, Gaithersburg, MD, USA

TH-030

Application of Statistical Dynamical X-Ray Diffraction Theory to Defective Semiconductor Heterostructures

P. K. Shreeman and R. J. Matyi

College of Nanoscale Science and Engineering, SUNY – University at Albany, Albany, NY, USA

TH-031

Withdrawn

TH-032

A Lumped Element Model for Near-Field Microwave Microscopy of Bulk and Thin Film Semiconductors

V. V. Talanov

Solid State Measurements, Inc., Pittsburgh, PA, USA

Abstracts

1-1

Research Challenges for CMOS Scaling: Industry Directions

Tze-chiang (T.C.) Chen

IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, USA

ABSTRACT

In last 40 years, the silicon microelectronics industry has seen an unprecedented record of continuous and systematic increase in transistor density and performance, guided by CMOS scaling theory and described in “Moore’s Law”. As the silicon industry moves into the nanometer dimension, significant technology challenges are being imposed by the approach toward atomistic and quantum-mechanical physics boundaries. These issues are frequently cited as the reasons Moore’s Law is “broken”, or why CMOS scaling is coming to an end.

This presentation will describe industry directions for addressing the challenges facing the coming nanometer era, by introducing new materials and device structures. These innovations include device performance enhancement through further use of stress films to increase the channel mobility, the introduction of high-k gate dielectrics and metal gates to mitigate gate leakage and permit renewed gate length scaling, the adoption of alternative device structures such as Fin-FET, UTSOI, or silicon nanowires to mitigate variability and power dissipation, and the exploitation of 3D-silicon technology for system improvement. The infusion of innovations in new materials and device structures, coupled with innovations in circuit design and system architecture, will ensure up to another ten years of continued CMOS development.

Keywords: CMOS scaling, Moore’s Law, nanotechnology

1-2

Abstract Not Received At Time of Press

1-3

Nanoelectronics Landscape In Europe: New Opportunities for Research and Innovation

Gisele Roesems Kerremans and Dirk Beernaert

European Commission DG INFSO, G1 Nanoelectronics, Avenue de Beaulieu 31, B – 1049 Brussels

ABSTRACT

The European Semiconductor Landscape is concentrated in a few regions of excellence. These are:

The Dresden (D) area (Infineon, AMD, Qimonda, FhG CNT, AMTC, NaMLab, RDC etc.) offering access to the most advanced manufacturing (including memory and processors, but now also targeting foundry) and offering specific world class competence in power electronics and smart power technology essential for energy efficient application and automotive and e.g. future electric car.

The Grenoble (F) area (STM, SOITEC, LETI, MEMSCAP,…) offering access to the most advanced technologies targeting derivative or add-on technologies building upon the most advanced basic CMOS processes and offering specific world class competence in many application specific fields including wireless communication, systems on chip, low power technology. SOITEC is a world leader in SOI technology essential for many future low energy consuming applications. Integration technology is a major competence.

The Leuven/Eindhoven area (B, NL) (NXP, ASML, Philips, IMEC) offering access to the most advanced process knowledge world-wide; in particular ASML is dominating the market for advanced photolithography equipment. IMEC in Leuven, B, is considered to be a leading semiconductor R&D centre for developing new IC technologies next to Sematech, US, Selete, J, Albany CSR, US. It is involving all top 10 semiconductor companies, including the top five memory companies in their cooperation. The cluster offers specific world class competence in application specific ICs targeting communication, medical and integration technologies including organic.

The Dublin area (IRL) (Intel, Irish universities) includes one of the most advanced and largest manufacturing sites world-wide producing the most advanced Intel processors in the most advanced Intel technology. World class manufacturing competence is supported by a network of Irish universities and support organizations. Moreover Intel Ireland is connecting further with many other institutes and organizations Europe wide.

The area of Catania (I) (Numonix, ST, Catania university) is offering access to more advanced technology in particular for embedded memories, for advanced add on technologies to CMOS and for integration technologies. These activities are also lined up with the activities in Grenoble.

There are still approximately 250+ operational manufacturing and R&D lines on European territory, most of them dedicated to added value products and using specific technologies.

Europe is strongly positioned to maintain its excellent track record in semiconductor innovation. Europe can draw on a long established network of excellent university laboratories and research centres and an efficient culture of co-operation between universities, research institutes, and industry. In addition to the Commission's Framework Programmes and the nanoelectronics clusters under the Eureka programme (MEDEA/CATRENE), the recently launched ENIAC Joint Undertaking is offering further opportunities. ENIAC is a unique Europe wide public-private partnership that combines funding from industry, the European Commission, and the Member and Associated States over a 10 year period to ensure Europe’s knowledge leadership in this area

Post Nano Metrology for Harmonizing Science with Human

Koji Kuroda

Expert Adviser Senior Researcher (Analytical Technology)
Research & Development Center Dai Nippon Printing Co., Ltd.
1-1-1, Ichigaya-Kagacho, Shinjukku-ku, Toky162-8001, Japan
e-mail: koji-Kuroda@mail.dnp.co.jp

ABSTRACT

Even in nano science the accumulation of tacit knowing through is most important for our innovative thinking. We cannot see nano structure without analytical devices but we can grasp nano-level response through integration of our sense of hearing, smelling, touching, seeing and more.

Nano metrology or characterization should be changed to post nano metrology in order to communicate materials voice with human sense more directly, from static to dynamic, from structure drawing to behavior imaging, from amplitude to phase sensitive or " What was happened? " to "What is happening?" for " Make it happen! ". By knowing real time material response, especially dynamic correlation between nano & macro response in processing, we will be able to estimate and manage the following phenomena at each stage, finally controlling the total process.

We should grasp the communication path and timing with dynamic feature of materials as well as with human, not only through knowledge but also their response feelings.

Target of Analysis			Energy Response		FUNCTION
Bulk Analysis ⇒		Nano Area ⇒ (surface/bulk/interface)		Processing	
＊Amount ⇒		＊Position ⇒		＊Dynamics	
＊Composition ⇒		＊Steric Texture ⇒		＊Formation	
＊Binding ⇒		＊Alignment ⇒		＊Polarization	
Function of Analysis	＊Sensitivity & Dynamic Range ＊Uniformity (Space) & Stability (Time) ＊Atmosphere Control				CONTROL
Analysis ⇒	Fine & High Speed ＊Multi Probe & Multi Sensing Integration				
Detection ⇒	Large Area & Rare Defect ＊Phase Sensitive (Space & Time)				
Knowledge Integration ⇒	Energy Response & Time Resolved Analysis ＊Human Interface (Sensuous Harmonization)				

TABLE 1. Post Nano Metrology Comcept

We have started the mobile analytical laboratory carrying 120,000 frames/sec high-speed VTR for visualizing printing dot (10~200 μ m) behavior in real process that transfers from the plate to the paper faster than 1msec. The VTR picture is effective for both understanding between process experts and analytical researchers. From high-speed picture of ink wetting we have realized the molecular structure on the interface has its own rearrangement relaxation time that defines the next behavior of the droplet deformation.

In this talk high-speed YTR of new splash phenomena, polyimide molecular alignment in coating process, organic EL crystallization due to solvent and ink structure formation on the interface will be presented.
We should change thinking and analytical instrument from "static" to "dynamic" in order to hear materials voice.

Metrology harmonized with human should be the frontier eye and the leader for the 21st new science.

FIGURE 1. Water ink on Water Splash

FIGURE 2. Toluene on Toluene Splash

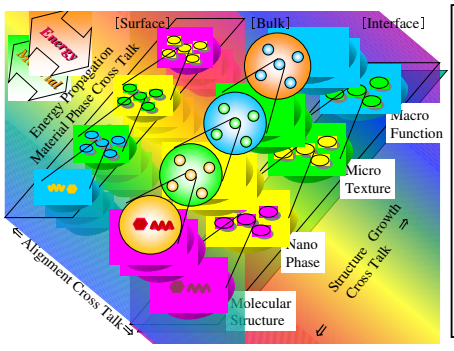

FIGURE 3. Nano Material Coating Process

Static	⇒	Dynamic
Low Speed	⇒	High Speed
Equilibrium	⇒	Relaxation Rate
Dilute	⇒	Conc
Uniform	⇒	Structural
Data	⇒	Visual Image
Material Flow	⇒	Energy Flow
Ideal	⇒	Actual
Laboratory Solution	⇒	By Site Solution

TABLE 2. 21st Science Innovation

2-1

Overview of the Nanoelectronics Research Initiative: An Industry-Government-University Innovation Partnership

Jeffrey Welser

Director, SRC Nanoelectronics Research Initiative
IBM Almaden Research Center, 650 Harry Road, San Jose, CA 95120
T: 408-927-1017 F: 408-927-3616 jeff.welser@src.org

ABSTRACT

For over 35 years, the ability to achieve increased performance per dollar in integrated circuits by scaling the dimensions of the field-effect transistor (FET) in Complementary Metal Oxide Semiconductor (CMOS) technology has been the driving engine behind the semiconductor industry. As the ultimate limits to the scaling of CMOS are getting closer, new approaches in emerging areas in electronics at the nanoscale need to be explored. The Nanoelectronics Research Initiative (NRI) was chartered by a consortium of Semiconductor Industry Association (SIA) member companies to develop and administer a university-based program to address this challenge.

NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe. The devices must show significant benefit over ultimate FETs in power, performance, density, and/or cost to enable the industry to extend the historical cost and performance trends for information technology.

NRI has partnered with both the federal and state governments to fund and manage research at multi-university, virtual centers with the goal of creating a *goal-oriented, basic-science* research program. This structure maintains a balance between sufficient autonomy for university researchers to explore radical new ideas and guidance of these ideas towards a practical device through strong interaction with industry assignees and liaison teams.

In 2007, NIST joined NRI as a full participant, not only expanding the work at the university centers, but also formalizing a strong connection to the cutting-edge metrology science research going on in the NIST labs. It is hoped that by working between the universities and the labs, we will accelerate the progress on finding a new logic device and on advancing the state of the art for metrology and characterization tools, both vital to future innovations in electronics. This talk will give a brief background on the NRI program and its motivation, and will focus on some of the projects and research areas being explored for new nanoelectronic device applications.

Western Institute of Nanoelectronics	Institute for Nanoelectronics Discovery & Exploration	SouthWest Academy for Nanoelectronics	Midwest Institute for Nanoelectronics Discovery
UCLA, UCSB, UC-Irvine, Berkeley, Stanford, U Denver, Iowa, Portland State	**SUNY-Albany**, GIT, RPI, Harvard, MIT, Purdue, Yale, Columbia, Caltech, NCSU, UVA	**UT-Austin**, UT-Dallas, TX A&M, Rice, ASU, Notre Dame, Maryland, NCSU, Illinois-UC	**Notre Dame**, Purdue, Illinois-UC, Penn State, Michigan, UT-Dallas
Theme 1: Spin devices Theme 2: Spin circuits Theme 3: Benchmarks & metrics Theme 4: Spin Metrology	Task I: Novel state-variable devices Task II: Fabrication & Self-assembly Task III: Modeling & Arch Task IV: Theory & Sim Task V: Roadmap Task VI: Metrology	Task 1: Logic devices with new state-variables Task 2: Materials & structs Task 3: Nanoscale thermal management Task 4: Interconnect & Arch Task 5: Nanoscale characterization	Theme 1: Graphene device: Thermal, Tunnel, and Spin Theme 2: Interband Tunnel Devices Theme 3: Non-equilibrium Systems Model / Meas. Theme 4: Nanoarchitecture

FIGURE 1. Current NRI-NIST research centers.

2-2

Metrology for Emerging Materials, Devices, and Structures

Alain C. Diebold
College of Nanoscale Science and Engineering
University at Albany
255 Fuller Road
Albany, NY 12203

ABSTRACT

Metrology continues to be challenged by the extension of CMOS and by the materials and devices under investigation for replacing CMOS, ie., "Beyond CMOS". The introduction of new materials, devices, and structures is driving measurement science and technology to become capable of characterizing new phenomena at near atomic dimensions. CMOS extension refers to the development of either planar and non-planar device structures based on transistors that use charge carriers. New materials such as high k, metal gates, and ultra-thin SOI are expected to evolve to meet the needs of 16 nm ½ pitch devices and below. Although high k and metal gate materials have been introduced to manufacturing, research and development of manufacturing capable measurements continues. Air gap and new low k materials will also evolve for on-chip interconnect needs. 3D interconnect is expected to continue to evolve to meet the needs of chip to chip interconnect. Metrology research and development is also addressing new challenges as the semiconductor industry focuses its efforts toward research into "Beyond CMOS". The International Technology Roadmap for Semiconductors continues to provide the most up to date information on both CMOS Extension and Beyond CMOS. Measurement research and development needs can be found in the Metrology, Emerging Research Materials, and Emerging Research Devices Roadmaps. The ITRS can be found at www.itrs.net

New phenomena abound at nanoscale dimensions. Quantum confinement impacts materials properties and measurement itself. Berry Phase corrections to carrier transport measurements are widely recognized. New materials such as graphene are difficult to find, manipulate, and measure. New switches are being designed based on carrier spin, excitons, and other properties. Microscopy of graphene serves to illustrate the numerous advances necessary for new device research. One key question is the number of graphene layers in a sample and the stacking of multilayer samples. Multiple characterization methods are necessary including transmission electron microscopy (TEM), Low Energy Electron Microscopy (LEEM), nano-Raman, and several scanned probe methods. Multislice simulations are a useful guide in determining TEM capability and imaging conditions. Initial simulation work points to the ability to distinguish stacking patterns. Recent work indicates that LEEM can determine the number of layers and the morphology of a graphene sample.[1] Raman provides an excellent means of determining the number of layers in a stack of graphene. Single electron transistors have mapped electron-hole puddles across a sample area.[2] Quantum confinement and Berry Phase corrections are two examples of quantum phenomena that alter the properties of nano-scale structures.[3] Optical and electrical properties must be understood before they are measured. This presentation will cover the research and development of metrology for CMOS Extension and Beyond CMOS.

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2-3

Characterization of Integrated Nano Materials

Amal Chabli, François Bertin, Philippe Andreucci and Jean-Christophe Gabriel

CEA, LETI, MINATEC, F38054 Grenoble, France

ABSTRACT

The role of the physical and chemical characterization is to support all together, the material choice and its improvement, the analysis of scaling effects and their use or correction, and the design of integration processes and their validation. Depending on the level of the technological developments, the characterization techniques are mature to support them or still require protocol definition and relevance demonstration for the issues addressed. For Beyond CMOS and Extreme CMOS Devices, the integration of nano-objects like nanowires and carbon nanotubes, brings about analysis requirements that are at the frontier of the state-of-the-art characterization techniques. Furthermore, the Beyond CMOS technology issues would call for anticipating the characterization challenges related to the 3D-information that will be needed. The integration of nano material has to deal with process selectivity; process reproducibility and uniformity; self organisation; localisation; connection and manipulation at the nanoscale while keeping the basic properties of the nano material during these processes.

The increasing interest for size effects on material properties has driven an important effort in the development of physical and chemical characterization techniques at the nanoscale. Impressive capabilities in terms of sensitivity, selectivity, depth resolution and spatial resolution are demonstrated based on huge instrumental effort, advanced configurations of probe-sample interaction and/or powerful simulations for data interpretation [1-3]. All these improvements sustain nanoscience research promoting innovative nano component design. However, only few characterization developments address the integration issues.

In this paper, we will highlight the specific limitations of the use of the existing physical and chemical characterization techniques for integrated nano materials. In particular we will show how specific sample preparation may serve the extraction of the required 3D information, for example, using tomography modes [4-6]. Also, when nanostructures are integrated, in-situ localization and positioning become challenging specifically for Scanning Probe Microscopy. In that case, in-situ SEM observations and multiprobe tools would offer an important added value [7,8]. Moreover, the 3D integration and, MEMS and NEMS technologies set specific characterization conditions related to the very high aspect ratio and to the motion of the integrated nanostructures like nanowires and nanotubes. Thus we will also cover the emerging measurement developments [9] guided by the need for dynamic characterization of these components all along the manufacturing process.

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3-1

Boron Nanowires for Flexible Electronics and Field Emission

Jifa Tian, Jinming Cai, Chao Hui, Chengmin Shen and Hongjun Gao

Institute of Physics, Chinese academy of Sciences, Beijing 100190, P R China

ABSTRACT

Development of a rational synthetic method of flexible nanomaterials may enable exciting avenues in both fundamental research and novel device applications. In this presentation, flexible boron nanowires have been successfully synthesized on both Si(111) and scanning tunneling microscope (STM) W tips via thermoreduction of boron-oxygen compounds with active metal. These as-prepared nanowires, which are structurally uniform and single crystalline as shown in Figure 1(a) and (b), represent good semiconductor at high temperature. A stable field emission current was observed from a single boron nanowire with enhancement factor of 10^6 (Figure 1(c) and (d)). Electrical conductivity of these intrinsic nanowires can be improved two orders by introducing doping atoms. Tensile stress measurements demonstrate excellent mechanical property of as-synthesized boron nanowires as well as resistance to mechanical fracture even under a strain of 3% shown in Figure (e) to (h). Importantly, simultaneous electrical measurement reveals that the corresponding electrical conductance is very robust and remains constant under mechanical strain shown in Figure 1(i). Our results can be briefly explained by Mott's variable range hopping (VRH) model. Boron nanostructures with excellent controllability, remarkable mechanical flexibility and field emission characteristics represent promising candidates for flexible nanoelectronic circuits as well as electron emission nanodevices.

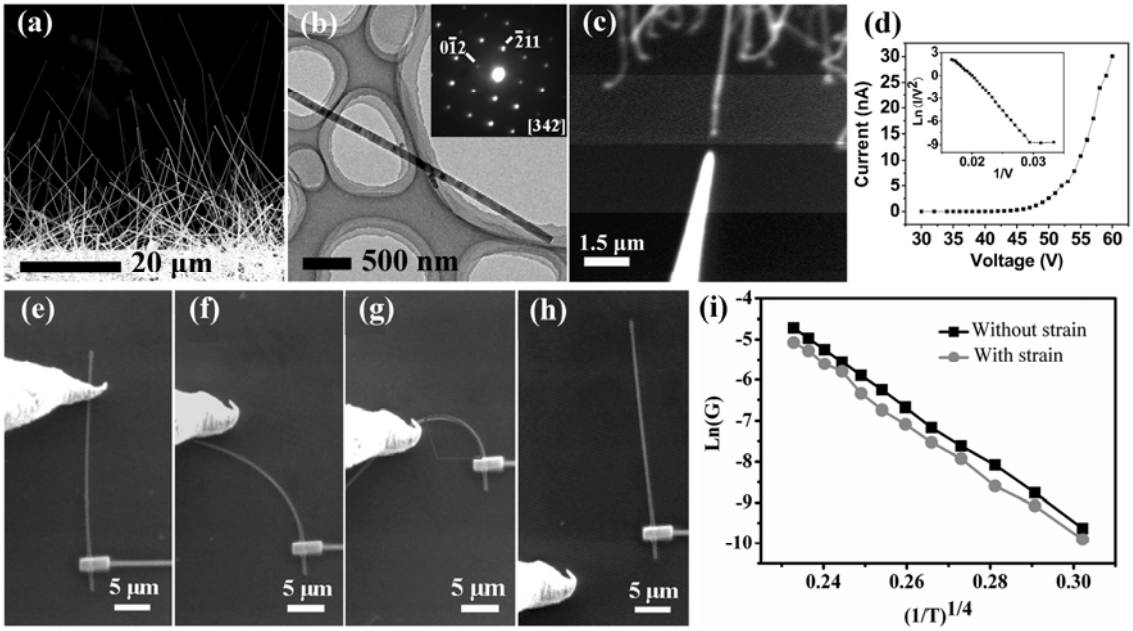

FIGURE 1. (a) A typical SEM image of boron nanowires on Si (111) substrate; (b) TEM image of a single boron nanowire. The inset is the corresponding SAED pattern which can be indexed to β-Rhombohedral boron; (c) Field emission measurement from a single boron nanowire; (d) The relationship between applied voltage and emission current; (e-h) SEM images showing mechanical bending process; (i) Temperature dependence of conductivities of nanowires with and without mechanical strain.

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3-2

Nanoscale Measurement Methods for Novel Material Characterization

J. Alexander Liddle, Gila E. Stein,[1] Joseph A. Stroscio, Nikolai B. Zhitenev, P. N. First, and W. A. de Heer

Center for Nanoscale Science and Technology, National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899
School of Physics, Georgia Institute of Technology, Atlanta, GA 30332

ABSTRACT

New materials and devices are under development to support both the "more Moore" and "more than Moore" approaches to sustaining the progress the semiconductor industry has made over the past decades. In most cases new measurement techniques are needed to satisfy two needs: the first is the characterization of the behavior of these materials and devices at a fundamental level and the second is to provide precise information at high throughput for process control.

In this paper we will report on new measurements on three material systems: diblock copolymers, graphene and organic blends. Diblock copolymers are materials with nanoscale domain sizes controlled by the molecular weights of their constituents. They can be made to align congruently with underlying lithographic patterns. They have the potential to increase the pattern densities that can be achieved with conventional lithographic processes and also, with judicial choice of the two polymers, to reduce line-edge roughness. We have developed x-ray scattering measurements to probe feature profile and edge width in these materials.

Graphene, with its high mobility and unusual electronic properties, is a strong candidate to replace silicon as the channel in field-effect transistors, particularly if high on/off ratios can be obtained routinely. However, much remains to be done, both in terms of investigating its intrinsic properties and in determining how to fabricate devices from it. We have used low-temperature scanning tunneling microscopy to measure the effect of single defects[1] and to probe the unique, high-magnetic field quantization behavior of the material (Fig. 1)[2].

Blending organic materials can be used to create nanostructured materials with applications in displays and photovoltaics. Understanding which aspects of their structure are important to their function is challenging. We have developed novel measurement methods using a conducting atomic force microscope to provide data on the combination of topography and photoresponse to probe the workings of these materials.

In this paper we will report on the details of these techniques and some of the initial results they have provided.

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[1] Now at University of Houston, Department of Chemical and Biomolecular Engineering

The "Business" of Nanotechnology. Translating Innovation into Real Technological Breakthroughs

Alain E. Kaloyeros and Alain Diebold

College of Nanoscale Science and Engineering
The University at Albany
Albany, New York 12203

ABSTRACT

The evolution of disciplined human exploration has led to the establishment of nanotechnology as the primary enabler for innovation and education in science and engineering in the 21st Century. With its ability to control the formation of individual building blocks of matter at the molecular level, atom by atom, to form physical, biological, and chemical systems with customized properties and precise functionalities, nanotechnology is transforming and reshaping the research, educational, and economic landscapes. The importance of nanoscale know-how to the U.S. research, pedagogical, and business agendas is captured in the multi-billion dollar National Nanotechnology Initiative (NNI), signed into law by the U.S. President in 2004, which proclaims nanotechnology as "leading to the next industrial revolution." These conclusions are echoed by almost every study, blueprint, report, and analysis published by a governmental body, corporate organization, academic entity, think tank, and cross-organizational panel across the globe.

The technical complexity and financial cost associated with the unprecedented nanotechnology innovations are generating a radical transformation in the prevailing R&D and commercialization paradigm of the nanoelectronics industrial and university communities. From an R&D perspective, the challenges involved in the identification, screening, and selection of radically different sets of material and processing solutions represent a daunting challenge. This challenge is driving a sweeping change in nanoelectronics technology development and deployment protocols away from the conventional, individual university and/or company centric model to an intellectually open approach. From a financial perspective, the cost for future IC manufacturing nodes will continue to rise exponentially, with the investments required per IC technology node nearly tripling in less than three device nodes. According to Synopys, the total cost for design, process R&D, and one manufacturing fab is projected to rise from ~$4.0B for the 65nm chip platform to ~$9.0-$12.0B for its 32nm node counterpart. This exponential cost increase "….creates elitism with a few haves and most have nots….."

The convergence of ever more intricate technological obstacles and taxing financial constraints are forcing even the handful of remaining "haves" of mega nanoelectronics corporations to participate in inter-disciplinary, university-industry, vertically and horizontally integrated R&D consortia centered on a state-of-the-art, multi-dimensional, "Switzerland" type business model. Such model ensures the pooling of the intellectual assets and physical resources necessary to guarantee timely technology demonstration and delivery, while providing the leveled playing field required by each consortium participant to leverage its investments and protect its privacy and confidentiality.

In response to these R&D and commercialization challenges and opportunities, the College of Nanoscale Science and Engineering ("CNSE") at the University at Albany ("UAlbany") was developed as a novel innovation resource and business paradigm for R&D, workforce education, and economic outreach in nanotechnology and nanotechnology-enabled high technology industries of the 21st century. This presentation describes key elements of the CNSE strategic plan, including pertinent details of its implementation pathways, achievement to-date, and lessons learned, with particular emphasis on nanoscale metrology and characterization.

TU-01

Wave Front Sensor for Highly Accurate Characterization of Flatness on Wafer Surfaces

A. Nutsch[a], I. Lazareva[a], L. Pfitzner[a], T. Grandin[b], S. Bucourt[b]

[a] *Fraunhofer IISB, Schottkystrasse 10, 91058 Erlangen, Germany*
[b] *Imagine Optic, 18 Rue Charles de Gaulle, 9410 Orsay, France*

ABSTRACT

New lithography technologies, as for example Extreme Ultra Violet (EUV), require high flatness of the exposure surfaces as the depth of focus is impacted. Semiconductor manufacturing processes start on bare silicon substrates having excellent surface flatness. In the subsequent process chain of manufacturing of integrated circuits, it is crucial to maintain this initial surface flatness. Integrated device manufacturers use different technologies involving materials such as metals, semiconductors, and isolators to build three-dimensional structures and patterns on the wafer. The miscellaneousness of materials and patterns on the surface of highly integrated circuits limits the use of metrology developed for flatness analysis of bare silicon wafers. Nevertheless, it is essential for semiconductor manufacturing to measure and control the topography of wafer surfaces at nanometer scale. In-plane geometrical defects on wafer surfaces extending lateral in the millimeter range and in vertical in the nanometer range are of increasing importance becoming a severe yield limiting factor in the future technology generations.

Wave front sensing was developed to characterize topography on bare and patterned wafer surfaces. The strategy to provide a solution for inspection requires both, a field of view smaller than the wafer diameter and an instant measurement. A reflection of an initially planar wave front is measured. The reflection contains the sample surface flatness information. The reflected and deformed wave front was analyzed by using a Shack Hartmann sensor. A field of view smaller than the wafer surface enables highly accurate determination of flatness as the number of data points providing the base for the topography is improved. Figure 1 shows examples of high resolution topographies on bare and STI wafer surface. The Shack Hartmann module provides 128 × 128 points. The field of view on the bare wafer was 25 mm × 25 mm, on the STI wafer it was 80 mm × 80 mm.

Post processing of the acquired data applied 2 D double Gaussian high pass filters to obtain the flatness data. Global geometry such as tilt, bow and warp are removed to access the flatness information. The standard deviation of the flatness data after filtering was almost independent with respect to the lateral resolution. On bare wafer surfaces, it was found to be below 0.1 nm, on patterned surfaces the standard deviation was smaller than 1 nm. Changes in reflectivity were found to impact the measured topography as well as filtering limits the absolute accuracy of the topography determination found below 10 nm. The results were validated by using a wavefront sensor according to the method of Makyoh. The instantaneous acquisition time is a key to use the technique for inspection.

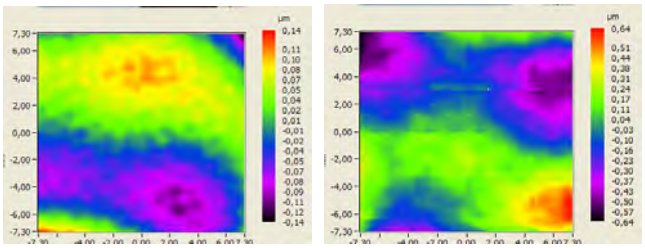


FIGURE 1. Topography of a bare wafer surface measured with 0.195 mm lateral resolution (left side); Topography of a STI wafer surface measured with 0.62 mm lateral resolution (right side).

Keywords: wave front sensing, flatness, Shack Hartmann

VOC & Metallic Contaminant Control For SOI Process Monitoring

Roland Brun[1], Cécile Moulin[1], Christophe Girard[1], Bill Usry[2], Robert Newcomb[2]

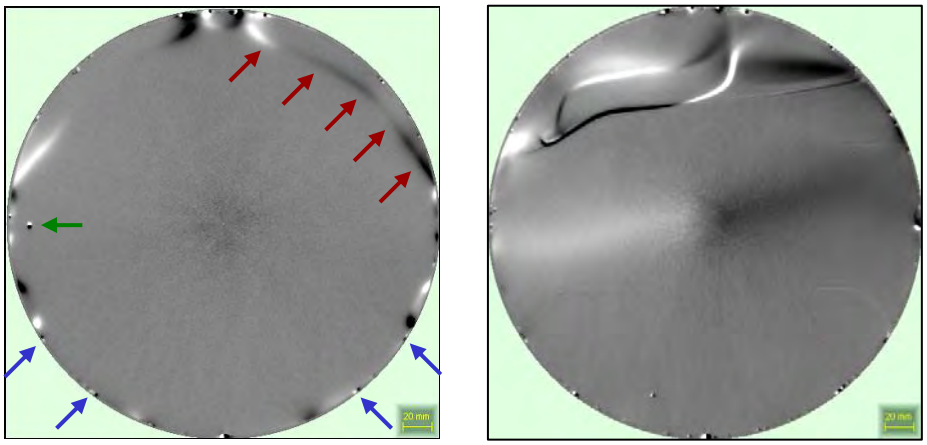
[1]*Soitec, Parc technologique des Fontaines, Bernin, 38926 CROLLES Cedex France*
[2]*Qcept Technologies, 75 Fifth Street NW, Suite 740 Atlanta, GA 30308 USA*

ABSTRACT

Silicon-on-Insulator (SOI) is an enabling technology for nanoscale devices. Already in use as the basis for today's most advanced devices, SOI is expected to be adopted even more widely in the future. Incoming wafer quality is especially critical to an SOI manufacturer, because two starting wafers are required to produce a single final SOI wafer. In the past, the industry has relied primarily on particle measurements to determine the cleanliness of a wafer. However, we have found that particle measurements give only one aspect of the cleanliness of a wafer. Real time characterization of metallic and organic wafer surface contaminants is key to assess wafer quality and improve yield.

ChemetriQ[(1,2)] is a tool developed by Qcept that non-destructively measures surface potential variation. Full mapping from ChemetriQ inspection provides spatial signatures of the contamination over the full wafer surface. This spatial information is critical in understanding which defects at intermediate process steps impact final yield. Additionally, its unique capability to detect the real edge of the wafer allows applications like troubleshooting edge handling/chuck systems, and to perform product signature root cause analysis.

Soitec developed, in cooperation with Qcept, front side and backside inspections for 200mm and 300mm wafers. An effective and powerful wafer quality control for metallic and organic wafer surface contamination becomes possible with this new technique. Figure 1 shows images from ChemetriQ inspections for two incoming prime silicon wafers. The wafer in Figure 1a) shows edge point defects near the edge (blue arrow), an interior defect that is likely metallic in nature (green arrow) and a FOSB outgassing signature (red arrow). Figure 1b) shows a wafer from the top slot in a FOSB. This particular wafer has a strong signal residue contamination on the top section of the wafer.



a) b)

FIGURE 1. ChemetriQ inspection images for incoming wafers

Keywords: Non-Visual Defect, contamination, inspection

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TU-03

Nanoscale Characterization Of Ultra-Thin Dielectrics Using Scanning Capacitance Microscopy

O. Ligor, A. Descamps, D. Albertini, L. Militaru, N. Baboux and B. Gautier

Lyon Institute of Nanotechnology (INL), UMR CNRS 5270, Université de Lyon
7, Avenue Capelle, F-69621 VILLEURBANNE, FRANCE

ABSTRACT

Scanning Capacitance Microscopy (SCM) is a widely used tool for dopant mapping in the semiconductor structures [1] because it is particularly efficient to discriminate between n-type and p-type dopants in spite of a relatively poor resolution compared to other techniques like Scanning Spreading Resistance Microscopy [2]. SCM relies on the presence of an oxide on the surface, necessary to form the Metal-Oxide-Semiconductor stack which is at the basis of the SCM operation. This oxide is usually a burden for SCM because it has to fulfill contradictory requirements : it has to be grown at low temperature in order to avoid dopant redistribution but has to contain as less charges as possible; it must be thin so that the signal to noise ratio is good but not too thin to avoid leakage currents...

In order to test the quality of the top oxide for SCM operation, Scanning Capacitance Spectroscopy (SCS) has been developed, that record the SCM signal ($\Delta C/\Delta V$) as a function of the applied continuous voltage V_{DC} [3]. SCS has been used mainly in order to test the quality of the top oxide used for SCM operation i. e. SiO_2 [4] or ZrO_2 [5], however, it can be used to characterize any dielectric (in that case, the doping level of the underlying semiconductor is supposed to be well known) [5].

In this communication, SCS is used in order to characterize the electrical properties of ultra thin dielectrics. The aim is to determine the best experimental conditions that lead to a reliable measurement of the characteristics of the oxide (charging, flat band voltage...) and to the best signal to noise ratio. Comparisons are made with macroscopic C-V curves obtained with an impedance analyzer, to test the reliability of the results obtained by SCS. In particular, we study the role of the tip-sample contact on the shape of the SCS (width, additional peaks...) and show that a vacuum environment and/or a controlled atmosphere during SCM operation is needed to obtain reliable information with no parasitic features introduced by SCS itself, especially in the case where characteristic parameters of the oxide are to be extracted from SCS (densities of interface states, charging effects ...).

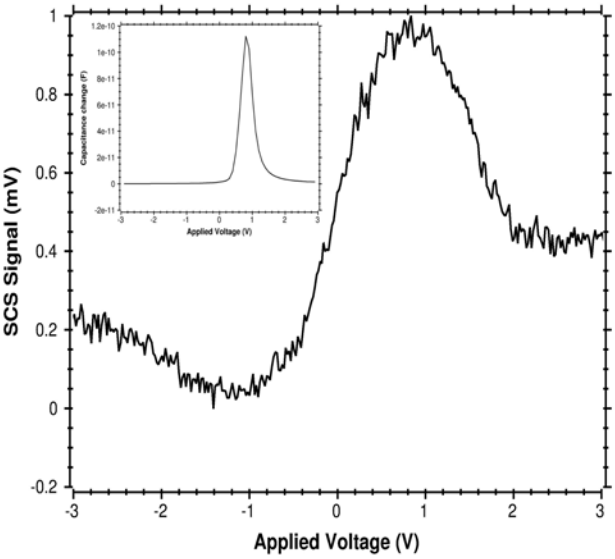

Figure 1. Example of SCS obtained on a thermal 5 nm thick SiO_2, compared to the macroscopic C-V curve (insert), the peak is at the correct place compared to macroscopic C-V curves, but the width of the peak is far larger and a second peak has appeared in the inversion zone due to the quality of the tip-sample contact

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KEYWORDS : Atomic Force Microscope, Ultra-thin dielectrics, C-V characteristic

TU-04

Reference-free Characterisation Of Semiconductor Surface Contamination And Nanolayers By X-Ray Spectrometry

B. Beckhoff, R. Fliegauf, P. Hönicke, M. Kolbe, M. Müller, B. Pollakowski, F. Reinhardt, J. Weser and G. Ulm

Physikalisch-Technische Bundesanstalt
Abbestr. 2-12. 10587 Berlin, Germany

ABSTRACT

X-Ray Spectrometry (XRS) is a wide spread technique for revealing reliable information concerning the elemental composition and binding state in various materials. Reference-free quantitation in XRS is based on the knowledge of both the instrumental and fundamental atomic parameters [1]. In different configurations, both matrix and trace constituents of a sample or layer thicknesses can be determined, even providing lateral or depth-profiling elemental information [2]. With respect to very flat samples, such as semiconductor wafers or structures, the photon energy and the angle of incidence of the exciting radiation determines the probing depth of XRS analysis. In total-reflection geometry, i.e. having an angle of incidence smaller than the critical angle of total external reflection, only surface contamination and the surface-near layer of a few nm contributes to the fluorescence spectra. Allowing the angle of incidence to be varied from close to zero up to about four times the critical angle of total external reflection, the probing depth ranges from a few up to several hundreds of nm.

The methodological development of XRS at the Physikalisch-Technische Bundesanstalt (PTB), Germany's national metrology institute, is, among other issues, dedicated to high-end investigations in the R&D of semiconductor samples requiring reference-free methods, in particular for novel materials for which not enough appropriate reference materials are available. PTB can handle 200 mm and 300 mm silicon wafers as well as smaller semiconductor wafers in its XRS instrumentation. The instrumentation for 200 mm and 300 mm Si wafers is equipped with an EFEM module. The use of undulator radiation in the PTB laboratory at BESSY is advantageous for off-line contamination control on semiconductor surfaces as it provides very high photon fluxes for the efficient excitation of light elements. Optimizing the respective excitation conditions such as the angle of incidence and the incident photon energy, detection limits of light elements in the fg range can be achieved.

Grazing incidence investigations demonstrated the capability for depth profiling of light elements in nanolayers [3]. Reference-free XRS has the potential to contribute to the thickness and composition analysis of nearly vertical sidewalls of semiconductor test structures [4]. This technique is also able to contribute to the elemental depth-profiling of ultra-shallow junctions (USJ), i.e. near-surface implantation profiles in wafers, as a complementary approach to other analytical techniques. At a given incident angle, XRS can be combined with X-ray absorption spectroscopy (NEXAFS, XANES or EXAFS), revealing information on the depth profile of the chemical structure in a sample, e.g. about buried nanolayers [5] or interfaces with varying chemical state.

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TU-05

Polarized Optical Scattering Measurements of Metallic Nanoparticles on a Thin Film Silicon Wafer

Cheng-Yang Liu, Tze-An Liu and Wei-En Fu

Center for Measurement Standards, Industrial Technology Research Institute
Room 216, Building 8, 321, Sec. 2, Kuang Fu Road, Hsinchu, Taiwan

ABSTRACT

Light scattering has shown its powerful diagnostic capability to characterize optical quality surfaces [1]. As a result, instruments based on light scattering satisfy many of the metrology and inspection requirements for semiconductor industries, such as high throughput and high sensitivity. In this study, the theory of bidirectional reflectance distribution function (BRDF) was used to analyze the metallic nanoparticles' sizes on wafer surfaces. The BRDF of a surface is defined as the angular distribution of radiance scattered by the surface normalized by the irradiance incident on the surface [2,3]. A goniometric optical scatter instrument has been developed to perform the BRDF measurements on polarized light scattering on wafer surfaces for the diameter and distribution measurements of metallic nanoparticles. The designed optical scatter instrument is capable of distinguishing various types of optical scattering characteristics, which are corresponding to the diameters of the metallic nanoparticles, near surfaces by using the Mueller matrix calculation. The measurement range of metallic nanoparticle diameters is 10 nm to 60 nm on 4 inch thin film wafers. These measurement results demonstrate that the polarization of light scattered by metallic particles can be used to determine the size of metallic nanoparticles on silicon wafers.

FIGURE 1. Goniometric optical scatter instrument.

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Fundamental SIMS Metrology Development and Considerations for Molecular Depth Profiling of Photoresist Materials on Silicon

Christopher Szakal,[a*] Steve Hues,[b] Joe Bennett,[c] and Greg Gillen[a]

[a]*National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899-8371*
[b]*Micron Technology, Inc., 8000 S. Federal Way, P.O. Box 6, MS 1-717, Boise, ID 83707-0006*
[c]*SVTC Technologies,2706 Montopolis Drive, Austin, TX 78741*

cszakal@nist.gov
Phone: (301)-975-3816; Fax: (301)-417-1321

ABSTRACT

In collaboration with International Sematech and SVTC technologies, we investigated the considerations necessary for the cluster secondary ion mass spectrometry (SIMS) molecular depth profiling of organic photoresist overlayers on silicon, and in particular, high-quality PMMA films on silicon. At NIST, we have been actively developing methods for organic and molecular surface analysis of semiconductor materials using SIMS technologies. Recent advances in cluster (SIMS) have led to the ability to perform molecular depth profiling for a range of organic materials. Cluster ion beams such as Au_3^+, Bi_n^+, SF_5^+, and C_{60}^+ have shown varying abilities to probe through organic films and soft substrates. The work has been successful because of the premise of sufficiently high target sputter yields that remove beam-induced molecular damage as it is created. Hence, molecular signals can be maintained without significant damage cross sections at ion beam fluences well beyond the traditional "static limit" employed with atomic ion beam analysis. However, in certain modalities, it has been postulated and in some cases demonstrated that a "dual beam analysis" can be exploited for maximum sputtering yield and minimum damage of the erosion beam, while acquiring imaging data with a better-focused smaller cluster beam such as Bi_n^+. This study finds that the effects of the analysis fluence shall not be considered negligible to the imparting of permanent beam-induced damage within the organic materials being depth profiled. Instead, it is found that increasing the analysis fluence can degrade the quality of the interface widths of a high-quality PMMA film on silicon, despite the prospects of the sputter beam to remove accumulated beam-induced damage. This set of findings has broad implications for the surface analysis of organic molecules on silicon, and a discussion will be made as to the applicability of the cluster SIMS methods to study the fundamental metrology of next-generation semiconductor devices and nanoelectronics.

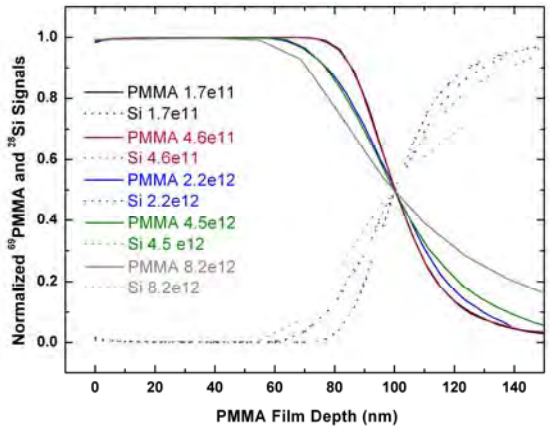

FIGURE 1. Cluster SIMS molecular depth profile of normalized PMMA and Si signals vs. depth as a function of increasing primary ion analysis fluence.

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TU-07

Abstract Withdrawn

TU-08

Built-In Self Test Capability For MEMS Microhotplate Temperature Sensors

M. Yaqub Afridi, Christopher B. Montgomery, Elliot Copper-Balis, Stephen Semancik, Kenneth G. Kreider, and J. Geist

Semiconductor Electronics Division and Process Measurements Divisions
National Institute of Standards and Technology
Gaithersburg MD 20878-9957

ABSTRACT

We describe a novel microhotplate temperature-sensor calibration technique suitable for Built-In Self Test (BIST) of MEMS microhotplates. The technique only requires short-term temperature stability from the polysilicon resistive temperature sensors that are commonly used in microhotplates and that often also serve as microhotplate heaters. Long term stability and BIST functionality must be provided by two independent temperature sensors whose calibrations do not drift significantly with time, but which need not be capable of direct calibration, because they can be calibrated against the polysilicon temperature sensor immediately following its direct calibration. The thermal efficiency (heater power versus heater temperature) of the microhotplate and a platinum/rhodium thermocouple were used as the BIST temperature sensors. Temperature measurements were carried out on a microhotplate at eleven different times over a period of three months during which the microhotplate was operated in a way designed to simulate normal use over two years in a typical application of a microhotplate-based gas sensor. Microhotplate temperature measurements that were based on a single thermal efficiency calibration carried out at the beginning of the three month period agreed with those based on a single thermocouple calibration also carried out at the beginning of the three month period to plus or minus 1.5 degrees from 100 to 400 degrees Celsius. On the other hand, measurements based on a single direct calibration of the polysilicon temperature sensor varied erratically within a range greater than twenty degrees over the same three month period at temperatures above 275 degrees Celsius.

Key Words: BIST, Built-In Self Test, MEMS, Microhotplate

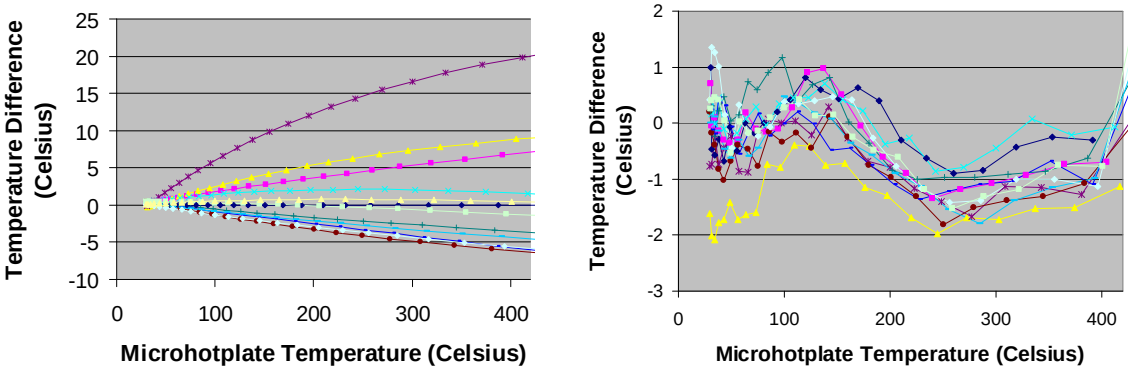

FIGURE 1. (Left) The difference between the actual microhotplate temperature and the microhotplate temperature measured by the polysilicon temperature sensor based on a direct calibration carried out at the beginning of a three-month test period. (Right) The difference between the microhotplate temperature calculated from the microhotplate thermal efficiency calibration carried out at the beginning of the same three month period and that calculated from thermocouple calibration also carried out at the beginning of the same three month period.

TU-09

Enhanced Spatial Resolution Scanning Kelvin Force Microscopy Using Conductive Carbon Nanotube Tips

Joseph J. Kopanski[1], Paul McClure[2], and Vladimir Mancerski[2]

[1] *Semiconductor Electronics Division*
National Institute of Standards and Technology
100 Bureau Dr., stop 8120
Gaithersburg, MD 20899

[2]*Xidex Corporation*
8906 Wall Street, Suite 703
Austin, Texas 78754

ABSTRACT

The Scanning Kelvin Force Microscope (SKFM) is an interesting instrument with which to examine work function variations in a variety of materials and structures of interest for nanoelectronics. However, SKFM suffers from poor spatial resolution due to the capacitive coupling of all parts of the tip and cantilever to the sample. The magnitude of the contribution to the total capacitive signal of any element of the probe assembly varies with the inverse square of the distance between any part of the tip/cantilever and the sample. In operation, abrupt boundaries between two materials with different work functions can not be precisely located and local measurement of work function is effected by the work function of surrounding material. A simple model predicts that tips with high aspect ratios will achieve better spatial resolution. This means that the ideal tip for SKFM would be a cylinder. Carbon nanotube tips mounted on the end of conventional micromachined silicon tips are close to this ideal shape.

A SKFM constructed at NIST uses an external feedback loop implemented with a Digital Signal Processor and external lock-in amplifiers to implement both amplitude-modulated and frequency-modulated SKFM. As all parameters controlling the operation of the SKFM can be precisely set and monitored using this instrument, it makes an ideal platform for evaluating the performance of different tips in SKFM. We have begun evaluating carbon nanotube tips for electrical scanning probe microscopy measurements on semiconductors and structures for integrated circuits. Areas of interest include two-dimensional dopant profiling, measurement of the work function of gate stack materials and of the tips themselves, measurement of dielectric constant for measuring damage to plasma etched low-k dielectrics, measurement of strain induced work function changes in semiconductors, and the use of the SKFM as a sensor for detecting work function changes in a surface due to contaminates in the ambient atmosphere.

TU-010

Application of Micro-thermal Analysis for Metal, Oxide, and Non-oxide Thin Film Materials

Nathan Carlie, Jonathan Massera, Laeticia Petit, and Kathleen Richardson

Clemson University School of Materials Science and Engineering / COMSET,
161 Sirrine Hall, Clemson University, Clemson, SC 29630

ABSTRACT

The use of micro-thermal analysis for the measurement of thermal properties in thin film materials is relatively new [1]. The micro-thermal analyzer (TA Instruments model μTA-2990) combines an electrically heated wire probe and a standard AFM. This allows both micro thermal imaging of the sample surface and measurement of micro-thermal transitions. This technique enjoys higher lateral resolution as compared to infrared imaging techniques for the determination of thermal conductivity [2], and avoids the possibility laser-induced material modifications which may occur during laser flash measurements on non-oxide materials such as chalcogenide glasses [3]. For the measurement of thermodynamic or viscosity-related transition temperatures, such as softening points, the technique has the ability to acquire accurate data while the film is still attached to its substrate, and without special prior preparation of the sample [4].

In order to leverage these advantages, careful optimization of variables such as probe temperatures and heating rates [5], understanding the influence of film thickness [6], and calibration of the instrument against background heat losses [7-9] is critical. In this presentation, we explain first the calibration of the micro-thermal analyzer using baulk materials with known thermal properties, by thermal imaging of patterned silicon wafers. The experimental methods have also been optimized for thermal properties measurements on thin films with the composition $Te_2As_3Se_5$, known to have low thermal conductivity and glass transition temperature. The effect of film thickness and substrate of the measurement of thermal conductivity and dilatometric softening point of these films is discussed.

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TU-011

Work Function Measurements in Kelvin Force Microscopy: Analytical Understandings of Experimental Parameters Effects

K. Kaja, N. Chevalier, D. Mariolle, G. Feuillet, F. Bertin, A. Chabli

CEA, LETI, MINATEC, F38054 Grenoble, France
khaled.kaja@cea.fr

ABSTRACT

The importance of the experimental protocol optimisation of the sample surface preparation in Kelvin Force Microscopy (KFM) has already been emphasized [1, 2]. We extrapolate these works by investigating the influence of the most relevant experimental parameters on the Work Function (WF) difference measurements obtained using KFM technique operating in both a nitrogen and ambient environment. Effects of the separation distance between the tip and the sample (Lift height), the ac bias potential applied to the tip (V_{ac}) and the environment relative humidity (R.H.%) were investigated. Measurements were done, in the same conditions, on various metallic samples (Au, Ru, Cu, Pt, Al). Similar trends of the WF difference variations as a function of the lift height changes were observed for all samples (figure 1). A thorough understanding of these effects is of great importance to interpret the quantitative measurements made by KFM. Using the method of images, we developed an analytical model, based on the interpretation of surface patches charge distribution issued from the WF anisotropy over the sample surface [3,4]. Figure 1 shows the agreement between the analytical model (lines) and experimental results (points) obtained on all metallic samples cited above. In conclusion, we propose a mechanism for the observed WF dependence on experimental parameters.

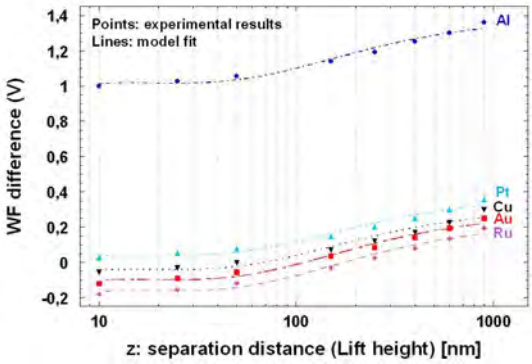

FIGURE 1. Agreement between the model fit and the experimental WF difference changes as a function of the lift height.

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Keywords: KFM, Work function, Lift height dependence

TU-012

Contact Resistance Measurements of Metal on HOPG and Graphene Stacks

Archana Venugopal[§], Adam Pirkle[*], Robert M. Wallace[*], Luigi Colombo[¥], and Eric M. Vogel[§, *]

[§]*Dept. of Electrical Engineering, University of Texas at Dallas. of Texas at Dallas*
[*]*Dept. of Materials Science and Engineering, University of Texas at Dallas*
[¥]*Texas Instruments Incorporated, Dallas, TX*

ABSTRACT

Contact resistance is one of the major factors limiting the performance of future nanoelectronic devices. Although there has been significant progress in graphene based devices since 2004[1,2,3], there have been few studies of factors such as metal type, metal workfunction and number of layers in the graphene stack on metal/graphene contact resistance. In this work, contact resistance measurements of various metals (Cr, Ni, Pd, Pt) on Highly Oriented Pyrolytic Graphite (HOPG) and graphene (single layered and few layered) were performed. Fig.1 shows an example of transfer length measurements (TLM) of various metals on HOPG. The total resistance as a function of distance between contacts is shown. The total resistance is independent of distance indicating that the total resistance is dominated by contact resistance. The contact resistance is observed to be similar for a wide variety of metals although the metal workfunction varies from 4.3 eV to 5.6 eV. Similar measurements will be presented for metal on single- and multi-layer graphene. The electrical results will be compared to XPS measurements of thin metal on HOPG. Issues regarding the characterization and interpretation of contact resistance on metal/semimetal systems will be presented.

Key words: Graphene, contact resistance

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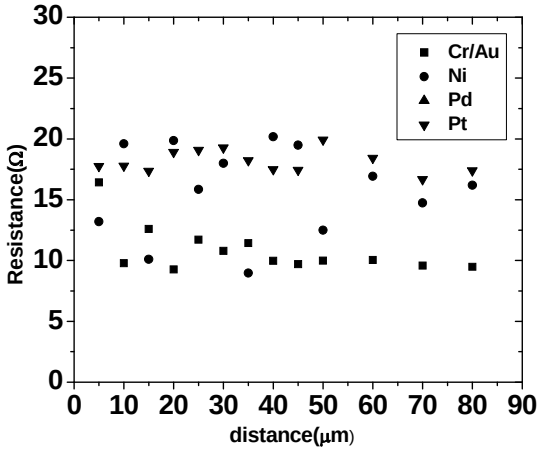

FIGURE 1. TLM Plots for metal contacts on Highly Oriented Pyrolytic Graphite.

Sub-Surface Nano-Metrology of Buried Patterns and Structures in EUVL and DUV Masks Using Ultrasound

***Gajendra Shekhawat*[1#] *,Arvind Srivastava*[2] *and Vinayak Dravid*[1,2]**

[1]Institute for Nanotechnology, Northwestern University, Evanston, United States

[2]Depart. of Material Science and Engineering, Northwestern University, Evanston, USA

Corresponding Author: Gajendra Shekhawat, 1161 Cook Hall, 2220 N Campus Dr, Northwestern University, Evanston, IL 60208, (847) 491-3204, Email: g-shekhawat@northwestern.edu

ASTRACT

The need for non-destructive nanoscale high resolution imaging of buried and embedded structures in materials, devices, and pattern recognition is critical for numerous materials, structures and phenomena as they continue to shrink, and the micro/nanofabrication paradigm moves from planar to 3D or stacked platforms. This will not only provide new technique for in-line buried patterns inspection in semiconductor industry, but also avoid the complex processing to visualize the defects buried under the surface using cross-section SEM and transmission electron microscopy.

We have developed a novel technique called: scanning near-field ultrasound holography (SNFUH), which combines the nanometer-scale spatial resolution of conventional scanning probe microscope (SPM) with the surface and subsurface imaging capabilities. This technique fills the critical void in characterization and investigation of the static and dynamic mechanics of nanoscale systems and address emerging issues in imaging and analysis of diverse “embedded” nano and microscale structures, and engineered systems [1]. The SNFUH development integrates three major approaches: a unique combination of scanning probe microscope platform (which enjoys excellent lateral and vertical resolution) coupled to microscale ultrasound source and detection (which facilitates “looking” deeper into structures, section-by-section) and a novel holography approach (to enhance phase resolution and phase coupling in imaging).

We have demonstrated the unique applications of SNFUH in semiconductor test structures by identifying buried microelectronics patterns using model sample which is equally spaced dots patterned using e-beam lithography, which are buried under multi-layer thin film stacks of Mo-Si layers in a non-destructive way. Each dot has a diameter around 70 nm. The thickness of the multi-stack Mo-Si layers was around 300 nm. Figure 1A show a schematic of buried dots under stack of multi-layers having thickness of 300 nm. Figure 1B depicts the conventional topography image, while Figure 1C is the corresponding (simultaneously recorded) spectacular SNFUH phase image. The topography scan shows uniform and featureless surface. However, the corresponding SNFUH *phase* image shown in Figure 1C reveals phase contrast reminiscent of buried e-beam patterned dots under multi-stack layers. The dark contrast in the phase image corresponds to buried patterned dots, which undergoes a distinct viscoelastic response.

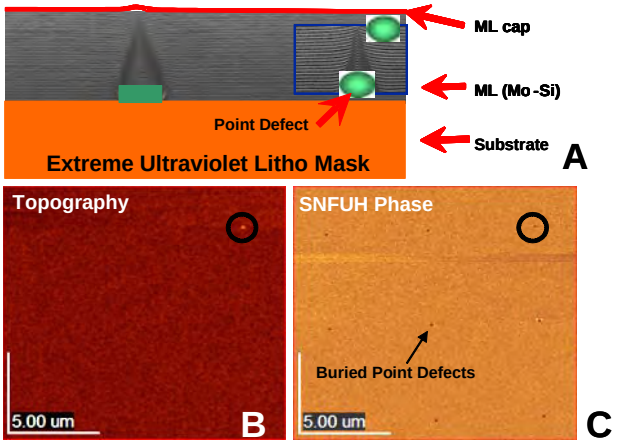

Figure 1: (A) Schematic illustration of a model sample with e-beam patterned dots on silicon substrate and buried under reflective Mo/Si multilayer films. The thickness of the layers is around 280 nm. Typical AFM (topography) image shows featureless and smooth surface and (C) shows a remarkable SNFUH phase image clearly showing the buried dots with high definition under multi-layer stack. The FWHM of dots width is around 70 nm.

We believe that this novel application of our SNFUH system will open up its potential application in identifying bubbles, inclusions and pits at the interface of quartz substrate and Mo/Si layers used for EUVL mask without damaging it. This will also open up new application paradigm in imaging cracks in DUV photo masks and point defects in gate oxide.

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TU-014

Advanced Capacitance Metrology for Nanoelectronic Device Characterization

Curt A. Richter[1], Joseph J. Kopanski[1], Chong Jiang[1], Yicheng Wang[2], M. Yaqub Afridi[1], Xiaoxiao Zhu[3], D.E. Ioannou[3], and Qiliang Li[3]

1-Semiconductor Electronics Division, 2- Quantum Electrical Metrology Division, National Institute of Standards and Technology, Gaithersburg, Maryland 20899, USA. 301-975-2082; 3-Department of Electrical and Computer Engineering, George Mason University, Fairfax, Virginia 22030: e-mail: Curt.Richter@nist.gov

The component capacitance of individual nm-scale nanoelectronic devices for future generations of integrated circuitry defies easy measurement. Emerging nanoelectronic devices such as those fabricated from semiconductor nanowires (NWs) and quantum dots, as well as FINFET type devices have capacitances that are much smaller than those measurable by conventional LCR meters. The intrinsic device capacitances of these deep-submicron devices (such as the gate-drain, source-drain, or gate-channel capacitances) determine the operational characteristics of the structures and an accurate knowledge of their values is required for accurate device modeling and predictive computer-aided design. We are developing methods to combine probe stations with the sophisticated capacitance measurement equipment and expertise associated with maintaining the capacitance standard for the farad to enable measurments of critical capacitances in nanoelectronic devices at the aF-level.

We designed and fabricated a test chip (consisting of an array of metal-oxide-semiconductor (MOS) capacitors and metal-insulator-metal capacitors ranging from 0.3 fF to 1.2 pF) for use in evaluating the performance of new measurement approaches for small capacitances. By measuring the complete array of capacitances, a "fingerprint" of capacitance values is obtained (Figure 1) which -- after correcting these data for pad and other stray capacitances -- can be used to assess the relative accuracy and sensitivity of a capacitance measurement instrument or circuit.

As a first step towards measuring the capacitances of individual semiconductor NW devices, we designed and fabricated a capacitance test structure consisting of many Si-NWs in parallel. This structure (schematically shown in the insert to Figure 2) utilized a HfO_2 gate dielectric formed via atomic-layer deposition and was fabricated by using a "directed self-assembly" approach [1] in which the SiNWs are grown (by the vapor-liquid-solid process) from catalysts in predefined locations. Typical capacitance-voltage and conductance-voltage data obtained by using the methods developed in characterizing the MOS test structure are shown in Figure 2.

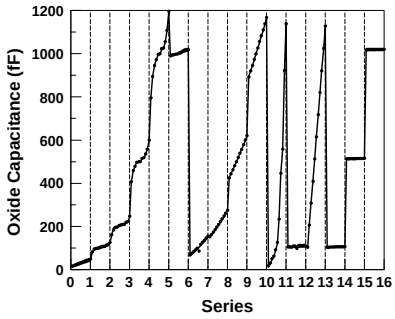

FIGURE 1. Capacitance "fingerprint." Points - typical experimental capacitance values; solid line-calculated values.

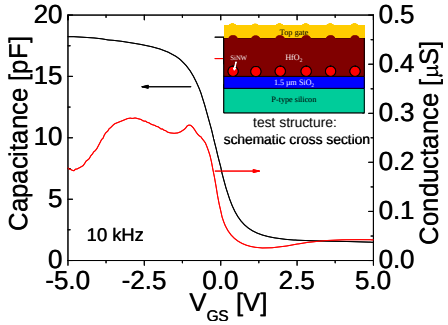

FIGURE 2. Typical capacitance and conductance vs. voltage data (at 10 kHz) for a multi-Si nanowire test structure.

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TU-015

The Effect of Surface Conditioning on Silicon Wafer Resistivity Monitoring

E. Tsidilkovski[1], A. Bertuch[2]

1. Semilab USA, 1 North Ave, Burlington MA 01803, 2. 132 Marlborough St, Boston MA 02116

ABSTRACT

Measurement of semiconductor doping density has been a key component in epitaxial film growth and wafer manufacturing process control. Most standard methods used to control doping density are sensitive to wafer surface condition or surface charge distribution, e.g. a continuous growth of native oxide may lead to 4pp measurement drift [1].

We present an improved non-contact method of surface conditioning that allows us to achieve an accurate and repeatable measurement of doping density with the standard ac-SPV (Surface Photo-Voltage) technique [2]. This method includes low-temperature UV-assisted oxidation, followed by surface charging with ionizing corona of appropriate polarity. Surface oxidation is performed using a uniquely controlled UV process environment, which creates a highly homogeneous and uniform SiO_x film, within few minutes.

This technique has been used to demonstrate a measurement repeatability performance of 0.5% 1-sigma, over a 5-day period. Comparison of this method with 4 pp [1] and CV measurement data show better repeatability and uniformity across the wafer during the investigated period, Figure 1.

The advantage of this type of measurement is due to the precise control of wafer surface charge with integrated preconditioning equipment. The two critical and well-controlled pretreatment steps establish a stable and reproducible state of inversion for the ac-SPV resistivity measurement.

Key words: real-time monitoring, surface control, Surface Photo-Voltage

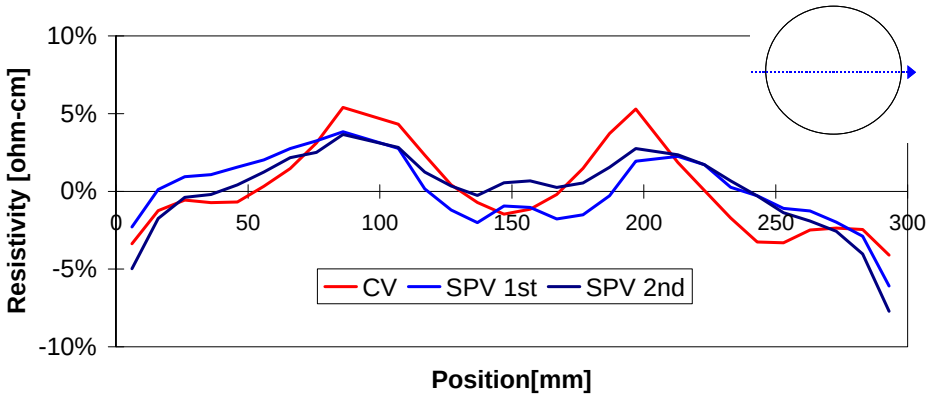

FIGURE 1. 30 Ohm-cm Si wafer diameter scan. Measurement order: UV, Corona, SPV → 5 days later → Corona, SPV → CV.

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TU-016

Variable Temperature Measurements in Cryogenic Probe Stations

Jeffrey Lindemuth

Lake Shore Cryotronics, 575 McCorkle Blvd, Westerville Oh 43082

ABSTRACT

Electrical property measurements of nanoscale materials are important for characterization and understanding of materials and devices. Equally important is to measure these properties at various temperatures. These measurements are facilitated with cryogenic probe stations that provide a variable temperature environment over a wide range of temperatures. However, until this time a major inconvenience was caused by the thermal expansion of the probe tips and probe station as the temperature changed. To prevent the tip movement from damaging the sample, the normal procedure is to lift the probe tips as the temperature changes. This prevents the implementation of totally automated variable temperature measurements.

We present results using a new probe design that allows the probe tips to remain in contact to sample during temperature changes. With this new design we demonstrate, with optical microscopy, the total tip movement of less than 2 microns when the temperature of the sample changes from 4.2K to 300K. The same probes that eliminate the movement from thermal expansion also improve the isolation of the measurements to external vibrations. In standard cryogenic probe stations with sample in vacuum the vacuum pump must be isolated from the probe station to eliminate vibrations, or the pump turned off during the measurements. Using these probes it is possible to make measurements with the pump on. There is no significant difference in the measurement with pump on or pump off. Typical noise levels in well designed measurements are 10 parts per million (RMS) for resistance ranges from 1 ohm to 100K ohm.

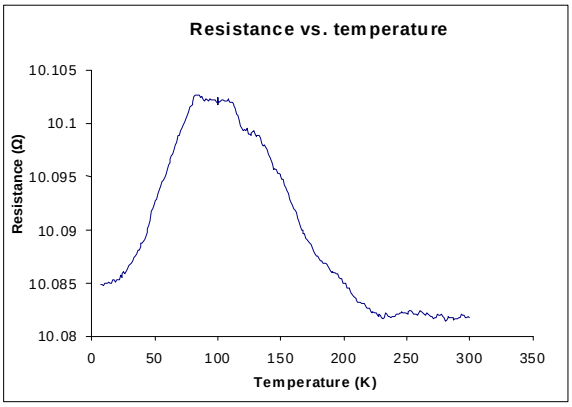

FIGURE 1. Continuous variable temperature measurement of 10 ohm resistor in cryogenic probe station

TU-017

Inline 90nm Technology Gate Oxide Nitrogen Monitoring With Non Contact Electrical Technique

Nicolas Pic[1], Gennadi Polisski[2], Emmanuel Paire[1], Véronique Rizzo[1], Catherine Grosjean[1], Benjamin Bortolotti[1], John Damico[3]

(1) STMicroelectronics, Z.I. de Rousset, BP2, 13106 Rousset Cedex, France
(2) Applied Materials GmbH, Philipp-Hauck-Str.6 D-85622 Feldkirchen, Germany
(3) Semiconductor Diagnostics Inc, 3650 Spectrum Blvd, Ste. 130, Tampa, FL33612, USA

The continuous race to reduce the dimensions of IC components has lead to the introduction of nitrogen in the thin gate oxide layer in order to increase the dielectric constant and to improve the gate dielectric properties. It is mandatory to apply inline monitoring to control the amount of nitrogen, ensuring that electrical behavior is correct over time.

Historically, this monitoring was performed by measuring the delay to reoxidation (D2R) with an ellipsometer. But, this method is not suitable in production as it is depending on both initial oxidation and reoxidation reproducibility, which implies implementing dedicated quality tasks at these two specific processing steps.

We are here presenting an alternative method to D2R for 90 nm Technology gate oxide grown by Rapid Thermal Process. Applying a non-contact Metrology technique, which couples Kelvin probe surface voltage measurement with surface Corona deposition [1], directly after the nitridation step, the interface trapped charge (Q_{IT}) is obtained by integration of the interface state density over the space charge region. In the Figure 1 the Q_{IT} exhibits a good correlation to D2R. Figure 2 demonstrates Q_{IT} correlation to the low Nitrogen dose generated from different process conditions (nitridation temperature and time) and measured by X-ray Photoelectron Spectroscopy (XPS) and Secondary Ion Mass Spectrometry (SIMS).

In summary, this electrical non contact monitoring:

- is more sensitive to the Nitrogen content compared to ellipsometer measurement after nitridation (35% vs. 5%) or after D2R (35% vs. 30%).
- is less sensitive compared to D2R to any initial oxide variation (3% vs. 15%).
- allows simplifying the procedure of qualification of this process step skipping the reoxidation.

Additional electrical parameters that show correlation to Nitrogen content in dielectric such as electrical thickness, obtained by Capacitance-Voltage curve, or Leakage current will be discussed as well.

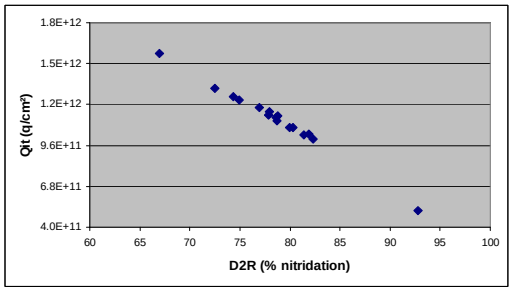

FIGURE 1.
Correlation between Interface trapped charge and % of nitridation (D2R)

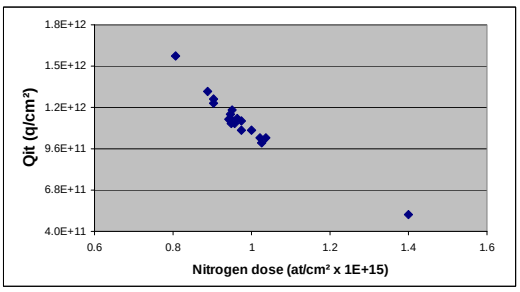

FIGURE 2.
Correlation between Interface trapped charge and Nitrogen dose obtained by XPS

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Keywords: Nitrogen, Interface trapped charge, Rapid Thermal Process

TU-018

Compact X-ray Tool For Critical-Dimension Metrology

Boris Yokhin[1 *], Alexander Krokhmal[1], Alexander Dikopoltsev[1], David Berman[1], Isaac Mazor[1], Byoung-Ho Lee[2], Dong-Chul Ihm[2] and Kwang Hoon Kim[2]

[1]*Jordan Valley Semiconductors Ltd., Ramat Gabriel Ind. Zone, Migdal Haemek, Israel, 23100*
[2]*Samsung Electronics, San#16 Banwol-dong, Hwasung-City, Gyeonggi-Do, Korea 445-701*

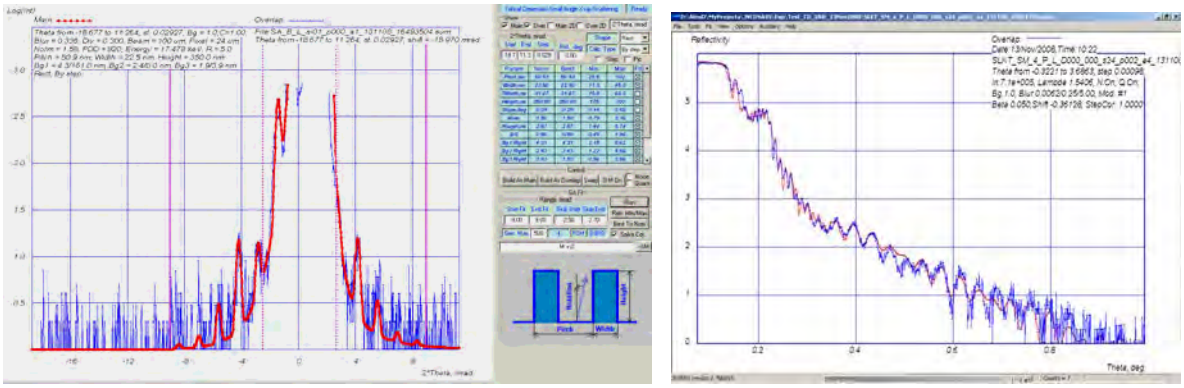
* Contact: boris@jordanvalley.com

In the era of technology nodes 32 nm and below, lithography control becomes a great challenge. Extendibility of existing methods like CD-SEM and OCD for measurements of CD profiles, overlays, and lines roughness becomes more and more limited. Small Angle X-ray Scattering (SAXS) is a possible candidate to complement and, in a longer term, to replace them. Previously reported CD-SAXS results were very promising; however as obtained using bulky sources [1] as synchrotron, they are most often restricted to research rather than production control.

We have designed a pilot set-up (XCD™) around a commonly available μ-focus X-tube, high-luminosity focusing mirror-monochromator and pixilated detector, having in mind that after further optimization of the components, the tool will have a suitable footprint and acceptable throughput. The system operates on MoKα (17.4 keV) beam shining through the wafer, from below. The measurement spot size is 100 μ. The angular resolution allows to measure structures with a pitch 100 nm and below. A software package was developed to simulate and process XCD spectra, taking into account all the components contributing to the instrumental function of the system. A special technique was developed for alignment [2].

For the purpose of the feasibility study a special CD structure was prepared. It consists of Si trenches with 50 nm pitch. It was found that in a relatively short time, pitch and width can be extracted with a precision on the level 1% RSD. The depth of the trenches was measured using another independent X-ray channel (fast XRR [3]) operating on the CuKα line (8 keV) at the grazing angle, striking normally to the trenches direction.

In the paper we will present quantitative data obtained on the pilot unit, and the projected performance of the future tool.



XCD and XRR spectra obtained from the Si comb-like structure 50 nm pitch.

Keywords: Critical Dimension, X-ray metrology, XCD, CD-SAXS, XRR.

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TU-019

Porous SiOCH Post Plasma Damage Characterization Using Ellipsometric Porosimetry

C. Licitra[1], R. Bouyssou[2], T. Chevolleau[2], N. Rochat[1] and F. Bertin[1]

[1]*CEA, LETI, MINATEC, F38054 Grenoble, France*
[2] *LTM/CNRS (CEA, LETI, MINATEC), F38054 Grenoble, France*

Christophe LICITRA: Phone: +33 438785641, Fax: +33 438785273, christophe.licitra@cea.fr

ABSTRACT

Down-scaling of complementary metal oxide semiconductor (CMOS) devices requires the development of new materials for advanced interconnects to reduce resistance-capacitance delay. For the sub-45 nm technology node, one solution is to introduce porous ultra low-κ (ULK) dielectrics with low permittivity (κ<2.5). Since the porosity leads to an increased sensitivity of the material to cleaning, etching and ashing plasmas, new characterization techniques are needed to assess the ULK properties during its integration.

In this study, we show that ellipsometric porosimetry (EP), especially with water as solvent, can be successfully used to characterize porous SiOCH with different post etching plasma treatments, using reducing and oxidizing chemistries (NH_3, H_2, CH_4 or O_2). Based on spectroscopic ellipsometry measurements, ellipsometric porosimetry consists of the calculation of the optical index of the porous material while a solvent is filling the pores. Therefore, several parameters can be deduced from the measurement, such as the mean pore radius, the pore size distribution and the open porosity [1, 2].

Blanket wafers with porous SiOCH films deposited by PECVD were used for this work (BD2.35^{TM} from AMAT with a porosity of 28% and k=2.35). Figures 1 and 2 show, respectively, the adsorption and desorption curves of different solvents before and after a NH_3 plasma treatment. We observe that the treatment is damaging the SiOCH layer, leading to moisture uptake and a slow down of the methanol adsorption and desorption. In contrast to methanol, toluene (a bigger molecule) is no longer adsorbed due to the modified surface layer that acts as a barrier. The characterization of the damaged layer of the porous SiOCH will be presented and discussed in terms of thickness, pore sealing efficiency, hydrophobicity (EP and water contact angle) and k value. In addition, infrared spectroscopy (FTIR and MIR) will be used to quantify both the methyl (Si-CH_3) depletion and moisture uptake. Finally the barrier effect will be quantified by studying the solvent penetration kinetics.

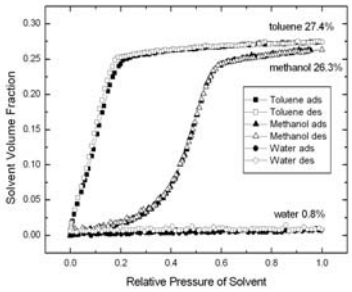

FIGURE 1. Isotherms of a non modified SiOCH

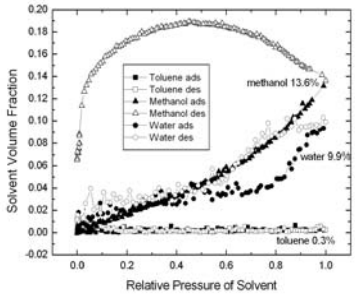

FIGURE 2. Isotherms of a plasma (NH_3) modified SiOCH

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TU-020

EBSD Analysis of Narrow Damascene Copper Lines

Roy H. Geiss[1], David T. Read[1], Glenn B. Alers[2], and Rebekah L. Graham[2]

[1]*Materials Reliability Division, National Institute of Standards and Technology, Boulder CO 80305*
[2]*Physics Department, University of California at Santa Cruz, Santa Cruz CA 95064*

ABSTRACT

Electron back scatter diffraction (EBSD) has been used to examine crystallographic orientation and grain size of damascene Cu lines 25 to 50 nm in width [1, 2]. Electron-beam lithography with a dual hard mask was used to pattern trenches in TEOS-SiO_2. Ta and Ti barrier layers were used with electrodeposition of Cu to produce lines with overburden thicknesses of 120, 240, and 480 nm. The overburden was removed by chemical-mechanical processing (CMP), followed by cleaning for 20 minutes in hydrogen plasma at 200˚C, to form the damascene lines. EBSD operated at 20 kV with 8x8 binning at > 10 frames per second, fps, sometimes produced an excessive number of unindexable pixels; 4x4 binning, at ~ 3 fps, provided more robust acquisition of crystallographic texture and grain size in the lines. The lines generally had the bamboo structure, with one grain filling the whole line width. The distribution of grain lengths along individual lines had a large standard deviation. The thickness of the overburden was clearly correlated with the crystallographic structure of the lines, for both Ta and Ti barrier layers, independent of line width. For the 120 nm overburden, the grain structure of the overburden, visible in extended areas of Cu at the ends of arrays of lines, Fig. 1a, was continued into the lines. As a result, the grains in lines with 120 nm overburden were longer than in those with the thicker overburdens, Fig. 1b; for overburdens of 240 and 480 nm, the average grain length was independent of line width. The texture in the plane normal direction, ND, in the overburden is dominantly <111>, while that of the lines varies from <001> to <111>, with almost no <110>.

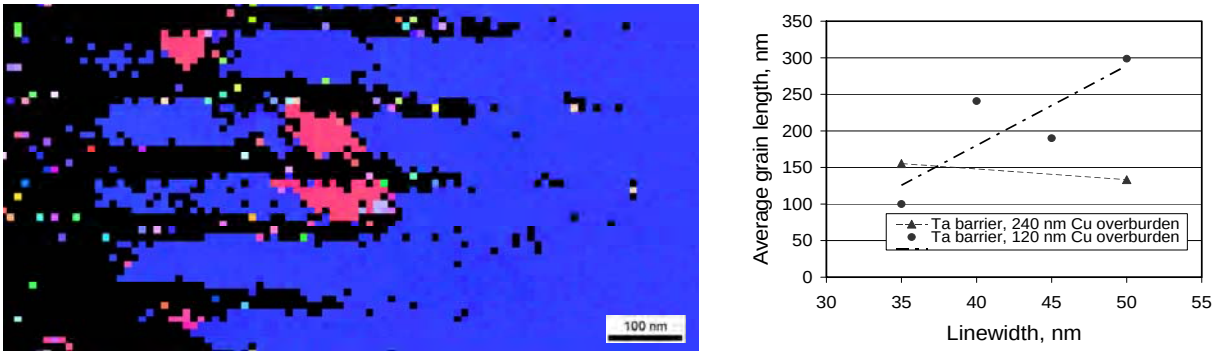

FIGURE 1. a) EBSD data for lines and overburden showing the continuation of the structure of the overburden into the lines, for the Ti barrier, 120 nm overburden, and 35 nm lines; blue color represents <111> ND; b) plot of grain length against line width, for two overburden thicknesses with Ta barrier layers, showing the different behavior of grain size in the lines made with 120 and 240 nm overburdens.

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Keywords: grain, microstructure, texture

TU-021

Characterization of Electrodeposited Copper Films with Time-of-Flight SIMS

H. Demers[1], E. Lifshin[1] and A. C. West[2]

1 College of Nanoscale Science and Engineering, University at Albany, Albany, NY
2 Department of Chemical Engineering, Columbia University, New York, NY

ABSTRACT

This paper summarizes recent experimental results that address concerns about the difficulty in achieving desired grain structure for optimal copper interconnect line resistivity and reliability. Comparison of electrodeposited copper blanket films with a medium current density (10 mA/cm^2) and a high current density (30 mA/cm^2) shows that bigger grains are obtained with a higher current density. Time-of-Flight SIMS quantitative analysis shows that chlorine and sulfur incorporation concentration into copper decrease with a higher current density. These results relate the observed grain size variation with the electrodeposition current density with the impurities concentration.

Figure 1 shows the effect of current density variation on impurity concentration during the electrodeposition. The chlorine and sulfur concentration are obtained by quantitative analysis with a Time-of-Flight SIMS (ToF-SIMS) instrument. The impurities incorporation rate depends on the overpotential, which is modified by the change of the current density. The ToF-SIMS results show a decrease of the impurities concentration when the current density increases (medium to high current). Impurity concentration increase is observed when the current density is decreased (high to medium current). But the explanation of the sharp increase is not known. Further experiments are planned to elucidate possible mechanisms.

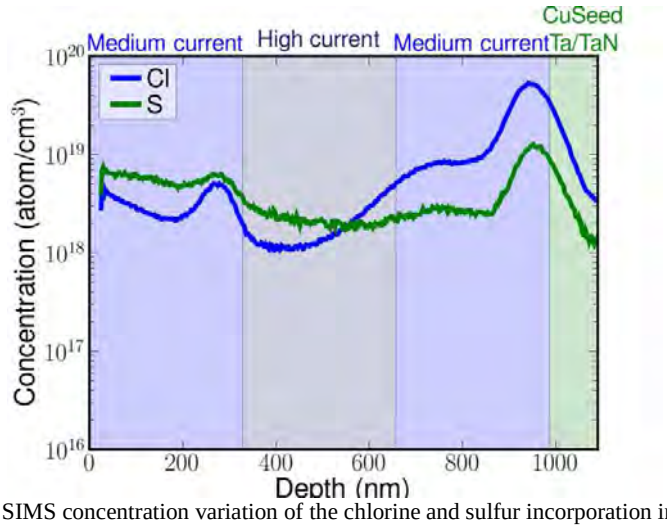

FIGURE 1. Time-of-Flight SIMS concentration variation of the chlorine and sulfur incorporation in electrodeposited copper film with change in the current density during the electrodeposition.

This research is supported by the Semiconductor Research Corporation's Global Research Collaboration under the New York Center for Advanced Interconnect Science & Technology (NY-CAIST) Task 1292.046.

Key words: Time-of-Flight SIMS, Copper interconnect, Electrodeposition.

TU-022

Analysis and Metrology with Back Scattered Helium

Sybren Sijbrandij, John Notte, Colin Sanford

Carl Zeiss SMT, One Corporation Way, Peabody, MA 01960, USA

ABSTRACT

The ORION™ helium ion microscope has recently demonstrated high resolution images with several valuable advantages over the standard SEM and gallium FIB. A focused probe size of 0.30 nm has been attained - the direct result of reduced diffraction and chromatic aberrations compared to the SEM. The images provide surface specific information which is the direct result of the secondary electrons being generated primarily from the incident beam, and not the backscattered beam. The images offer contrast mechanisms that are distinctly different from SEM images because the helium ions interact with matter in a distinctly different manner. Aside from generating images, the helium ions offer several opportunities for quantitative analysis. One method of analysis is based upon the simultaneous measurement of the scatter angle and the scatter energy of the backscattered helium.

Recently, an innovative backscattered helium detector has been constructed to complement the imaging capabilities of the ORION™ helium ion microscope. The detector subtends an angle of 0.024 steradians and measures the energy of both the ionized and the neutral helium atoms. In some metrology applications the thickness of a film (of known elemental composition) can be determined from the energy spectrum. In other applications, where there is a thicker layer, the energy spectrum can be used to determine elemental composition. Figure 1 shows the energy spectrum for three different materials in this device cross section. The smallest analyzable region can be significantly smaller than that of a SEM equipped with an X-Ray spectrometer.

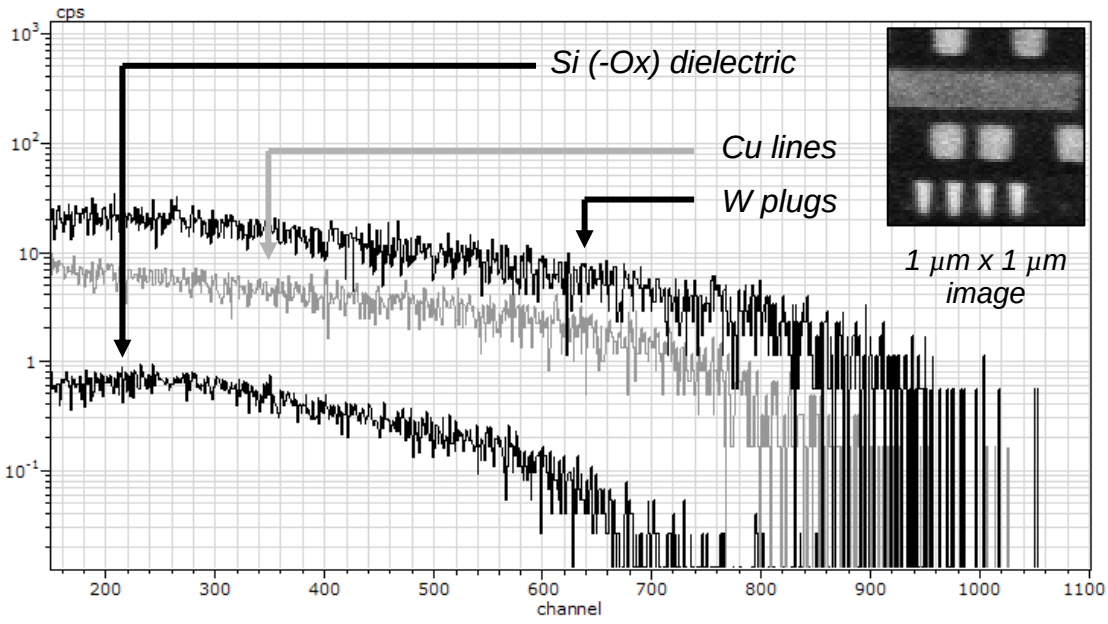

FIGURE 1. Energy spectra of the backscattered helium are distinctly different for tungsten, copper, and SiOx.

TU-023

Scanning Acoustic Microscopy of 3D-Interconnect

LayWai Kong[1]
A. Rudack[2] and S. Arkalgud[2]
A.C. Diebold[1]
[1] College of Nanoscale Science and Engineering, University at Albany, Albany, N.Y. 12203
[2] International SEMATECH, Albany, N.Y. 12203

The College of Nanoscale Science and Engineering at the University at Albany in collaboration with International SEMATECH is investigating the use of Scanning Acoustic Microscope (SAM) for 3D Interconnect. SAM is a non-destructive metrology technique which utilizes high frequency ultrasound to generate a microscopic image of the internal parts of a specimen. The goal of this project is develop microscopies for evaluating Through-Silicon Vias (TSVs) for 3D-Interconnects. Preliminary data shows voids and other defects in the interface between bonded wafers as shown in Figure 1.. Our SAM laboratory system operates at 300 MHz and has a spatial resolution of 6µm and sampling depth of 23µm on silicon wafer. The spatial resolution and sampling depth depend on the ultrasonic frequency, sound velocity, focal length and diameter of piezoelectric crystal. Typically, the silicon wafers have a thickness of 775µm before they are bonded. Our initial work is focused on unpatterned wafers in order to develop the bonding process. The next step is bond wafers with test die where the patterning obscures the interface. This paper will discuss the limitations of SAM and compare it to infrared microscopy which is another important imaging capability for 3D Interconnect. WE also discuss the status of research into more advanced acoustic microscopy methods and how this will impact 3D Interconnect imaging.

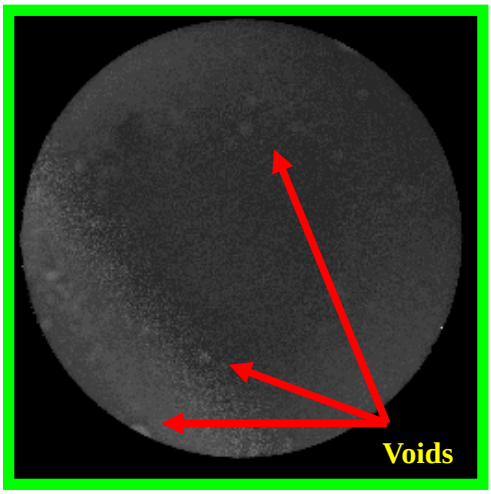

Figure 1: Scanning Acoustic Microscopy Image of Bonded Silicon Wafers.

TU-024

Abstract Withdrawn

TU-025

A Critical Comparison of X-ray Scattering Methods for Porosity Metrology of Low-*k* Thin Films

C.M. Settens[1], R.J. Matyi[1], V.K. Kamineni[1], A.C. Diebold[1], G.A. Antonelli[2] and A. Grill[3]

[1]*College of Nanoscale Science and Engineering, SUNY – University at Albany, Albany, NY 12203*
[2]*Novellus Systems, Inc., Tualatin, OR 97062*
[3]*IBM, T.J. Watson Research Center, Yorktown Heights, NY 10598*

ABSTRACT

Successful fabrication of future generations of integrated circuits demands materials with lower dielectric constant *k* values in order to decrease cross talk and RC delay. Introducing pores into a material effectively reduces dielectric constant but also decreases mechanical strength. X-ray scattering is a non-destructive analytical technique capable of detecting electron density fluctuations probing mesoporous and nanoporous structures; x-ray methods have the potential to provide fully quantitative porosity analyses including pore interconnectivity [1-4]. Specular x-ray reflectometry (XRR) is an established technique that offers accurate calculation of thickness, density, and roughness of the thin film. Two diffuse scattering techniques – offset specular (θ/2θ) XRR and grazing incidence small angle x-ray scattering (GISAXS) – have been implemented to provide insight into the pore size and pore size distribution of the low-*k* films. Both methods utilize a grazing-incidence geometry, where the effects of refraction and reflection from the surface and buried interface are corrected via the distorted wave Born Approximation (DWBA). However, offset specular XRR and GISAXS do have fundamental differences in scattering geometry that may bias interpretations of pore size measurements. Our preliminary results for pore size and pore size distribution of PECVD prepared SiCOH thin films show good agreement between the two diffuse scattering techniques.

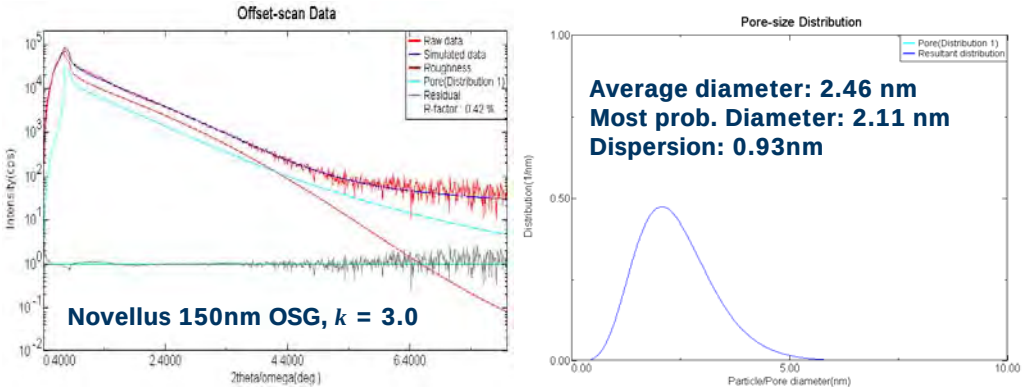

FIGURE 1. Offset specular XRR scans and the resultant pore-size distribution from p-SiCOH (*k* = 3.0)

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TU-026

Spectroscopic Ellipsometry of Porous Low-κ Dielectric Thin Films

Vimal Kamineni[1], Alfred Grill[2], A. Antonelli[3], Charles Settens[1], Richard Matyi[1], Alain Diebold[1]

[1]*College of Nanoscale Science and Engineering, University at Albany, Albany, New York – 12203.*
[2]*IBM T. J Watson Research Center, Yorktown Heights, New York – 10598.*
[3]*Novellus, Tualatin, Oregon - 97062*

ABSTRACT

Low-κ dielectric films are replacing the insulating SiO_2 dielectric material to reduce charge buildup, power consumption, crosstalk, and signal propagation delays in semiconductor manufacturing. Porous SiCOH films prepared from diverse deposition processes are the prime candidates of low-κ dielectric thin films.[1] Variable Angle Spectroscopic Ellipsometry (VASE) measurements in both IR & VUV range of wavelengths were used to measure the thickness, pore volume fraction, gradation in the total pore volume fraction and chemical bonding of porous low-κ SiCOH films. Generalized oscillator models were used to model the thickness of the thin films and Bruggeman's Effective Medium Approximation was used to calculate the total pore volume fraction.[2] Absorption coefficients in the IR wavelength were used to characterize the chemical bonding in the SiCOH films. These Spectroscopic Ellipsometry measurement techniques will be used to compliment and accelerate X-ray Reflectivity (XRR) measurements.

Keywords: Low-κ dielectrics, Ellipsometry, Thin-films and Porosity.

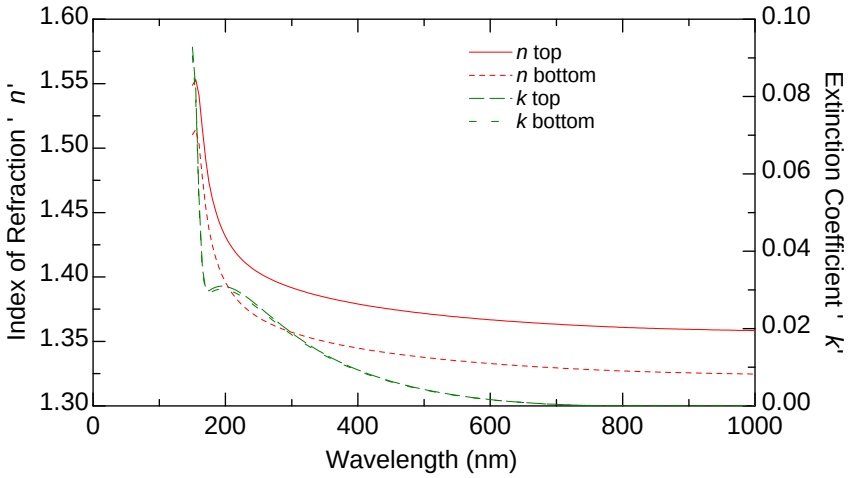

FIGURE 1. Real and Imaginary part of the complex Index of Refraction for an optically graded porous SiCOH film.

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TU-027

Electron Transport Metrology: Ballistic Electron Emission Microscopy Studies of Hot Electron Scattering in Copper

J. J. Garramone, J. R. Abel, I. L. Sitnitsky, L. Zhao*, I. Appelbaum*, and V. P. LaBella

College of Nanoscale Science and Engineering,
University at Albany, SUNY, Albany, New York 12203, USA
** Department of Electrical and Computer Engineering,*
University of Delaware, Newark, Delaware 19716, USA

ABSTRACT

Cu is a widely used metal for electrical interconnects within integrated circuits and recently as a base layer for hot electron spin injection and readout into silicon[1]. In this study we measure the hot electron attenuation length of Cu by means of ballistic electron emission microscopy (BEEM) on Cu/Si(001) Schottky diodes. BEEM is a three terminal scanning tunneling microscopy (STM) based technique, where electrons tunnel from a STM tip into the grounded metal base of a Schottky diode[2]. BEEM has been demonstrated to be a useful metrology tool for measuring attenuation lengths in various metals, but surprisingly not for Cu[3]. A Schottky height of 0.67 ± 0.02 eV was measured with BEEM, in good agreement with previous current-voltage measurements[4]. The measured hot-electron attenuation length of Cu is 37.5 ± 1.2 nm at a tip bias of 0.9 eV and a temperature of 80 K. Both the Schottky height and hot electron attenuation length measurements can be seen in Fig. 1. The attenuation length decreases with increasing tip bias and is in good agreement with electron-electron scattering as derived from Fermi liquid theory, with the addition of an elastic scattering term that is independent of tip bias. This provides insight into sources of both elastic and inelastic scattering of electrons in Cu.

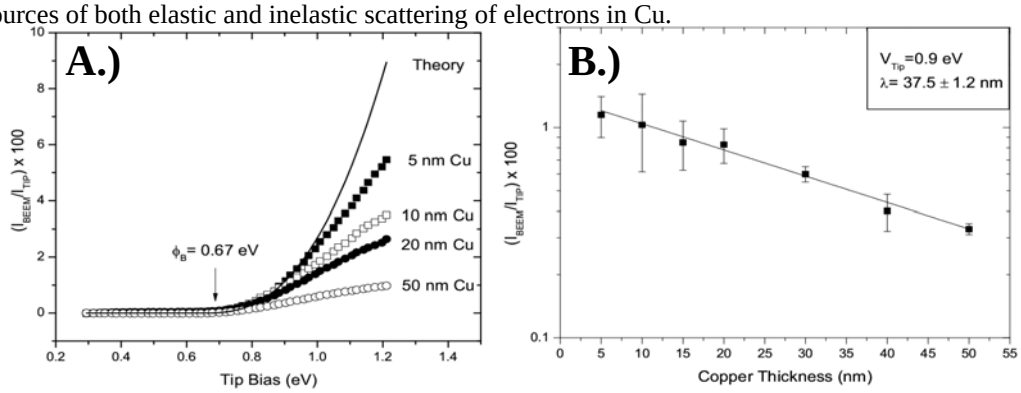

FIGURE 1. A.) Multiple BEEM spectra obtained from a Cu/Si(001) Schottky Diode with a tunneling current of 1.0 nA and Cu thickness as indicated. The average Schottky height was found to occur at 0.67 ± 0.02 eV. The line represents a fit to the 5 nm sample using $I_{BEEM}/I_{Tip} \alpha (V_{Tip} - \varphi_B)^{5/2}$. B.) Normalized BEEM current as a function of Cu thickness for a tip bias of 0.9 eV. The hot electron attenuation length was determined to be 37.5 ± 1.2 nm.

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Keywords: Copper, Electron Transport, Attenuation Length

TU-028

Controlled Oxidation of Silicon Nanowires

S. Krylyuk, A. Davydov, I. Levin, A. Motayed, M. D. Vaudin

Material Science and Engineering Laboratory, National Institute of Standards and Technology, Gaithersburg, Maryland 20899, USA; Tel. (301) 975-5600; Fax (301) 975-4553; E-mail: sergiy.krylyuk@nist.gov

ABSTRACT

Great interest in silicon nanowires (SiNWs) as building blocks of novel nanodevices is caused, in particular, by their high compatibility with the modern CMOS technology. A vast volume of knowledge accumulated on processing, characterization and measurements on thin-film silicon device structures can be transferred to SiNW structures to facilitate their integration into functional nanodevices. However, the utilization of processing and measurement methods to SiNW structures remains poorly accommodated.

This paper reports on metrological aspects of Rapid Thermal Oxidation (RTO) of SiNWs. Nanowires used for oxidation were grown by vapor-liquid-solid method utilizing gold catalytic particles; nanowire dimensions ranged from 10 nm to 30 nm in radius and 20 μm to 30 μm in length. RTO was used to form the SiNW-core/oxide-shell structures, as a first step towards realization of novel top- and wrap-gated field-effect nano-transistors. For such devices, an accurate control over the oxide shell thickness is critical. Oxidation kinetics of SiNWs was studied at 900 ºC and 1000 ºC in dry oxygen for exposure times ranging from 1 min to 7.5 min. Oxide thicknesses as measured by TEM ranged from 3 nm to 33 nm depending on processing conditions. We found that RTO of SiNWs in dry oxygen at these temperatures is notably different from conventional furnace oxidation[1,2]. For example, RTO exhibits much weaker dependence of oxide thickness on the initial radius of SiNWs; it also eliminates oxide growth retardation with respect to planar Si (Fig. 1). These features are beneficial for well-controlled oxidation of SiNWs for the device structures. The effect of combination of RTO and rapid thermal annealing (RTA) on the oxidation kinetics and characteristics of top-gated SiNWFETs will also be presented.

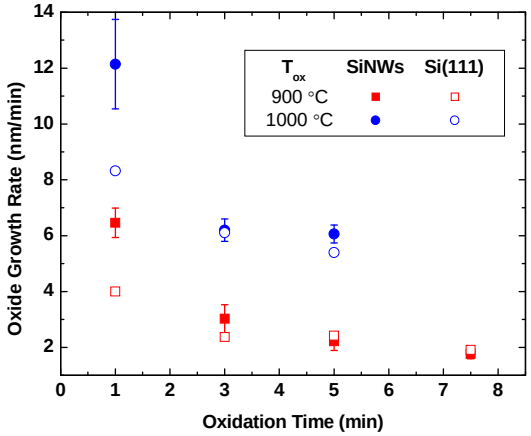

FIGURE 1. Average oxide growth rate for SiNWs and planar Si(111) vs. oxidation time for 900 ºC and 1000 ºC.

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Keywords: Silicon nanowires; Rapid Thermal Processing; Oxidation Kinetics

TU-029

Gate Stack Interfaces in Post-Si Nanoelectronics

Tian Feng, Hang Dong Lee, Lyudmila Goncharova, Sylvie Rangan, Eric Bersch, Ozgur Celik, Chien-Lan Hsueh, Alan Wan, Lei Yu, Len Feldman, Torgny Gustafsson, Robert Bartynski, and Eric Garfunkel

Departments of Chemistry and Physics,
Laboratory for Surface Modification, and
Institute for Advanced Materials Devices and Nanotechnology
Rutgers University, Piscataway, New Jersey, 08854

We present results of the composition and electronic structure of interfaces critical for future nanoelectronic devices, focusing on novel metal electrodes, high-K dielectrics, and high mobility semiconductors (e.g. TiN/HfO_2/Ge). We show high resolution compositional profiling results from ion scattering and other methods, discussing reactivity and interdiffusion between layers. We review recent results on Ge and III-V substrates, focusing on chemical passivation and defects. In one set of studies, we use isotopic labeling methods to demonstrate how oxygen reacts and diffuses within films, as oxygen stoichiometry is critical to understanding device defects. Other work concentrates on metal and semiconductor stability as they interact with ALD grown high-K dielectrics. We then present results of the electronic structure, including energy band alignment, at individual interfaces in these structures. The band alignment across metal/high-K/semiconductor stacks is controlled to some extent by the strength and nature of the interaction between the dielectric and the metal. Proper passivation is also critical to avoid Fermi level pinning in these systems. Finally, the interplay between interface chemistry and nanoelectronic device properties is elucidated.

National Science Foundation and Semiconductor Research Corporation support are gratefully acknowledged.

TU-030

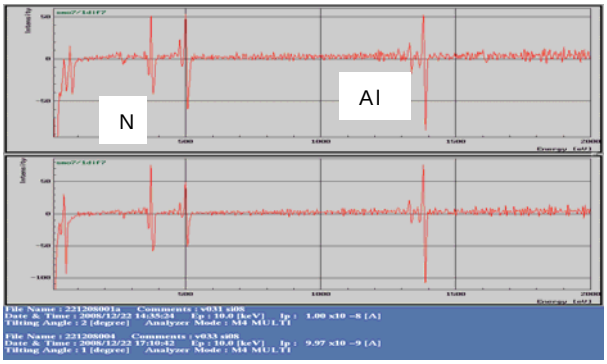
Surface, Sub-surface and Interface Characterization and Analysis of semiconductor nanofilms

R. GOPAL Krishnan

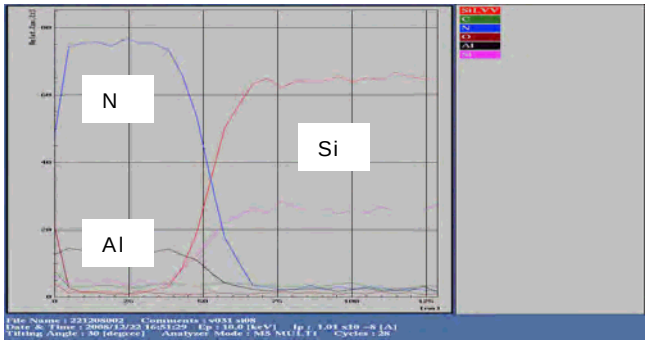
A*STAR Institute of Microelectronics, Agency for Science, Technology and Research,
11 Science Park Road, Science Park II, Singapore - 117685.

Advanced analytical and test support play an indispensable and significant role in variation management. The variations can be from materials property , process development &monitoring, and product performance. The growth, charcterization and optimization of MBE-assisted GaN and MOCVD-assisted Cd/MgZnO thin film properties from chemical composition perspective are presented and discussed through the application of FEAUGER spectroscopy, TOF-SIMS and FIB-assisted transmission electron microscopy.

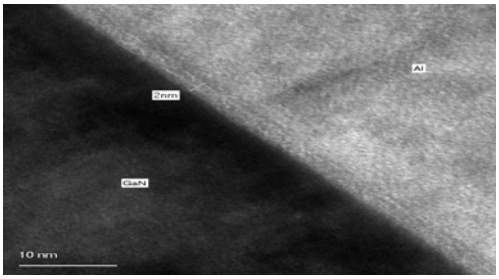
Keywords: MBE/MOCVD Growth, GaN/AlN/Si interface, FIB/TEM and FEAUGER/TOF-SIMS



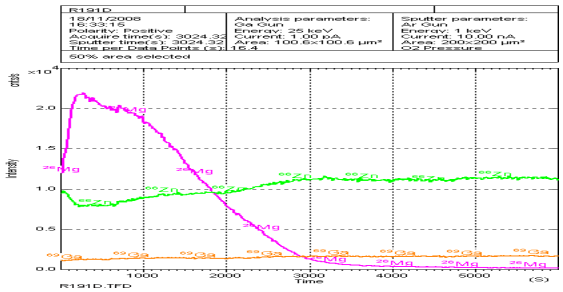
FEAUGER spectra of AlN at two MBE process



Three Dimensional variation of key elements of AlN/Si interface by FEAUGER spectroscopy



FIB assisted TEM Micrograph of a typical GaN/Al interface



TOF-SIMS Depth profile of MOCVD-assisted MgZnO thin film

TU-031

Atomic Force Microscopy Measures Single Electron Charges on Quantum Dots in Ambient Conditions

R. Olac-vaw[1], N. Guz[2], M. Dokukin[2], V. Mitin[1], and I. Sokolov[2,*]

[1]*Dept. of Electrical Engineering, University of Buffalo, The State University of New York*
332D Bonner Hall, Buffalo, NY 14260-1920
[2]*Dept. of Physics, Clarkson University, Potsdam, NY 13699-5820*
**contact email: isokolov@clarkson.edu*

ABSTRACT

Here we describe a method to measure electrical charges accumulated on cadmium selenide (CdSe) quantum dots with the help of Atomic Force Microscopy (AFM). The sensitivity of the method allows detecting charges up to the single electron value even in ambient conditions. Quantum dots capped with tri-n-octylphosphine oxide (TOPO) were charged by using photon excitation with green laser and the action of a conductive AFM probe. After the charging, the AFM was switched to the Lift mode with AC (resonance oscillating) scanning while using multiple lift heights [1]. This allows measuring the shift of the resonance frequency which is proportional to the gradient of force acting between the AFM probe and individual dots. This force occurs due to induction of the mirror charge in the conducting volume of the AFM probe. Simple electrostatic model is used here to find the value of the charge on the dot.

Using the presented method, we are able to measure single electron charges on the quantum dots dispersed from toluene solution onto graphite film (graphene). Fig.1 shows the results of measurements for a number of quantum dots, the resonance frequency shift as a function of the probe-dot distance. Solid lines show theoretical dependences corresponding to one and two electron charges.

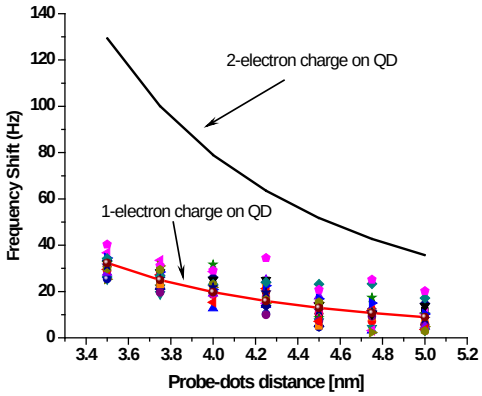


FIGURE 1. Measurements of the charges on quantum dots and comparison with theory.

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Key words: single electron charge; quantum dots; atomic force microscopy.

TU-032

Thermal Conductivity And Thermal Rectification In Graphene Nanoribbons: A Molecular Dynamics Study

Jiuning Hu[1], Xiulin Ruan[2], Zhigang Jiang[3] and Yong P. Chen[4]

[1]*School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA*
[2]*School of Mechanical Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA*
[3]*School of physics, Georgia Institute of Technology, Atlanta, Georgia 30332, USA*
[4]*Department of physics, School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA*

ABSTRACT

We have used molecular dynamics based on the Brenner potential[1] to calculate the thermal conductivity of symmetrical and asymmetrical graphene nanoribbons. For symmetrical nanoribbons, the calculated thermal conductivity is on the similar order of magnitude of the experimentally measured value for graphene. We have investigated the effects of edge chirality and found that nanoribbons with zigzag edges have considerable larger thermal conductivity than that of nanoribbons with armchair edges (FIGURE 1(a)). We also studied the effects of defects and found that vacancies in the ribbons can significantly decrease the thermal conductivity. For asymmetric nanoribbons, we have found considerable thermal rectification (FIGURE 1(b)). For example, for a 6nm-long triangular shaped nanoribbon, the thermal conductivity from the wider end to the narrower end is nearly 2.3 times that from the narrower to the wider end. Furthermore, the thermal rectification is robust for rough edges and can be further enhanced by increasing the size of the asymmetrical nanoribbon. Such rectification effects can be potentially useful in nanoscale thermal management or information processing using heat.

Keywords: molecular dynamics, graphene nanoribbons, thermal conductivity and thermal rectification.

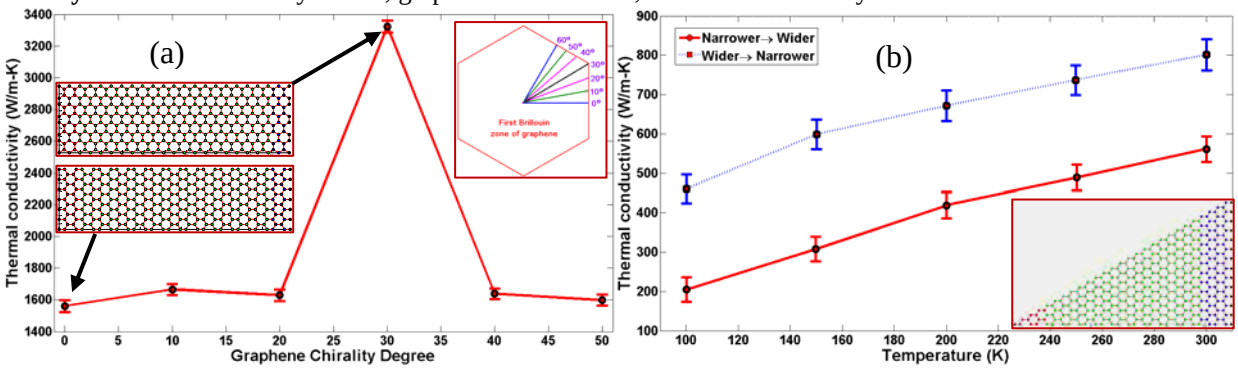

FIGURE 1. (a) Thermal conductivity in symmetrical graphene nanoribbon with different edge chirality (left two insets show ribbons with armchair (bottom) and zigzag (top) edges and right inset is the definition of the chirality degree in the first Brillouin zone of graphene) and (b) thermal rectification in an asymmetrical graphene nanoribbon.

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TU-033

Raman-Based Graphene Thickness And Defect Metrology

G. Rao, S. McTaggart, J. U. Lee, and R. E. Geer[1]

College of Nanoscale Science and Engineering, University at Albany, SUNY, Albany, NY 12203

ABSTRACT

Nanoscale metrology (thickness, defectivity) of graphene-based devices is a substantial challenge due to the difficulty of probing the atomic structure of single graphene sheets and subsequent correlation to electron transport and device performance. Distinguishing the number of graphene layers for a particular test structure as well as quantifying the impact of disorder in single and n-layer graphene is critical for the study graphene based devices. Raman spectroscopy has proved to be an appropriate approach in both regards. For AB stacked n-layer graphene exfoliates the Raman 2D peak profile is a highly reliable approach for distinguishing the number of layers. In addition, the graphene Raman G, D, and 2D bands enable comparative determination of linear defect density and electron-phonon coupling[2].

We have successfully established micro-Raman thickness metrology protocols with for ZYH exfoliate n-layer graphene, ZYA exfoliate n-layer graphene and CVD graphene samples (monolayer, bilayer, and trilayer) based on the Raman 2D peak signatures. For the exfoliate graphene samples the thickness evolution in the Raman 2D peak signature agrees with attribution of the 2D peak profile to double resonance Raman scattering (DRRS). We also have performed initial analysis for evolution of defects in ZYH and ZYA n-layer graphene exfoliates created by electron beam irradiation with controlled dose. The dose of irradiation was varied continuous and sequentially for multiple sets of monolayer and bilayer exfoliates. Raman analysis of irradiated graphene samples show increase in linear defect density (I_D/I_G ratio) with increase in irradiation dose, however the linear defect density is substantially larger in monolayer graphene samples as compared to Bernal bilayer graphene samples (Fig 1a). Also, increased defect density due to electron radiation results in variations to the G-band line-width associated with increased electron-phonon coupling (broadening) or self-doping (narrowing)[3,4]. Surprisingly, the defect-induced increase in electron-phonon coupling appears more dramatic in bilayer versus monolayer ZYH graphene samples despite the lower linear defect density of the former (Figs. 1b and 1c) although induced defects do not alter the registry of these flakes. Initial theoretical analysis based on density functional theory (DFT) and STM analysis will be presented.

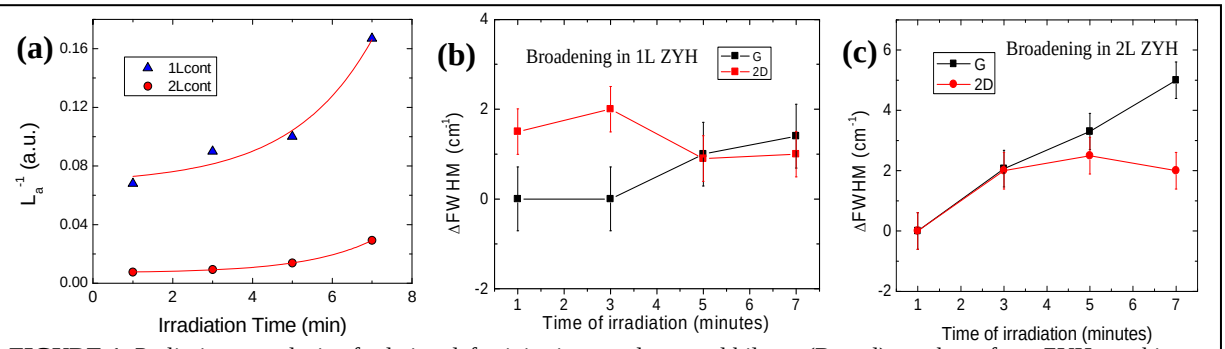

FIGURE 1. Preliminary analysis of relative defectivity in monolayer and bilayer (Bernal) graphene from ZYH graphite. (a) Average linear defect density in monolayer and bilayer graphene versus electron irradiation time. (b) Raman peak broadening in G-band and 2D-band for 1L graphene. (c) Raman broadening in G-band and 2D-band for 2L graphene.

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TU-034

New Methods for Nanoscale Characterization and Functionalization of Templated Ge(Si) Quantum Dot Arrays

J. Thorp*, J.F. Graham* and R. Hull*+

** University of Virginia, Dept. of Materials Sci. and Eng., 116 Engineers Way, Charlottesville, VA 22904*
** Rensselaer Polytechnic Institute, Dept. of Materials Sci. and Eng., 110 8th Street, Troy, NY 12180*

ABSTRACT

We have previously developed methods for templated growth of Ge(Si) nanostructures that enable nanoscale precision in the assembly of epitaxial Ge quantum dot (QD) arrays on Si(100) surfaces. This is achieved by pre-growth templating of the Si substrate by low dose (~10^{14} cm^{-2}) Ga^+ focused ion beam (FIB) implants prior to quantum dot growth. In this work, we present new data on the evolution of patterned Si(100) surface structure and deposition of Ge QDs using in-situ imaging methods in a low energy electron microscope (LEEM). This instrument enables real time imaging of these processes at acquisition rates << 1 s, lateral spatial resolution c. 5 nm, and monolayer vertical resolution. Figure 1 shows the surface structure of a Si(100) surface that has been patterned with a Si focused ion beam, demonstrating a regular array of flat terraces between the FIB features, believed to form because the FIB features serve as efficient sinks for steps. This observed surface structure will be expected to substantially influence subsequent Ge growth, because adatom diffusion to nucleation sites at the FIB features will be correspondingly more rapid as surface step barriers do not need to be overcome.

Coupled with these LEEM experiments, we are developing methods for generating a broad range of FIB species to allow more controlled chemistries for FIB substrate templating, and also allow direct nanoscale electronic and magnetic doping of individual QDs. The vast majority of FIBs currently in use worldwide use Ga^+ liquid metal ion sources (LMIS), as we have in our previous work, due to the combination of low vapor pressure at the melting point, chemical inertness with respect to the liquid metal support, and electrical conductivity necessary to form a Taylor cone for field ionization. Only a few metallic elements fulfill these criteria, with Ga^+ being almost ubiquitously employed because, additionally, of its low melting temperature. For assembly and functionalization of potential QD- based nanoelectronic devices, we wish to create nanoscale beams of Si and Ge for non-electronically invasive templating, and p-, n- and spin dopants (e.g. B, As, Mn) for electronic / magnetic functionalization. We have created nanoscale beams of all these species using an ion column equipped with a mass-selecting filter, thereby enabling separation of beams from alloy LMIS (e.g. Si from AuSi, Mn and Ge from MnGe and As and B from PdAsB). These capabilities are of great relevance to the LEEM experiments described above, where the use of a Si beam separates chemical effects from the surface evolution and QD templating processes. We are also demonstrating the ability to target individual quantum dots with doping beams, as illustrated in Figure 2.

This work performed in collaboration with C. Kell, C. Nolph, P. Reinke and J. Floro (UVa), and F. Ross and R. Tromp (IBM).

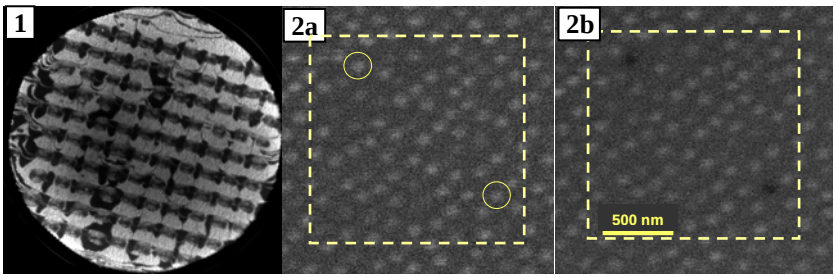

Figure 1 (Left). LEEM dark field image using dimer reflection of a Si(100) surface patterned with a Si focused ion beam. 5 µm field of view. **Figure 2** (Center, Right) In-situ secondary electron images in our mass-selecting FIB of field of Ge QDs on a Si(100) surface before (a) and after (b) targeting of individual QDs with a 1 pA $^{11}B^+$ beam with a 0.25 s dwell (exposures can be < 1 µs).

4-1

Evolution of the Ultimate Nano-Transistor

Bruce B. Doris

IBM Research at Albany NanoTech, 257 Fuller Rd., Albany, NY 12203, USA

ABSTRACT

State-of-the-art transistors have achieved their potential through evolution rather than revolution. This evolutionary scaling process has enabled us to create high-end microprocessors for enterprise server applications with well over 1 billion transistors. For the past few decades, MOSFET scaling has followed Moore's law, which states that the number of transistors that can be placed inexpensively on an integrated circuit doubles about every two years[1]. In 1974 Bob Dennard taught us the rules to achieve the transistor density doubling[2]. Simply put, the transistor size can be reduced by a factor of 0.7X provided that channel doping increases by 0.7X, gate oxide thickness shrinks by 0.7X, and the supply voltage drops by a factor of 0.7. This prescription for scaling feature sizes worked for many years until the ability to shrink the gate dielectric, among other things, became limited.

At the 90-nm node generation conventional gate dielectric scaling came to a significant slow-down. Physical thickness of the gate dielectric was about 1.2 nm at this time and further thickness reduction resulted in excessive gate leakage and reliability issues. Thankfully, performance improvements continued in the form of mobility enhancements. Channel strain from stressed contact etch-stop layers and embedded SiGe S/D resulted in significant increases in circuit performance.[3] However, the mobility enhancement techniques did not enable gate length scaling. A hallmark of each technology is a ground rule shrink from the previous node. In particular, the distance between adjacent transistors (gate pitch) needs to shrinks typically by a factor of 0.7 to enable doubling of the transistor count. Until recently, the lack of significant gate length scaling has not posed an issue for gate pitch scaling. However, as the gate pitch scales below 100 nm, gate length scaling is needed. Introduction of high-k and metal gates has provided some relief in gate length scaling. It is also worth mentioning that not only is gate-length scaling needed but also source-drain contacts also require aggressive scaling to meet pitch targets.[4] Recently we have demonstrated the smallest SRAM cell using high-k metal gate stacks and 25 nm gate-lengths.[5] However additional gate-length scaling is needed for future technology nodes. Alternate device architectures like Extremely Thin Silicon on Insulator (ETSOI)[6] or FinFET[7] do not rely on the conventional methods to achieve gate length scaling. Next generation technology may likely feature one of these thin channel device options. Will these be the ultimate transistors? Although the basic architecture for ETSOI and FinFET is somewhat different compared to conventional transistor technology they are along the evolutionary path of standard Si CMOS.

Another important consideration in the quest for the ultimate transistor is the power – performance trade off. Simply packing more transistors on the same or smaller area does not necessarily translate into improved performance or functionality. In fact it has been illustrated that reducing parasitic capacitance and improving sub-threshold swing are also vital to next generation transistors.[8]

Beyond Si CMOS there is a great deal of excitement and activity on carbon nanotubes, grapheme, and III-V devices such as HEMTs and HBTs. Recent demonstrations of carbon nanotube ring oscillators bring hope that revolutionary solutions may be on the horizon.[9] Is one of these options the ultimate transistor? For any option to replace Si-based CMOS, it should have extraordinary transport properties. But more importantly, it should be capable of being integrated into a microprocessor with over 1 billion functional transistors, fit gate pitch well below 100-nm, and mass produced with low cost and high yield.

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Nanoscale Strain Metrology of Microelectronic Devices by Dark-Field Electron Holography

Martin Hÿtch, Florent Houdellier, Florian Hüe and Etienne Snoeck

CNRS ; CEMES ; 29 rue Jeanne Marvig, F-31055 Toulouse, France
Université de Toulouse ; UPS ; F-31055 Toulouse, France

ABSTRACT

Strain in silicon channels is now a mainstream technique in state-of-the-art CMOS technologies due to the associated increase in carrier mobilities. Different ways have been employed to engineer strain in devices leading to complex strain distributions in 2 and 3 dimensions. Without accurate methods of measuring strain at the nanoscale, however, manufacturers cannot have complete mastery of device design or of device reproducibility. Developing methods of strain measurement at the nanoscale has therefore been a major goal of recent years but has proven illusive in practice. None of the techniques combine the necessary spatial resolution, precision and field of view. For example, Raman spectroscopy or X-ray diffraction techniques can map strain at the micron scale, and transmission electron microscopy (TEM) at the nanometre scale but over relatively small areas[1].

Here we present a new technique capable of bridging this gap and measuring strain to high precision, with nanometre spatial resolution and for micron fields of view[2,3]. The method combines the advantages of the conventional moiré technique with the flexibility of off-axis electron holography and is applicable to standard focused-ion beam (FIB) prepared samples. We will present measurements of strain in the active regions of strained-silicon MOSFET devices and compare the results from finite element modelling.

Keywords: strain metrology, transmission electron microscopy, electron holography

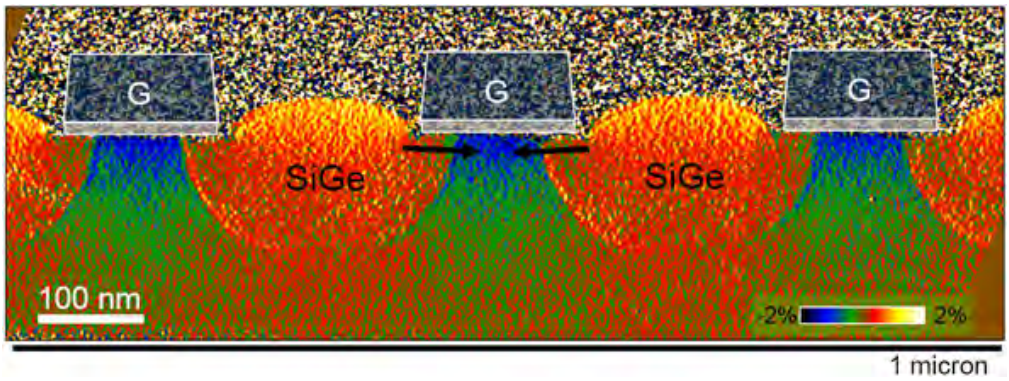

FIGURE 1. Strain map of a p-MOSFET with recessed $Si_{80}Ge_{20}$ sources and drains applying compressive strain to the channel.

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4. This work was partially supported by the European Commission through the projects PullNano (Pulling the limits of nanoCMOS electronics, IST-026828), and ESTEEM (Enabling Science and Technology through European Electron Microscopy, IP3: 0260019).

4-3

FINFET doping: Fabrication and Metrology Challenges.

W.Vandervorst [a,b]

[a]Imec, Kapeldreef 75, B-3001 Leuven, Belgium

[b]also IKS, KULeuven, Leuven Belgium

Whereas the introduction of 3D-dimensional devices such as FINFETs may be a solution for next generation technologies, they do represent significant challenges with respect to the doping strategies and the junction characterization. Aiming at a conformal doping, classical beam implants fail due to reduced incorporation efficiency depending on the impact angle and the effect of wafer rotation. Although large tilt angles at isolated devices lead to acceptable results, this solution is not appropriate for densely spaced FINs due to shadowing effects. Plasma immersion doping is an alternative approach which holds the promise of conformality. However a detailed analysis of the electrostatics shows that plasma doping suffers from similar limitations which can only be overcome by relying on secondary processes such as resputtering, deposition and in diffusion etc. Even then its implementation is compromised by concurrent artifacts, sputter erosion being the most important one. It is clear that the optimal conformality can be achieved using gas phase based processes like CVD, VDP, deposition in plasma doping etc.. In all the cases build on energetic beams, one needs to consider also the problems related to impact of amorphization and the effect of the finite volume/seed on the recrystallization.

In order to study the FINFET doping in detail we have developed various approaches towards the measurement of the 3D-dopant distribution and the identification of conformality. Metrology concepts based on 3D-Scanning Spreading Resistance Microscopy, SIMS through FINs, resistors and the Tomographic Atomprobe will be discussed in detail.

A 3D stacked nanowire technology. Applications in advanced CMOS and beyond

T. Ernst, S. Bécu, P. Cherns, L. Durrafourg, C. Dupré, P. Andreucci, A. Hubert, J.-M. Hartmann, J.-P. Colonna, M. Jublot, G. Delapierre, V. Delaye, K. Tachi, E. Saracco, J.-F. Damlencourt, J. Foucher, and O. Faynot

CEA- LETI, MINATEC, F38054 Grenoble, France, thomas.ernst@cea.fr

ABSTRACT

In this paper we will present CMOS nanowire matrices technologies recently developed by using a top down approach. Some electrical and mechanics properties as well as possible interests of the obtained nanowire structures will be discussed both for sub-22nm advanced CMOS devices and for ultimate co-integration of novel functionalities. Some specific needs for characterization and metrology will be discussed, in particular in line 3D critical dimensions measurements and out of line structural characterisation. For CMOS scaling, Silicon-On-Insulator (SOI) nanowires or innovative Silicon-On-Nothing (SON) based 3D stacked technologies are proposed with common or independent gates. Ultra-low static consumption (I_{OFF}<50pA/µm) as well as high driving current (up to I_{ON}=6.5mA/µm) are achieved thanks to 3D stacked Gate-All-Around (GAA) nanowire channels. The top-down nanowire techniques also open up new opportunities for hybridizing CMOS with novel functionalities such as 3D memories, nano-oscillators and bio nano-sensors. In particular, for ultra low mass sensing applications, a few molecule aggregates (i.e a few 10^{-21} g to 10^{-24} g) could be measured with enhanced surface capture through 3D stacking.

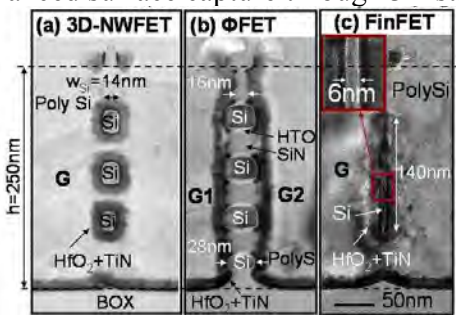

FIGURE 1. Left. Cross-sectional TEM pictures of (a) 3D-NWFET: 15nm-diameter stacked nanowires are obtained (b) ΦFET: Spacers are introduced to obtain stacked nanowires with independent gate operation (c) FinFET: a very high aspect ratio (AR) is obtained (6nm×140nm, AR=23)

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KEYWORDS: nanowires, 3 D, top-down

5-1

Overview of Carbon-Based Nanoelectronics

Ji Ung Lee
College of Nanoscale Science and Engineering, University at Albany-SUNY

The metal oxide semiconductor field-effect transistor (MOSFET) is the most ubiquitous electronic device. As transistor scaling approaches its limit, new materials that provide superior properties and greater functionality than Si based electronics are needed. Here, we provide an overview of carbon nanotube and graphene devices and describe their promise in future electronics. We provide an overview of key developments that have made the current progress possible, and examine new approaches that are being investigated that may lead to scalable fabrication techniques. Based on electronic properties extracted from transistor and diode devices, we provide fundamental material properties that show their superior characteristics. Yet, there are still unresolved fundamental electronic properties, including bandgap and mobility, and we explore metrology needs to address them. Finally, we discuss novel device concepts that transcend electronic charge as device state variable. These concepts could lead to new device architectures with greater functionality than current rigid CMOS based architectures.

5-2

Scanning Single Electron Transistor Microscopy on Graphene

Jens Martin

Department of Physics, Harvard University, Cambridge, MA 02138, USA

ABSTRACT

We use a scanning single electron transistor to measure the local inverse compressibility of graphene. Unlike STM, which probes the single-particle density of states, the inverse compressibility, addressed here, measures the many-body density of states that includes information on the exchange and correlation energies as well. We review the basic principle of scanning single electron microscopy.
For graphene at zero magnetic field and in the vicinity of the neutrality point our results confirm the existence of electron-hole puddles[1]. These puddles could explain graphene's anomalous non-zero minimal conductivity at zero average carrier density. Moreover, we find that, unlike non-relativistic particles the density of states can be quantitatively accounted for by considering non-interacting electrons and holes.
At high magnetic field we investigate the appearance of localized states[2]. Particle localization is an essential ingredient in quantum Hall physics. In conventional high mobility two-dimensional electron systems Coulomb interactions were shown to compete with disorder and to play a central role in particle localization. Surprisingly, despite the stronger disorder in graphene compared to the standard two-dimensional systems, our findings indicate that localization in graphene is also dominated by Coulomb interactions and not single particle physics.

KEYWORDS: scanning single electron transistor, graphene, electron-hole puddles

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5-3

Spin Torque Transfer Nonvolatile Devices for CMOS Integrated Circuits

Hideo Ohno

Laboratory for Nanoelectronics and Spintronics
Research Institute of Electrical Communication
Tohoku University, Sendai 980-8577, Japan

ABSTRACT

Spin torque transfer (STT) switching of magnetization direction in magnetic tunnel junctions (MTJs) showing a very large tunnel-magnetoresistance (TMR) offers a new possibility of integrating nonvolatile memory and logic for next generation CMOS integrated circuits. An MTJ consists of two metal ferromagnetic layers separated by a thin insulator through which electrons tunnel. The resistance of an MTJ depends on relative orientation of the two magnetizations of the layers, making it possible to encode information in a nonvolatile way on the direction of one of the layers (recording layer), while keeping the other layer's direction fixed. The resistance of the device is low when the magnetizations are parallel and high when antiparallel. The resistance difference divided by the low resistance is TMR. The unique features and potentials offered by the STT nonvolatile MTJs are the combination of nonvolatility, fast read and write, virtually unlimited rewrite, CMOS compatibility with back-end process, small footprint, and scalability, which does not easily be matched by other nonvolatile memory technologies. I will summarize first the physics involved in STT nonvolatile MTJs. Then I show that the combination of MTJ with CMOS [1, 2] could solve many of the major challenges, the so-called red-brick walls, current CMOS integrated circuit technology are facing. Operation of prototype MTJ/CMOS logic blocks will be presented [1]. I end my talk with discussing the remaining challenges, which include the needs for spaciotemporal metrology in understanding nanoscale magnetization dynamics, to establish the technology.

Work partly supported by the "Research and Development for Next-Generation Information Technology" program from the Ministry of Education, Culture, Sports, Science and Technology of Japan.

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5-4

Scaling Effects on Ferro-Electrics: Application in Nanoelectronics and Characterization

Bertrand VILQUIN, Brice GAUTIER and Guy HOLLINGER

Institut des Nanotechnologies de Lyon
Université de Lyon, Ecole Centrale de Lyon, INSA de Lyon, CNRS
France

ABSTRACT

Ferroelectric thin films have been attractive for multifunctional devices like nonvolatile memory (FeRAM) using hysteresis behavior, DRAM using high permittivity, micro-actuator using piezoelectricity, infrared sensor using pyroelectricity, optical switch shutter display, etc. Thin-film nanoscale device structures integrated onto Si chips have made inroads into the semiconductor industry. Recent prototype applications include ultra-fast switching, cheap room-temperature magnetic-field detectors, piezoelectric nano-tubes for micro-fluidic systems, electro-caloric coolers for computers, phased-array radar, and three-dimensional trenched capacitors for dynamic random access memories. Terabit-per-square-inch ferroelectric arrays of lead zirconate titanate have been reported on Pt nano-wire interconnects and nano-rings with 5-nanometer diameters. These applications need not only ferroelectric high quality materials but also ability to conserve the ferroelectricity at low dimension after fabrication of nano-scale objects. For these reasons, advanced characterization techniques for probing the properties of ferroelectric materials at nano-scale dimensions are now required. Among them, techniques based on the Atomic Force Microscope (AFM) have proved their efficiency for mapping the ferroelectric behaviour of thin films with a nanometric resolution : the distribution of the direction of the polarisation can be observed directly by combining the observation of the piezoelectric vibration in a direction perpendicular to the surface and in the surface. Moreover, the polarisation state can be very simply changed by applying a bias between the AFM tip and the back electrode. Ferroelectric domains can be tailored this way with a nanometric resolution, with important applications in the design of the surface acoustic waves devices (SAW). This technique may also evolve toward the measurement of the quantitative piezoelectric coefficients of the films in the direction perpendicular to the surface (d_{zz}).

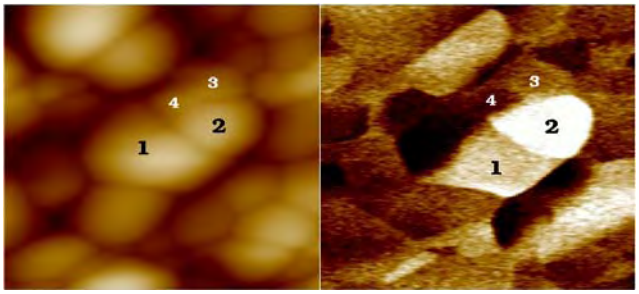

FIGURE 1. Figure 1 : AFM topography (left) and PFM cartography of the ferroelctric domains in lithium niobate (LN). The difference of contrast between domains arises from a different polarisation direction. Antisymetric domains appear with an opposit sign.

6-1

Overview of 3D Interconnect Requirements

Sitaram Arkalgud PhD
Director - Interconnect
SEMATECH
257 Fuller Road, Albany, NY 12203

The twin drivers of all advances in the semiconductor industry have been ever-increasing performance and productivity. With tremendous strides in lithography and device development over the last several decades, achieving both has been possible. However, with fundamental issues and cost concerns about new technology elements at 32nm and below (such as low-k or high-k dielectrics, metal gates, and EUV lithography), the viability of traditional lithography and device scaling to stay on the productivity curve becomes questionable. One of the technologies gaining popularity has been through-silicon vias (TSVs) for stacking chips in the third dimension. This approach promises to improve performance and permit higher density and functionality while possibly reducing costs. Several integration approaches to 3D are possible. For example, vias can be formed at the beginning, at the end, or in the middle of the process flow. In bonding, it is possible to bond metal to metal, oxide to oxide, polymer surfaces to each other, or a hybrid combination of these. In addition, face-to-face bonding, back-to-face bonding, die-to-wafer stacking, or wafer-to-wafer stacking are all possible. To move 3D TSV technology from demonstrating feasibility to high volume manufacturing, cost-effective integration schemes with demonstrated manufacturability are necessary. Consequently, appropriate metrology techniques rank high among the critical elements in manufacturing. This presentation will give an overview of 3D TSV technology and discuss the metrology requirements, taking into consideration applications, a possible timeline, and relative manufacturability.

6-2

Cross Sectional Characterization of Planar and Non-planar Nanostructures using X-ray Scattering

Chengqing Wang[1], Ronald L. Jones[1], Kwang-Woo Choi[1,2], Jimmy Price[3], Benjamin Bunday[4], Wen-li Wu[1]

[1]*Polymers Division, NIST, Gaithersburg, MD 20899-8541*
[2]*Intel Corporation, Santa Clara, CA*
[3]*International SEMATECH, Austin, TX*
[4]*International SEMATECH Manufacturing Initiative (ISMI), 255 Fuller Rd 359, Albany, NY 12203*

ABSTRACT

Critical Dimension Small Angle X-ray Scattering (CD-SAXS) is a transmission X-ray scattering technique with proven capabilities to provide sub-nm precision in dimensional measurements of planar nanostructures, e.g. line gratings with their CD at 15 nm. In line gratings we have demonstrated that line width, line height, sidewall angle, pitch as well as line edge roughness can all be measured with CD-SAXS[1, 2].

Nowadays non-planar architectures have been considered for next generation electronics and one of the representative structures is tri-gate or FinFET. Key to this device architecture is the integration of sub-5 nm thick, conformal high dielectric constant layers wrapping around the Fin. With its high aspect ratio, small dimensions, and multiple materials, FinFET presents unique challenges to current measurement methods. Here, we present data from CD-SAXS measurements of a model FinFET sample to demonstrate the capabilities and limitations of the technique. Measurements are compared quantitatively with analogous measurements performed using top-down scanning electron microscopy (SEM) and cross sectional transmission electron microscopy (X-TEM). CD-SAXS data taken from a single angle of incidence (Fig. 1) is shown to provide quantitatively information of dielectric layer thickness. Deviations in measured values with electron microscopy measurements are explained by the differences in the definition of the measured dimensions.

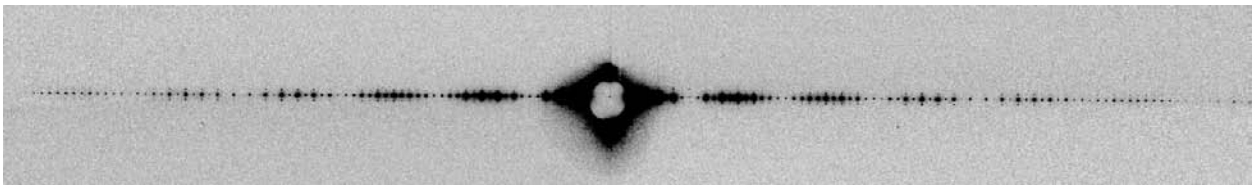

FIGURE 1. Normal incidence CD-SAXS data collected for a line/space array of a model FinFET. There are at least THREE modulation frequencies in the above scattering pattern; the repeating length is 400 nm instead of 200 nm specified in the mask design. This indicates the existence of a super structure in the test pattern.

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6-3

X-RAY MICROSCOPY FOR INTERCONNECT CHARACTERIZATION

Wenbing Yun, Michael Feser, Jeff Gelb, Andrei Tkachuk

Xradia, Inc. 5052 Commercial Circle, Concord, CA 94520

ABSTRACT

X-ray computed tomography (XCT) offers powerful non-destructive three dimensional imaging capability widely used in diverse fields, including medical diagnosis, biomedical and material research, geology, petrology, and archeology. XCT with micrometer resolution is being rapidly adopted for semiconductor packaging process development and failure analysis by creating virtual cross sections without the time consuming destructive cross sectioning processes. Thanks to rapid advance in x-ray imaging technology, XCT with 30nm and 50nm resolution (nanoXCT) has been developed using synchrotron and laboratory x-ray sources, respectively. The nanoXCT can image internal structures of semiconductor IC devices that are fabricated using the latest IC manufacturing technology. This new capability is very valuable to the characterization of semiconductor interconnects for process development and failure analysis. We will present the design, specification, and operation of the nanoXCT. 2D and 3D tomographic reconstruction images from IC devices will be presented to show the tomography microscope's outstanding performances.

7-1

Facts And Artifacts In Atom Probe Tomography

F. Vurpillot, M. Grüber, E. Cadel, R. Larde and B. Deconihout

Groupe de Physique des Matériaux UMR 6634 CNRS, Université de Rouen
Avenue de l'Université,B.P. 12 76801 Saint – Etienne du Rouvray Cedex, France
Tel : +(33) 2 32 95 51 70 ; Fax : +(33) 2 32 95 50 32 ;
Contact : francois.vurpillot@univ-rouen.fr

ABSTRACT

Recent semiconductors applications have highlighted the need for nano analyzing technique with extremely high spatial resolution and sensitivity. Since semiconductors structures change from 1D-2D structures to 3D structures, 3D capabilities is also of fundamental need. The only technique approaching these requirements is the Atom probe Tomography. Even if limitations coming from specimen preparation and sample breakage exist, the theoretical performances are incomparable. The depth resolution is for instance better than the best resolution given by the SIMS (figure). The 3D spatial resolution in pure metal approaches the lattice resolution. When good analyzing conditions are used the detection efficiency is identical for all elemental species and can approach 80% in the probed region[1]. Nevertheless the problem is that the spatial resolution is strongly dependant of the material studied[2-4]. We will show that the presence of different species in the material can reduce significantly the performances of the instrument. The presence of reconstruction artifacts can induce interpretation errors in reading 3DAP images [2-4]. Even if most of these artifacts could be corrected, a very careful attention should be addressed.

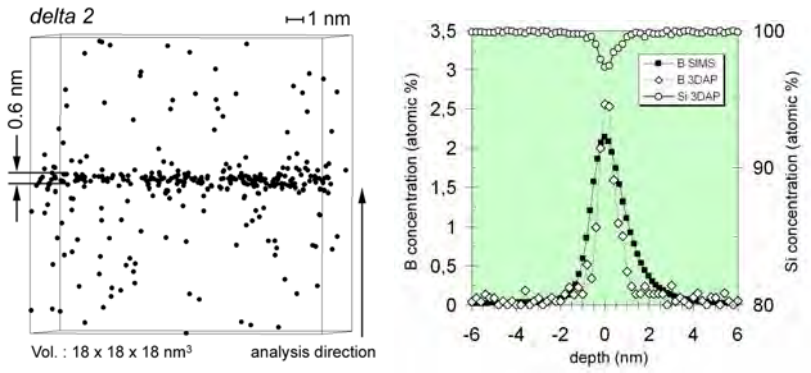

FIGURE 1. (a). 3D atom probe reconstruction of a test sample composed of a delta impulse of Boron in silicon. (b) Concentration profile of boron and silicon through the delta. Concentration profile of boron derived from the 3D are obtained by moving a thin slice of 0.2 nm using a step of 0.2 nm in a direction perpendicular to the three first boron deltas. The surface area of the sampling box is 25 nm x 25 nm. The corresponding SIMS profile is superimposed for comparison.

Key words : Atom probe Tomography, methodology, data reconstruction

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7-2

Synchrotron-Based Nanometrology

[1,2]P.Bleuet, [1]P. Cloetens, [2]P. Gergaud and [1]J. Susini

[1]*European Synchrotron Radiation Facility, BP 220, 38043 Grenoble Cedex, France*
[2]*CEA, LETI, MINATEC, F38054 Grenoble, France*

ABSTRACT

The advent of nanosciences calls for development of multi-scale local probes to characterize heterogeneous and ill-ordered nanomaterials. Based on 3rd generation synchrotron sources and thanks to the great progresses in x-ray optics, x-ray decananometer analyses can now be performed to open new possibilities for characterization and metrology of micro and nanodevices. In the lecture five important synchrotron-related topics are outlined and possibilities, advantages and limitations are explicitly given.

A first asset of synchrotron radiation is the ability to image bulk and packaged devices. Here, the penetration depth of hard x-rays (E>6keV) is exploited to provide the complete 3D morphology of objects of a few hundreds of micrometers thick at a resolution of down to 60 nanometers [1]. Besides direct imaging, coherent diffraction imaging [2] will be discussed since it has a great potential for nanocharacterization.

Using scanning x-ray fluorescence microscopy, quantitative chemical mappings can be performed with detection limits reaching sub-ppm values, typically for trace element analyses and contamination assessment. Eventually 3D quantitative chemical images can be reconstructed using fluorescence tomography.

With diffraction, local stress analyses can be performed on nanostrucures, *e.g.* copper lines, using the now well-established Laue white beam method [3]. Monochromatic beams can also be used for identification of diluted phase in nanomaterials and in 3D [4] while x-ray reflectivity gives surface/interface information.

The potential of microspectroscopy is discussed in the lecture. Basically, the oxidation state, chemical speciation and short range structure of a given element can be investigated by changing the energy of the excitation beam around its absorption edge (XANES, XPEEM [5]).

Another asset of synchrotron radiation is the easiness in performing *in-situ* studies. Thanks to the large focal distance of the x-ray optics, *in-situ* devices can be inserted for temperature studies, stress evolution induced by electromigration or stress effect observation in polarized components.

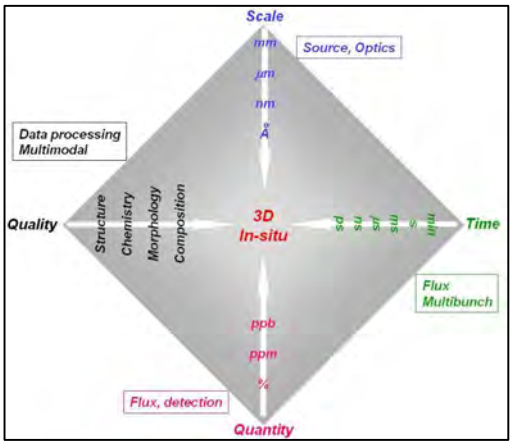

FIGURE 1. Synchrotron radiation offers muti-scale and multi-technique possibilities

Keywords: Nanotomography, diffraction, spectroscopy

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7-3

Application of TOF-SIMS and LEIS for the Characterization of Ultra-Thin Films.

Derk Rading[1], Thomas Grehl[1], Hidde Brongersma[1], Ewald Niehuis[1], Rik ter Veen[2], Michael Fartmann[2], Birgit Hagenhoff[2],

[1]ION-TOF GmbH, Heisenbergstr. 15, 48149 Muenster, Germany
[2]TASCON GmbH, Heisenbergstr. 15, 48149 Muenster, Germany

ABSTRACT

The continuous scaling of semiconductor devices (film thickness, junction depth) to smaller dimensions increases the challenges for the established analytical methods. In addition, new and more complex materials are introduced into the devices. Secondary Ion Mass Spectrometry (SIMS) and more recently Time-of-Flight (TOF-) SIMS have become workhorses for the semiconductor industry. The depth distribution of implants as well as impurities is regularly monitored using Cs and O2 sputter depth profiles. Meanwhile sputter energies as low as 200 eV are routinely used in order to achieve a high depth resolution. Even at these low sputter energies the transient effects prevent establishing a reliable depth scale and deriving quantitative information on the first few nm. In addition, concentrations exceed the dilute limit, thus further complicating the quantification process. In this situation, complementary techniques become increasingly important. One of the emerging techniques is Low Energy Ion Scattering (LEIS) using high sensitivity analyzers. It is extremely surface sensitive and provides quantitative information on the outermost atomic layer of a solid. Low energy (1 – 10 keV) noble gas ions (He, Ne, ...) are used as projectiles. The energy of the back-scattered ions from elastic collisions is characteristic for the masses of the target atoms and is measured using an electrostatic energy analyzer. Quantification is comparatively straightforward and bulk standards can be used to determine the sensitivity factors. In addition, information can be gained on the surface near depth distribution of elements (1 – 10 nm) by measuring the extra energy loss of ions scattered in deeper layers (non destructive, "static mode"). This can be combined with conventional sputter depth profiling using a separate beam of low energy noble gas ions ("dynamic mode").

In order to compare the performance of LEIS with TOF-SIMS results for the characterization of ultra-shallow layers we studied a variety of typical sample systems such as ultra-shallow As implants, high-k films, and diffusion barriers at different stages of ALD growth. The results are discussed with respect to information depth, ease of quantification and sensitivity. It can be shown that the static profiling approach of LEIS is extremely powerful in the first few nm of the profile whereas due to its higher sensitivity SIMS performs better after sputtering through the transient region.

THREE-DIMENSIONAL COMPOSITIONAL & STRUCTURAL CHARACTERIZATION OF SEMICONDUCTING MATERIALS WITH SUB-NM RESOLUTION

Ahmed Shariq [a], Kirsten Wedderhoff [a], and Steffen Teichert [b]

[a] Fraunhofer Center for Nanoelectronic Technologies, Koenigsbruecker Strasse. 180, D-01099 Dresden, Germany
[b] Qimonda Dresden GmbH & Co. OHG, Koenigsbruecker Strasse 180, D-01099 Dresden, Germany

ABSTRACT

The dimensions of devices are constantly shrinking down thanks to novel innovations in the microelectronics industries. These high demands persuade the usage of different analytic techniques to answer the questions regarding physical phenomenona at a scale which are approaching the resolution limits of most of the conventional metrological techniques. For example, nanoscale structures such as buried interfaces in multilayer structures, clustering of dopants at certain interfaces or dopant diffusion profiles around a source/drain contact are quite critical for continued miniaturization of devices. In the ITRS roadmap the atom probe tomography (APT) is mentioned as one of the most promising methods for the quantitative compositional analysis on the required scale [1]. APT is based on the laser assisted field evaporation of atoms from a sharp needlelike specimen. A position sensitive detector provides the spatial information of the ion hits, while, the elemental information is obtained by measuring the time of flight of these ionized atoms [2]. APT can provide spatial resolution in three dimensions down to 0.2 nm scale with an analytical sensitivity of around 10 atomic parts per million.

Two-dimensional dopant profiling of advanced silicon transistors has become an important technique for obtaining requisite electrical characteristics. The resulting p-n-junctions exhibit high dopant concentration values very close to the surface while limiting the junction depth. Knowledge of the spatial distribution of these dopants after annealing is critical for the performance of such devices. The distribution of B dopants is illustrated in fig. 1. Clustering of these dopants has been visualized from the data obtained from APT. Moreover, APT has been applied to multi layer stack of Ti based silicides. The data provides additional information for the lateral distribution of the segregated dopants, particularly on the clustering at selective interface. The data obtained from APT is compared with other characterization techniques such as SIMS and TEM.

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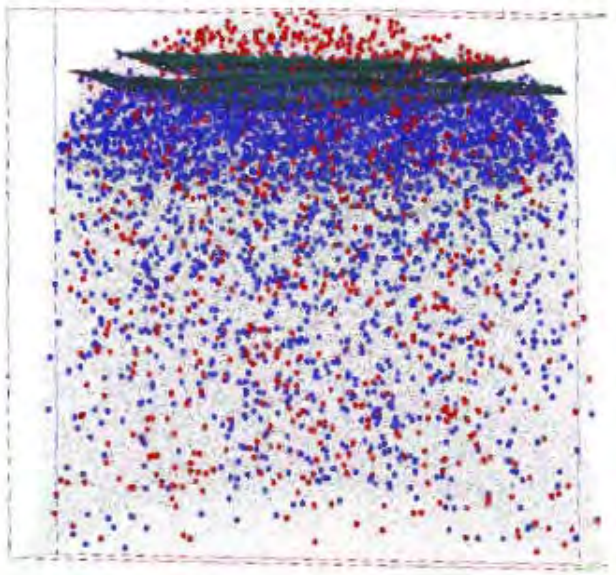

FIGURE 1. 3- Dimensional atomic distribution of Boron dopants in Silicon.

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WE-02

Effect of substrate engineering of AlN/Si(111) substrates on overgrown GaN films

M. Tungare, N. Tripathi, V. Jindal, G. Rao, R. Geer and F. Shahedipour-Sandvik

College of Nanoscale Science and Engineering, University at Albany-State University of New York, Albany, NY 12203

ABSTRACT

Ion implantation has been implemented as a useful technique for strain engineering whether it is to generate crack arresting compressive layers in sapphire and magnesium oxide crystals or to enhance the performance of complementary metal oxide semiconductors (CMOS). We have demonstrated a simultaneous reduction in crack density and dislocation density in 2µm thick overgrown GaN films using our novel ion-implantation assisted substrate engineering technique. Here we present stress analysis of AlN/Si(111) substrates before and after substrate engineering. It is shown that implantation is a key component in the success of this technique. Stress reduction is higher for thinner buffers, with a 36nm AlN buffer showing a decrease in stress by one order of magnitude from >1GPa to 0.1GPa after substrate engineering. The impact of this stress reduction on overgrown GaN films is presented. Jindal et al. have explained the effect of interfacial strain on growth rate and alloy composition of AlGaN nanostructures. Improved quality and compositional control of III-Nitride films is of great technological significance for the realization of better performance devices. Hence, besides the effect of this method on surface morphology, crack density, and dislocation density within the overgrown films, a low temperature photoluminescence (PL) study is also done to better understand the effect of substrate engineering on composition and optical quality.

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Characterization of Organic Contamination during Semiconductor Manufacturing Processing

A. Nutsch[a], B. Beckhoff[b], G. Bedana[c], G. Borionetti[c], D. Codegoni[d], S. Grasso[d], G. Guerinoni[c], A. Leibold[a], M .Müller[b], M. Otto[a], L. Pfitzner[a], M.-L. Polignano[d], D. De Simone[d], L. Frey[a]

[a] *Fraunhofer IISB, Schottkystrasse 10, 91058 Erlangen, Germany*
[b] *Physikalisch-Technische Bundesanstalt, Abbestrasse 2-12, 10587 Berlin, Germany*
[c] *MEMC Electronic Materials SpA, Viale Gherzi,31 28100 Novara, Italy*
[d] *Numonyx, Via Olivetti, 2 Agrate Brianza, 20041 Milan, Italy*

ABSTRACT

Organic contamination on wafer surfaces with impact on nanotechnologies and advanced microelectronics gets crucial as the continuously shrinking feature sizes get comparable to the dimensions of molecules and clusters of molecules. Especially, manufacturing of highly integrated circuits requires clean surfaces as processes might cause defects involving carbon and for example phosphorous and sulphur. Yield issues are observed e.g. due to change of gated oxide integrity by defects, thickness and degradation.

Different sources for organic contamination were identified. The environment used for the fabrication of microelectronics shows various sources for volatile organic compounds (VOC). The sources for VOC are e.g. packaging materials and carriers, or out-gassing and residues of resist layers from lithography. Especially, in lithography, non volatile residues remaining on the wafe

r surface became crucial for subsequent process steps.

The innovative approach to study organic contamination on wafer samples in this paper is the use of different methods. These are reference free Synchrotron Radiation Near Edge X-ray Absorption Fine Structure (NEXAFS) in the soft X-Ray range at the absorption edges of light elements (e.g. C, N, O, F) in total reflection geometry, Thermo Desorption Gas Chromatography Mass Spectrometry (TD GCMS), and Time of Flight Secondary Ion Mass Spectrometry (TOF SIMS). These methods enable detection of the whole range from non volatile to volatile organic compounds. The application of TXRF NEXAFS profits from multi-criteria evaluation of the spectra (see figure 1) and the study of reference samples matched with TOF SIMS and TD GCMS.

Silicon wafers from different steps during wafer processing were studied using TDGCMS and TXRF NEXAFS. Final clean and packaging were identified as areas where detectable organic contamination was transferred to the wafer surface. TOF SIMS analysis of the surfaces of wafers from lithography process after ashing showed sulphur compounds related to resist residues (see figure 1).

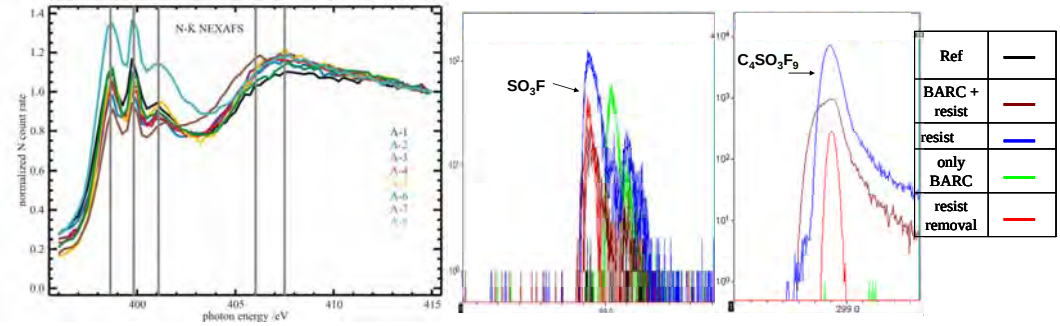

FIGURE 1. TXRF-NEXAFS (left) analysis of wafers treated by different final cleaning and packaging. TOF SIMS (right) analysis of different wafers from the lithographic process.

Keywords: organic contamination, TD GCMS, TXRF NEXAFS, TOFSIMS

WE-04

GIXRF In The Soft X-Ray Range Used For The Characterization Of Ultra Shallow Junctions

B. Beckhoff[1], P. Hoenicke[1], D. Giubertoni[2], G. Pepponi[2], M. Bersani[2]

[1]*Physikalisch-Technische Bundesanstalt,*
[2]*Fondazione Bruno Kessler, via Sommarive 18, 38100 Povo, Trento, Italy*

ABSTRACT

Grazing Incidence X-Ray Fluorescence Analysis (GIXRF) uses the in-depth changes of the x-ray standing wave field intensity dependent on the angle between the sample surface and the primary beam to gain information on the concentration profile [1,2]. This technique is very sensitive to near surface layers. It is therefore well suited for the study of ultra shallow dopant distributions. Arsenic implanted (100) Si Wafers with nominal fluence between $1x10^{14}$ cm^{-2} and $5x10^{15}$ cm^{-2} and implantation energies between 0.5 keV and 5 keV and Boron implanted (100) Si wafers with nominal fluence of $1x10^{14}$ cm^{-2} and $5x10^{15}$ cm^{-2} and implantation energies between 0.2 keV and 3 keV have been used to compare SIMS analysis with synchrotron radiation induced GIXRF analysis in the soft X-Ray range. The measurements have been carried out at the laboratory of the Physikalisch-Technische Bundesanstalt at the electron storage ring BESSY II using monochromatized undulator radiation of well-know radiant power and spectral purity. Here the use of an absolutely calibrated energy-dispersive detector for the registration of the B-Kα and As-Lα fluorescence radiation allows for the absolute determination of the total retained dose. An estimate of the concentration profile has been obtained by fitting the X-Ray fluorescence angular scans with profiles derived by simulation of the implantation process. A good match among the total retained dose measured with the different techniques has been observed (Figure. 1).

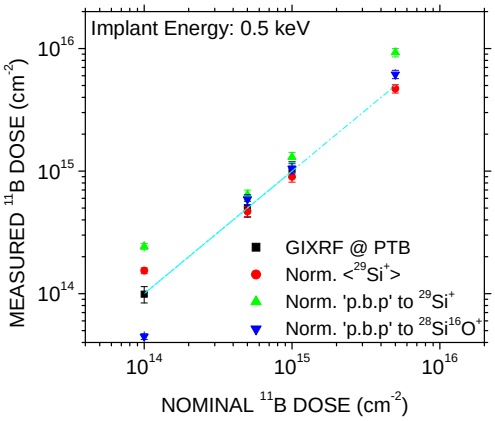

FIGURE 1. Comparison of the ^{11}B total retained doses for 0.5 keV implants in Si as determined by SR-GIXRF and SIMS.

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Ultra-thin AlO_x and LaO_x Metrology – WD-XRF Techniques Development

C. C. Wang, A. Bello, M. Ye, R. Wang, D. Liu, Y. Cao, X. Tang, Y. Uritsky and S. Gandikota

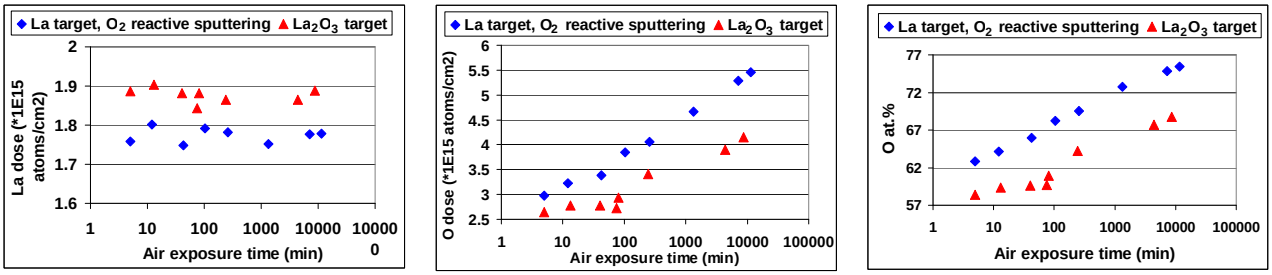
Defect and Thin Films Characterization Laboratory, Applied Materials, Inc., M/S 0203, 3100 Bowers Ave, Santa Clara, CA 95054

ABSTRACT

Beyond the 45 nm node, metal gate and high-k will replace the poly and silicon oxide based gate. Hence, new materials, HfO_2, Al_2O_3, and La_2O_3, are being developed for high-k gate oxide and work function tuning applications. Device performance demands stringent thickness and composition uniformity (1 to 2% 1σ) control on 300mm wafer. However, most of the popular metrology tools are incapable of measuring these ultra-thin (< 20 Å) films, either due to lack of sensitivity or due to strong correlation of thickness with composition or other properties, hence thickness and composition cannot be determined independently. To satisfy the new metrology needs, wavelength dispersive X-ray fluorescence (WD-XRF) techniques are being developed. This technique has the advantage of long term stability, good sensitivity, and robust data analysis algorithm. Its applications for the thickness and composition metrology of RF PVD aluminum oxide and lanthanum oxide ultra-thin films with 0.5 to 2% relative 1σ data precision were demonstrated.

Panalytical Inc. PW2830 WD-XRF system was used in this development. First, the tool was calibrated by carefully prepared thin film aluminum oxide and lanthanum oxide standards whose composition, thickness and density were determined by SEM/EDX and XRR. Once the tool was calibrated, experimental X-ray intensities were used to derive thickness and composition data of the thin films by recursive calculation using Fundamental Parameter (FP) Algorithm[1]. Metrology recipes were developed for such purposes. Detail study was carried out on its long term stability and precision/throughput as a function of film thickness.

WD-XRF metrology has been successfully used to characterize the dependence of the thickness and composition uniformity of the aluminum oxide on different deposition processes conditions. The versatility of this technique's composition and thickness measurement capability was further demonstrated by its monitoring of the lanthanum oxide thin film. Lanthanum oxide thin film is known to have extremely high reactivity with moisture in the air[2], which causes rapid change of its thickness and optical constants when exposed to air. The traditional metrology tool, ellipsometer, cannot determine its thickness accurately due to the strong correlation between thickness and optical constants for ultra-thin film samples. WD-XRF not only determined the amount of La deposited accurately, but also determined the composition change as a function of air exposure time (Fig. 1).



(a) (b) (c)

FIGURE 1. 10Å lanthanum oxide thin films air exposure data: (a) La dose remained constant with air exposure time; (b) oxygen dose increased with time due to moisture absorption by the lanthanum oxide thin film; (c) film composition (calculated based on La dose and O dose data) change in terms of oxygen atomic concentration.

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Key words: cap layer, XRF, metal gate.

On The Use of Synchrotron Radiation for the Characterization of "TiN/HfO_2" Gate Stack

C. Gaumer[a], E. Martinez[b], S. Lhostis[a], F. Fillot[b], P. Gergaud[b], B. Detlefs[c], J. Roy[c], Y. Mi[c], J. Zegenhagen[c], A. Chabli[b]

[a]*STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France*
[b]*CEA, LETI, MINATEC, F38054 Grenoble, France*
[c]*European Synchrotron Radiation Facility, BP 220, F-38043 Grenoble, France*

ABSTRACT

Understanding the electrical properties of the new "high-k/metal" MOSFET devices requires the use of advanced characterization techniques in order to identify the physical and chemical properties of the gate stack (1). However the physical limits of XRD or XPS experiments performed with laboratory X-ray sources are often reached. For XRD, the low thickness (< 10 nm) of the layers, correlated to small grain size induces wide peaks and low intensity on diffraction patterns. The use of hard X-rays on a synchrotron facility overcomes this problem thanks to the high brightness of the source. The X-ray wavelength can be tuned in order to optimize resolution in the reciprocal space for studies of stack components of low crystal symmetry. The probing depth in XPS with conventional laboratory X-ray sources is limited to a maximum of 10 nm, because of the short photoelectron inelastic mean free path. The escape depth of photoelectrons increases for kinetic energy above 2 keV, resulting in an increase of the depth sensitivity in hard X-ray photoelectron spectroscopy (HAXPES). Non-destructive analysis of the "Si/HfO_2" interface buried underneath the TiN top layer is thus enabled. The brightness of synchrotron radiation compensates the decrease of the photoemission cross-section for the high photon energies. Here we investigate the crystalline structure and the chemistry of TiN/HfO_2 gate stacks using grazing incidence XRD (GIXRD), reflectivity measurements and HAXPES (hν ~ 10 keV). Analyses were performed on the ID32 beam line at ESRF, Grenoble, France. 5 nm-thick HfO_2 is shown to be monoclinic. 5 and 10 nm-thick TiN is cubic (figure 1). No change of the crystalline structure is observed during the processing steps following the TiN deposition. The evolution of the stress state in the layers will be discussed from the diffraction peaks positions. HAXPES demonstrates the occurrence of nitrogen and oxygen diffusion from TiN and HfO_2 into the thin pedestal SiO_2. The impact of the steps subsequent to the TiN deposition on this phenomenon will also be discussed.

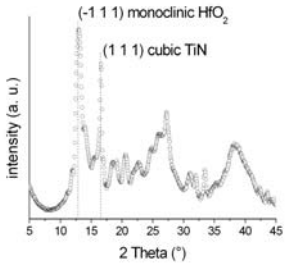

FIGURE 1. GIXRD diagram of a TiN (10nm)/HfO_2 (5nm)/SiO_2 (0.8nm)/Si gate stack measured using a 17.7 keV X-ray beam.

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KEYWORDS: Synchrotron radiation, GIXRD, HAXPES

WE-07

Designing an X-ray Reflectometry Standard Reference Material: An Inverse Problem for an Inverse Problem

David L. Gil and Donald Windover

Ceramics Division, MSEL, National Institute of Standards and Technology, Gaithersburg, MD

ABSTRACT

X-ray reflectometry (XRR) provides materials scientists with an accurate, first principles, method of determining thickness of uniformly deposited films in the 1 nm to 500 nm range [1]. However, several modeling difficulties arise: roughness of substrate and films can dampen interference features, multiple layers can create complex and multimodal parameter estimations, interface density gradients can wash out interference features, and layers of similar electron density may be completely indistinguishable. The use of XRR for accurate thickness determination fundamentally relies on sample alignment, instrument optics alignment, and instrument angle calibration; all of which could be enhanced through the use of a Standard Reference Material (SRM) of known structural character.

Developing an XRR SRM first requires selecting a thin film structure of the optimal characteristics for each type of calibration. A smooth, high electron density layer(s) on thick, high flatness Si will aid in specular rocking curve approaches for sample alignment. The quality and performance of instrument optics can be studied using high dynamic range, sharp features within the XRR data. Careful selection of deposited materials and layer thicknesses can generate sharp features covering 3 to 4 orders of magnitude, which are ideal for optics calibration. Goniometer calibration requires numerous interference features which provide information to verify angle encoding on instrumentation. Thick films provide this type of high density fringe information.

The NIST approach for structure development has been two-fold: 1) interaction with the semiconductor community to select existing deposition processes with uniformity and minimal inter-diffusion and roughness, and 2) development of first principles, statistically rigorous, XRR modeling methods which can estimate model parameter uncertainties on actual and simulated data [2]. In this presentation we show results of this material structure selection process and provide the uncertainty estimates from our structure selection study.

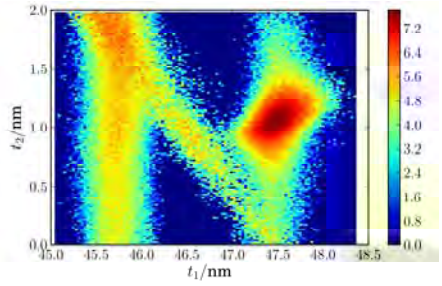

FIGURE 1. Monte Carlo Markov Chain parameter estimation for a two-layer structure showing complex multi-modality.

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Multi-technique characterization of arsenic ultra shallow junctions in silicon within the ANNA consortium.

D. Giubertoni[1], G. Pepponi[1], B. Beckhoff[2], P. Hoenicke[2], S. Gennaro[1], F. Meirer[3], D. Ingerle[3], G. Steinhauser[3], M. Fried[4], P. Petrik[4], A. Parisini[5], M.A. Reading[6], C. Streli[3], J.A. van den Berg[6] and M. Bersani[1].

[1]*Fondazione Bruno Kessler, via Sommarive 18, 38100 Povo, Trento, Italy.*
[2]*Physikalisch-Technische Bundesanstalt, Abbestrasse 2-12, 10587 Berlin, Germany.*
[3]*Atominstitut der Oesterreixhischen Universiteaeten, TU Wien, Stadionallee 2, 1020 Wien, Austria.*
[4]*MFA-KFKI, Konkoly Thege Rd. 29-33, 1121 Budapest, Hungary.*
[5]*CNR-IMM, Via P. Gobetti 101, 4129 Bologna, Italy.*
[6]*School of Computing, Science and Engineering and Institute of Materials Research - University of Salford, M5-4WT, Salford, UK.*

ABSTRACT

The ongoing size reduction of silicon CMOS devices has required the development of processes able to create ultra shallow junctions in order to match the specifications for source and drain extensions. The latter demand very steep dopant distributions confined in the first 10-20 nm of the substrate. The characterization of those distributions is known to be extremely challenging. For instance, secondary ion mass spectrometry (SIMS) has been often used to determine the chemical depth distribution of dopant in Si, due to its high dynamic range and sensitivity, excellent depth resolution and good reproducibility. However, matrix effects and initial transient width hinder the accuracy of the technique when applied to distributions close to the surface. Furthermore, the early formation of roughness and different sputtering rates between surface SiO_2 and the Si substrate may distort the depth calibration and resolution. Therefore a complementary analytical approach is desirable if critical information like retained dopant dose, junction depth and junction abruptness have to be evaluated. In this work results obtained within the EC financed ANNA project (Analytical Network for Nanotechnology, co. n. 026134(RII3)) in which one of the activities is related to the characterization of ultra shallow distributions of As in Si, will be summarized. A matrix of samples has been prepared by ion implantation in order to test the capabilities of the different analytical techniques represented within the consortium. As^+ implant energy varied between 0.5 and 5.0 keV whereas the doses were between 5×10^{14} and 5×10^{15} cm^{-2}. These samples were then characterized by SIMS, grazing incidence x-ray fluorescence spectroscopy (GIXRF), soft x-ray GIXRF using synchrotron radiation, tilted sample high angle annular dark field scanning transmission microscopy (HAADF-STEM), neutron activation analysis (NAA), spectroscopic ellipsometry (SE) and medium energy ion scattering (MEIS). Cross comparison of the dose measurements, 'near-surface' dopant distribution and damage build-up behavior have enabled a detailed characterization of these implanted samples. They have also identified the overlap in information gained from the different analytical techniques present in our consortium.

Keywords: ultra shallow junctions, arsenic, silicon.

WE-09

NIST High Resolution X-Ray Diffraction Standard Reference Material: SRM 2000

Donald Windover, David L. Gil, Albert Henins, and James P. Cline

Ceramics Division, MSEL, National Institute of Standards and Technology, Gaithersburg, MD

ABSTRACT

The National Institute of Standards and Technology has recently completed a Standard Reference Material (SRM) for calibration of high resolution X-ray diffraction (HRXRD) laboratory, synchrotron, and fabrication-line instrumentation. HRXRD supplies information on slight lattice distortions in thin expitaxial films – a critical parameter for development of the next generation of strained Si on insulator (SOI) substrates needed in advanced CMOS processing. Currently, accuracy in HRXRD lattice measurements relies in assuming apriori, the substrate Si lattice constant, $d_{substrate}$, and measuring the difference between the substrate, $d_{substrate}$, and strained surface features, $d_{strained}$. SRM 2000 provides an International System of Units (SI) traceable determination of the substrate Si lattice constant, d_{SRM}, on a specimen which can be provided directly to the instrument user community. The NIST certified reference parameter and field measurements can be combined to calibrate the performance of an HRXRD instrument – providing the user with information about either the instrument's monochromator wavelength or its angle measurement uncertainties.

We present the SI traceability chain used in the determination of the transmission lattice constant for the substrate Si (220) lattice planes, d_{SRM}, and describe challenges encountered in angle and wavelength metrology. The SI traceability chain relies on X-ray/optical interferometry measurements of the Si lattice spacing performed at Germany's PTB for the Avogadro Project [2] and on Si boule inter-comparison measurements performed on the NIST lattice comparator [3]. The same SI-traceability approach will be used in future NIST HRXRD, X-ray reflectometry, and powder diffraction SRM projects.

We provide the measurement strategy used for the HRXRD measurements including the instrument and sample alignment methods used for the SRM. To achieve high accuracy in the certification, we used a transmission Bond method [4] for feedstock measurements and used serial measurements of a reference crystal from the Avogadro Project to reduce instrument uncertainty budget. The use of this "sequential delta-d" method has allowed setting the expanded uncertainties on the lattice spacing of less than a femtometer (10-15 meters). We illustrate suggested field uses of and measurement designs for the SRM for various instrument configurations. We conclude with a discussion of our plans for recertifying the SRM in 2009 with certified parameters from the nominal 50 nm, SiGe epitaxial surface layer.

TABLE 1. Certified reference values for SRM 2000

Quantity	Reference value	Expanded Uncertainty $U(i)$ for k=2
d_{SRM}	0.1920161 nm	0.87 fm

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WE-010

Characterization of HfO_2 and Hafnium Silicate Films on SiO_2/Si

E. Bersch*, M. Di*, S. Consiglio**, R.D. Clark**, G.J. Leusink**, A.C. Diebold*
**College of Nanoscale Science and Engineering, University at Albany, 255 Fuller Rd., Albany, NY 12203*
*** TEL Technology Center, America, LLC, 255 Fuller Rd. Albany, NY, 12203*

ABSTRACT

As the MOSFET SiO_2-based gate dielectric layer approaches its fundamental physical limits, the investigation of high-k oxides is ongoing in order to determine which oxides can best continue the scaling of the MOSFET. HfO_2 and hafnium silicates are leading candidates due to their relatively large band gaps, thermal stability in proximity to Si and relatively high dielectric constants. We have used a combination of x-ray photoemission spectroscopy (XPS) and spectroscopic ellipsometry (SE) to measure the band offsets between the high-k layers and the Si substrates. Shifts in band alignment that occur upon deposition of the HfO_2 layer and annealing of the $HfO_2/SiO_2/Si$ film stack will be discussed in light of XPS spectra. Non-destructive compositional depth profiles constructed from angle resolved XPS data will also be presented and film thicknesses determined from them will be compared to thicknesses measured by SE..

WE-011

Non-Traditional Spectroscopy for Analysis of Semiconductor and Photovoltaic Thin Films Materials

Fuhe Li and Scott Anderson

Air Liquide Electronics - Balazs NanoAnalysi,46409 Landing Parkway, Fremont, CA 94538
fuhe.li@balazs.com; scott.anderson@airliquide.com

Chemical characterization of semiconductor thin films has long been determined by a number of traditional surface analysis techniques; RBS, SIMS, XPS and FTIR to name only a few. Depth profiles, contamination in the thin film or quantitative stoichiometry are specific application examples which predicate the technique best suited for the analysis need. The evolution of thin film compositions with new chemistries and growing importance of atomic layer deposition for photovoltaic and nanoscale applications provide a sustaining need for thin film analyses along with an avenue for new analytical tools.

In this paper we discuss the application of two non-traditional surface analysis techniques for the electronics industry, laser ablation inductively coupled plasma mass spectrometry (LA ICP-MS)[1-2] and glow discharge optical emission spectroscopy (GD-OES)[3]. Depth profiles are shown in Figure 1 along with the ability to analyze single monolayers (single nm) as well as analysis in the bulk (μm thickness) using both techniques. Depth resolution capabilities allow analysis of atomic layer deposition applications without surface equilibrium issues seen with other techniques. In addition, the charging effect that can cause issues with electron and ion beam techniques is avoided with the glow discharge and laser ablation techniques.

Contaminant analysis in thin films is very straight-forward as elements across the periodic table are analyzed in a simultaneous mode with both techniques. Detection limits to part-per-billion levels are achieved and quantitation at low concentrations up to 100% can be achieved with LA ICP-MS and GD-OES. Accuracy and precision is excellent and figures of merit for both will be shown. It will be discussed that for some thin film applications, LA ICP-MS and GD-OES provide advantages over more traditional techniques, and these advantages as well as complementary features will be presented.

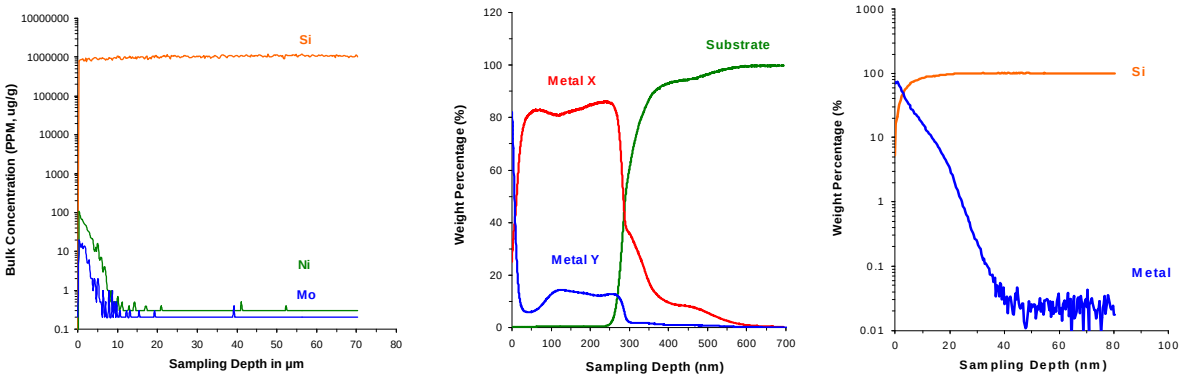

FIGURE 1. Depth profiles across a range of applications are shown for photovoltaic and semiconductor materials via LA ICP-MS and GD-OES.

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Key words: semiconductor, solar, film

WE-012

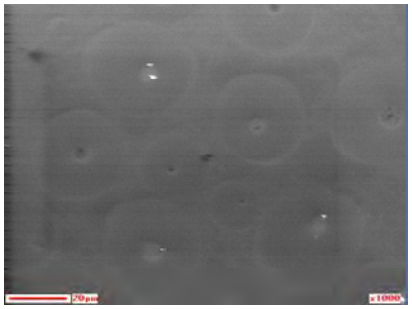
An Investigation on Airborne Particular& Molecular Condensation Through Liquid Nitrogen Assisted Cooling

R. GOPAL Krishnan and G. Yaadhav Raaj*

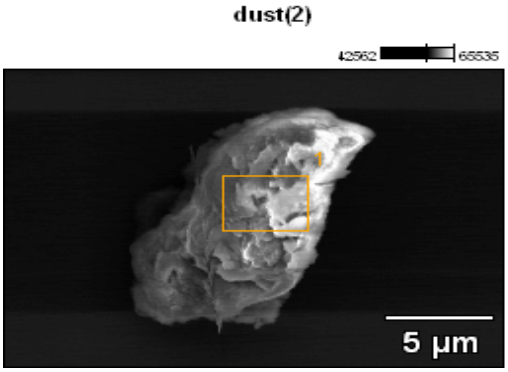
A*STAR Institute of Microelectronics, Agency for Science, Technology and Research,
11 Science Park Road, Science Park II, Singapore - 117685.

*** Raffles Junior College, Singapore**

Several research papers have attempted to characterize and analyse the volatile and condensable organic and inorganic contaminations found in clean rooms, controlled enclosures and open ambience. It is clear that condensation of airborne molecular species from a wide variety of sources such as solvents, construction materials, cleaning solutions, eating places, automotive exhaust, storage materials have a impact on the quality of air we breathe. In this study, analysis of water and particulates collected on LN2 cooled - silicon wafer surfaces from various locations are presented and discussed. A battery of advanced analytical techniques such as SEM/EDX, FIB, FEAUGER, ICP-MS/OES have been employed to understand the chemical composition and its relevance to particular environment.
Keywords: Advanced Analytical Technologies, Chemical Analysis and ambience.



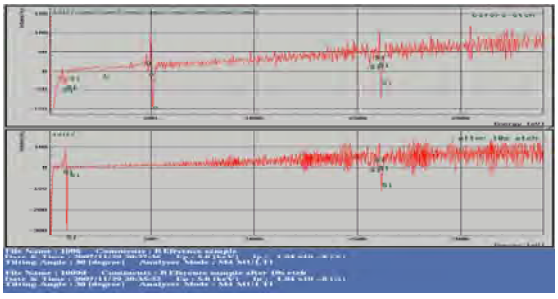
FEAUGER SEM micrograph of water marks on a Si surface



SEM micrograph of a typical particle

Anion	#1	#2	#3	#4	#5
Fluoride	1.04	0.07	1.11	1.54	0.33
Chloride	2.59	0.46	3.55	7.39	1.56
Nitrite	0.08	0.87	0.31	0.39	0.10
Bromide	<0.01	<0.01	0.02	0.02	<0.01
Nitrate	4.46	0.97	1.67	0.49	0.90
Phosphate	0.27	0.2	0.72	1.62	1.86
Sulfate	2.67	0.66	2.80	1.50	2.60

Condensed water analysis for key anion concentration of few samples by ICP-MS



FEAUGER Spectra of Si surfaces after and before condensation

WE-013

Detection of Metal Contamination on Silicon Wafer Backside and Edge by New TXRF Methods

Hiroshi Kohno, Motoyuki Yamagami, Joseph Formica*, Liyong Shen*

Thin-film Analysis Group, Rigaku Corporation, 14-8 Akaoji-cho, Takatsuki-shi, Osaka Japan
**Semiconductor Fab Products, Rigaku Americas Corporation, 9009 New Trails Drive, The Woodlands, TX 77381*

ABSTRACT

In conventional 200mm wafer processing, backside defects have not been considered much of an issue because defects were obscured by wafer backside topography. However, in current 300mm wafer processing in which both sides of a wafer are polished, backside defects require more consideration. In the beginning, backside defect inspection examined particle contamination because particle contamination adversely influences the depth of field in lithography. Recently, metal contamination is of concern because backside metal contamination causes cross contamination, and backside metals easily transfer to the front surface.

As the industry strives to yield more devices from the area around the wafer edge, edge exclusion requirements have also become more important. The current International Technology Roadmap for Semiconductors requires a 2mm edge exclusion. Therefore, metal contamination must be controlled to less than 2mm from the edge because metal contamination easily diffuses in silicon wafers.

To meet these current semiconductor processing requirements, newly developed zero edge exclusion TXRF (ZEE-TXRF) and backside measurement TXRF (BAC-TXRF) are effective metrology methods.

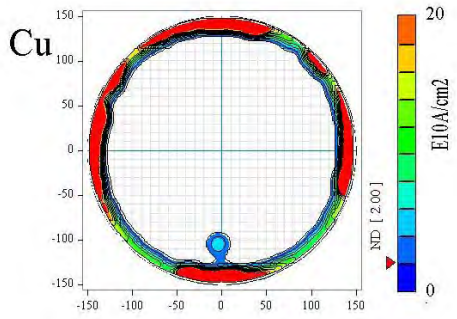


FIGURE 1. Cu contamination detected on the wafer back side near the edge. (Measured by BAC-TXRF)

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WE-014

In Situ, Real-Time Gas Phase Absorption Measurements During Atomic Layer Deposition

J.E. Maslar, W.A. Kimes, J.T. Hodges, B. Sperling, D.R. Burgess, E.F. Moore

National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899

ABSTRACT

In situ monitoring of atomic layer deposition (ALD) processes is expected to yield insights that will enable improved efficiencies in film growth, in the development of deposition recipes, and in the design and qualification of reactors. *In situ* diagnostics can be used to measure a number of process parameters; a relatively common application being the measurement of precursor flux into the reactor. However, such measurements are of limited value when trying to optimize deposition chemistry. Potentially more useful would be rapid and species selective measurements of deposition precursor and product gas phase concentrations near the wafer surface. Measurements of this type would allow one to probe the properties of near-surface thermal/gas velocity boundary layers that exist in many industrial ALD reactors. Since the boundary layer is strongly affected by the wafer surface, gas phase measurements in the boundary layer would also provide information about the state of the wafer surface.

In this work, we present several real-time ALD diagnostics based on gas phase laser absorption measurements near the wafer surface. We investigated the ALD of hafnium oxide produced by the reaction of tetrakis(ethylmethylamino) hafnium (TEMAH) and water. Assuming complete reaction, the products of this reaction also include methyl-ethyl-amine (MEA), a volatile species under deposition conditions. We performed time resolved measurements of water by probing a rovibrational absorption transition of water vapor occurring in the near-infrared spectral region. This measurement utilized a distributed feedback diode laser and wavelength modulation scheme. We used amplitude modulation spectroscopy to probe absorption features of TEMAH and MEA in the mid-infrared and near-infrared regions, respectively. The measurements of TEMAH utilized a quantum cascade laser and those of MEA employed an external-cavity diode laser. *In situ*, time-resolved Fourier-transform infrared spectroscopy measurements were used to complement the laser-based measurements. All measurements were performed in a single-wafer, warm-wall reactor and probed an axis parallel to the wafer surface. In an effort to correlate gas phase measurements with surface processes, we measured deposition precursor and product concentrations under a range of deposition conditions. Finally, we compare the performance of the various spectroscopic measurements, and we describe efforts to model the observed concentration gradients using reactor-scale computational fluid dynamics models.

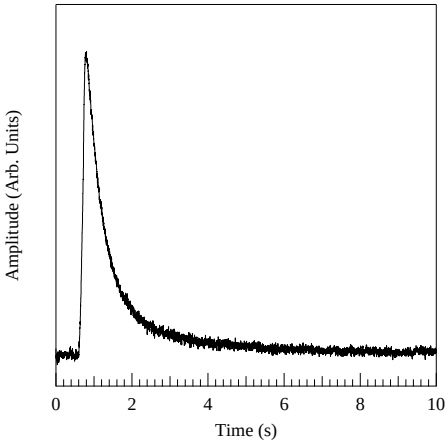

FIGURE 1. *In situ*, time-resolved diode laser spectroscopic measurement of water vapor absorption.

Key Words: Atomic Layer Deposition; In Situ Diagnostics; Optical Spectroscopy

WE-015

Vacuum-Ultraviolet Reflectometry of Ultra-thin HfO_2 films

Jeffrey Hurst[1] and Victor Vartanian[2]

[1]*Metrosol Inc., 2101 Donley Drive, Suite 101, Austin, TX 78758*
[2]*ISMI, 255 Fuller Road, Suite 359, Albany NY 12203*

ABSTRACT

Hafnium-based films deposited by atomic layer deposition (ALD) are being widely used in ultra-thin high-κ gate dielectrics as a replacement for traditional thermal SiO_2. This includes variants of this film, such as HfSiO and HfSiON where Si and N are added to HfO_2 to increase its thermal stability [1,2]. For optical metrology of these multi-component high-κ materials, the basic constituents (HfO_2, SiO_2, Si_3N_4, etc.) are combined in an optical model either as a mixture or as discrete layers. As an essential building block for most high-κ applications, it is important to have strong process control for HfO_2. HfO_2, like most dielectric materials, exhibits an increasing extinction coefficient as the wavelength decreases into the vacuum-ultraviolet (VUV). This general attribute gives VUV metrology strong sensitivity to ultra-thin dielectric thickness variations.

In this work blanket HfO_2 wafers deposited by ALD on bare Si were measured using a commercial vacuum-ultraviolet spectroscopic reflectometer (VUV-SR), Metrosol VUV-7000, to obtain reflectance data from 120-800nm (10.33-1.55eV). The reflectance measurement results were compared with both XRR reference data and process conditions. Measurements were performed to investigate sample uniformity and the measurement capability of the VUV-SR instrument. The measurement results indicate VUV reflectometry provides Angstrom-level thickness measurement capability. A linear correlation coefficient, R^2, of 0.9914 to the number of ALD HfO_2 cycles demonstrated sensitivity for the thickness range studied, 1.5 to 37Å, while the mean precision for thickness measurements (1-σ) was 0.05Å. There did not appear to be any correlation between the precision and the nominal film thickness.

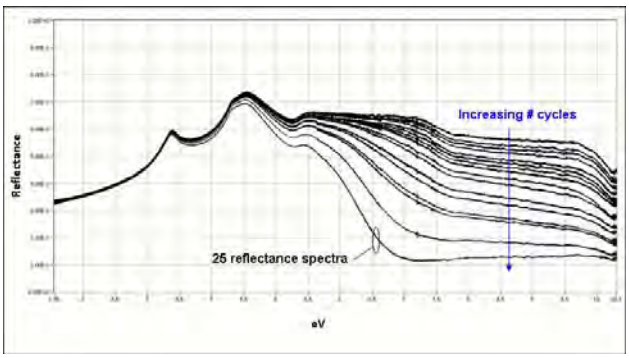

FIGURE 1. VUV reflectance measurements for 16 wafers (25 spectra/wafer) covering 2-40 HfO_2 ALD cycles.

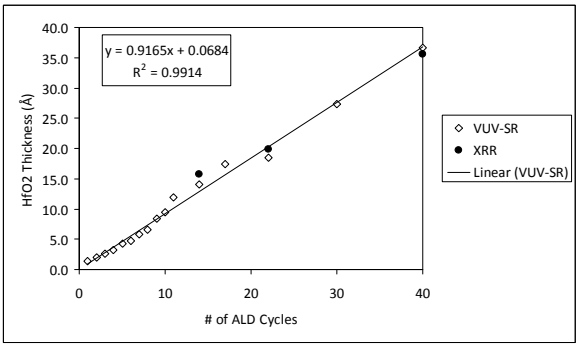

FIGURE 2. Measurements by XRR and VUV-SR for 2-40 HfO_2 ALD cycles.

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Key words: VUV reflectance, high-κ, thin film measurement

Stress Measurement In Microstructures By Raman Microscopy

Benjamin Uhlig[*1], Jens-Hendrik Zollondz[2], Matthias Goldbach[2], Harald Bloeß[2], Peter Kücher[3]

[1]*Fraunhofer -Institut für Keramische Technologien und Systeme, Winterbergstrasse 28, 01277 Dresden, Germany*
[2]*Qimonda Dresden GmbH & Co. OHG, Königsbrücker Strasse 180, D-01099 Dresden, Germany*
[3]*Center of Competence CoC Metrology/Analytic, Fraunhofer-Center Nanoelektronische Technologien CNT, Königsbrücker Straße 180, D-01099 Dresden, Germany*

- *e-mail: buhlig@ikts.fraunhofer.de*

ABSTRACT

Stress plays a vital role for the electronic performance of advanced nanoscale semiconductor devices. Uncontrolled stress in the microstructures due to different thermal expansion coefficients can lead to cracks, delamination or electrical shorts in the circuits. On the other hand intentionally induced and controlled stress applied to a transistor gate channel will increase carrier mobility. For the detection and measurement of stress a suitable and reliable technique for today's structures in the nanometer range has to be developed and established. One promising option is Raman microscopy, which is fast, nondestructive and very stress sensitive. Two dimensional Raman maps of real chip structures could be generated, which gave us a detailed insight into the microstructural stress situation, unmatched up to now in respect to precision and accessibility by any other measuring technique. To compare the results we find good qualitative agreement with electrical measurements performed on Si/SiO2 structures of different sizes.

Keywords: Micro-Raman, stress, silicon.
PACS: 78.30.-j (CHECK: Infrared and Raman spectra (for vibrational states in crystals and disordered systems, see 63.20.-e and 63.50.+x respectively))
http://www.aip.org/pacs/index.html)

Application Of The SPV-based Surface Lifetime Technique To In-Line Monitoring Of Surface Cu Contamination

John D'Amico[a], Alexandre Savtchouk[a], Matthew Wilson[a], Chul Hong Kim[b], Hyung Won Yoo[b], Chang Hwan Lee[b], Tae Kyoung Kim[b] and Sang Hoon Son[b]

[a]*Semiconductor Diagnostics, Inc. 3650 Spectrum Blvd. Suite 130, Tampa, FL 33612*
[b]*Hynix Semiconductor, Inc. San 136 Ami-ri Bubal-eub Icheon-si Kyoungki-do 467-701 Korea*

ABSTRACT

Implementation of Cu interconnects into Silicon Integrated Circuits (IC's) has been instrumental in the continuing improvement of IC device performance. Copper as a well known Gate Oxide Integrity (GOI) killer [1,2] requires extensive protocols to minimize the possibility of cross contamination. Despite such protocols the risk for cross contamination exists, and consequently there is the need for in-line Cu cross-contamination detection metrology. Preferably the metrology will be non-destructive, fast, and capable of mapping on product wafers.

Up to now the most common approaches for monitoring Cu contamination in IC fabrication lines either measure Cu in the bulk Si, which is not applicable to Cu cross-contamination monitoring because Back-End-of-the-Line thermal budgets restrict the ability to diffuse the surface Cu into the bulk Si; or the techniques are not optimal for in-line monitoring due to their destructive, time-consuming, or costly nature. In this work we demonstrate for the first time the application of the ac-Surface PhotoVoltage (ac-SPV) surface lifetime approach [3] to in-line, full wafer coverage mapping of low level (<1E9cm^{-2}) surface Cu contamination. The low level sensitivity is achieved through integration of a novel preferential surface Cu activation procedure into a production ready metrology system. Furthermore, because the metrology is non-contact (utilizing edge-grip handling) and non-destructive, it is directly applicable to measurement of production wafers. In-line fab data acquired using this metrology is presented and compared to data from other surface techniques, such as Total Reflection X-ray Fluorescence (TXRF) and Inductively Coupled Plasma Mass Spectroscopy (ICP-MS) (Figure 1 below). (Keywords=Copper, Cross-Contamination, Metrology)

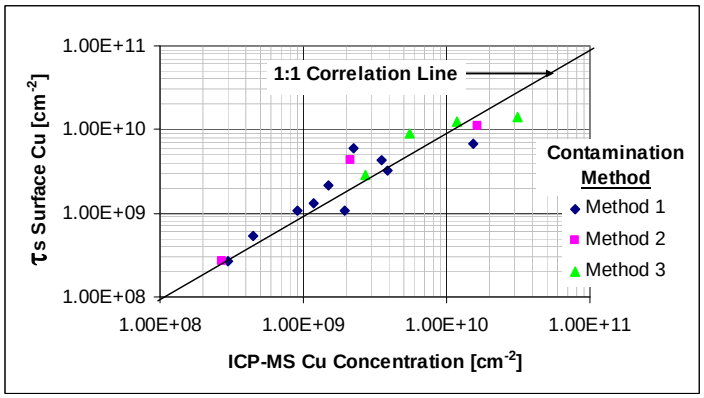

Figure 1. Correlation of surface Cu measured by ac-SPV τ_s and ICP-MS for three surface Cu contamination methods.

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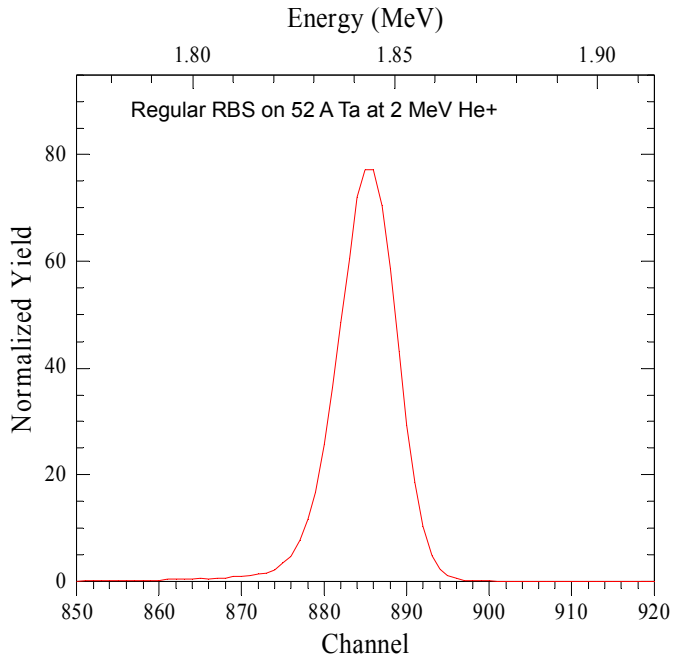
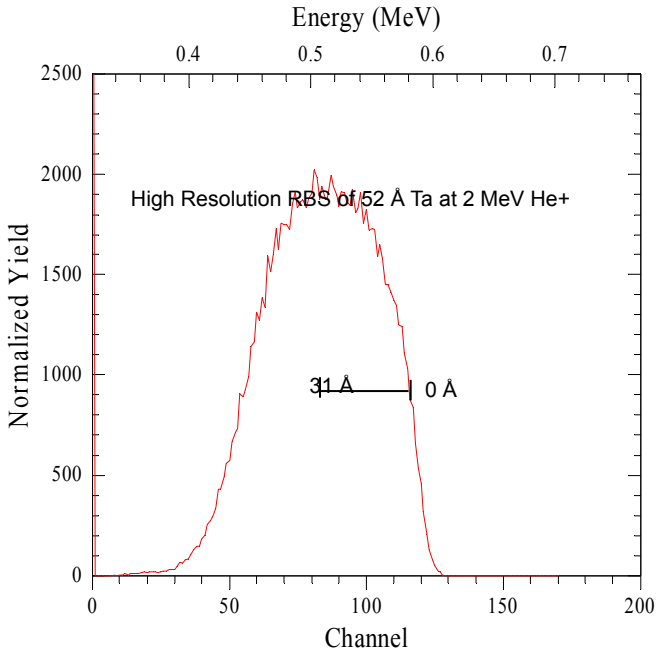
WE-018

High-Resolution Rutherford Backscattering Analysis of Nanoscale Thin Films

Joshua LaRose and Mengbing Huang
SUNY-Albany

Rutherford backscattering spectroscopy (RBS) has been an important analytic method for determination of the depth distribution of elemental concentrations in materials. The depth resolution of RBS is typically limited by the energy resolution of ion detectors. In this work we demonstrate the use of a compact magnetic spectrometer as the ion energy detector for high-resolution RBS analysis. The magnetic spectrometer offers several advantages: (1) a high energy resolution $\Delta E/E \sim 1/2000$; (2) a large bending power for MeV ions; and (3) a particular configuration allowing for true 180° RBS analysis. By combining this magnetic spectrometer with the grazing angle geometry, we have achieved a depth resolution better than 5 Å for RBS analysis of concentration distributions in elemental (e.g., Ta) and compound (e.g. HfO_2) thin films using 2 MeV helium ions. These experimental results suggest that high-resolution characterization of nanoscale thin films can be realized using MeV ions in conjunction with such magnetic spectrometers. The advantages of our method for nanoscale thin film analysis over medium energy ion scattering (MEIS) will be discussed.





Ion channeling study of activated boron and disordered Si atoms in silicon ultra-shallow junctions

Lakshmanan Vanamurthy[1], Mengbing Huang[1], Hassaram Bakrhu[1],Toshiharu Furukawa[2], Nathaniel Berliner[2], Josh Herman[2], Zhengmao Zhu[2], Paul Ronsheim[2], Bruce Doris[2], Ming Li[3], Peter Banks[3], Susan Felch[4]
[1]College of Nanoscale Science and engineering, University at Albany-SUNY, Albany NY 12203
[2]IBM corporation, 255 Fuller Road Albany NY 12203
[3]AMAT, 255 Fuller Road Albany NY 12203
[4]Spantion Inc, Sunnyvale 94085

Abstract

Successful fabrication of ultra shallow junctions for sub 32 nm node CMOS device scaling has become a great challenge due to increased difficulty in material characterization. A good understanding of activation (dopant atoms on substitutional sites in the Si lattice) and defect formation in Si can be acquired using ion channeling techniques. In addition, ion channeling can be combined with room-temperature UV-assisted oxidation and chemical wet etching for obtaining high-resolution (~0.5 nm) depth distributions of boron atoms and silicon lattice defects in Si ultra-shallow junctions.

The ultra shallow junction samples analyzed in this work were prepared by the implantation of 200 eV B ions to a dose of 1×10^{15} atoms/cm^2 in a silicon wafer preamorphized by Ge Ion-implantation. The samples were annealed either using a 1100 °C rapid thermal anneal (RTA) or 1250 °C laser anneal to recover from the damage caused by ion implantation. The 1100 °C RTA process resulted in higher activation of boron than the laser anneal Furthermore more disordered Si atoms were detected in the surface region (within ~10 Å below the native oxide) in the laser annealed sample. These findings combined with other measurements (secondary ion mass spectroscopy and sheet resistance) would help achieve an understanding of how the ultra-shallow junction properties are affected by various materials processing conditions.

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WE-020

Evaluation of experimental techniques for In-line Ion Implantation Characterization

L. Vignoud[a]; F. Milesi[a]; E. Nolot[a]; A. Danel[a]; S. Favier[b]

a – CEA-LETI MINATEC, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France
b – ST MICROELECTRONICS, 850 rue Jean Monnet, 38920 Crolles Cedex, France

ABSTRACT

Implant is a key process in advance IC manufacturing covering many applications: doping processes (i.e.: USJ, Contacts, Well …), Smart-cut™ process, surface treatments (i.e.: nitridation …). Despite several methods are proposed or under development to perform in-line monitoring. In practice, characterization of implant is still mainly based on invasive techniques: SIMS, sheet resistance. This work proposes an as exhaustive as possible review of methods witch can (could) be applied for in-line monitoring of implant: specifically develop ones (photothermal based technique[1], Low-energy Electron-induced X-ray Emission Spectrometry[2], and Junction Photo Voltage (JPV)[3]), others under validation[4] (light scattering and spectroscopic ellipsometer), and new methods under development (alternating current Surface Photo Voltage (acSPV)[5], Surface Potential Difference Imaging (SPID)[6]). In this work, a large range of conditions for ion implantation were selected: i) various techniques of implant (beam line ion implant and plasma immersion ion implant), ii) several of ions (H^+, P^+, As^+, and B^+), iii) broad range of energy (sub keV to 200keV) and iv) broad range of dose (9×10^{13} to 6×10^{16} at/cm^2). Each method has been evaluated from global capability point of view: as implanted and/or post annealing, range of dose (Fig.1a: Example of metrology capability: Haze (wide oblique) versus dose for As^+ and H^+); and methods performances have been compared (Fig.1b : Example of comparison between metrology dynamic : Haze (wide oblique) and sheet resistance applied to As^+, 200keV, 10^{14} at/cm^2 implant). A global synthesis will be proposed.

Fig. 1a

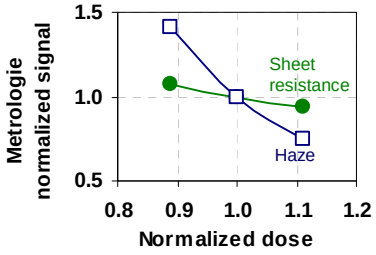
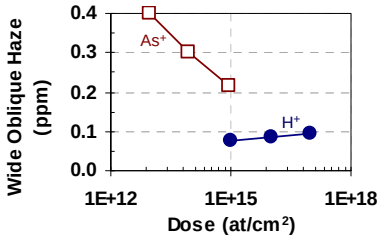


Fig. 1b



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WE-021

High Temperature X-ray Diffraction for the Determination of Thin Film Phase Diagrams of High-k Dielectrics

L. Wilde,[1] S. Teichert,[2] P. Reinig,[2] S. Schmidt,[3] W. Weinreich,[1] and P. Kücher[1]

[1] *Fraunhofer Center Nanoelectronic Technologies, Königsbrücker Str. 180, D-01099 Dresden, Germany*
[2] *Qimonda Dresden GmbH & Co. OHG, Königsbrücker Str. 180, D-01099 Dresden, Germany*
[3] *Westsächsische Hochschule Zwickau, Dr.-Friedrichsring 2A, D-08056 Zwickau*

ABSTRACT

According to the ITRS roadmap [1] the further shrink of DRAM devices can be reached only by the application of suitable high-k dielectric materials in the capacitor. Combining the request of the relative permeability k and the well known Clausius-Mossotti relation [2] only crystalline dielectric materials are supposed to provide a sufficient large k value for next generation DRAM capacitors. It is obvious that besides the selection of a proper material composition the material density, hence, the formed crystalline phase will play a crucial role to achieve the desired permeability.

Supporting the running development activities, we performed high temperature X-ray diffraction in grazing incidence geometry (HT-GIXRD) for the determination of thin film phase diagrams of several high-k materials in a thickness range between 4–20 nm. As the use of Synchrotron radiation is associated with applicatory drawbacks (limited availability, high costs) we used a conventional thin film laboratory diffractometer with optimized optics and experimental conditions, where the measurement time was reduced to 2-3 hours per sample.

Examples of phase diagrams of Y-, Ti & Si doped HfO_2 films as well as of thickness dependent crystallization of undoped ZrO_2 films on different substrate materials are shown. In 10 nm thick ALD deposited $Hf_{1-x}Si_xO_2$ films, the Si concentration has a significant influence on the resulting crystal phase on the one hand, and of the crystallization temperature on the other hand. Below x = 0.06, the film crystallizes in the monoclinic phase, whereas for $x \geq 0.06$ the preferred cubic/tetragonal phase is formed at temperatures between 510–680°C (Fig. 1).

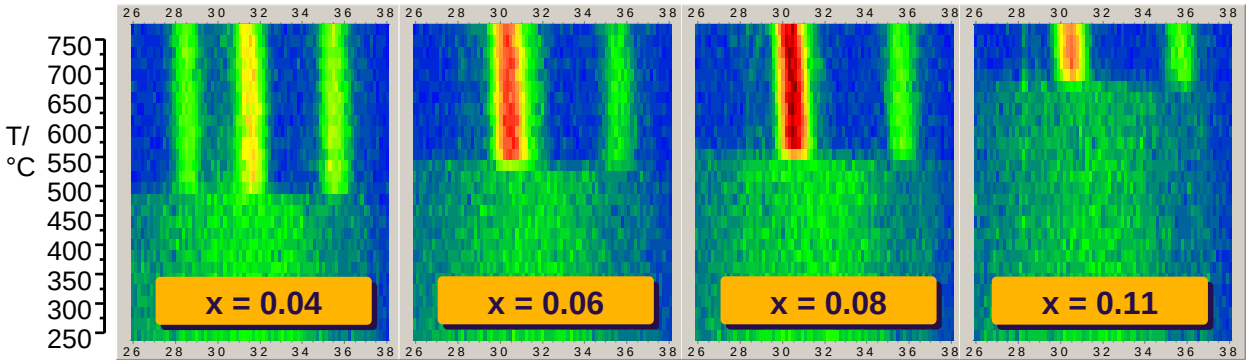

FIGURE 1. High temperature.GIXRD measurements on 10 nm $Hf_{1-x}Si_xO_2$ films deposited by ALD.

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WE-022

Advanced Gate and Stack Dielectric Characterization with FastGate® Technology

Robert J. Hillard[1], Louison Tan[1] and Kimberly G. Reid[2]

[1] *Solid State Measurements, Inc. Pittsburgh, PA 15275*
[2]*Associated with Tokyo Electron America Austin, TX, USA*

ABSTRACT

In this paper a non-damaging and non-contaminating method for performing Capacitance-Voltage (CV) and Current-Voltage (IV) electrical characterization of advanced gate dielectrics and stack capacitor films is presented. Key electrical parameters that are measured are, Capacitive Effective thickness (CET), Equivalent Oxide thickness (EOT), Interface Trap Density (D_{it}), delta V_{FB} Hysteresis (ΔV_{FB}) , leakage current density (J_{LK}) , Field-to-breakdown (F_{BD}), Charge-to-breakdown (Q_{BD}) and Stress Induced Leakage Current (SILC). The probe is an Elastic Material Probe (EM-Probe) (1) that is made of semiconductor compatible material and forms a gate contact diameter of about 30 to 50 microns. Measurements can be made either on blanket wafers or in scribe line test areas on product wafers.
An example of the sensitivity of D_{it} and ΔV_{FB} to high-k process conditions is shown in Figure 1.

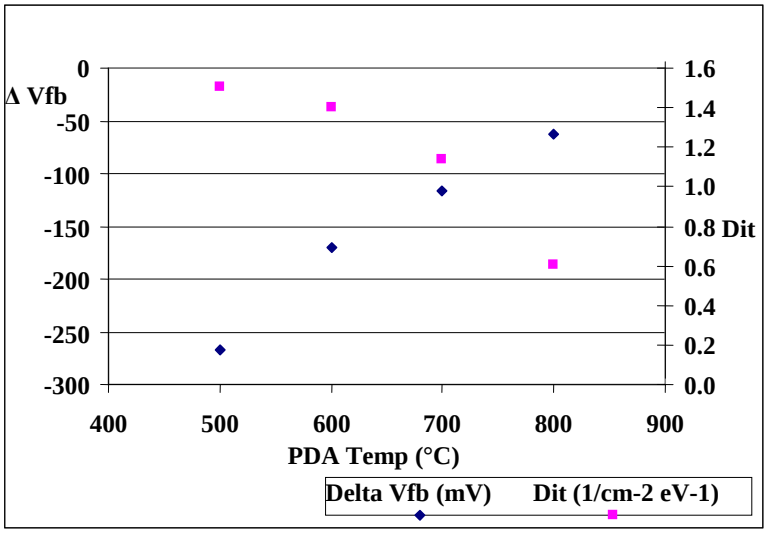

FIGURE 1. EM-Probe D_{it} and ΔV_{FB} measured on a Hf based high-k dielectric with different post deposition anneals.

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WE-023

Nanocalorimetry of Thin Film Solidification and Nickel Silicide Formation

David A. LaVan[1], Feng Yi[1], Ravi K. Kummamuru[1,2], Lito De La Rama[2], Liang Hu[2], Mark D. Vaudin[1] and Leslie H. Allen[2]

[1] *Ceramics Division, Materials Science and Engineering Laboratory, National Institute of Standards and Technology (NIST), 100 Bureau Drive, Gaithersburg, MD 20899, USA*
[2] *Department of Materials Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA*

ABSTRACT

The investigation of transient materials processes at high reaction rates, and the development of novel nanomaterials requires small scale, high speed measurement of thermodynamic properties. Thermodynamic measurements such as enthalpy and entropy are essential to understand fundamental properties of materials, as they provide direct and quantifiable insight into phase transitions. In many cases, relevant materials may only be synthesized as thin films; membrane based nanocalorimeters allow direct measurement of such materials[1-3]. The low heat capacity of nanocalorimeters means that heating and cooling rates as high as 10^6 °C/s can be achieved. Recent developments in nanocalorimetry at NIST will be presented, including the characterization of the formation of nickel silicides[4] at the interface of nanometer scale thin films of silicon and nickel. In addition, the rapid cooling rate allows the characterization of metastable phases. As an example, measurements on an aluminum thin film (Figure 1) will be shown. Future directions will be discussed as well.

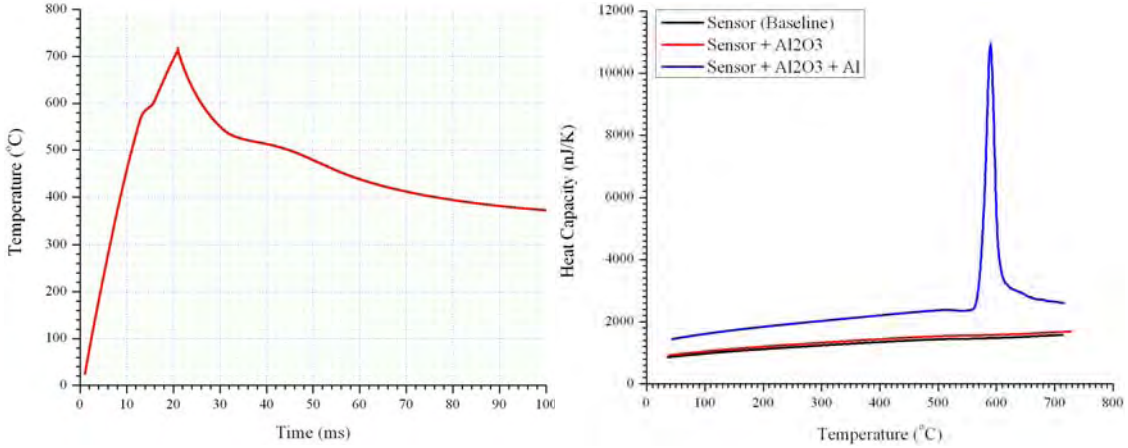

FIGURE 1. Measurements made on a 50 nm aluminum film deposited over an alumina barrier layer (a) Measured temperature as a function of time; the heating cycle reached 700 °C in 20 msec. (b) Calculated heat capacity of the bare nanocalorimeter sensor, sensor with alumina barrier layer and sensor, alumina and aluminum sample.

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Towards Routine Backside SIMS Sample Preparation for Efficient Support of Advanced IC Process Development

M.J.P. Hopstaken[1*], C. Cabral Jr.[1], D. Pfeiffer[1], C. Molella[2], and P. Ronsheim[2]

1. IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA
2. IBM East Fishkill, Hopewell Junction, NY 12533, USA

Secondary Ion Mass Spectrometry (SIMS) is one of the most universally applied analytical techniques for depth profiling of thin films and interfaces with nm-resolution in semiconductor materials. In conventional front-side SIMS depth profiling, depth resolution can be adversely affected by several physical and chemical effects induced by dense ion bombardment, leading to artificial tailing for high-concentration species from the over-layer into the underlying layer.

Inversing the sputter direction (*i.e.* 'Backside SIMS') has been proposed to circumvent the aforementioned degradation of depth resolution, by approaching the layer of interest from the backside [1, 2]. Analysis of high-k dielectrics and the underlying interlayer and channel region may greatly benefit from backside SIMS approach [3]. Though this appears to be trivial and elegant solution, large practical barriers in backside sample preparation prohibit a wider and more routine use of backside SIMS.

Current backside preparation schemes require an in-built etch stop (*e.g.* buried oxide of an SOI wafer) to enable selective removal of the Si-substrate and elaborate sample preparation, with the backside high-precision polishing being the most critical, labor intensive and time-consuming step because of the subsequent wet etching step [1, 3]. Wet etching of the remaining Si-substrate is commonly performed using TMAH or KOH wet etching solutions. However, etch rates are highly anisotropic with the etch rate of the {111} crystallographic orientation being 2-3 orders of magnitude lower than on the other major crystallographic orientations [4]. Wet etching of thick and roughly polished remaining Si inadvertently leads to the formation of <111> faceted Si-pyramids, prohibiting successful SIMS backside analysis [5]. For these reasons, the high-precision polishing step (down to a few μ) with ultra-smooth finish is currently limiting the success rate and turn-around time for SIMS backside preparation.

Here, we propose the use of XeF_2 dry etching instead of wet etching for removal of the residual Si-substrate [6]. The former process is essentially isotropic with similar etch rates for the different crystallographic orientations and highly selective towards the dense thermal oxide (BOX). This eliminates the need for high-precision polishing of individual samples, reducing the substrate removal to a few coarse and relatively rapid polishing steps (down to 25-40 μ thickness) only. Moreover, XeF_2 etching can be performed in unattended fashion and simultaneously on multiple samples, greatly increasing volume and turn-around time for backside sample preparation. We will explain the different practical aspects and demonstrate the feasibility of this novel approach for backside preparation for different front-end (S/D contact silicide metal, high-k metal gate) and back-end (ECD-Copper) of line applications.

In conclusion, availability of a robust and reliable procedure for backside SIMS sample preparation with rapid turn-around is highly beneficial for a more efficient analytical support of advanced IC process development.

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*Corresponding author:
Tel: 914-945-2570 / Fax: 914-945-4184
E-mail: marco.hopstaken@us.ibm.com

WE-025

X-ray Photoelectron Spectromicroscopy Of Doped Silicon Patterns

N. Barrett[1], M. Lavayssière[2], O. Renault[2] , L. F. Zagonel[1], A. Bailly[2]

[1] *CEA DSM/IRAMIS/SPCSI, CEA Saclay, 91191 Gif sur Yvette, France*
[2] *CEA, LETI, MINATEC , F38054 Grenoble, France*

ABSTRACT

The quantitative analysis of semi-conductor images displaying dopant-dependent contrast is of prime importance in nanoelectronics. A very well suited technique is PEEM [1] which is complementary to other methods such as electron holography, due to its non-destructive character, its decananometric spatial resolution and its surface sensitivity. X-ray excited PEEM (XPEEM) with energy-filtering brings additional crucial spectroscopic information on surface chemical and electronic properties of semi-conductors.

Contrast from p-n highly doped patterns have already been studied [2] but the interpretation is still not well understood: band alignments and work function [1], hot electrons absorption near the Fermi level [3] or the oxide layer [4] are factors playing a role in the contrast mechanisms.

We present first results obtained with a state-of-the-art XPEEM spectromicroscope (NanoESCA), which allows energy filtered and aberration corrected XPS and UPS imaging [5]. We studied highly n and p doped patterns on p^- and n substrate respectively. Using synchrotron radiation, we obtained spectroscopic image series across the valence band and the Si 2p core-level. We fitted extracted local Si 2p spectra from several regions (400nmx400nm squares) presented in the first image of the Figure 1 with standard literature parameters. Ultimately, we can extract, after suitable treatments, local spectra from a region size down to one pixel (here 33.3 nm).

We were able to characterize completely the energy and the spatial distribution with high resolution of those patterns and to directly estimate the real band bending at the interface as a function of the doping. [5]

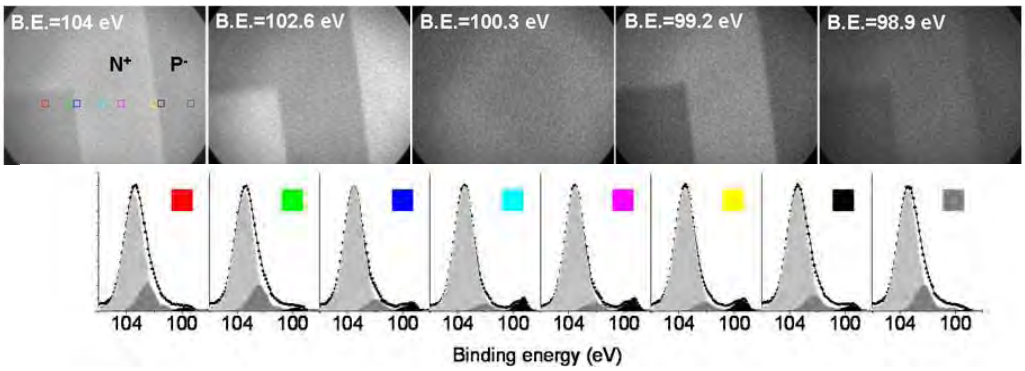

FIGURE 1. Top: selected XPEEM images from the energy filtered image series across the Si 2p core level on sample n^+/p^-. Bottom: local Si 2p core level spectra and best least squares fits: the Si^{4+} component due to the native SiO_2 oxide is in light grey, the sub-oxide components grey and the Si_0 substrate component black. [5]. Field of view is 25 µm.

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Keywords : spectromicroscopy, XPEEM, silicon doped.

WE-026

Spectroscopic Ellipsometry Characterization of High-k films on SiO_2/Si

Ming Di,[1] Eric Bersch,[1] Parul Tyagi, [1] Steve Consiglio,[2] Robert Clark,[2] Gert Leusink,[2] Arun Srivatsa,[3] and Alain C. Diebold[1]

[1] *College of Nanoscale Science and Engineering, University at Albany, 255 Fuller Rd., Albany, NY 12203*
[2] *TEL Technology Center America, LLC, 255 Fuller Rd. Albany, NY, 12203*
[3] *KLA-Tencor Corp., One Technology Drive, Milpitas, CA 95035*

ABSTRACT

Spectroscopic ellipsometry (SE) with VUV wavelength region has been used to characterize high-k films grown on SiO_2/Si. The high-k stack thickness measurements by SE are compared to other metrology techniques such as angle resolved x-ray photoemission spectroscopy. The optical properties of hafnium silicate change with silicate concentration, which is the mechanism for SE to measure this quantity. Other factors that affect high-k optical properties are also investigated.

WE-027

Abstract Withdrawn

WE-028

Quantitative Analysis of Stress Components in Si Device Structures Using UV Raman Spectroscopy

Tetsuya Tada, Vladimir Poborchii and Toshihiko Kanayama

MIRAI, Nanodevice Innovation Research Center (NIRC), National Institute of Advanced Industrial Science and Technology (AIST), 1-1-1 Higashi, Tsukuba, Ibaraki 305-8562, Japan
Tel : +81-29-861-2628, Fax : +81-29-861-2576, E-mail: t-tada@aist.go.jp

ABSTRACT

Raman spectroscopy is expected to be used for local stress measurements in Si device structures. However, the stress is a three-dimensional tesor quantity composed of six independent components, which makes it difficult to analyze stress quantitatively from Raman shifts. In this work, we show that the quantitative analysis of stress components is possible in shallow trench isolation (STI) structures using polarization dependence of Si Raman spectra measured on a lower symmetry surface.

We utilized a UV confocal Raman microscopy system with the 364 nm excitation wavelength. The system has very high-spatial-resolution, ~130 nm, using an immersion lens with a numerical aperture (NA) of 1.3 [1]. The resolution can be improved to 80 nm using deconvolution technique.

The sample STI structure used in the present work is shown in Fig.1 (a). The spatial variation of Raman spectra of the STI structures were measured along the line AA' on the cross sectional (-110) surface with *xx* (polarization directions of both the excitation and detection light are [110]) and *xz* configurations (the polarization direction of excitation light is [110], and that of the detection light is [001]). We calculated the stress tensor components, σ_{xx} and σ_{zz}, from the measured Raman shifts using the fact that the Raman spectra taken with the above polarization configurations correspond to different modes of triply degenerated optical phonons in Si. As shown in Fig.1 (b), the compressive [110] stress decreases as the probing point moving down from A to A', while the compressive [001] stress increases below the Si stripe bottom. Our finite element method (FEM) simulation indicates that the increase of σ_{zz} is caused by bending of the upper part of the cleaved surface toward the front due to stress relaxation.

Figure 1(c) shows the spatial variation of the Raman spectra along the line BB' at the trench bottom on the (001) surface with the *xx* configuration. The observed stress induced Raman shifts shows the drastic change from negative to positive values near the edge, which means the tensile stress becomes compressive near the edge. We confirmed by the FEM simulations that this is also due to elastic deformation out of the cleaved surface.

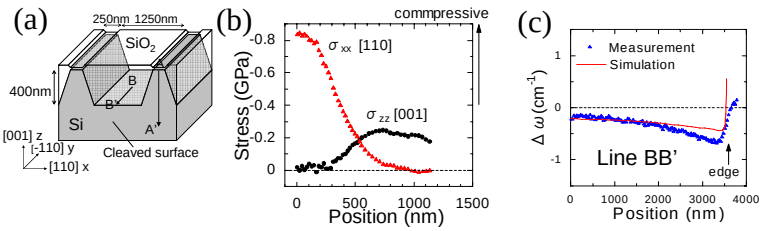

FIGURE 1 (a) The sample STI structure used in the present work. (b) The stress components, σ_{xx} (▲) and σ_{zz} (●) calculated using the Raman data. (c) The stress induced Raman shift plotted as a function of the probe position along the lines AA' (▲). The solid line denotes the Raman shift calculated with the FEM simulations.

This work was partly supported by NEDO.

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Keywords: Raman spectroscopy, stress distribution, Si STI structures

Photoreflectance Spectroscopic Characterizations of Charge States in High-κ Dielectric Layers

Tianhao Zhang,[1] Ming Di,[1] Eric J. Bersch,[1] Houssam Chouaib,[2] Alex Salnik,[2] Lena Nicolaides,[2] Steve Consiglio,[3] Robert D. Clark,[3] and Alain C. Diebold[1]

[1] *College of Nanoscale Science and Engineering, State University of New York, 255 Fuller Road, Albany, NY 12203*
[2] *KLA-Tencor Corp., 160 Rio Robles, San Jose, CA 95134*
[3] *TEL Technology Center America, LLC, 255 Fuller Road, Albany, NY 12203*

With the continuing scaling down of MOSFET devices, the thickness of SiO_2 based gate dielectric layer is approaching its fundamental physical limits. Alternative gate oxide materials with higher dielectric constant (κ) are demanded to satisfy the decrease of device dimensions. Hafnium oxide, hafnium silicate and nitrided hafnium silicate, with large permittivity, good thermal stability in proximity to silicon and compatibility in fabrication processes, are promising candidates. However, high-κ layers typically contain more surface and interface defect states compared to SiO_2. Charges trapped at these defect states degrade device performances through effects including current leakage, shift of the threshold voltage, and reduced carrier mobility.[1]

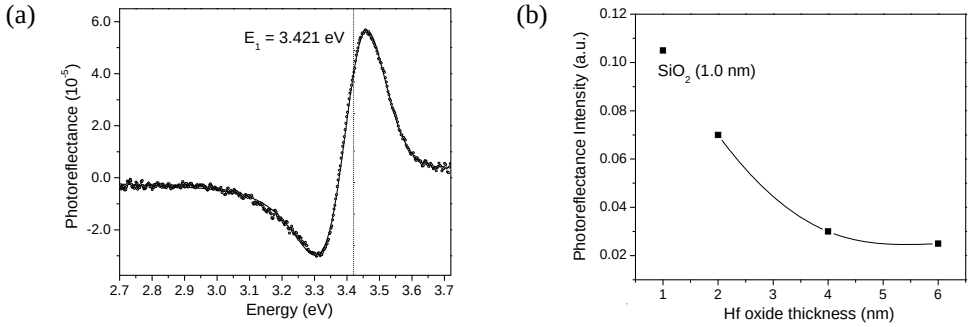

FIGURE 1. (a) A typical PR spectrum (dotted line) and the fit to a model (solid line); (b) PR intensity decreases with the thickness of Hafnium oxide layer.

We utilize photoreflectance (PR) spectroscopy to investigate the charge states in hafnium silicate layers on silicon. The change in reflectance is measured while the built-in electric field in the material being studied is modulated by a pump laser with photon energy greater than the band gap.[2] Sharp derivative spectral features are presented in the region where optical excitation occurs, even in room temperature. PR is sensitive to energy band structures at surfaces and interfaces, and the intensity of PR spectrum reflects the band bending due to charges in the layers.[2] Hafnium silicate samples of different composition and layer thickness were studied with PR apparatus developed in KLA-Tencor Corp. A typical PR spectrum is shown in Figure 1(a), along with the fit to a third-derivative functional form model. As shown in Figure 1(b), PR intensity decreases with the thickness of hafnium oxide layer, since the interface potential is reduced with the increase of positive charge defects in the layer. This result is in good agreement with the theoretical calculation in Ref. [3]. In addition, the E_1 critical points in hafnium oxide and silicon were obtained from the fit. An energy shift of E_1 in silicon is observed, as a result of the interface layer strain in the presence of oxide.

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WE-030

Quantification of Hafnium in Hafnium Oxide Film for Reference Materials

Toshiko Takatsuka,[1] Isao Kojima,[1] Yoshinori Kobayashi,[1] Kouichi Hirata,[1] Naoko Nonose,[1] Tadayuki Ohchi,[2] Chikara Ichihara,[3] Hideaki Matsue,[4] Mizuho Morita,[5] Hikari Takahara,[6] Toshiyuki Asano[7]

[1]National Metrology Institute of Japan, National Institute of Advanced Industrial Science and Technology, Central 5, 1-1-1 Higashi, Tsukuba, Ibaraki 305-8565, Japan,
[2]NTT-AT-Nanofabrication Co., [3]Kobe Steel, Ltd., [4]Quantum beam science directorate, Japan atomic energy agency,
[5]Graduate school of engineering, Osaka univ., [6]Technos CO., LTD.,
[7]Ibaraki Prefectural Industrial Technology Center

ABSTRACT

Hafnium oxide (high-k) dielectric films are being introduced into silicon-based semiconductor devices in order to achieve higher performance. The front-end processes require that the thin dielectric films are well-controlled in thickness for gate stacks. According to the international technology roadmap for semiconductors 2007, thickness of dielectric films should be controlled in 4 % process range after the year 2010. It becomes difficult to obtain the accurate thickness in length unit since the films are getting to be near atomic dimension and consist of complex structure like interface layers, which may involve atomic fluctuations. Reference materials whose properties are well-calibrated should shed light on quantification of the film thickness with small uncertainties. This study aims to compare capabilities and evaluate uncertainties in quantitative analyses by several techniques, and finally to develop reference materials applicable to semiconductor manufacture.

Hafnium oxide films were deposited on 4-inch Si wafers by magnetron sputtering method and the targeted thickness is 2.5 nm with homogeneity within 1%. Hafnium amounts in the films were quantified by metrological techniques such as ID-ICPMS (Isotope diluted-inductively coupled plasma mass spectroscopy), INAA (instrumental neutron activation analysis), H-RBS (high resolution Rutherford backscattering spectrometry), XRR (X-ray reflectometry), TXRF (total reflection X-ray fluorescence), and AR-XPS (angle resolved X-ray photoelectron spectroscopy). The results are shown next.

ID-ICPMS: Specimen and $^{179}HfO_2$ were dissolved in HNO_3+HF+H_2SO_4 solution. The calculated mean value of 4 specimens was $(5.993 \pm 0.065) \times 10^{15}$ atoms/cm^2 in area density and standard uncertainty. Main source of the uncertainty was from measurement uncertainty of isotope ratio.

INAA: In the gamma-ray spectrum, a doublet peak come only from ^{181}Hf was selected to calculate the hafnium amount in the film. The calibrated area density was 5.9×10^{15} atoms/cm^2 with an uncertainty around 1 %.

HRBS: He^+ ions were irradiated into the surface at 400 keV in “random direction” of Si crystal. The evaluated area density was 5.87×10^{15} atoms/cm^2 with the uncertainty in repeatability less than 1.7 %.

XRR: The thickness in length unit was measured. Calibrated results showed 3-layered structure consisting of adsorbates 0.27 nm, HfO_2 2.44 nm, and SiO_x 1.1 nm.

TXRF: The relative area density of Hf in the films was measured. Inhomogeneity in a wafer was less than 0.9 % and the uncertainty in repeatability was 0.6 %.

AR-XPS: Maximum entropy method was used to evaluate the layered structure. The estimated thickness was 2.4 nm of HfO_x with additional surface adsorbates and interface layers.

Thus we see that the results approximately agree with one another. More detailed results are discussed to understand the differences in capabilities and uncertainties among metrological techniques above.

KEYWORDS: reference materials, uncertainty, high-k dielectric films

WE-031

Process Tool Contamination - From Starting Material to On-Wafer

Victor K.F. Chia

Balazs NanoAnalysis, 46409 Landing Parkway, Fremont, CA 94538, USA

ABSTRACT

Organic contamination in tools is less understood compared to particle and metallic contaminations. The sources of organic contamination is diverse and may be introduced from the fab environment or from within the tool. In-tool contamination sources may be direct from material outgassing in the tool, organic contaminants in the gases or precursors and excess application of lubricant. Or, it may be indirect from outgassing of bags, containers or foam liners used to package the cleaned tool parts and assemblies and from the gloves used during PM and tool assembly. AMC-MC such as DOP commonly found in cleanroom construction materials will become SMC-SMOrg that may contaminate tool parts during PM when the parts are most vulnerable to the fab environment. No matter what the organic source is the organics will stick to the silicon surface during processing resulting in residual carbon that may degrade the tool performance. For example, organic compounds may decompose to form SiC and affect GOI and polysilicon deposition. Delamination of films is frequently attributed to organics on the surface. Organophosphorus compounds may decompose and n-dope silicon wafers. Organics in lithography tools may cause optics to fog resulting in reduced transmission. This paper focuses on organic contamination of starting materials and on-wafer during processing. We will discuss methodology for detecting and reducing organics and illustrate the difficulty of controlling organic contamination in tools with an escalation study.

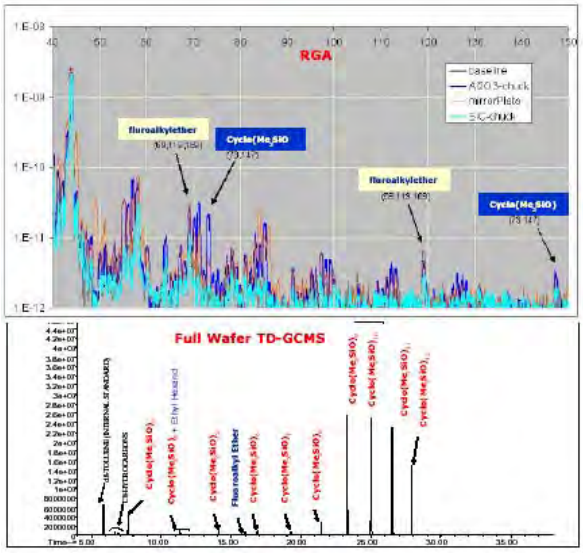

FIGURE 1: Comparison of RGA and TD GC-MS data

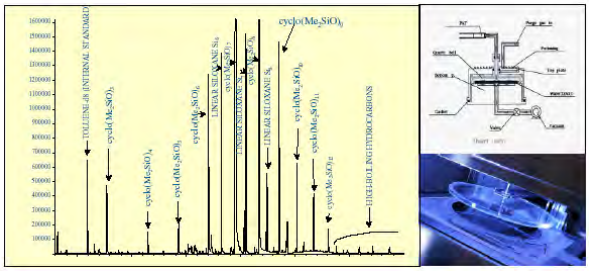

FIGURE 2: Full wafer TD GC-MS outgassing instrument and results.

WE-032

Thickness Measurement of Thin Metal Films by Optical Metrology

Vimal Kamineni[1], Mark Raymond[2], Eric Bersch[1], Bruce Doris[3], Alain Diebold[1]

College of Nanoscale Science and Engineering, University at Albany, Albany, New York – 12203.
AMD, Albany, New York – 12203.
IBM, Albany, New York - 12203.

ABSTRACT

Determining the thickness of thin metal films using an optical source has been one of the major challenges in metrology. Thin metal films have thickness dependent optical properties and the imaginary part of the dielectric function of thin metal films is non-zero in a wide optical range (150 nm – 33 μm). The non-zero nature of the imaginary part of the dielectric function is due to the absorption of light from Far Infrared (IR) frequency to the Plasmon frequency by free and bound electrons in metals. The absorption of light till the Plasmon frequency by free electrons in metals can be described by a Drude Oscillator (zero restoring force).[1] At higher frequencies some metals absorb light due to electronic transitions from the d-shell to the conduction band.[1] These interband transitions of bound electrons in metals can be described by a Lorentz Oscillator.

Ni and NiSi (metal gate electrode) thin films on a 300 mm wafers of varying thicknesses (< 20 nm) were used to develop a robust optical model using Drude and Lorentz oscillators. The optical model is built with a correlation between the thickness of the film and the average grain radius.[2] This correlation was built to show the dependence of the electron relaxation time on the average grain size of polycrystalline metal films.[2] Variable Angle Spectroscopic Ellipsometers (VASE) in both IR & VUV range of wavelengths were used to measure the thin films. X-ray Reflectivity (XRR), X-ray Photoelectron Spectroscopy (XPS) and Rutherford Back Scattering measurements on thin metal films were performed to compliment the ellipsometric measurements.

Keywords: Ellipsometry, Metal Thin-Films, and Metrology.

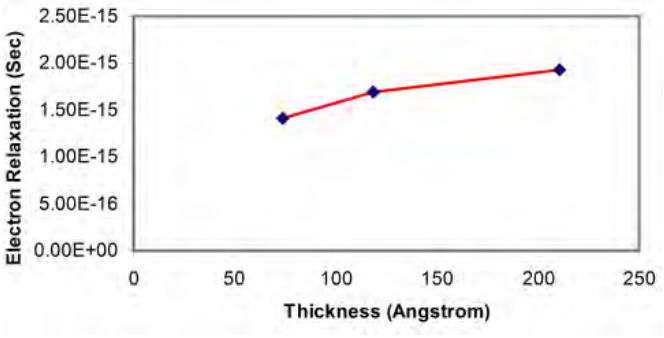

FIGURE 1. Electron Relaxation Time versus thickness of thin film metal films of Ni.

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WE-033

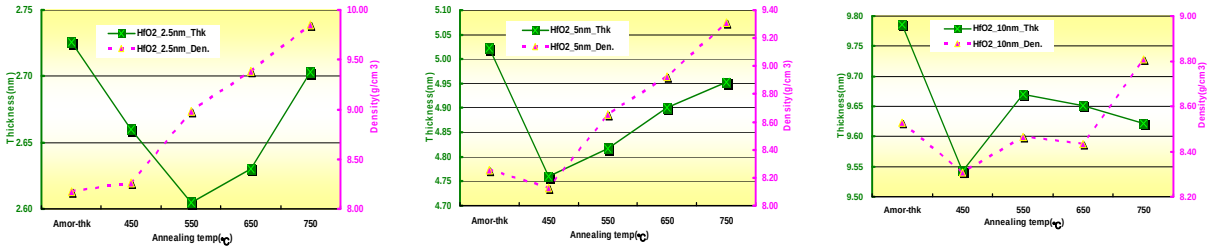
Post-Deposition Annealing Analysis for HfO2 Thin Films Using GIXRR/GIXRD

Wei-En Fu, Emma Chang and Yi-Ching Chen

Center for Measurement Standards, Industrial Technology Research Institute
Room 216, Building 8, 321, Sec. 2, Kuang Fu Road, Hsinchu, Taiwan

ABSTRACT

High-k materials, such as HfO_2, Al_2O_3, and many others, have been employed to replace SiO_2 insulator in gate dielectric device in order to offer significant gate leakage reduction [1-3]. In this study, the physical properties of hafnium dioxide (HfO_2) thin films in the cases of 'as-deposited' and 'post-deposition annealing' (PDA) were analyzed and characterized. Ultra-thin hafnium dioxide films of thickness 2.5, 5 and 10 nm were deposited on Si (100) substrates using atomic layer deposition (ALD) at temperature of 300 . After deposition, the films were annealed using furnace in Ar ambient for 10 minutes at 450 , 550 , 650 and 750 . The thickness, density, roughness and the crystalline evolution of the HfO_2 films were investigated by Grazing Incidence X-Ray Reflectometry (GIXRR) and Grazing Incidence X-Ray Diffraction (GIXRD) for both as-deposited and post-annealing conditions. Transmission Electron Microscope (TEM) was used to provide image verification of the two-layer model applied in XRR fitting analysis. Furthermore, the grain sizes were evaluated by X-ray diffraction peak-broadening (full width at half maximum, FWHM) calculation according to the Scherrer method. The experimental results showed that the annealing temperatures had significant impact on the thickness, density and roughness of the HfO_2 and SiO_2 layers, as shown in Figure 1. In addition, the experimental results demonstrated the grain sizes depend on not only the thickness of the film, but also the annealing temperatures in the crystallization process.



(a) 2.5 nm HfO_2 (b) 5 nm HfO_2 (c) 10 nm HfO_2

FIGURE 1. The divergence of the density and the thickness for HfO_2 for as-deposition and annealing films.

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KEY WORDS: High-k materials; Grazing incidence X-ray reflection; Grain size

8-1

Progress Towards Low Vacuum Critical Dimension Metrology

Brad Thiel and Vaso Tileli

College of Nanoscale Science and Engineering, University at Albany, 255 Fuller Road, Albany, NY 12203

ABSTRACT

Two of the most persistent and difficult challenges for electron beam-based critical dimension metrology are electronic charging and hydrocarbon contamination. These phenomena are particularly problematic for highly insulating systems, such as photolithographic masks. Low vacuum scanning electron microscopy addresses both of these issues by creating a weak plasma in the gas surrounding the mask (~10 Pa). The resolution of the most advanced versions of these tools is comparable to their high vacuum counterparts, therefore making the technology a viable solution.[1] The presence of a gas, however, means that the probe characteristics and secondary electron amplification, detection, and signal-to-noise ratio differ significantly from conventional high vacuum tools. In order for low vacuum approaches to be viable, all of the processes must be understood and described with the accuracy currently available on high vacuum systems. This talk will outline the basic principles of the technology and demonstrate the charge control and contamination reduction capabilities. Progress towards analytical descriptions for probe characteristics, signal amplification, and signal-to-noise ratio will be presented.

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8-2

Nanotechnology: An Overview and Impact on Metrology

M. Meyyappan

NASA Ames Research Center, Moffett Field, CA 94035

ABSTRACT

There is a tremendous amount of activity across the world on nanostructured materials and their applications in a wide range of fields. These materials are different from their bulk counterparts in physical, chemical, electrical. mechanical. optical, magnetic and other properties. Industrial metrology practices rely on one or more of these properties to develop the instruments, equipments and approaches; so it is easy to see the potential of nanostructured materials in developing future metrology systems. This talk will provide an overview of nanotechnology developments related to metrology. Specific examples will include carbon nanotubes(CNTs) as atomic force microscopy(AFM) probes, miniaturization of spectrometers and instruments such as SEM , and X-ray spectrometers using CNT field emission electron sources and various sensors and finally the use of in-situ exteriments in TEM to determine melting point of nanomaterials while imaging. The author acknowledges contributions from Cattien Nguyen, Xuhui Sun, Bin Yu, Jing Li, Y. Lu, Prabhu Arumugam, Hua Chen, and Jun Li.

8-3

Aberration-Corrected TEM For Nanoelectronics Applications (include multi-slice modeling)

Christian Kisielowski

National Center for Electron Microscopy, Lawrence Berkeley National Laboratory, One Cyclotron Rd, Berkeley, CA 94720, USA

ABSTRACT

In recent years a new generation aberration-corrected electron microscopes is being developed within DoE's TEAM project[1]. A prototype instrument became user facility in 2008[2] that currently performs at a resolution limit around 0.5Å in scanning (STEM) and stationary (TEM) imaging modes[2]. In particular the instrument enables lattice imaging at 80 kV with a resolution below 1 Å, which was exploited to provide outstanding images of single carbon atoms and defects in graphene[3,4]. The availability of a monochromator[5], a high brightness gun[6] and aberration correction are key hardware elements for this achievement. Scientifically, there is growing interest in utilizing graphene as a novel material for nanoelectronics[7].

However, the high performance of such instruments requires a fresh assessment of microscope capabilities. For example, image resolution is not longer limited by instrument parameters. Instead, it is now limited by the objects themselves[8]. A narrow focal spread of only 0.7 nm – 1 nm in TEM mode does not necessarily ease image interpretation[2]. Instead, image analysis is generally more complex even if aberration correctors are employed. Further, radiation damage becomes a limiting factor that, however, can be addressed[4]. As a result, it is essential to maintain a close relation between experiments and image simulations.

This contribution addresses such aspects by comparing experimental results with image simulations obtained for graphene and for thin films of germanium crystals[9]. It will be shown that signal-to-noise ratios have improved to an extend that allows for single atom detection across the Periodic System of Elements. Image simulations can be used to adequately describe the experiments. Noise remains a limiting factor as shown in Figure 1. Further it becomes obvious that a reconstruction of the electron exit wave function from focus series of lattice images holds intrinsic advantages if compared with direct imaging of the crystal structure. Single, aberration-corrected images are only directly interpretable if the crystal thickness is homogeneous across the field of view and comparable with the focal spread of < 1 nm. In spite of increasingly complex experiments, the three-dimensional structure of thin crystals can now be recovered from a single projection if prior knowledge of the crystal periodicity is exploited.

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Keywords: Aberration-corrected electron microscopy, graphene, image simulations

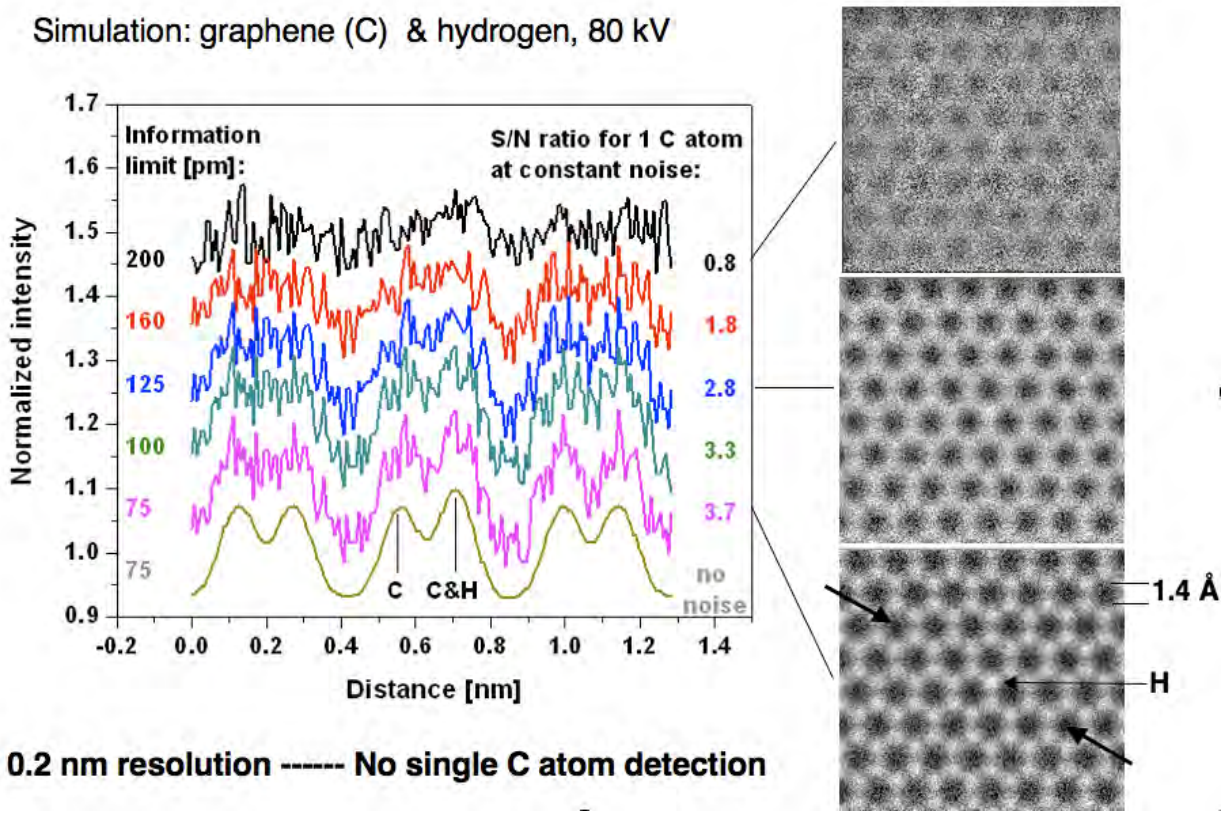

FIGURE 1. Image simulation of a hydrogen atom attached to a sheet of graphene. The effects of noise and resolution are considered. It is unknown if a hydrogen atom can be kept in place in the presence of beam damage. A signal-to-noise ratio of better than 4 would be required for the detection of a single hydrogen atom.

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8-4

Corrected Electron Optics - Improved Resolution and New Analysis Capabilities

M. Steigerwald, G. Benner, U. Mantz, and D. Preikszas

Carl Zeiss NTS GmbH, Carl Zeiss Strasse 56, 73447 Oberkochen, Germany

ABSTRACT

Semiconductor Process Control has always been the key to successful and fast development of new technologies and good yield. In the past, the use of charged particle microscopes in wafer fabs have been restricted to mainly CD measurements and SEM review for inline process control purposes and high-resolution TEM imaging in the analysis lab. For technology nodes below 100 nm, new materials and 3D structures are important factors for success towards progression on the ITRS roadmap. Unfortunately, with increasing complexity, process variations across a wafer as well as within chips start to significantly contribute to yield loss. Even worse, traditional metrology techniques that are based on wafer test sites or large spot test wafer analysis methods cannot fulfill today's requirements of high-resolution, local process characterization.

Innovative charged particle imaging instruments overcome many of the limitations of conventional analysis methods. Resolution improvements and enhanced analysis capabilities are achieved by advanced SEM and TEM electron optics as well as innovative detector schemes.

In our presentation we will discuss in a first part a mirror-corrected SEM, offering high-resolution analytics with efficient productivity to visualize even the most sensitive materials by use of electrons with energies far below 1 keV. At these energies the resolution of conventional instruments is often very low, but compensating for the aberrations of the objective lens can overcome this obstacle. The aberration correction by means of an electron mirror significantly increases the resolution especially for low energies [1]. For example, a resolution well below 1 nm at a primary energy of 500 eV seems to be possible. Additionally, the beam separator that is used for incorporating the electron mirror to the SEM column enables the detection of nearly all the signal electrons that are emitted or scattered from the sample. Even the analysis of these signal electrons based on their energy can be easily achieved.

The second part of this contribution will be focused on the application of high-resolution and energy-filtered TEMs. Nowadays, TEMs are available with spherical aberration correctors both in the imaging path (C_S TEM) and in the illumination system (C_S STEM). STEM methods are already widely used in Semiconductor industries. The C_S STEM provides a sub-angstrom resolution and 10 times higher probe currents. This results in an improved signal to noise ratio and makes the analysis faster and more reliable.

The integration of a C_S-corrector [2] in the TEM delivers a higher lateral resolution and dislocation-free imaging. This makes the TEM imaging suitable for the measurement of critical dimensions (gate oxides) down to the one angstrom range, which in the past could only be examined by STEM methods. Equipped with a highly corrected imaging energy filter and a monochromator the EFTEM features highly resolved spectroscopy e.g. for band gap measurements. Furthermore, the acquiring of EFTEM series (Spectrum Imaging) at the nanometer scale with an energy resolution < 0.2 eV enables the investigation of the interaction of light and material required for optoelectronics and nanophotonics.

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Energy filtered PhotoElectron Microscopy

K. Winkler[*1], M. Escher[+], B. Krömker[*], D. Funnemann[*]

[*]*Omicron NanoTechnology GmbH, Limburgerstr. 75, 65232 Taunusstein, Germany*
[+]*FOCUS GmbH, Neukirchner Str. 2, 65510 Hünstetten-Kesselbach, Germany*

ABSTRACT

Photoelectron emission microscopy (PEEM) in combination with a high-resolution energy filter (ΔE in the 100meV regime)[1] is a non-destructive and versatile surface characterisation technique with the ability to solve upcoming scientific metrology issues [2].

Looking at the Roadmap for Semiconductors today, scaling down of devices faces growing complexity of the related issues. To overcome these issues often requires detailed analysis at a local scale where understanding of materials in the form of small objects or patterns is of great importance. Hence the need for new spatially-resolved, non-destructive and comprehensive analysis tools becomes clear.

To identify the chemical compounds in a local sample area, energy-filtered PEEM is a very valuable metrology tool combining high spatial resolution with high-resolution spectroscopy. Continuous improvements of PEEM instruments nowadays enable local nano-spectroscopy with the highest lateral resolution in convenient laboratory conditions [3]. Imaging XPS with unsurpassed lateral resolution and quantitative analysis of the local work function allow for a detailed understanding of the surface chemistry, including locally resolved doping effects [4] on small structures used for semiconductor devices and even smaller silicon nano-wires[5].

In addition, recent experiments have shown the feasibility for a new class of experiments for band structure analysis. Advanced spectroscopic PEEM instruments allow a new approach to analyse the electronic structures of samples. Thus band structure mapping with a large acceptance angle of ±90° without the need for eucentric sample rotation becomes possible [6]. Together with full control over the analysed local area, the technique is ideally suited to investigate the electronic properties of single grains or small devices. Hence, this method opens up the path to a new class of experiments allowing e.g. dedicated local band structure tailoring.

The instrument's performance strongly depends on the availability of the highest brightness and high energy light sources. Emerging technology from the growing market for CW and pulsed lasers in the UV and XUV regimes has recently also greatly improved this situation.

To identify potential device and materials technologies or to extend and compliment CMOS technology often requires a deep understanding of the basic materials science. In this field energy-filtered PEEM has established itself as a valuable surface metrology technique with numerous contributions to basic materials research. Copper, as it progressively replaces aluminium for interconnects, has an increasing importance in micro- and nano-electronics. The PEEM technique has helped to better understand the preparation processes leading to microstructured crystallization. Today PEEM instruments play a key role in the growing field of plasmon and plasmon dynamics research [7,8]. Moreover, the growing number of major scientific contributions have also helped to gain a deeper understanding of magnetic devices [e.g. 9].

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[1] [*]k.winkler@omicron.de

8-6

Understanding the Imaging and Metrology using the Helium Ion Microscopy

Michael T. Postek. Andras E. Vladar and Bin Ming

Manufacturing Engineering Laboratory
Precision Engineering Division
National Institute of Standards and Technology,
100 Bureau Drive MS 8210
Gaithersburg, MD 20899

ABSTRACT

Instrument resolution remains one barrier to innovation confronting all phases of nanotechnology. The scanning and transmission electron microscopes have incrementally improved in performance and other scanned probe technologies such as atomic force microscopy, scanning tunneling microscopy and focused ion beam have all been applied to nanotechnology with various levels of success. A new tool for nanotechnology is the scanning Helium Ion Microscope (HeIM). The HeIM is a new approach to imaging and metrology for nanotechnology which may be able to overcome this barrier. As a new methodology, it is just beginning to show promise and the plethora of potentially advantageous applications for nanotechnology and nanometrology have yet to be exploited. This presentation will discuss some of the progress made in understanding the imaging and metrology for semiconductor research using this new instrumentation.

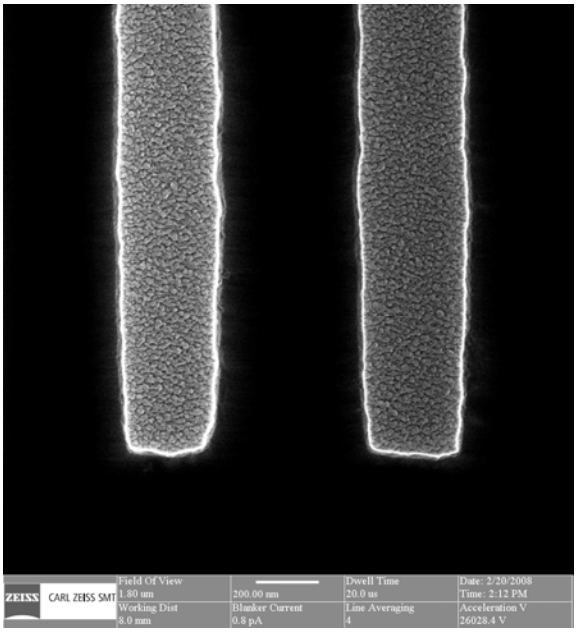

FIGURE 1. Chromium on quarts photomask viewed in the helium ion microscope (field of view = 1.8 um).

Simulations of Scatterometry Down to 22 nm Structure Sizes and Beyond

W. Osten[*a], V. Ferreras Paz[a], K. Frenner[a], T. Schuster[a], H. Bloess[b]

[a]*Institute of Applied Optics, Stuttgart University,Pfaffenwaldring 9, 70569 Stuttgart, Germany*
[b] *Qimonda Dresden, Koenigsbruecker Str. 180, 01099 Dresden, Germany*
** corresponding author: osten@ito.uni-stuttgart.de, Tel. +49(0)71168566074*

ABSTRACT

In recent years, scatterometry has become one of the most commonly used methods for CD metrology [1]. With decreasing structure size for future technology nodes, the search for optimized scatterometry measurement configurations gets more important to exploit maximum sensitivity. As widespread industrial scatterometry tools mainly still use a pre-set measurement configuration, there are still free parameters to improve sensitivity. Our current work uses a simulation based approach to predict and optimize sensitivity of future technology nodes. Since line edge roughness is getting important for such small structures, these imperfections of the periodic continuation cannot be neglected. Using fourier methods like e.g. rigorous coupled wave approach (RCWA) for diffraction calculus, nonperiodic features are hard to reach. We show that in this field certain types of fieldstitching methods [2] show nice numerical behaviour and lead to useful results.

a) b) c)

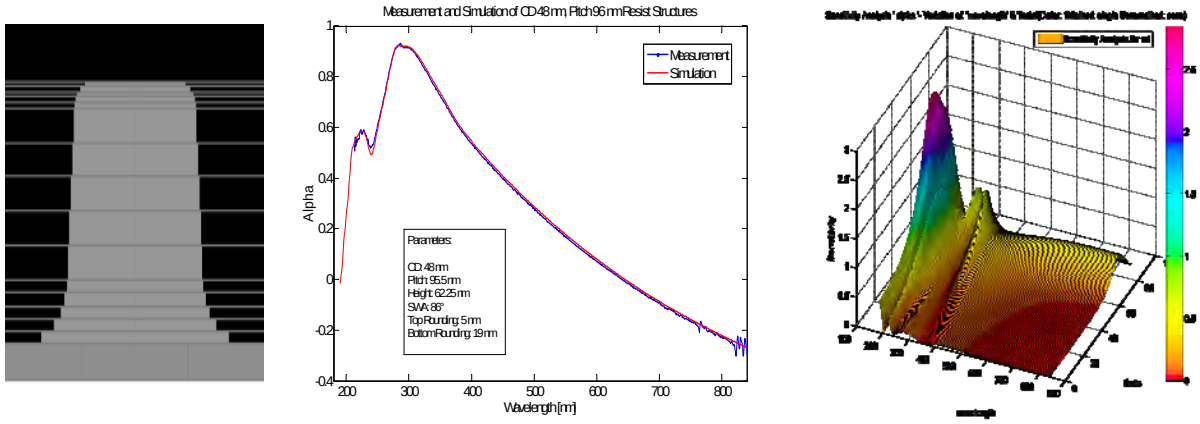

FIGURE 1. a) modelling, b) measuring, c) simulating : steps towards CD - sensitivity analysis for scatterometry

KEYWORDS: scatterometry, LER, RCWA

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9-2

Challenges and Opportunities for Modeling and Simulation

Mark Lundstrom
Network for Computational Nanotechnology
Birck Nanotechnology Center
Purdue University, West Lafayette, Indiana

Simulation has played a critical role in the success of the electronics industry since the development of Spice 1 by Nagel and Pederson in 1971. With the development in the 1980's by Bob Dutton and Jim Plummer of the integrated circuit manufacturing process simulator, SUPREM and of device simulation programs like Mark Pinto's PISCES-II, simulation became an integral part of device and process research and development. Today, computer simulation is integral to semiconductor device research, development, design, and analysis. There is certainly more to Moore's Law, and more and more powerful CAD tools will be essential to realize the ultimate potential of silicon technology. At the same time, shrinking device dimensions, increasing sensitivity to atomistic details, statistical variations in devices, increasing densities of devices, and reliability concerns will require increasingly sophisticated CAD tools. Developing such tool presents many challenges, and the economic stakes are enormous, but the challenges and opportunities are reasonably well understood to the point where pre-competitive industry roadmaps can be defined to develop industry-wide solutions. My purpose in this talk is to address other challenges.

Research in nanoelectronics is characterized by an enormous breadth. Nanotubes, nanowires, nanonets, graphene, spintronics, and bio-electronics are just a few examples. One can envision two scenarios for the development of this field. The first is that new technologies emerge from research to either compliment traditional electronics or to address markets not well addressed by current technologies. The second is that the techniques and understanding being developed in nanoelectronics research be refined and developed and applied to problems in conventional electronics, which more and more involve nanotechnology. Nanoelectronic devices present two challenges to the traditional way that we simulate devices. The first is the need to address quantum mechanical effects - often including details at the atomistic level. The second is the need to simulate electronic transport in random media – nanostructured materials, silicon with random dopant fluctuations, nanocomposites, polycrystalline and amorphous materials. Atomistic, quantum level models are rarely suitable for such problems. We believe that engineers will need to develop a fundamentally new conceptual and computational framework to address the challenges and opportunities presented by nanotechnology.

Making simulation effective involves social as well as technical aspects. Computational experts are not monolithic; many different types of people develop and use simulations. According to Leo Kadanoff, there are three different reasons to simulate: 1) to explore uncharted territory, 2) to resolve a well-posed question, and 3) to make a good design. Simulation programs are developed for two different reasons: 1) for answers and understanding, and 2) for software that allows others to answer questions and develop understanding. Finally, there are two different types of engineers and scientists: 1) builders or experimentalists and 2) theorists or analysts. For simulation to be effective, those who develop simulations must be connected with those who do the experiments or design and build the devices. Just as important, however, is the challenge of creating a community of the very broad range of scientists and engineers who develop and use simulation. The Network for Computational Nanotechnology (www.ncn.purdue.edu) was created to address these challenges, and one of its key strategies involves the creative application of cyberinfrastructure embodied in its science gateway, nanoHUB.org, which now serves an international user base of more than 90,000. This talk will describe some of the approaches that NCN is taking to the scientific and social challenges of making simulation an effective partner with theory and experiment in realizing the opportunities for electronic device research and manufacturing in the 21srt Century.

10-1

Pushing Resists To Their Limits: Creating New Targets for Metrology

Christopher K. Ober

Materials Science and Engineering
Cornell University
310 Bar Hall, Ithaca, NY 14853

ABSTRACT

New approaches to patterning and lithography are enabling the large-scale creation of patterned structures smaller that 20 nm. In all cases, untraditional materials are being used and will demand the need for new methods of metrology. This presentation will discuss two classes of patterning materials, molecular glass resists and self-assembling block copolymers, in the context of their performance and what questions need to be answered in terms of near molecular level characterization.

The first type, molecular glass photoresists [1], are organic materials of small molecular size, with many of the characteristics of polymers. Recent results suggest that there is general improvement in LER provided that diffusion of resist components is minimized. Improved metrology of molecular level aspects of glass resists may enable greatly improved performance.

Similarly, new block copolymer resists lack appropriate metrology tools for assessing their self-assembly characteristics [2]. An improved in-situ assessment of the processing of these materials may lead to even greater control over their pattern formation. Techniques such as grazing incidence small angle X-ray scattering (GISAXS) and near edge X-ray absorption fine structure (NEXAFS) studies, both synchrotron based methods, will be discussed.

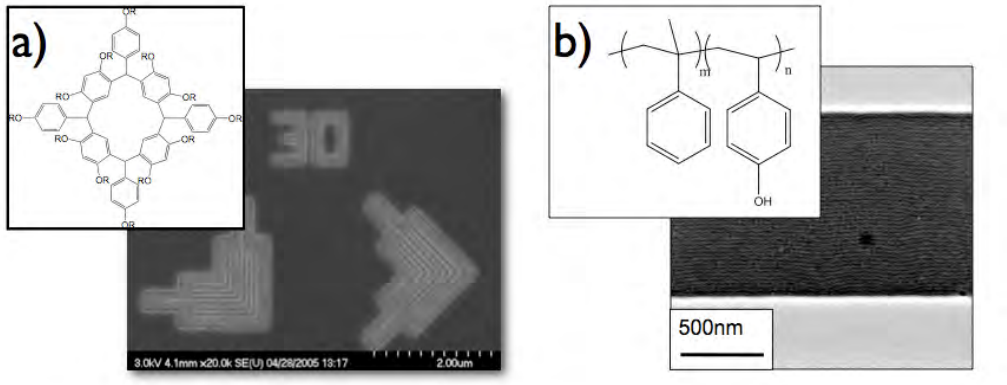

FIGURE 1. a) Molecular glass resist and pattern: block copolymer resist and parallel lines using graphoepitaxy.

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10-2

Metrology for Advanced Patterning and Overlay

Bart Rijpers[1], Arie den Boef

ASML, R&D, PO BOX 324, 5500 AH Veldhoven, The Netherlands

ABSTRACT

At the 45 nm technology node more advanced Metrology techniques are used. Proven techniques such as top down CD-SEM after litho and etch processes will continue to be utilized throughout the introduction of new technology nodes. More advanced techniques such as Scatterometry will be used more often than before, because the information provided by CD-SEM is not sufficient anymore and in some cases not accurate [2]. Cross section Metrology is needed to calibrate these Scatterometry models, for the development and optimization of resist and etch processes, for the calibration of CD-SEM equipment and for the development of more advanced process flows such as Double Patterning Lithography [3]. For all these applications Measurement Uncertainty plays an important role at the 45 nm node and beyond. The generation of statistically valid information is needed when for example scatterometry and cross section STEM data are compared. Scatterometry is using a large measurement spot (in the order of several 10's of microns) whereas STEM is a local measurement technique. Comparing one STEM image with a scatterometry data point will not be successful, because of the high sampling uncertainty of STEM compared to scatterometry [4]. In this paper we present a new and patented technique called MUSCLE [1] to generate statistically valid profile information. We will show the advantage of this technique and will show how this information is used to calibrate scatterometry models used for CD and Overlay Metrology. Sampling Uncertainty can be successfully reduced when this MUSCLE technique is used for the analysis of STEM cross section data. Also, this technique will give information on Line Width Roughness in two dimensions. The use of this information for the development of advanced patterning methods will be explained.

[1] Bart.rijpers@asml.com, phone: +31 40 268 5721, fax: +31 40 268 4550

Keywords: Cross Section Metrology, STEM, scatterometry

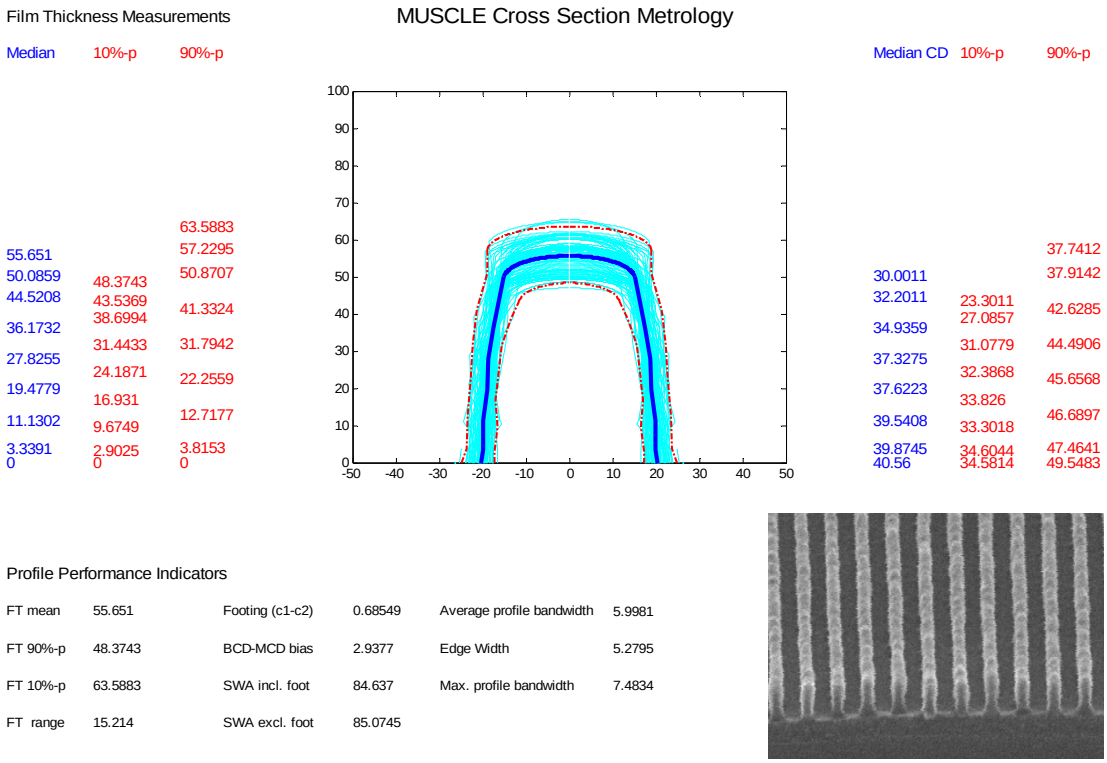

FIGURE 1. Results from MUSCLE [1] cross section analysis using 90 averaged profiles. Inlay is a cross section SEM image of the same location. Clearly, the information content of the SEM image is not sufficient for comparison with Scatterometry models. Also LWR information cannot be deduced from these type of images.

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10-3

Mask Metrology – Current and Future Challenges

Greg Hughes

SEMATECH
257 Fuller Road Suite 2200
Albany, NY 12203

ABSTRACT

The mask-making challenges and the metrology needed to address the challenges are constantly changing and posing more barriers. Not only are the specifications becoming continuously more stringent as the industry tries to keep up with the ITRS, but the mask technologies are changing with the new forms of mask that the next generation lithography dictates (e.g., EUV masks and nanoimprint masks). Both traditional specifications must be tightened, along with the metrology, as well as the pattern environment within which the metrology works. With the intensive use of optical proximity correction (OPC), the device patterns within a chip field become very complex and difficult to measure, yet it is the metrology on these patterns that best represents the important images that will be printed on the wafer.

This paper will highlight these new challenges to mask making and the metrology that is needed to support it. In particular, issues of critical dimension (CD), pattern registration, defect inspection and review, phase, and transmission and reflection metrology as applied to die patterns on optical, EUVL, and imprint masks will be elaborated.

TH-01

Thermal Diffusivity and Boundary Resistance Analyses in Resistance Random Access Memory (ReRAM)

Hiro Akinaga and Hisashi Shima*

Nanodevice Innovation Research Center,
National Institute of Advanced Industrial Science and Technology (AIST),
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan
**Nanotechnology Research Institute, AIST*
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan

ABSTRACT

Resistance random access memory, ReRAM, having a metal/oxide/metal trilayer structure is drawing much attention as a high-density, high-speed and low-power-consumption nonvolatile memory. Recently, we have demonstrated that the low-current and high-speed resistance switching as well as the excellent controllability of the resistance in CoO-based ReRAM with the Ta electrode, where the trilayer consists essentially of Ta / CoO / Pt [1]. Since the huge resistance switching comes from the electrochemical redox reaction at the heterointerface between Ta and CoO, the thermal management at the heterointerface is crucial to improve the reliability of the ReRAM performance. The redox reaction is considered to be affected by current-induced Joule heating. In this contribution we report the successful quantitative characterization of the thermal diffusivity and the thermal boundary resistance of the CoO-based ReRAM structure.

Figure 1 show the temperature development curve generated by one pulse application of heat. The signal was taken in the Ta / CoO / Pt stacking layer. The thermal diffusivity and boundary resistance can be determined from the areal diffusion time of samples with different thicknesses and the curve-fitting analyses (not shown) [2]. The boundary resistance of the Ta and CoO heterointerface was determined to be about 2.7×10^{-9} m^2K/W, which was larger than that at the Pt / CoO interface. This fact agrees well to the fact that the switching operation of ReRAM with the Ta / CoO interface is better than that of ReRAM only with the Pt / CoO interface. The detailed model and the explanation will be shown in the conference.

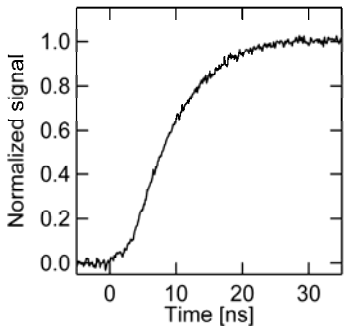

FIGURE 1. Temperature development curve taken in the Ta / CoO / Pt stacking layer.

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Keywords: ReRAM, Thermal diffusivity, Thermal boundary resistance

TH-02

Lithography with Helium Ions

Donald Winston[1], Bryan M. Cord[1], Bin Ming[2], David C. Bell[3], William F. DiNatale[4], Lewis A. Stern[4], Andras E. Vladar[2], Michael T. Postek[2], Mark K. Mondol[1], and Karl K. Berggren[1]

[1]*Massachusetts Institute of Technology, Cambridge, MA 02139*
[2]*National Institute of Standards and Technology, Gaithersburg, MD 20899*
[3]*Harvard University, Massachusetts Hall, Cambridge, MA 02138*
[4]*Carl Zeiss SMT Inc., Peabody, MA 01960*

ABSTRACT

Focused ion-beam lithography[1] is not as widely practiced as scanning-electron-beam lithography, in part due to resolution constraints and in part due to substrate sputtering. Helium ions, which cause less sputtering than larger ions, achieved ~ 200 nm lithographic resolution as early as twenty years ago[2]. Recently, a sub-1-nm-resolution scanning-helium-ion microscope was commercialized[3]. We have used this microscope to investigate lithography of poly(methyl methacrylate) (PMMA) and hydrogen silsesquioxane (HSQ) on silicon. As shown in Figure 1, resolution of ~ 10 nm was achieved in HSQ using a computer-controlled pattern generator and a salty development process[4].

Key words: lithography, helium-ion, HSQ

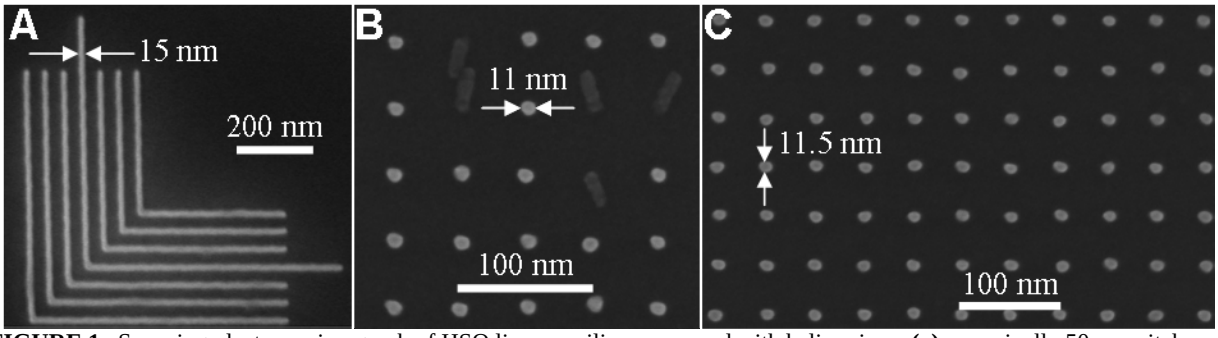

FIGURE 1. Scanning-electron micrograph of HSQ lines on silicon, exposed with helium ions; **(a)** a nominally 50-nm-pitch nested "L" pattern; **(b)** a "pillar" array in which some of the HSQ pillars have fallen, showing a 3:1 aspect ratio ; **(c)** a pillar array of higher dose than in (b), resulting in fewer pillar collapses.

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TH-03

Abstract Withdrawn

TH-04

PREDICTING OVERLAY DISTORTIONS ON A LITHO-SCANNER

Kevin T. Turner[1] and Jaydeep Sinha[2*]

[1]Department of Mechanical Engineering, University of Wisconsin, Madison, WI 53706
[2]Wafer Inspection Group, KLA-Tencor, 3 Technology Drive, Milpitas, CA 95035.
[*]contact author: jaydeep.sinha@kla-tencor.com

Wafer geometry variations result in elastic deformation that can cause significant in-plane distortion and overlay errors in lithographic patterning. As feature sizes shrink, overlay errors due to wafer geometry on a scanner before patterning become a larger fraction of the error budget and must be controlled. In this work, a finite element mechanics model and lithographic correction post processing scheme was developed to predict overlay errors from high-density wafer shape measurements on KLA-Tencor's WaferSight 2 tool. Using the model, overlay errors due to chucking were examined for multiple wafers with different geometries. The results show that long spatial wavelength corrections cause significant distortion, but can be largely mitigated through the use of simple first-order corrections applied on a typical lithography scanner. In contrast, higher frequency spatial variations cause distortions that cannot be corrected and hence can lead to meaningful overlay errors. The results presented provide fundamental insight into chucking-induced overlay errors and can serve as a basis for the development of higher order scanner correction schemes that explicitly account for the wafer geometry. Wafer geometry measurements can also be used by the scanner to meet the overlay requirements at smaller nodes.

TH-05

A Comparison of Linewidth Measurements on sub-20 nm Graphene Nanostructures

J.J. Peterson [1] , M.A. Rodriguez [2] , V. Tileli [2] , M. Sprinkle [3] , C. Berger [3] , B.L. Thiel [2], W.A. de Heer [3]

1 Intel Corporation Assignee to INDEX, 255 Fuller Road, Albany, NY 12203

2 University at Albany-SUNY, 255 Fuller Road, Albany, NY 12203

3 School of Physics, Georgia Institute of Technology, Atlanta, GA 30332.

ABSTRACT

Although linewidth measurements of patterned graphene nanoribbons using the high resolution (HR) scanning electron microscope (SEM) have been reported in the literature [1], it is known that such measurements are generally destructive to the structures which are being measured. Furthermore, due to the destructiveness of the measurement, the critical dimensions may be changing even as the measurement is being made. For this reason, the atomic force microsope (AFM) and scanning probe microscope (SPM) has become an accepted method of linewidth measurement for graphene or hydrogen silsesquioxane (HSQ) on graphene structures [2], but this methodology is not scaleable to a manufacturing environment. For this reason, it is desired that a more manufacturable method of linewidth measurement may be developed for measurement of critical dimensions of graphene nanostructures. In this talk, we compare linewidth measurements sub-20 nm HSQ/graphene structures using the HR SEM and environmental-SEM (E-SEM) and report that E-SEM measurements will support the necessary resolution to enable linewidth measurements of graphene nanostructures without the damage associated with typical HR scanning electron microscopes. Furthermore, we make a comparison of linewidth measurements using both the SPM and E-SEM and discuss each respective method's advantages and disadvantages.

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TH-06

Integrated ODP Metrology Matching To Reference Metrology For Lithography Process Control

Patrick Kearney[1)], Junichi Uchida[1)] Sebastien Egret[1)], Heiko Weichert [1),]
Dmitriy Likhachev[2)], Göran Fleischer[3)]

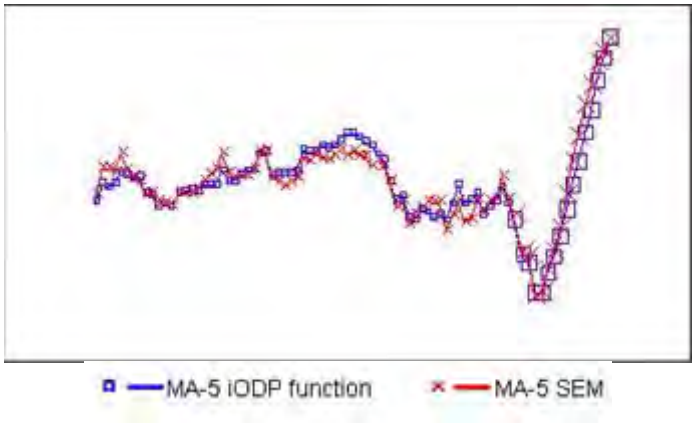
[1)] Tokyo Electron Europe Limited, German Branch, Moritzburger Weg 67, 01109 Dresden, Germany
[2)] Timbre Technologies, Inc., 2953 Bunker Hill Lane, #301, Santa Clara, CA 95054, U.S.A.
[3)] Qimonda Dresden GmbH & Co. OHG, QD P LM AM, Koenigsbruecker Str. 180, 01099 Dresden, Germany

ABSTRACT

Advanced DRAM manufacturing demands rigorous and tight process control using high measurement precision, accurate, traceable and high throughput metrology solutions. Scatterometry is one of the advanced metrology techniques which satisfies all of these requirements. Scatterometry has been implemented in semiconductor manufacturing for monitoring and controlling critical dimensions and other important structural parameters. One of the major contributing factors to the acceptance and implementation of scatterometry systems is the ability to match to reference metrology. Failure to understand the optimum matching conditions, can lead to wrong conclusions with respect to hardware stability and/or incorrect analysis of production data.

This paper shows the use of the integrated scatterometry system to control the lithography processes in a real production environment. In the control system, the scatterometry Optical Digital Profilometry (ODP^{TM}) data is referenced to sampled CD-SEM data. A significant improvement in matching between the two metrology systems was achieved following the implementation of a new (ODP^{TM})-*function*. The results also reveal a clearer roadmap for the implementation of an integrated scatterometry based control loop system. The results also pointed to how to achieve a reduced setup time as well as a deeper understanding of the relationship between test data and production data. It has been clearly shown that to achieve the desired sub-nanometer matching in scatterometry measurements for advanced process control, we need to pay scrupulous attention to matching data not only from test wafers but from production data in order to derive functions that will produce the optimum matching conditions.

FIGURE 1. iODP function data matched to SEM data using both FEM and production data.



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Keywords: scatterometry, integrated CD metrology, Optical Digital Profilometry (ODP^{TM}), reflectometry, reference metrology, matching

TH-07

A High Resolution X-Ray Reflectometry Study Of Extreme Ultraviolet Photoresists

R.J. Matyi and R.L. Brainard

College of Nanoscale Science and Engineering, University at Albany, Albany, New York 12203

ABSTRACT

As the semiconductor industry continues to follow Moore's Law, there is a continuing demand to generate smaller features using lithographic methods. Extreme ultraviolet (EUV, 13.5nm) lithography is the leading candidate for 22 nm half pitch manufacturing. Despite advances in EUV resists, simultaneously achieving the required resolution, line-edge roughness, and sensitivity remains a significant issue for EUV. These characteristics are sensitive to the physical properties of EUV photoresists, and we have employed high resolution X-ray reflectometry to better understand the relation between resist structure and its resultant properties and performance. Specular XRR scans (see Figure 1) have been recorded from a large number of EUV photoresists [1]. Accurate density measurements obtained by XRR were used in calculations of photoresist quantum yield and then relate the photochemical characteristics of the photoresists to lithographic performance. In all cases, a low-density layer was observed at the photoresist-substrate interface. The presence of this layer would be expected to alter the interfacial glass transition temperature of the resist and would thus affect its diffusion characteristics, thus altering lithographic performance. We have found, however, that the quantitative measure of the interfacial layer density is highly sensitive to details of the XRR analytical process. A rationalization for this sensitivity in terms of specular XRR measurement practice will be discussed.

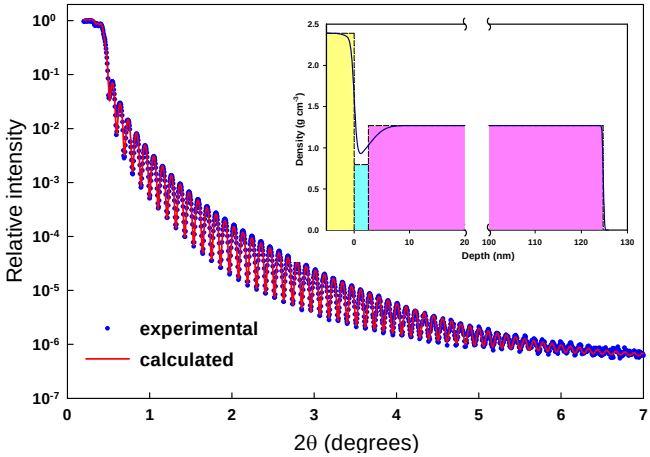

FIGURE 1. Experimental and calculated XRR profiles from EUV photoresist, with density profile in depth (inset)

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TH-08

Re-Calibration Of The SRM 2059 Master Standard Using Traceable Atomic Force Microscope Dimensional Metrology

Ronald Dixson, James Potzick, and Ndubuisi Orji

NIST Precision Engineering Division
100 Bureau Drive Stop 8212, Gaithersburg, MD 20899

ABSTRACT

The current photomask linewidth Standard Reference Material (SRM) supplied by the National Institute of Standards and Technology (NIST) is SRM 2059. [1] An in house tool developed at NIST, called the NIST ultra-violet (UV) microscope, was used as an optical comparator to calibrate the SRM 2059 photomasks for sale. One of the masks, serial number A013, was originally selected as an internal reference standard – and the features on this mask were calibrated using traceable critical dimension atomic force microscope (CD-AFM) dimensional metrology. Due to advances in CD-AFM metrology since the original work, it is now possible to refine the uncertainties on the reference mask. [2] In Fig. 1, the original and improved results on mask A013 are shown. More recently, we have performed measurements on a second mask, A006, which we plan to use as a supplemental reference mask to further improve uncertainties. When all the data have been analyzed, we expect to reduce the combined reported uncertainties for the nominal 0.25 μm linewidths by at least 40 %.

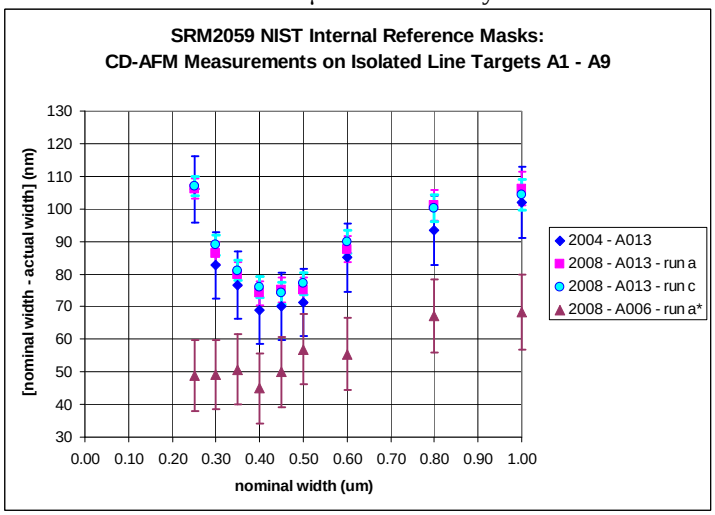

FIGURE 1. Current and prior CD-AFM measurements of isolated line features of SRM 2059 mask A013, and, now, on mask A006. Note that the large uncertainties on these preliminary mask A006 results are due to tip effects which we expect to reduce.

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Keywords: metrology, linewidth, photomask

TH-09

Measurements of Sub-30 nm structures over large areas using Grazing Incidence Small Angle X-ray Scattering

Ronald L. Jones[1], Kevin Yager[1], Chengqing Wang[1], Kwang-Woo Choi[2], Eric K. Lin[1], Wen-li Wu[1]

1 Polymers Division, National Institute of Standards and Technology, Gaithersburg, MD
2 Intel Corporation, Santa Clara, CA
3 Intel Corporation, Hillsboro, OR
4 Precision Engineering Division, National Institute of Standards and Technology, Gaithersburg, MD
5 International SEMATECH Manufacturing Initiative (ISMI), Austin, TX

ABSTRACT

Small Angle X-ray Scattering has the potential to provide critical measurement solutions for manufacturing of sub-30 nm structures by analysis of non-destructive diffraction of a sub-Angstrom wavelength beam on a sample with uniformly patterned areas. In contrast to transmission measurements developed by our group, termed "Critical Dimension SAXS", the grazing incidence geometry has the potential to provide additional information due to the surface sensitivity of the technique. The potential capability to compare top surface dimensions, nominally in the first 10-30 nm of the surface, relative to the bulk is challenged by the complex scattering models required to provide precise data due to factors such as resonance near the critical angle and multiple refraction. Additional complications are observed due to the balance of transmitted and reflected beams when measuring above the critical angle. We provide grazing incidence small angle x-ray scattering (GI-SAXS) data on a block copolymer system that assembles with sub-30 nm domains over large areas. The use of a block copolymer is motivated by its potential implications in discrete bit patterned media for data storage and potentially as a next generation fabrication technique in microelectronics. However the block copolymer is also a model system for development of GI-SAXS metrology due to the ability to measure the structure in transmission using Rotational Small Angle Neutron Scattering, providing a direct route to develop precise models of depth dependent structure in GI-SAXS. Results are shown for a series of GI-SAXS conditions and models are compared to R-SANS, scanning force microscopy, and x-ray reflectivity.

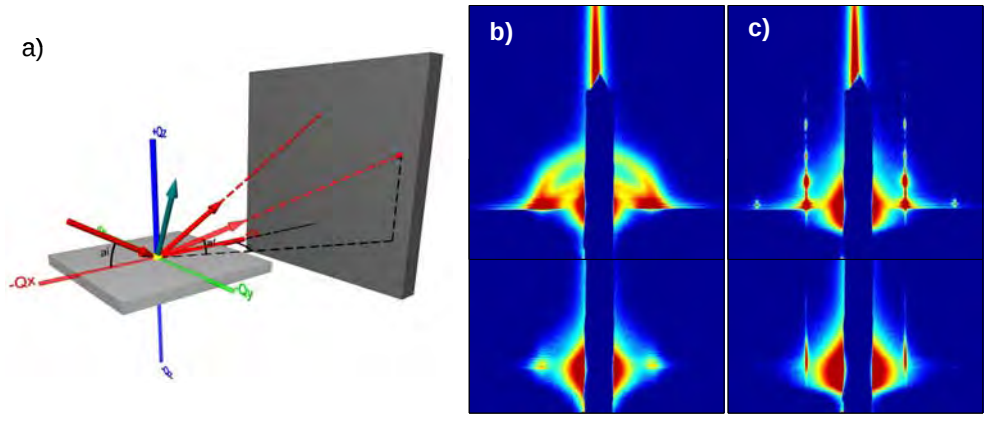

FIGURE 1. GI-SAXS geometry shown in (a) is used to measure a block copolymer organizing into sub-30 nm domains over large areas, starting off as an isotropically oriented phase (b) and evolving into an ordered phase (c).

TH-010

A novel wafer-plane dosimeter for EUV lithography

Steven Grantham and Charles Tarrio

National Institute of Standards and Technology
100 Bureau Drive
Gaithersburg, MD 20899

ABSTRACT

Extreme Ultraviolet Lithography (EUVL) incorporates 13.5 nm light for patterning wafers and requires in-situ wafer-plane dosimetry that can be tailored to the requirements of an EUVL stepper's environment. There are several types of detectors that are sensitive to EUV radiation including photodiodes, CCDs, scintillators, and pyroelectrics to name a few. All of these require electrical connections and can be intrusive in a stepper's projection optics box and will deteriorate with time causing changes to their calibration. The community has settled on using photoresist as a dosimeter in the wafer-plane because it is a convenient non-intrusive way to measure the dose in the wafer plane an it has very little overhead in the fab environment. However, recent experiments have found that the accepted values for the dose-to-clear for resists may not be accurate.[1] In addition, dosimetry using a photoresist can be dependent on fab conditions and cause uncertainty due to varying process conditions.

NIST has recently begun working on a wafer plane dosimeter, based on storage phosphor technology, which can pass through a stepper as a wafer surrogate. Storage phosphors act as passive detectors that store latent images until they are read out using a visible light laser-based scanner. They are sensitive to 13.5 nm and are linear over at least 4 orders of magnitude. A dosimeter based on storage phosphor can be constructed in a configuration such that it mimics a wafer and can be passed through a stepper just like a wafer. In addition, storage phosphors are reusable and can be recalibrated as needed. EUV-sensitive storage phosphors are extremely sensitive and tend to saturate at levels of order a few $\mu J/cm^2$, however we have developed attenuating polymer layers that can be deposited on the front surfaces. In this paper we will present the dosimeter along with the results of several experiments that characterize the performance of the dosimeter at 13.5 nm, such as in the attached figure.

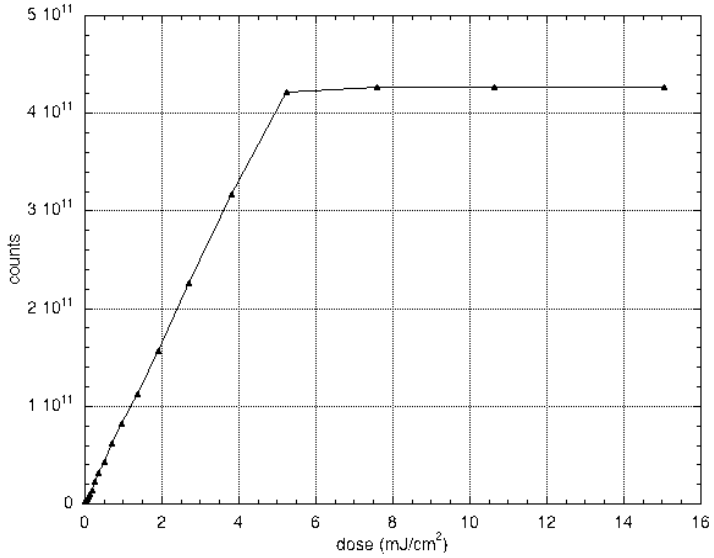

Figure 1. Storage phosphor count rate vs. incident dose, measured at 13.5 nm. Note the linearity up to ~5 mJ/cm2 and saturation at higher doses. The saturation level can be controlled by changing the thickness of a filter material on the front surface.

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Keywords: EUV lithography, EUV dosimetry wafer plane dosimeter

TH-011

Cross Sectional Characterization of Sub-50 nm Structures Using CD-SAXS

Chengqing Wang [1], Ronald L. Jones [1], Kwang-Woo Choi [2], Derek Ho[1], Eric K. Lin[1], Wen-li Wu [1], James S. Clarke [3], John S. Villarrubia [4], Benjamin Bunday [5]

1 Polymers Division, National Institute of Standards and Technology, Gaithersburg, MD
2 Intel Corporation, Santa Clara, CA
3 Intel Corporation, Hillsboro, OR
4 Precision Engineering Division, National Institute of Standards and Technology, Gaithersburg, MD
5 International SEMATECH Manufacturing Initiative (ISMI), Austin, TX

ABSTRACT

Critical dimension small angle x-ray scattering (CD-SAXS) is capable of measuring the average cross section and sidewall roughness in patterns ranging from 10 to 500 nm in pitch with a sub-nm precision[1]. These capabilities are obtained by measuring and modeling the scattering intensities of a collimated X-ray beam in transmission configuration with sub-Angstrom wavelength from a periodic pattern such as line gratings, arrays of vials and posts. In this work we evaluate the capability of both a laboratory based and a synchrotron based CD-SAXS equipment for line-width and line-width roughness (LWR) characterization. The test samples are line gratings with sub-50 nm linewidth and with programmed LWR fabricated with EUV lithography. An example of data comparison between the laboratory based and a synchrotron based instruments is given below, a linear correlation is observed with a slope of 0.985. The comparison of LWR results between CD-SAXS and top-down scanning electron microscopy will be discussed. In addition, the application of CD-SAXS to measure the thickness of high k dielectrics in FinFET will also be discussed.

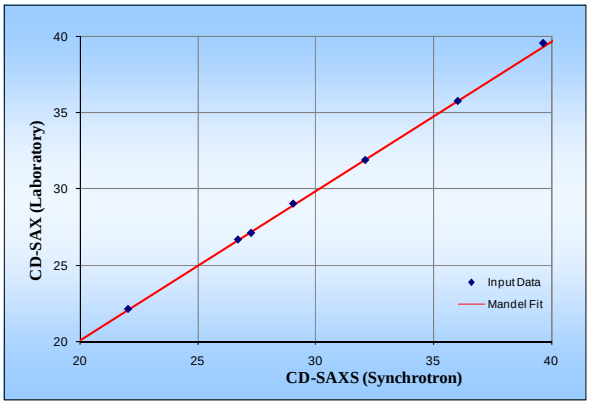

FIGURE 1. Excellent agreement was observed between the line width results measured with our laboratory based SAXS instrument and the synchrotron based one.

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TH-012

Interference Microscopy For Semiconductor Backend Patterning Metrology

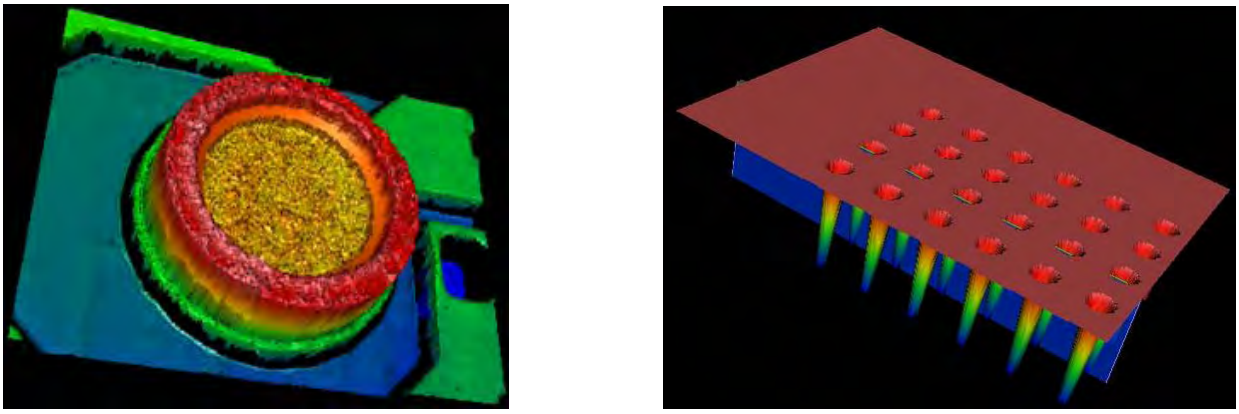
Xavier Colonna de Lega,[*] Peter de Groot,[*] Martin Fay,[*] Ryan Kruse,[*] David Grigg,[*] John Barnak[†]

[*] *Zygo Corporation, 21 Laurel Brook rd, Middlefield, CT 06455, USA*
[†] *Zygo Corporation, 2925 NW Aloclek Drive, Suite 110, Hillsboro, OR 97124, USA*

ABSTRACT

Advances in interference microscopy[1] of complex surface structures extend the unique metrology capabilities of this technique to CD, registration, film thickness, etch depth, planarity and roughness measurements. Semiconductor applications for interference microscopy now include metrology for Bump Redistribution Layer, Under Bump Metallization, Through Silicon Vias, post-CMP planarity. As specific examples, a first class of application is for TSV where a single measurement provides etch depth, CD and in some cases roughness. Via depth repeatability is better than 0.05-μm for vias as deep as 140-μm. A second class of applications relates to post-litho metrology for BRL. A single 3D measurement provides the information required to characterize photoresist thickness, top and bottom CD of bump windows, window registration with respect to buried contacts. Typical CD and registration repeatabilities are on the order of 0.3% 3σ. These examples illustrate the unique capabilities of and emerging applications for interference microscopy in semiconductor process control metrology.

Keywords: backend metrology, 3D topography, TSV.



(a) (b)

FIGURE 1. (a) 3D topography map for Under Bump Metallization metrology of depth, inner top, inner bottom and outer diameter. (b) 3D topography map for metrology of depth, CD and roughness of 70-μm deep Through Silicon Vias.

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TH-013

Spectroscopic Scatterfield Microscopy

Bryan M. Barnes, Hui Zhou, N. Alan Heckert*, and Richard M. Silver*

KT Consulting, Inc. 2545 West 10th Street, Suite A, Antioch, CA 94509
**National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20855*

ABSTRACT

Scatterfield microscopy has been defined as a set of techniques in which the illumination is engineered in combination with appropriately designed metrology targets to extend the limits of image-based optical semiconductor metrology. By maintaining the ability to image the surface, this type of microscopy permits the placement of one or many targets of interest within a single field-of-view. Though the individual targets themselves may contain features that are unresolved, comparisons of experimental data to electromagnetic simulation results can yield quantitative information about these features. While our initial studies[1,2] using scatterfield microscopy have depended solely upon changes in polarization and angle-of-incidence, we introduce here our first efforts to include spectroscopic capabilities to our optical platform. Details of the hardware modifications required for these experiments will be presented. Qualitative comparisons will be shown which demonstrate sensitivity to changes in critical dimension as a function of wavelength. The comparative advantages will be discussed between angular scanning and spectroscopic scanning for quantifying critical dimensions.

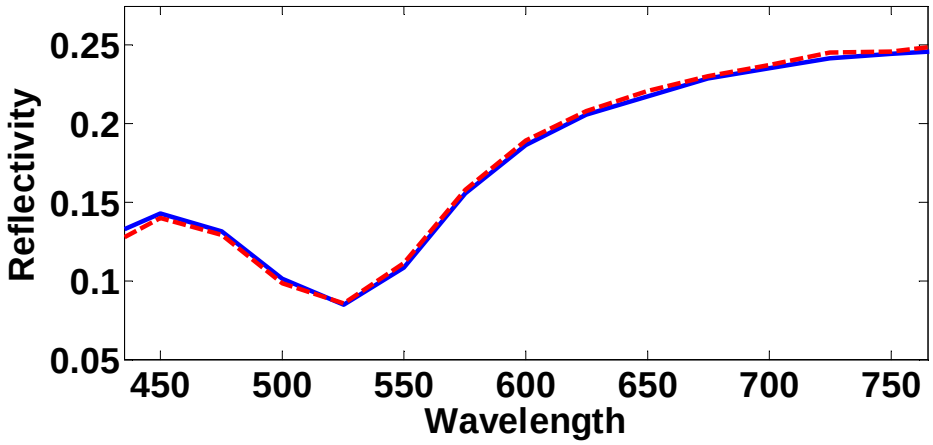

FIGURE 1. Preliminary demonstration of the reflectivity of line gratings as a function of wavelength using scatterfield microscopy. Nominal linewidths are 58 nm (dashed line) and 60 nm (solid line). The illumination is at normal incidence and the light has been linearly polarized across the lines of these grating arrays. Arrays have a nominal pitch to critical dimension (CD) ratio of 4:1. Instrumental errors have been corrected by the comparison of the measured intensity from an adjacent patch of unpatterned silicon, after the bare silicon intensity has been normalized to the theoretical reflectivity of silicon. Each curve above is the average of two scans. Ongoing efforts will be directed towards minimizing experimental uncertainties while maximizing parametric sensitivities.

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TH-014

Understanding the phase images from FIB prepared semiconductor devices.

David Cooper, Jean-Michel Hartmann, Pierrette Rivallin and Amal Chabli.

CEA, Leti, Minatec, F38054 Grenoble, France.

ABSTRACT

The exceptional stability of the latest generation of electron microscopes has allowed off-axis electron holography to become a relatively straightforward technique to perform[1]. Figure 1(a) shows a phase image of a 45-nm-gate transistor that has been prepared using focused ion beam (FIB) milling, the source and drain can be clearly seen. However, what are the artefacts in this image, especially regarding those introduced into the specimen during FIB milling? In this presentation we will discuss how the FIB affects the results obtained when using electron holography. We have simplified the experiment as much as possible by investigating Si *p-n* junctions that have been grown specifically for this study. Figure 1(b) shows the step in phase measured across a series of *p-n* junctions with different dopant concentrations as a function of crystalline specimen thickness measured using convergent beam electron diffraction (CBED). All of the specimens have been prepared using a FIB operated at 30 kV. From the x-intercept, an electrically inactive thickness is revealed which is strongly dependent on the dopant concentration[2]. Figure 1(c) shows the electrically inactive thickness as a function of dopant concentration. Here a detection limit can be revealed from the x-intercept. By extrapolating to the x-axis, we can see that to detect a dopant concentration of $1x10^{16}$ cm^{-3}, a minimum specimen thickness of 500 nm is required if the FIB is operated at 30 kV during specimen preparation. Therefore, it is important to account for the thickness of the specimen due to the electrically inactive thickness when considering the dopant concentrations measured from phase images. We will then show how the electrically inactive layer can be eliminated from these specimens, which extends the lower dopant detection limit. We will also show how the gallium which is implanted during FIB-milling can be removed.

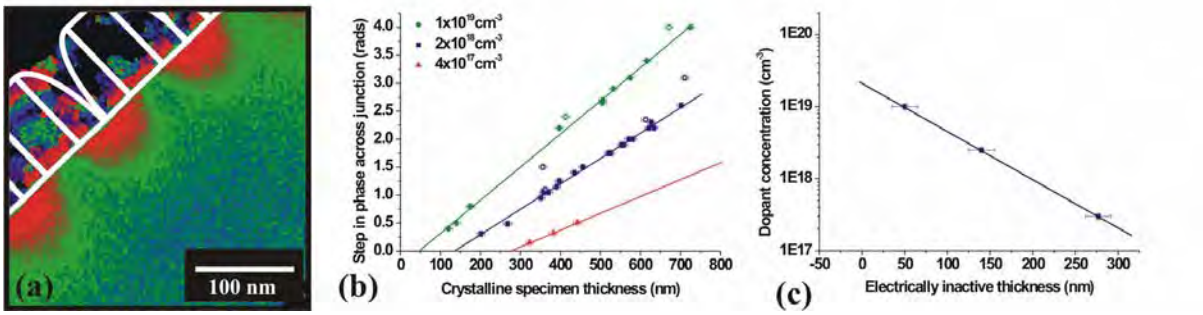

Figure 1(a) shows a phase image of a 45-nm-gate MOS device. (b) Shows the step in phase as a function of crystalline specimen thickness for a series of simple p-n junctions with different dopant concentrations. The electrically inactive thickness is revealed by the x-intercept. Figure (c) shows the electrically inactive thickness as a function of dopant concentration. From the x-intercept the dopant detection limit can be determined for a specimen of given thickness.

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Key Words: TEM, FIB, Dopant Profiling

TH-015

Simulation Study Of Transmission Electron Microscopy Imaging Of Graphene Stacking

F. Nelson[1], R. Hull[2], A.C. Diebold[1]

[1]*College of Nanoscale Science and Engineering, University at Albany, Albany, N.Y. 12203*
[2]*Rensselaer Polytechnic Institute (RPI), 110 8th St., Troy, NY 12180.*

ABSTRACT

Graphene is the subject of intense study due to its high mobility and mechanical integrity. These properties make it an attractive material for "beyond CMOS" technology. In order to accelerate research into fabrication methods, imaging and characterization of graphene must also be advanced. Due to the physical dimensions that are presently achievable for single and multi-layer samples, metrology methods are limited. For example, the spot size of ellipsometry is typically larger than available samples. Microscopy of graphene is also challenged. Carbon is a difficult element to image with electron microscopy because of its low atomic number. The current investigation explores HRTEM and STEM imaging of the different graphene stacking configurations, AAA/ABA/ABC. Although simulated images of 3 layer stacks of graphene show clear differences, this study will explore the minimum number of graphene layers necessary to observe a signal when experimental noise is taken into consideration. Future directions will be stated.

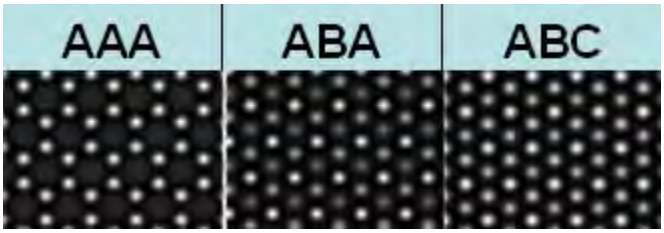

FIGURE 1. Simulated images of graphene with AAA/ABA/ABC stacking

TH-016

Scanning Tunneling Spectroscopies of Graphene

Gregory M. Rutter, [1] David L. Miller,[2] Kevin D. Kubista,[2] Ming Ruan, [2] Walt A. de Heer,[2] Phillip N. First,[2] Joseph A. Stroscio[1]

[1]*Center for Nanoscale Science and Technology, NIST, Gaithersburg, MD*
[2]*School of Physics, Georgia Institute of Technology, Atlanta, GA*

ABSTRACT

Graphene is projected to play an important role in a future generation of electronic devices. Epitaxial growth on SiC substrates offers the possibility of large-scale production and deterministic patterning of graphene for nanoelectronics [1]. This work addresses a fundamental challenge in graphene nanoelectronics which is to measure the detailed electronic properties for graphene on a nanometer scale. Three scanning tunneling spectroscopic techniques have been used to locally probe the electronic structure of epitaxial graphene on the few-nanometer length scale, without lithographic patterning (i.e., free of processing damage). First, we use point defects as local probes of the electronic structure via images of the energy-dependent standing-wave patterns that appear in maps of the differential tunnel conductance. Fourier transform analysis extracts the local energy-momentum dispersion $E(k)$ [2]. Secondly, local spectroscopies at fixed high magnetic field B yield discrete energy levels (Landau levels) due to quantization of cyclotron orbits. The peak positions show multilayer epitaxial graphene exhibits electronic properties characteristic of a single layer [3]. Finally, tunneling magneto-conductance oscillations, similar to Shubnikov-de Hass oscillations in magnetoresistance, are measured by ramping the magnetic field at fixed carrier-injection energy [3]. In contrast to conventional transport measurements, which probe at the Fermi level only, this new method is used to map the band structure over an extended energy range by varying the injection energy. The energy and wavevector resolution of all three methods described can exceed that of photoelectron spectroscopies, and furthermore can enable a probe of both filled and empty electronic states. Application of Landau level spectroscopies to the study of point-defect electronic structure will also be discussed.

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Key words/phrases: Graphene, Scanning Tunneling Spectroscopy, and Landau Quantization.

TH-017

Enhanced TEM Sample Preparation Using In-situ Low Energy Argon Ion Milling

Heiko Stegmann[1], Yvonne Ritz[2], Dirk Utess[2], Ehrenfried Zschech[2]

[1]*Carl Zeiss NTS GmbH, Carl-Zeiss-Str. 56, 73447 Oberkochen, Germany*
[2]*AMD Fab 36 LLC & Co. KG, Wilschdorfer Landstrasse 101, 01109 Dresden, Germany*

ABSTRACT

Sample preparation is a critical step in transmission electron microscopy (TEM) that significantly determines the quality of structural characterization and chemical analysis of the smallest and most critical structures in semiconductor manufacturing. In recent years, the accuracy requirements for the preparation of TEM cross-sections of nanoelectronic structures have drastically increased, and the rapid advance in TEM technology has demanded the highest standards of sample quality. Combination of a focused low-energy Ar ion beam column with a focused ion beam (FIB) column and scanning electron microscope (SEM) in a triple beam instrument provides precise positioning as well as minimum thickness, surface damage and roughness of the cross-section.

Two beam scanning electron microscope (SEM)/focused ion beam (FIB) instruments offer high quality site specific TEM sample preparation with high throughput and precision [1]. However, using high-energy (typically 30kV) Ga ions modifies the specimen by implanting Ga, and by structurally altering the material in a layer that extends up to 30nm beneath the surface. As the damage layer thickness is in the same range as the maximum specimen thickness required for high resolution TEM [2], TEM image quality and analysis sensitivity are degraded.

The Ga contaminated damage layer can be reduced to some extent in a final milling step using the focused Ga ion beam at low voltage (2-5kV), but it can be completely removed and the specimen be further thinned using low-energy (<2kV) Ar ion polishing [3]. While Ar polishing has typically been done using a broad Ar ion beam in a dedicated preparation tool, the system used here combines SEM and FIB with a small diameter low energy (500-1000V, 10nA, diameter ≈100µm) scanning Ar ion beam within a single instrument. The three beams are coincident on the sample surface so that the polishing process can be precisely controlled by real time SEM imaging.

Optimum process parameters for preparing TEM samples of advanced CMOS devices were determined for the triple beam system within a long-term collaboration project between the equipment manufacturer and semiconductor industry. In this study, we show at cross-sections of TEM lamellas that the 20nm thick damage layer in Si after 30kv Ga ion milling is reduced to <3nm applying in-situ Ar polishing. High resolution TEM image quality is, thus, greatly improved and provides, e.g., more precise characterization of ultrathin films and interfaces in high-k metal oxide/metal gate layer stacks. Samples with complicated geometry that cannot be polished with a broad Ar ion beam due to redeposition of sputtered material onto the cross-section have been proven to be readily polishable in this system. Thus, in-situ Ar polishing provides the TEM lamella quality that is needed for metrology and failure analysis of nanoelectronic products manufactured in future technology nodes.

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TH-018

TEM Spectral Imaging and Tomography for Chemical Imaging of Three-Dimensional Nanoelectronic Devices

Ian M. Anderson and Andrew A. Herzing

National Institute of Standards and Technology, Surface and Microanalysis Science Division
100 Bureau Drive, Gaithersburg, MD 20899-8371 USA

ABSTRACT

The revolutionary changes in device technology needed to sustain long-term improvements in the performance of nanoelectronics demand the development of metrology solutions capable of imaging complex three-dimensional (3D) structures comprised of nanometer-scale components. Transmission electron microscopy (TEM) combined with now established tomography methods provides a 3D nanometer-resolution metrology solution, and can be combined with spectroscopic techniques that provide the necessary contrast to distinguish chemically distinct components of the device. Here, we examine the relative merits of various TEM-based spectral imaging (SI) and tomography methods and their application to a FinFET device structure. Shown below is the result of energy-filtered (EF) TEM SI using only the low-loss region of the electron energy-loss spectrum (EELS). A series of 104 512x512 pixel EF images was acquired with a 1-s exposure, 3-eV energy window and 1-eV step, registered using filtered cross-correlation, and analyzed with linear multivariate statistical methods. Although the characteristic K-edges of N and O were not sampled, differences in the plasmon-loss region of the spectrum coupled with a chemical shift at the Si-L edge were sufficient to distinguish silicon oxide (green) and oxynitride (cyan) phases from the silicon semiconductor (blue, red). A separate spectral component (yellow) is identified at the semiconductor-oxide interface. Factors complicating tomographic reconstruction include multiple plasmon excitation (x2, x3) in silicon, giving rise to a nonlinear spectral response, and the absence of spectral contrast to distinguish the HfO_2-rich oxide layer, which was evident in bright-field images from mass-thickness contrast.

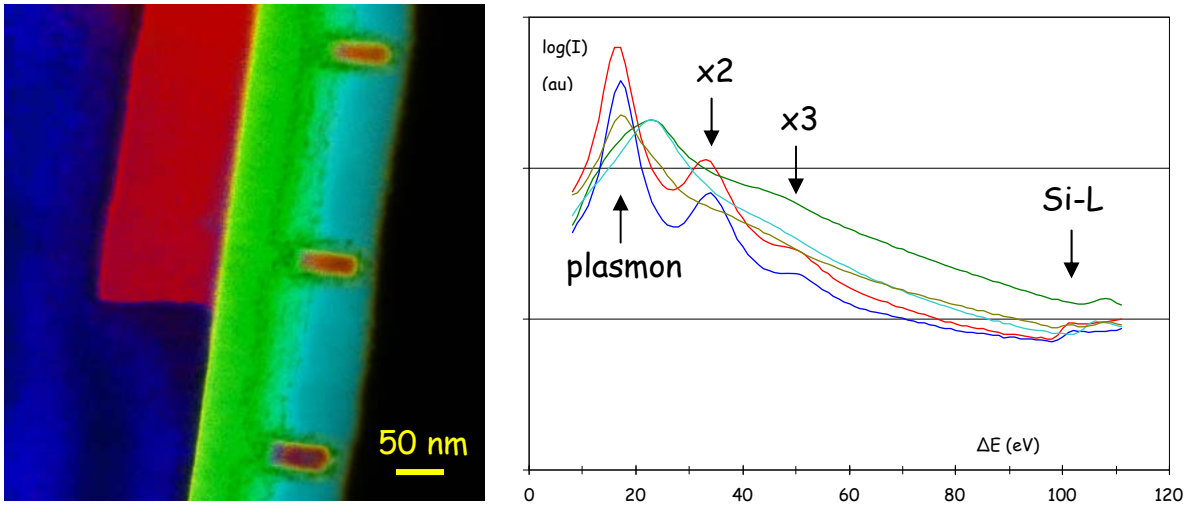

FIGURE 1. EFTEM-SI of FinFET device structure: (a) chemical image; (b) component spectra. The high signal of the low-loss region of the EELS spectrum, to just beyond the Si-L edge at ~100 eV, allows rapid acquisition of 3D chemical images.

TH-019

Hysteresis Correction of SPM Image by Moving Window Correlation Method

Joseph Fu, Wei Chu, Ronald Dixson, George Orji, and Theodore Vorburger

National Institute of Standards and Technology, Gaithersburg, MD 20899-8212

ABSTRACT

Many scanning probe microscopes (SPMs), such as the scanning tunneling microscope (STM) and atomic force microscope (AFM), use piezoelectric actuators with open loop for generating the scans of the surfaces. However, nonlinearities mainly caused by hysteresis and drift of piezoelectric actuator might reduce the positioning precision and produce distorted image. A moving window correlation method is proposed in this paper to determine and quantify the hysteresis. This method requires taking consecutively a pair of trace and retrace images. With a window imposed on each of the profiles, correlations are implemented between the data inside two windows to find corresponding pixel pairs on two different profiles but same physical positions. The distances between pixel pairs are calculated and then a simple correction scheme is applied to reduce the distortion.

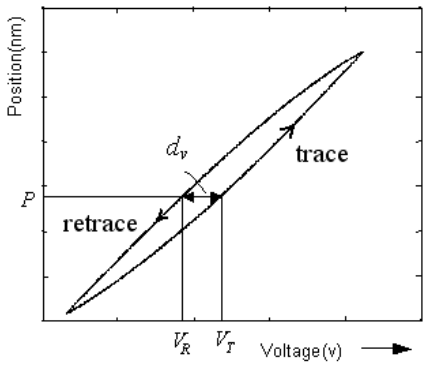

FIGURE 1. A sketch of typical hysteresis loop

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TH-020

Electrical Measurements By Scanning Spreading Resistance Microscopy: Application To Carbon Nanofibers And Si Nanowires.

N. Chevalier[1], D. Mariolle[1], L.Fourdrinier[2], C. Celle[2], C. Mouchet[2], S. Poncet[2], J.P. Simonato[2], H. Le Poche[2], E. Rouviere[2], F. Bertin[1] and A. Chabli[1]

[1] *CEA, LETI, MINATEC, F-38054 Grenoble, France*
[2] *CEA-LITEN/Hybrid Components Laboratory, F-38054 Grenoble, France*

ABSTRACT

In this communication, we report the electrical characterization of vertically aligned nano-objects by Scanning Spreading Resistance Microscopy (SSRM), which is an AFM-mode mapping simultaneously the topography and the local resistance of the sample. This technique is currently used on silicon substrate for the carrier concentration profiling [1]. In this paper, we show that this method is well suited to evaluate the individual electrical properties of carbon nanofibers (CNF) and of n-doped Si nanowires (NWs). In the first example, CNFs are grown on a TiN by radio frequency plasma system [2] and exhibit a wide range of resistance (figure 1.a), of a few kilohms up to several megaohms, which could be explained by the convolution of roughness and of surface oxidation of the TiN layer [3]. An interpretation based on electrical contact resistance model is proposed here to explain this observation. In the second example, n-doped Si NWs are grown on (111) oriented Si substrates by the vapour-liquid-solid (VLS) [4] method and the dopant addition is performed by adjusting the flow rate of phosphine. We will show that the Phosphorus/Silicon ratio has an effect on the resistance measured on individual Si NWs, which is a highlight of the control of the doping level (figure 1.b).

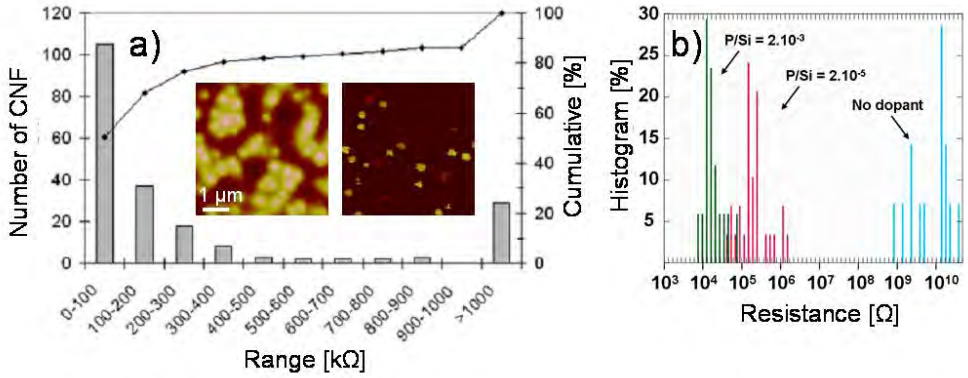

FIGURE 1. a) Histogram of resistances for 209 CNFs measured. (Inset: topographic and electrical images of vertically aligned NFCs on a 5x5 µm2 scanned area. Brightest points in the electrical image correspond to more conductive NFCs). b) Histogram of resistances for 30 Si NWs measured for different Phosphorus/Silicon ratios from 0 to 2.10^{-3}.

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Keywords : SSRM, Conducting AFM, Nanowires

TH-021

A Study of Gate-All-Around Transistors by Electron Tomography

P. D. Cherns[1], F. Lorut[2], C. Dupré[1], K.Tachi[1], D.Cooper[1], A.Chabli[1] and T. Ernst[1]

1. CEA, LETI, MINATEC, F38054 Grenoble, France
2. ST Microelectronics, 850 rue Jean Monnet, 38926 Crolles, France
Peter CHERNS: Phone: +33 438780650, Fax: +33 438785273, peter.cherns@cea.fr

ABSTRACT

The development of gate-all-around (GAA) Si nanowire based devices is one solution to the problem of off state leakage current, which leads to significant issues with power consumption as planar transistors become smaller. Stacked nanowire MOSFETs offer excellent electrostatic control combined with a high I_{ON} current. For devices such as these, three dimensional (3D) characterization becomes essential. We present a study of GAA devices by electron tomography, a transmission electron microscope (TEM) based technique which offers 3D morphological information with a resolution of ~2nm.

The nanowires are obtained by anisotropic etching of a SiGe/Si superlattice, followed by removal of SiGe. The nanowire morphology can then be adjusted by hydrogen annealing which significantly improves the electrical characteristics of devices by reducing surface roughness. After gate stack integration, the result is a stack of three 20-40nm diameter wires, each surrounded by 2nm HfO2 and 10nm TiN.

For this study, GAA transistors have been prepared in 350nm diameter needle shaped samples, using annular milling in the focused ion beam (FIB). This is found to be superior to a parallel sided preparation as the needles allow 360° rotation in the TEM, without problems of thickness changes or shadowing at high tilt. For each sample, a series of high angle annular dark field (HAADF) scanning TEM (STEM) images were acquired over a tilt range of +/-79°. The encapsulated wires are easily resolved, given the Z^2 contrast in HAADF images (Figure 1 (a)). The images are then aligned and reconstructed using FEI Inspect 3D software and a reconstruction such as that shown in Figure 1 (b) is obtained. We have used the technique to study morphological changes associated with hydrogen annealing of the wires. We demonstrate that electron tomography has potential to become a standard method of characterization for 3D devices of this type.

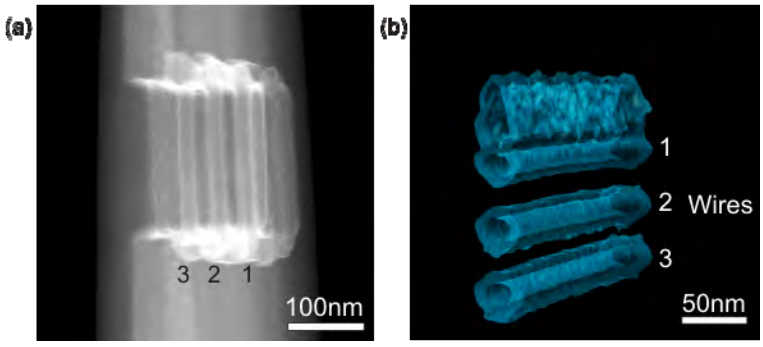

FIGURE 1. (a) HAADF STEM image of GAA transistor structure prepared by FIB in a needle shaped geometry. The Si nanowires are vertical in the image and are labeled 1, 2 and 3. (b) 3D reconstruction from the same sample.

Keywords: gate-all-around transistor, TEM, tomography

TH-022

QUANTIFYING AND ENFORCING THE TWO-DIMENSIONAL SYMMETRY OF SCANNING PROBE MICROSCOPY IMAGES OF PERIODIC OBJECTS

Peter Moeck[1*°], Bill Moon Jr.[1*], Erik Sánches[1°], Mahmoud Abdel-Hafiez[2], and Michael Hietschold[2]

[1] *Department of Physics, * Nano-Crystallography Group, Portland State University, Portland, OR 97207-0751, U.S.A.;* [°] *Oregon Nanoscience and Microtechnologies Institute, www.onami.us*
[2] *Institute of Physics, Solid Surfaces Analysis Group & Electron Microscopy Laboratory, Chemnitz University of Technology, 09126 Chemnitz, Reichenhainer Straße 70, Federal Republic of Germany*

The overall performance and correctness of the calibration of all kinds of scanning probe microscopes can be assessed in a fully quantitative way by means of "crystallographic processing" [1] of their two-dimensional images from samples that possess periodic features. This is because crystallographic image processing results in two residual indices that quantify by how much the symmetry in a scanning probe microscopy image deviates from the symmetries of each of the 17 plane groups [1,2]. When a likely plane group has been identified on the basis of crystallographic image processing, the symmetry elements in the scanning probe microscopy image can be enforced in order to obtain "clearer" images of the periodic objects. The crystallographic image processing (CIP) procedure will be demonstrated in this paper for a scanning tunneling microscopy image of mono-layers of fluorinated cobalt phthalocyanine ($F_{16}CoPc$) on graphite, Fig. 1. Atomic force microscopy images of a commercially available calibration standard with a regular array of pits provide a second illustration of the quantification of plane symmetries and illustrate the dependence of the residual indices on the operation conditions of the microscope.
Keywords: Scanning probe microscopy.

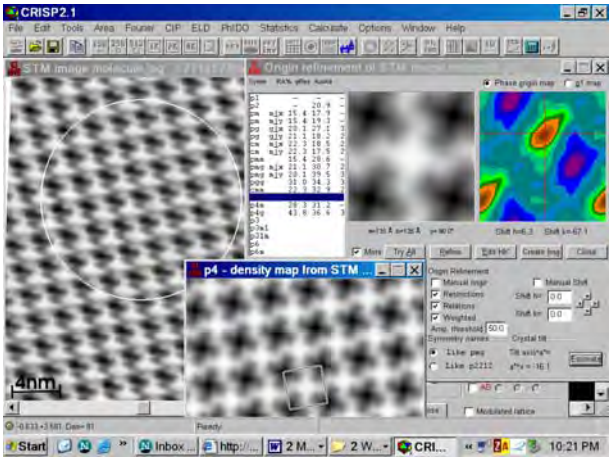

FIGURE 1. Screen shot of CIP on a scanning tunneling microscopy image of an $F_{16}CoPc$ mono-layer on graphite. The plane group symmetry p4 is enforced in the "density map".

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TH-023

STRUCTURAL FINGERPRINTING OF NANOCRYSTALS IN THE TRANSMISSION ELECTRON MICROSCOPE

Peter Moeck[1], Sergei Rouvimov[1], and Stavros Nicolopoulos[2]

[1] Nano-Crystallography Group, Department of Physics, Portland State University, Portland, OR 97207-0751 & Oregon Nanoscience and Microtechnologies Institute, www.onami.us; [2] NanoMEGAS SPRL, Boulevard Edmond Machterns No 79, Sint Jean Molenbeek, Brussels, B-1080 Belgium; nanomegas.com

Three novel strategies for the structurally identification of nanocrystals in a Transmission Electron Microscope (TEM) are presented [1]. Either a single High-Resolution Transmission Electron Microscopy (HRTEM) image [2] or a single Precession Electron Diffractogram (PED) [3] can be employed. The structural identification information is in both cases collected from an individual nanocrystal. PED from fine-grained crystal powders may also be utilized. Automation of the former two strategies shall lead to statistically significant results on ensembles of nanocrystals. The structural information that can be extracted from a HRTEM image of an approximately 5 to 10 nm thick nanocrystal is the projected reciprocal lattice geometry, the plane symmetry group, and a few structure factor amplitudes and phase angles. While the structure factor amplitudes suffer from dynamical diffraction effects and are in addition modified by the (not precisely known) contrast-transfer function of the objective lens, the structure factor phase angles are remarkably stable against dynamical diffraction effects and slight crystal misorientations.

Except for the structure factor phase angles, the same kind of structural information can be extracted from a PED. The information that can be used for structural fingerprinting is in this case, however, not limited to the directly interpretable resolution of the TEM. As precession electron diffraction avoids crystal orientations that result in the simultaneous excitation of more than one strong diffracted beam (as much as this is possible), quasi-kinematic reflection intensities are obtained for nanocrystals with thicknesses up to approximately 50 nm [3]. Simultaneously present reflections in higher order Laue zones and systematic absences in both the higher and the zero order Laue zones allow frequently for an unambiguous determination of the space group. Comparing kinematical electron diffraction simulations with experimental PEDs allows, therefore, for structure verifications. A universal precession electron diffraction device that can be interfaced to any older or newer mid-voltage TEM was recently commercialized by the NanoMEGAS company.

Searching for structural information that is extracted from HRTEM images or PEDs in commercial databases and matching it with high figures of merit to that of candidate structures shall allow for highly discriminatory identifications of nanocrystals, even without additional chemical information as obtainable in analytical TEMs. As an alternative to the commercial databases, one may use open-access databases [4-6] which provide together some 100,000 crystal structure data sets. **Keywords: structural fingerprinting, nanocrystals.**

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TH-024

AUTOMATED CRYSTAL ORIENTATION AND PHASE MAPPING OF IRON OXIDE NANO-CRYSTALS IN A TRANSMISSION ELECTRON MICROSCOPE

Sergei Rouvimov[1], Edgar F. Rauch[2], Peter Moeck[1], and Stavros Nicolopoulos[3]

[1]Nano-Crystallography Group, Department of Physics, Portland State University, Portland, OR 97207-0751, U.S.A & Oregon Nanoscience and Microtechnologies Institute, www.onami.us; [2] SIMAP/GPM2 laboratory, CNRS-Grenoble INP, BP 46 101 rue de la Physique, 38402 Saint Martin d'Hères, France; [3] NanoMEGAS SPRL, Boulevard Edmond Machterns No 79, Saint Jean Molenbeek, Brussels, B-1080, Belgium, nanomegas.com

An automated technique for the crystal phase and orientation mapping of polycrystalline materials in a transmission electron microscope (TEM) has recently beam developed [1]. This technique is based on template matching of experimental electron diffraction spot patterns to their pre-calculated theoretical counterparts. Very promising results have so far been obtained with this technique for precipitates in heavily deformed austenitic stainless steels [1]. It has also been demonstrated that precession of the primary electron beam [2] around the optical axis of the microscope during the recording of the diffraction patterns improves the reliability of this technique significantly. This is because more reflections are exited in precession electron diffraction spot patterns. For nanocrystal sizes of below about 50 nm, the intensities of these reflections are nearly kinematical [2]. Such precession electron diffraction patterns are, therefore, very useful for advanced structural fingerprinting of nanocrystals in a TEM [3]. This conference contribution will illustrate the application of this technique to a mixture of iron oxide nano-crystals of magnetite and maghemite. Note that the crystallite sizes of this mixture make it impossibly to fingerprint it structurally by conventional powder X-ray diffractometry.

Keywords: nanocrystal, orientation, phase.

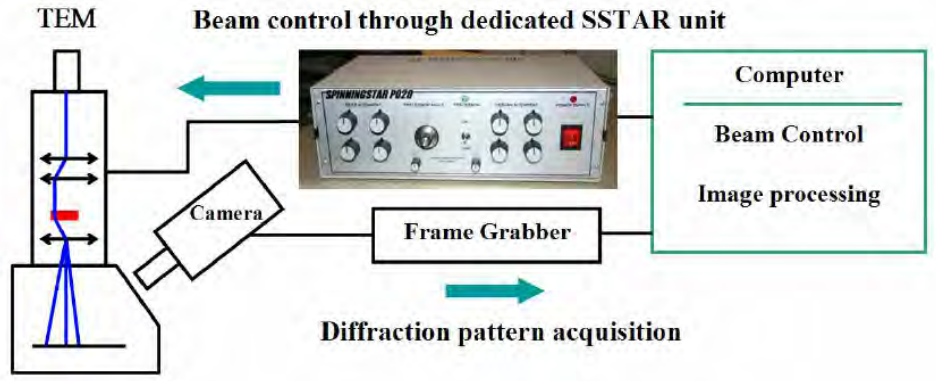

FIGURE 1. Sketch of NanoMEGAS' ASTAR crystal orientation and phase mapping system [1].

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TH-025

Helium Ion Beam Microscopy for Copper Grain Identification in BEOL Structures

Ruud J.J. van den Boom[a], Hamed Parvaneh[a], Dave Voci[b], David Ferranti[b], Chuong Huynh[b], Kathleen A. Dunn[a], Eric Lifshin[a]

[a] *State University of New York, University at Albany; 255 Fuller Road, Albany New York 12203*
[b] *Carl Zeiss SMT Inc.; 1 Corporation Way, Peabody MA 01960*

ABSTRACT

Due to the continued feature scaling in ULSI chips, the width of copper lines and vias has been pushed well under 100nm in the last few years. Historically, Focused Ion Beam (FIB) instruments were used to image the grain structure in these interconnects because of the dramatic orientation-dependent grain contrast[1,2] produced by ion irradiation. In recent years, however, this analysis has been hampered by the limited resolution of these instruments (~6-8nm). In addition, the continuous milling and implantation of gallium ions alters the surface being imaged, particularly at high magnifications; employing lower ion current to avoid this issue leads to increased noise in the image. While Scanning Electron Microscopy (SEM) offers better resolution than the FIB, the orientation contrast between different grains is minimal, making analysis difficult. Transmission Electron Microscopy (TEM) offers superior orientation contrast via diffraction[3,4], but requires time- and labor-intensive sample preparation.

Helium Ion Microscopy is a promising alternative for the analysis of narrow copper lines that combines the best of these techniques, including the potential for sub-nm resolution[5], FIB-like grain contrast mechanisms and minimal damage to the specimen, yet without the need for thin (membrane) specimen. To assess the potential of Helium Ion Microscopy for copper grain identification, we used samples of electrochemically deposited (ECD) copper. Two sets of specimens were prepared: (1) by a combination of mechanical polishing and low energy argon ion milling followed by an anneal in forming gas, and (2) by FIB cross-sectioning followed by a forming gas anneal. These preparation techniques were used to ensure a smooth surface with minimal oxidation (which can impair grain orientation contrast mechanisms).

The influence of beam current, accelerating voltage and incidence angle were investigated and images were taken both with a backscattered ion (RBI) and a secondary electron (SE) detector. Results show a good grain contrast for specimens prepared by mechanical polishing and argon ion milling for both backscattered ions (Fig 1A) and secondary electrons (Fig 1B). In addition it was found that lower accelerating voltages resulted in better contrast and a clear increase in contrast with increasing ion fluency, which we attribute to an increase in signal to noise ratio.

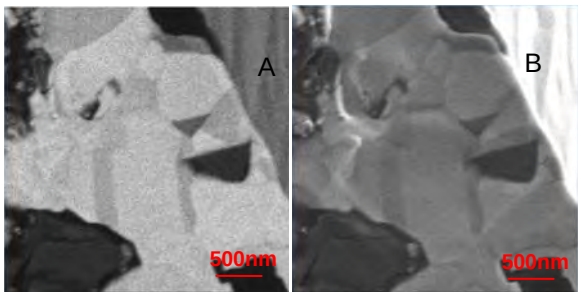

FIGURE 1. Helium Ion Microscope images with a field of view of 3µm. A) Backscattered ions B) Secondary electrons

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TH-026

Edge Structure of Suspended Graphene Confirmed by HRTEM

SeongYong Park, YoungJoon Suh, and Moon J. Kim

Department of Material Science and Engineering, The University of Texas at Dallas.
800 W. Campbell Road, RL 10 Richardson, Texas 75080, U.S.A

ABSTRACT

In order to elucidate the atomic and edge structure of graphene, HRTEM analysis on a suspended graphene sample was performed. This observation can provide clues about the electronic behavior of the graphene since its properties are exceptionally sensitive to lattice defects and edge structures [1]. A suspended graphene layer was prepared via micromechanical cleavage method. SU-8 epoxy was pasted on the surface of a meshed Cu TEM grid as an adhesive layer. Then natural graphite or highly ordered pyrolytic graphite (HOPG) was stamped on the grid. HRTEM and diffraction pattern analyses were carried out in a JEOL 2100F TEM/STEM.

A single layer region could be distinguished from a multi layer region by using the fact that the intensity of {1-100} diffraction spots is stronger than that of the {11-20} planes only in a single layer [2]. In the HREM image for the single layer has confirmed its hexagonal crystal structure with a C-C interatomic distance of 0.142 nm as shown in the inset of Fig (b). An unfolded graphene edge, which has yet to be reported using TEM, was also observed (Fig. 1 (b) and (c)). By characterizing the unfolded edge, we should be able to determine chirality and roughness of the graphene layer. All the possible edge types including a zigzag, an arm-chair shape and/or the combination of the two were detected. Additionally, we discovered that the images of the straight edges at a low magnification were misleading. The same edges exhibited some roughness at higher magnifications. The comparison between graphene films from natural graphite and HOPG and the detailed investigation on the edge structures and crystallographic defects will be discussed.

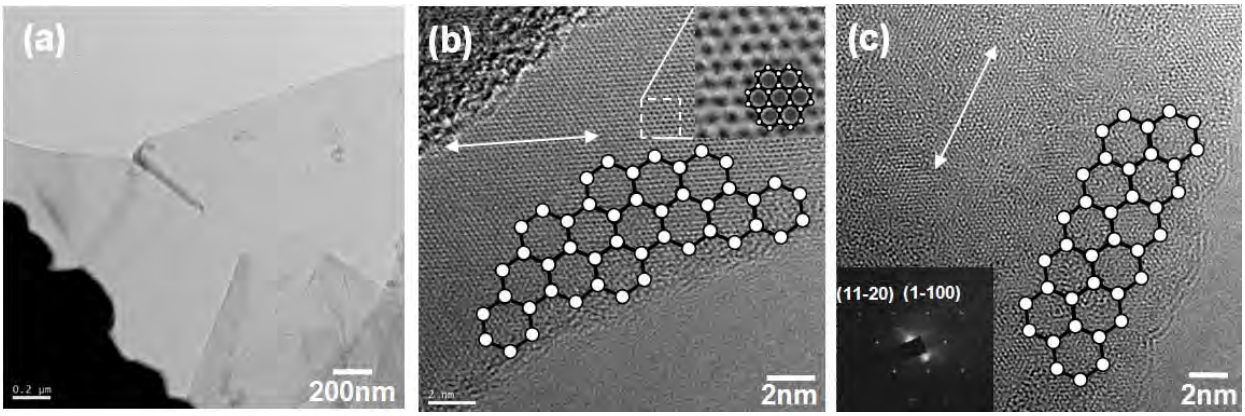

FIGURE 1. (a) Low magnification TEM image of suspended graphene; (b) and (c) HREM images representing edge directions of combination with zigzag and armchair and zigzag, respectively, arrows indicate zigzag direction.

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TH-027

Abstract Withdrawn

TH-028

Spectroscopic Polarimetry of Light scattered by Surface Roughness and Textured Films in Nanotechnologies.

F. Ferrieu[1].

[1]*STMicroelectronics, 850, rue Jean Monnet, F38926 CROLLES Cedex France.*

ABSTRACT

The Effective Medium Approximation, (EMA), theory validate the optical metrology with surface roughness. An approximate right scaling rule exists between the light wavelengths, and thin films roughness. In earlier papers[1-3], it was shown however that poly crystaline and textured films could induce light scattering, affecting sometimes the SE results. In Optics, exhaustives studies detail the Mueller matrices interesting properties through optical entropy and depolarization. These theories, have been first developped in a rather different fields, i.e., backscattering radar polarimetry. The mathematical basis, describing depolarizing systems, first given by S.R. Cloude[4], are an important issue. In the visible range optics, it has applications in thin grating films, scatterometry and complex biological turbid media medical applications and astronomy as well. The optical entropy, as shown in figure 1 below, through the Bernouilli model descriptor, provides a very powerful analysis technique yielding important surface parameters such as depolarization and roughness, differentiates roughness character, enabling even scatterer's classification. More precisely in the field of thin films characterization of nanotechnologies materials, spectroscopic polarimetry should detect surface properties and films textures.The comparison has also been made with simulated scattering models considering the Integral Equation Method[5]. An ultraviolet extended range of present polarimeters set up for imaging and quality control, promisingly, shall enhance for example, the present bidirectional reflectance distribution function (BRDF) and haze ultraviolet wafer measurements in conventional processes.

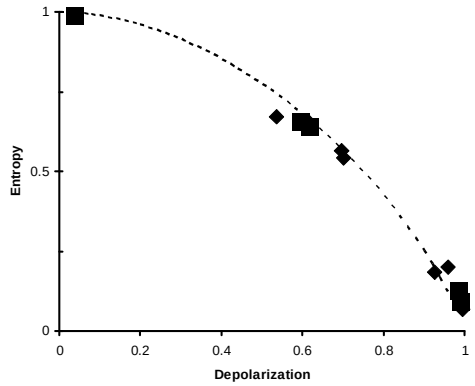

FIGURE 1 the Entropy depolarization space, corresponding to Mueller matrices with different surface roughness: (Diamonds and square filled are calculated from published Mueller matrices in references 1.and 6, Calculated curve follows the Entropy/Depolarization space limit equation from Leroy-Brehonnet[6]: rough surface (E=1, depolarization factor =0), smooth surface (0,1).

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TH-029

Density Functional Theory Studies of Defects in Graphene

Eric Cockayne

Ceramics Division, Materials Science and Engineering Laboratory, NIST, Gaithersburg, MD 20899-8520

ABSTRACT

An ideal graphene structure consists of a sheet with a honeycomb pattern of six-membered rings. The experimental growth of graphene sheets, however, is observed to produce samples with various defects [G. M. Rutter et al., Science 317, 219 (2007)]. These defects can form scattering centers which lower the carrier mobilities, thus adversely affecting device performance. Understanding the nature of these defects assists the ultimate goal of reducing or eliminating these defects. Density functional theory (DFT) calculations, as programmed in the VASP code, have been performed to elucidate the nature of graphene defects. The lowest energy defect found is Stone-Wales defect with energy 3 eV. A carbon vacancy has a higher energy of about 7 eV. The Stone-Wales defect replaces four carbon hexagons with two pentagons and two heptagons. A wide variety of defects can be built from such five and seven-membered carbon rings. A single pentagon-heptagon pair forms the termination of an edge dislocation with approximate energy 4 eV. Suitably arranged (as in Figure 1), a sequence of such pairs forms an extended, grain boundary, defect. The energy is further lowered if the sheet is allowed to buckle out of the plane. For a perfect graphene sheet, the DFT calculations show the electronic density of states (DOS) with a minimum of zero at the Fermi level, as expected. With grain boundaries present, there is a nonzero minimum in the DOS at the Fermi level.

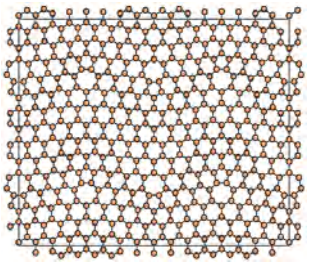

FIGURE 1. Structure of graphene with grain boundaries. The grain boundaries are the "vertical" lines that bisect adjacent five- and seven-membered carbon rings.

The calculated energies and symmetries of the the vacancy and Stone-Wales defects make them candidates to explain many of the experimentally-observed defects. Scanning tunneling microscopy (STM) experiments provide even further information about defects. STM topographic images show honeycomb patterns in defect-free graphene, and complicated patterns around defects that are very sensitive to the local electronic density of states. Software is being developed to directly simulate (Fig. 2) these STM images, with an aim of making a definitive identification of the observed defects.

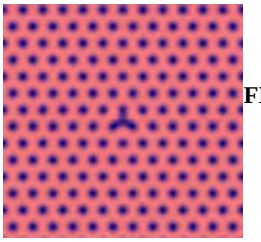

FIGURE 2. Simulated topographic image of graphene with one carbon vacancy in center. There is slight charge enhancement (5% to 10%) near the underbonded carbons surrounding the vacancy. The 3-fold defect observed in Rutter et al., op. cit., Fig. 1C has much greater enhancement of charge near the center. This could be due to the experimental defect being a substitution rather than a vacancy, to out-of-plane relaxation. or to the exact electronic state (amount of "doping") in the experiment.

TH-030

Application of Statistical Dynamical X-ray Diffraction Theory to Defective Semiconductor Heterostructures

P.K. Shreeman and R.J. Matyi

College of Nanoscale Science and Engineering, SUNY – University at Albany, Albany, NY 12203

ABSTRACT

Dynamical X-ray diffraction theory is extensively used to evaluate the structure of single crystals materials, where information on (for instance) chemical composition and strain can be readily extracted from rocking curves recorded under high resolution diffraction conditions. However, currently-available simulation software only allow quantitative analyses of materials that satisfy the basic requirement of dynamical diffraction: namely that the material under study exhibits high structural perfection. Most commercially-available high resolution X-ray analysis software does not provide the opportunity to incorporate the effects of partially defective layers structures. In contrast, many critical materials and structures (lattice-mismatched semiconductor heterostructures, or materials modified by ion implantation processing) may contain process-induced structural defects and thus cannot be modeled by conventional dynamical theory approaches. Variants of dynamical theory [1] incorporate a static Debye-Waller factor, while a semi-kinematical theory developed by various authors [2] uses dynamical models for the substrate and applies a kinematical model for the scattering from defective layers. Bushuev [3] and Punegov [4] have developed an approach based on Kato's statistical dynamical diffraction theory (SDDT [5]) that incorporates both incoherent (kinematical and diffuse) and coherent (dynamical) scattering. The newly implemented parameters of SDDT include long-range order (also known as the static Debye-Waller factor E) and a complex correlation length τ. Unfortunately, both approaches to the SDDT theory are mathematically intensive while being short on instructions on how to actually implement the theory in practice.

This paper fills this need by providing practical solutions and methods for implementing the mathematical approach for performing SDDT analyses on samples such as fully relaxed SiGe on Si (Figure 1). We are currently modifying our approach (specifically through the long-range and short-range order parameters E and τ) to provide a method for fully quantitative X-ray analyses of epitaxial and/or implanted structurally defective materials.

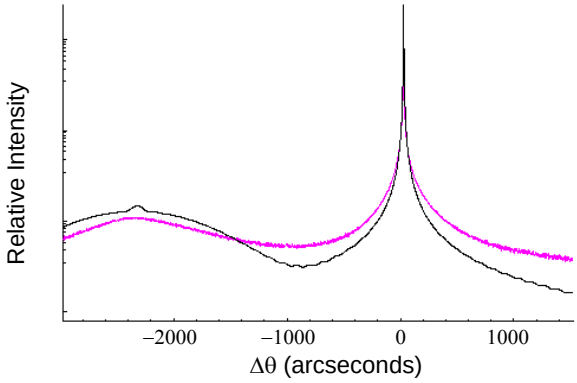

FIGURE 1. Comparison of experimental data and SDDT simulation of relaxed 170 nm 30% SiGe on Si.

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TH-031

Abstract Withdrawn

TH-032

A Lumped Element Model for Near-field Microwave Microscopy of Bulk and Thin Film Semiconductors

Vladimir V. Talanov

Solid State Measurements, Inc., 110 Technology Drive, Pittsburgh, PA 15275, USA

ABSTRACT

An accurate lumped element model for the probe-sample interaction in near-field scanning microwave microscopy is proposed. The Poynting complex theorem for energy conservation [1] is used to calculate the complex impedance of an arbitrary near-field microwave probe. It is shown that the probe response may be addressed with a single geometrical parameter *D* governed by the probe size, which is independent of the sample properties. The response of an electric near-field microwave probe is calculated for various materials such as dielectrics, semiconductors, metals, superconductors, and negative refraction index materials. It is shown that it can be either capacitive or inductive depending on the material dielectric function.

The model is validated via comparison it with the results of full-wave 3D finite element modeling (FEM) performed for bulk (see Fig. 1) and implanted semiconductors. Excellent agreement is demonstrated. Representative results of fitting the lumped element model to the 4 GHz finite element numerical data for a parallel strip-line probe [2] are shown in Fig. 1 for several probe sizes for a bulk Si sample. The open symbols are the FEM data for the magnitude and phase of the probe reflection coefficient S_{11} and the lines are the model fits using the probe size as a free parameter.

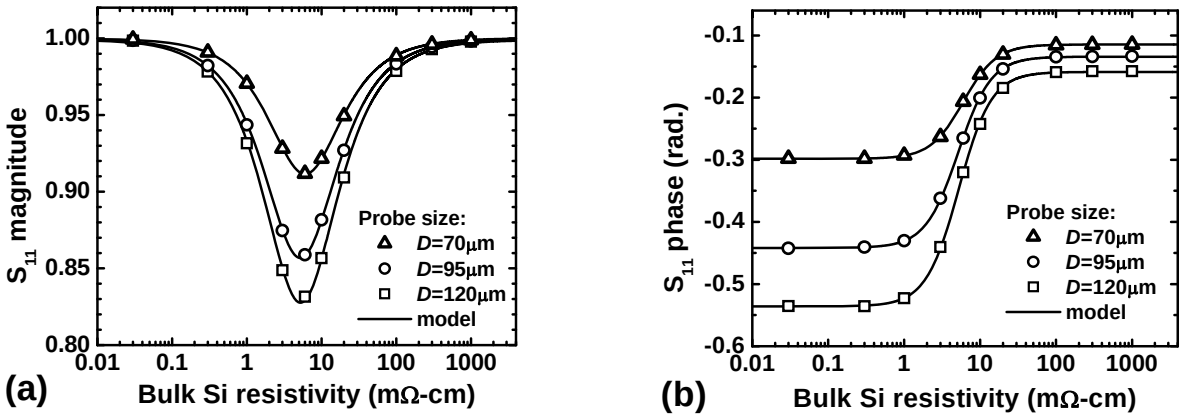

FIGURE 1. Magnitude **(a)** and phase **(b)** of the reflection coefficient S_{11} for a parallel strip line near-field probe at 4 GHz for bulk Si sample. Symbols are the FEM data for several probe sizes, solid lines are the results of the model fitting using the probe size *D* as the free parameter.

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Keywords: near-field microwave microscopy, finite element modeling, implants

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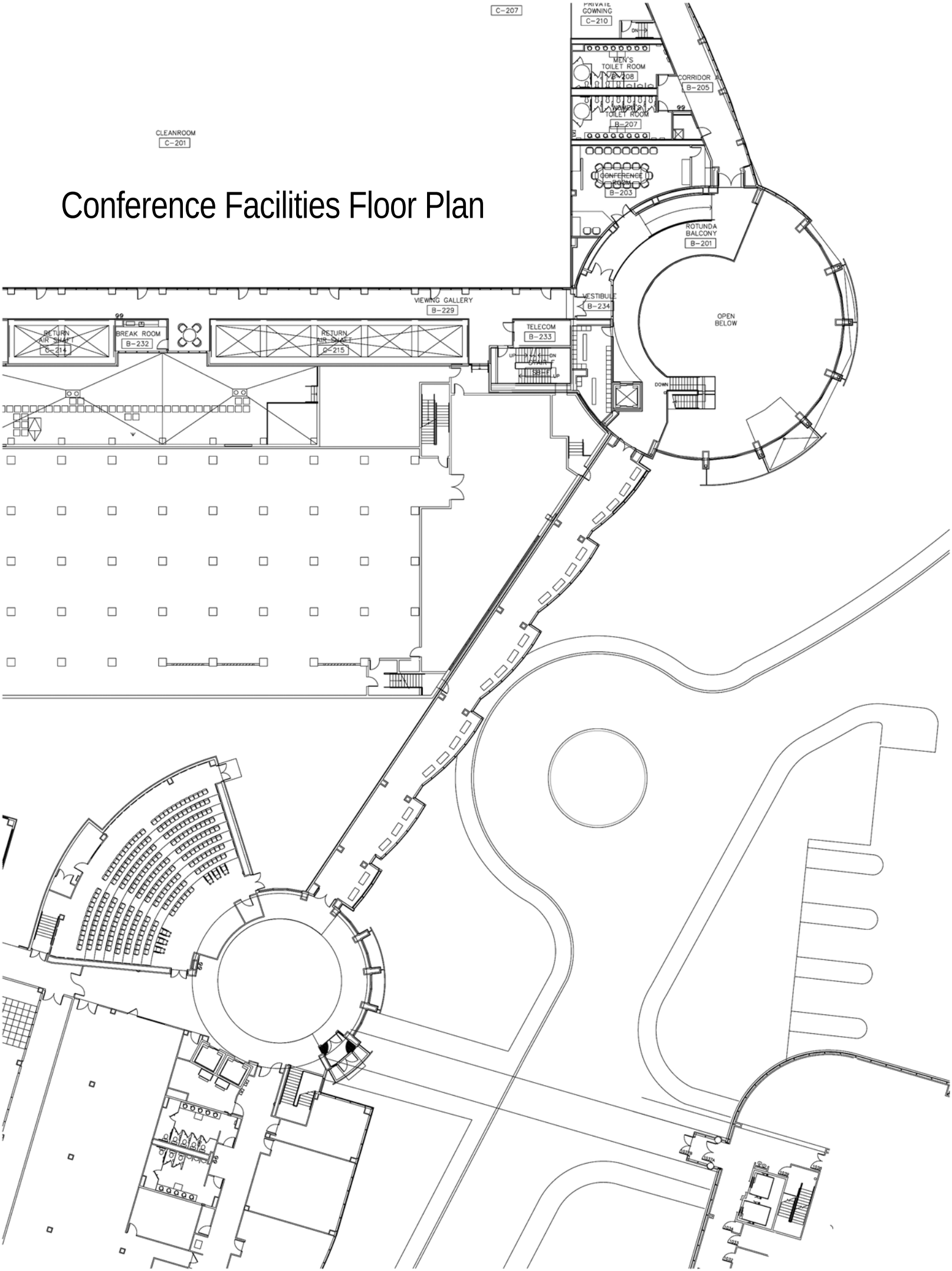

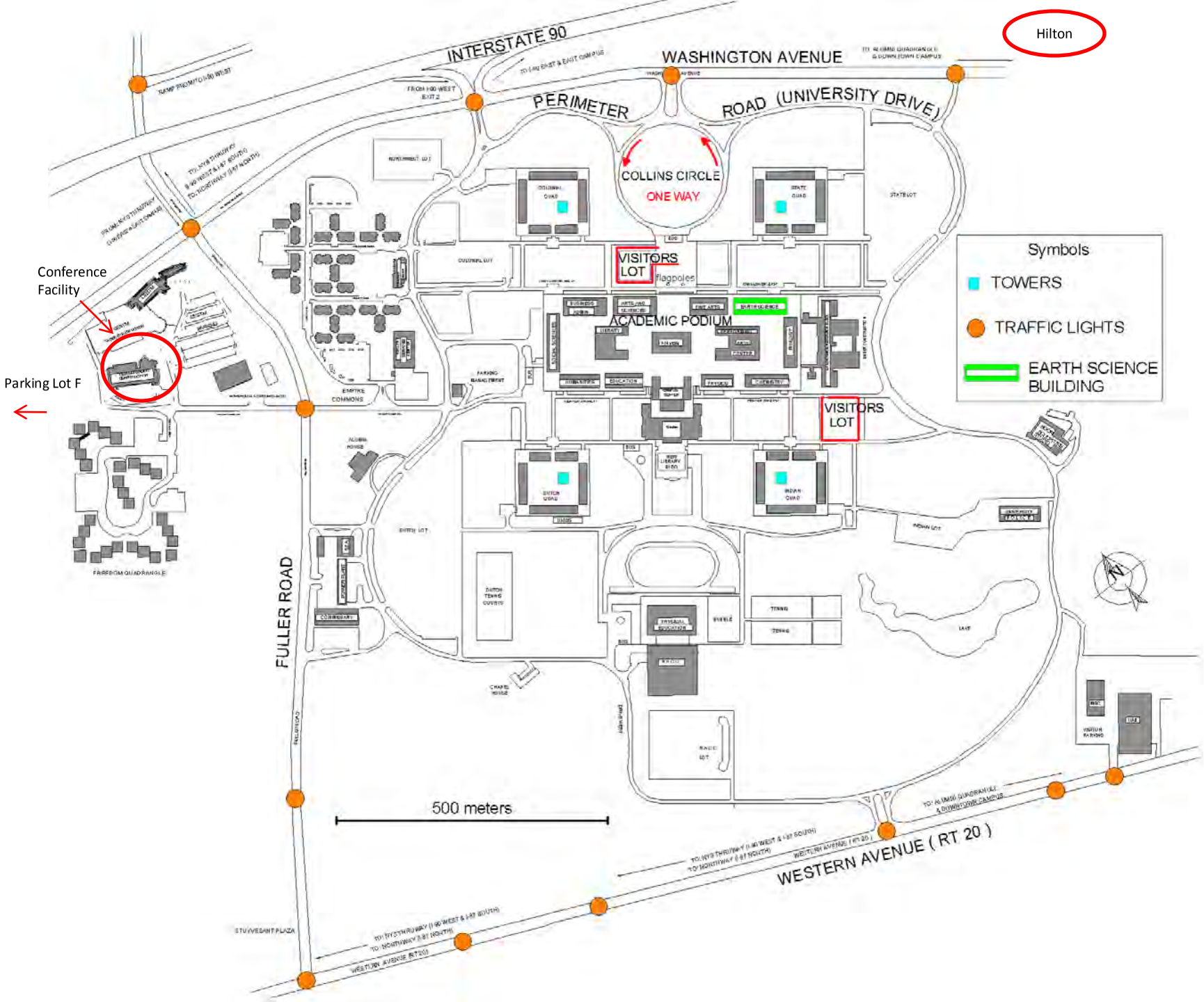
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Cover Caption: The fourier representation of three projections (-45°, 0°, 45°) through an object utilizing depth sectioning in an aberration corrected transmission electron microscope. This hybrid method is more efficient for tomographic data acquisition and post-processing. (Image Courtesy Peter Ercius, Cornell University)