Enabling Technologies for ≤20nm Generations

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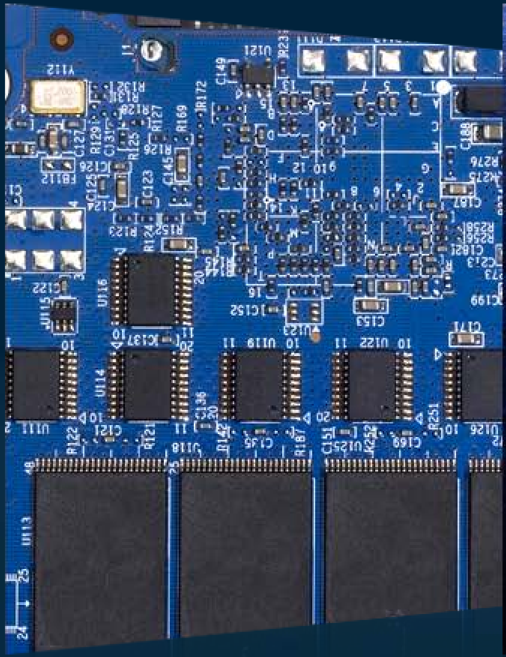
think it. apply it.™

APPLIED MATERIALS.

Key Drivers for Industry Growth



SSD

Low Power
User Convenience

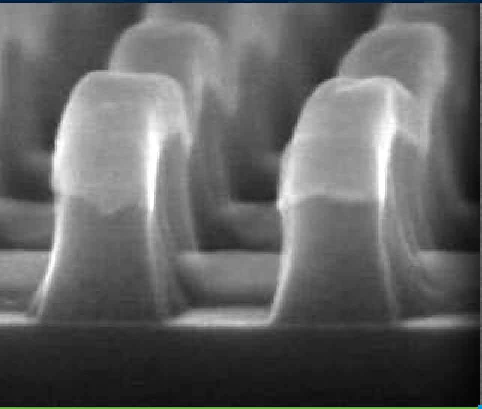
Mobility, Low Power

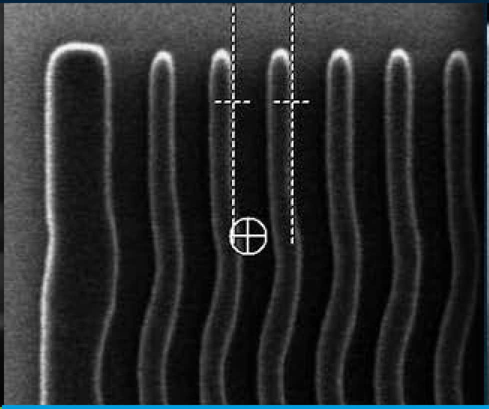
Mobile Internet Devices
Smart Phones

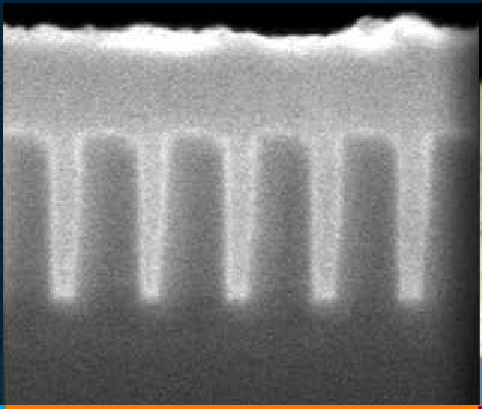
DDR3 DRAM

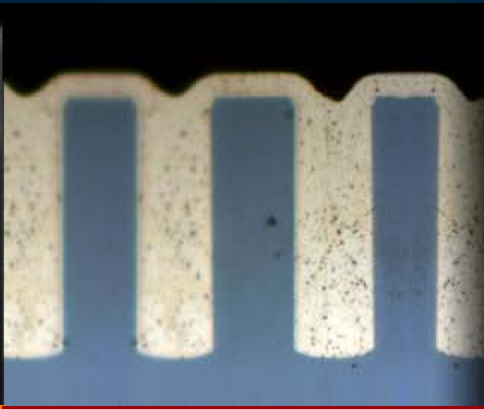
Low Power
Windows7™

Innovation Aligned with Inflections



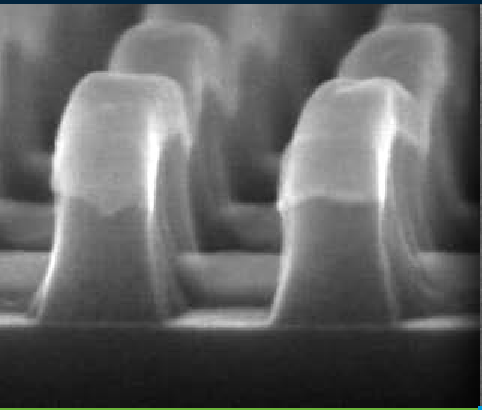
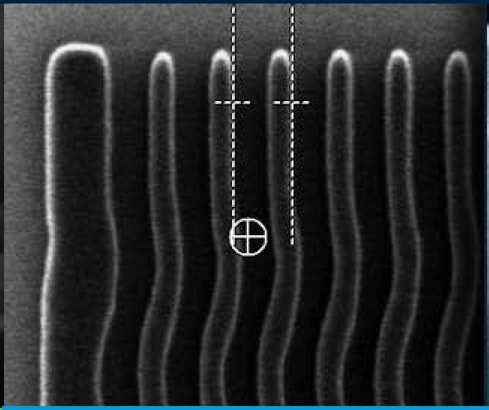
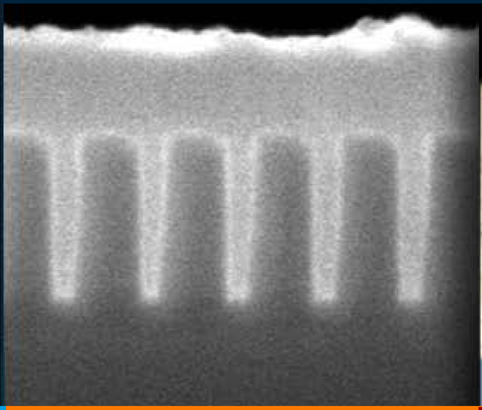
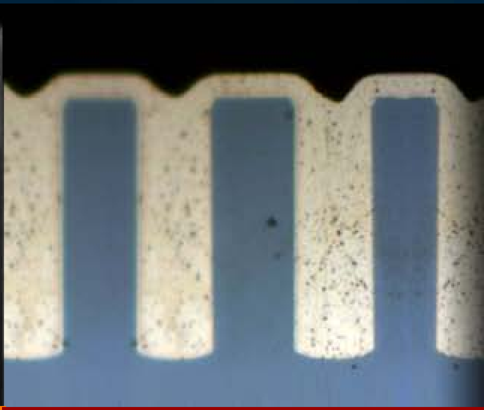






Transistor	**Patterning**	**Copper Interconnect**	**Wafer Level Packaging**
- Mobility, Low Power - DDR3 DRAM	- SSD - DDR3 DRAM	- Mobility, Low Power - SSD - DDR3 SRAM	- DDR3 DRAM - Mobility, Low Power - SSD

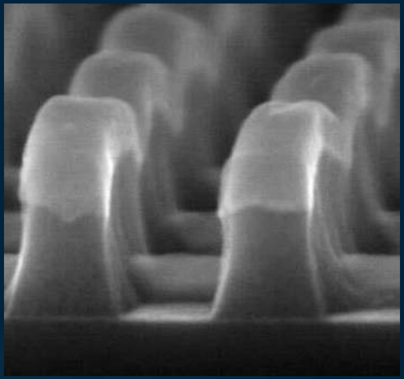
Innovation Aligned with Inflections

Transistor	**Patterning**	**Copper Interconnect**	**Wafer Level Packaging**
- High-k Metal Gate	- APF, DARC	- Dielectric CVD Etch	- TSV Etch
- High-k Etch	- APF/HM Etch	- Cu PVD	- Dielectric Liner CVD
- FinFET Etch, Doping	- SADP Etch	- Cu ECD (Semitool)	- Cu PVD
- STI Etch, Fill	- Spacer CVD, Etch	- Cu CMP	- Cu ECD (Semitool)
- CD, DR SEM	- CD, DR SEM	- BLOk	- Cu CMP
- Brightfield Inspection	- Brightfield Inspection	- Black Diamond	- DR SEM
	- Mask Inspection	- Brightfield Inspection	- Brightfield Inspection

Critical Metrology Remains Front-End Focused

Transistor

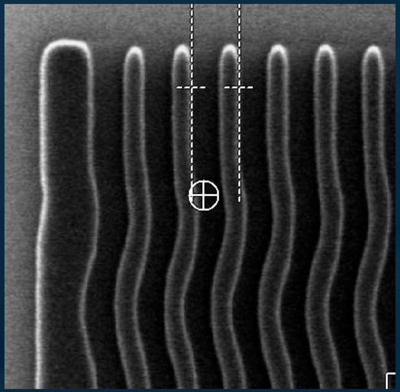


Characterization of new materials and defects

- Interface control
- Compositional stability

Non-planar inspection of 3D Transistors

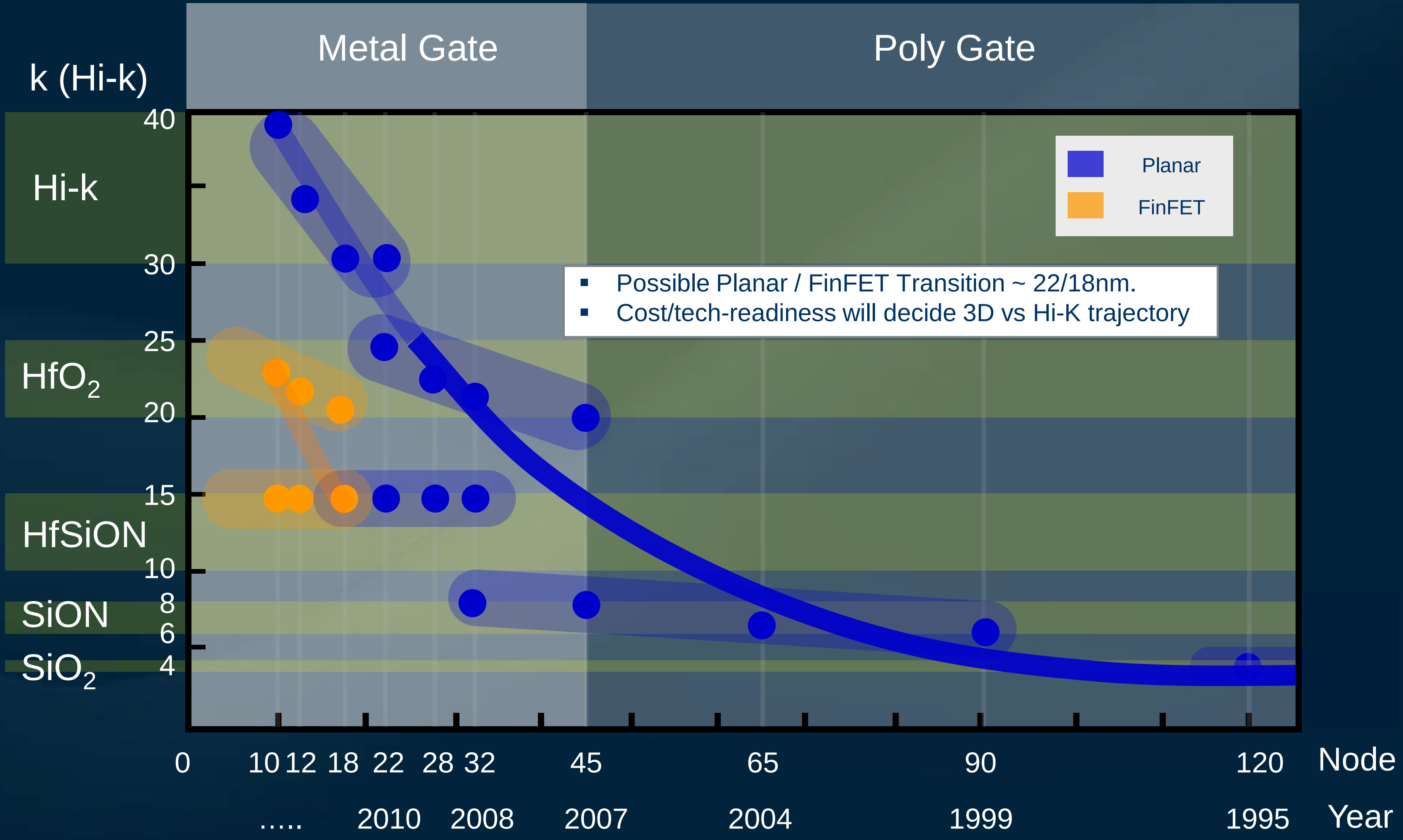
Patterning



Double patterning

Litho pattern transfer

Evolution of k - Scaling



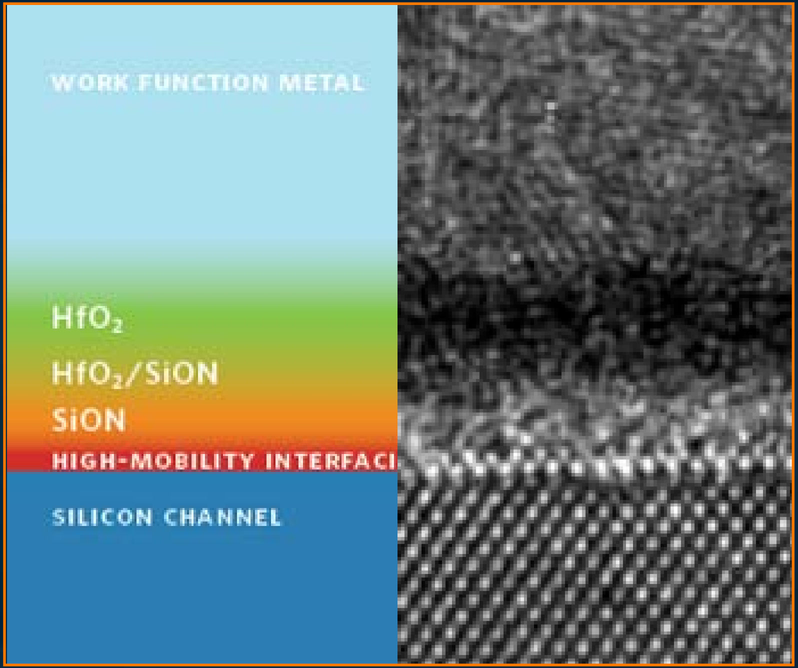
- Possible Planar / FinFET Transition ~ 22/18nm.
- Cost/tech-readiness will decide 3D vs Hi-K trajectory

APPLIED MATERIALS.

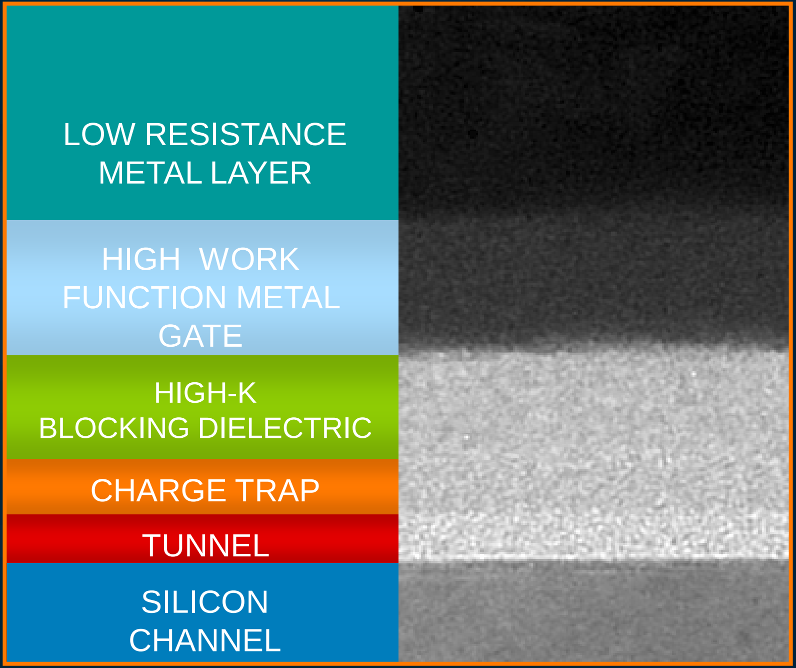
SILICON SYSTEMS GROUP

Interfaces Critical for High-k / Metal Gate

Logic High-k / Metal Gate Stack



NAND Charge Trap Flash



Issues and Challenges for Hi-k/MG Stack

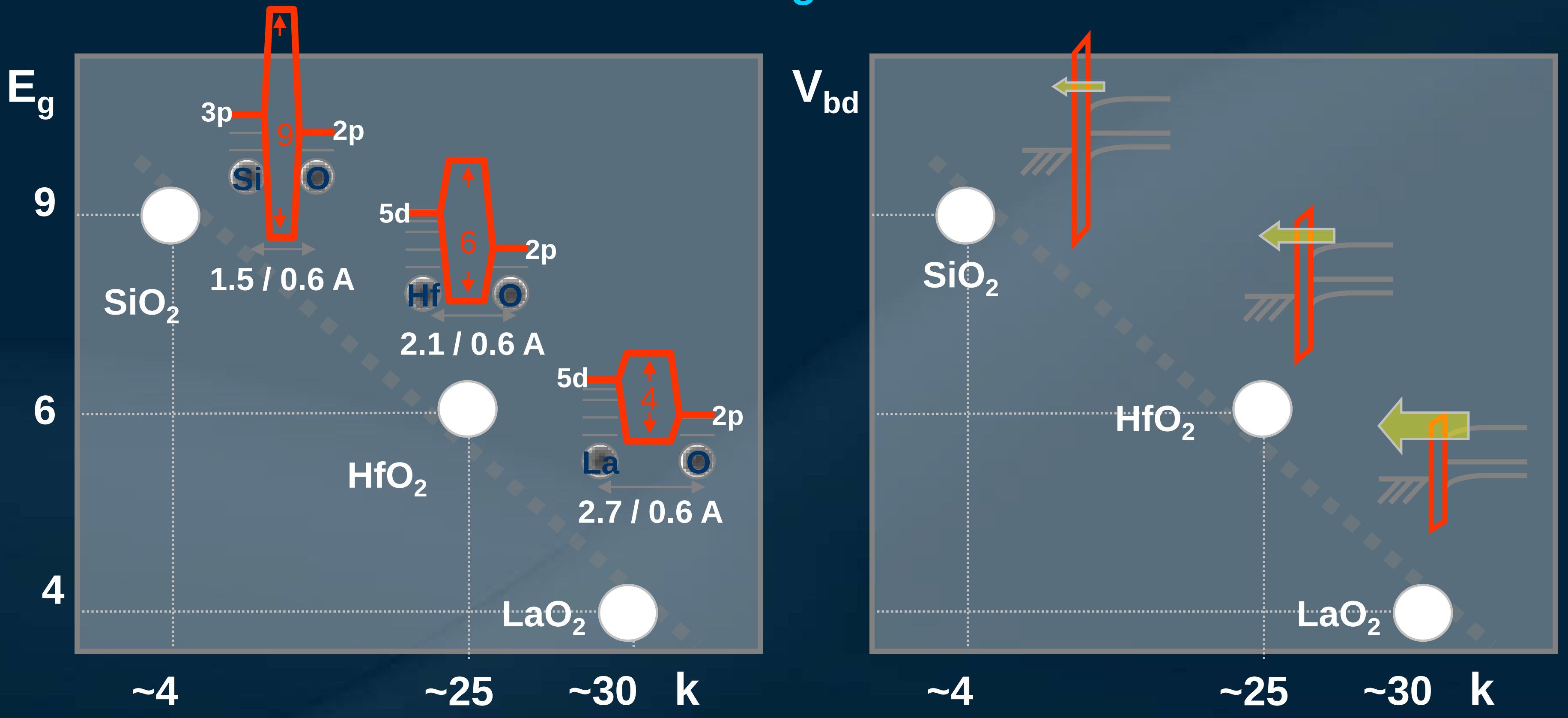
- Base Oxide
  - Development of sub-10A higher-k Box for EOT scaling
  - SiON: Proper N-dose and profile to maximize k and minimize EOT

- Hi-k
  - Morphology stability for GF & GL applications
  - Process control to minimize Oxygen vacancy (Vo)
  - Post deposition passivation for Oxygen vacancy suppression

- Capping Layer
  - Deposition sequence and etch selectivity
  - Insufficient Vt adjustment on PMOS with AlOx (requires $DV_t > 300mV$)
  - Mobility degradation due to over diffusion of La and Al species
  - Stringent uniformity requirement for Vt control WIW & WTW

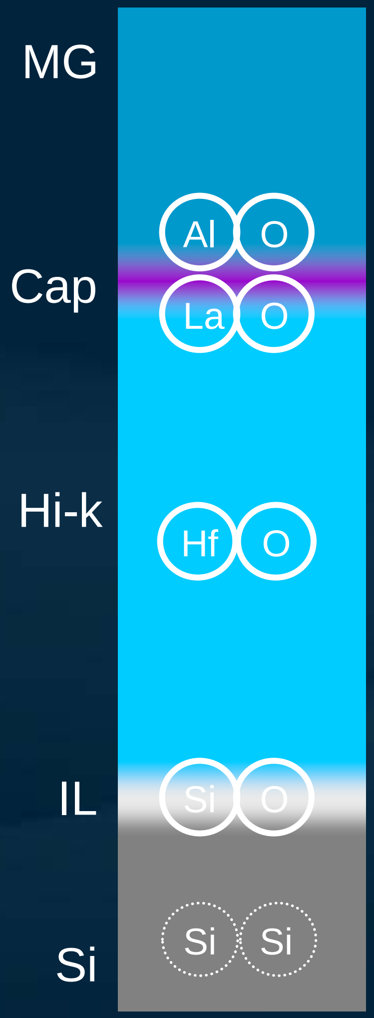
- MG
  - Deposition process control to prevent damage to cap layer & hi-k
  - Gap fill and overhang issue for both N and P devices

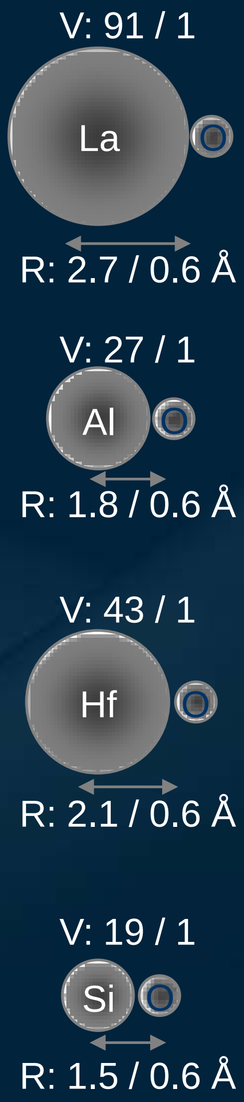
Fundamental Conflicts: E_g vs k vs V_{bd}



- Small bonding radius (ex SiO2): Larger Eg, smaller k, larger Vbd
- Large Bonding radius (ex LaO2): Smaller Eg, larger k, smaller Vbd

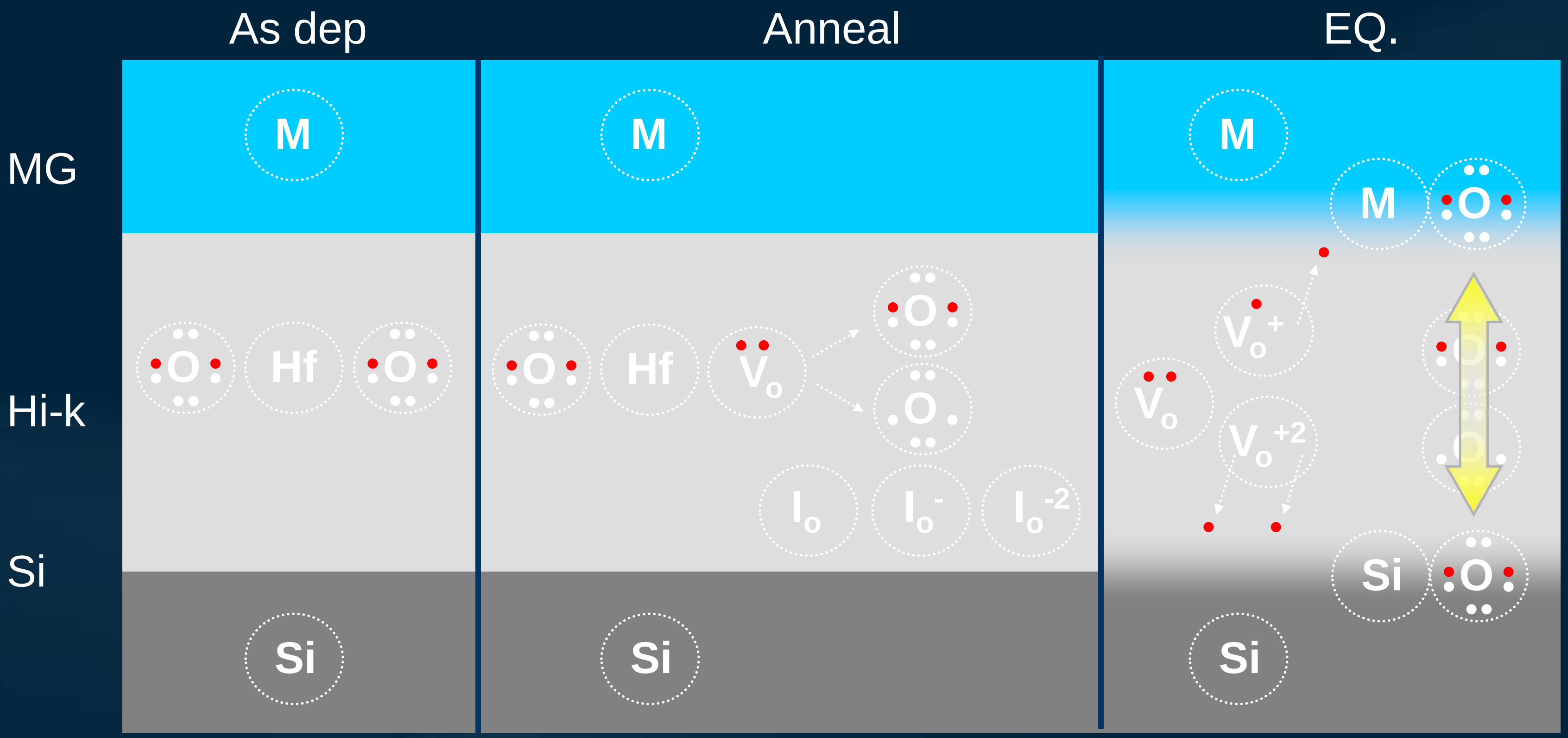
Stability of the Hi-k/MG Stack





Bonding pair	Bonding Energy (KJ/mole)
W-W	666
Ti-N	476
La-O	798
Al-O	501
Hf-N	535
Hf-O	801
O-N	631
Si-N	437
Si-O	799
Si-Si	310

Evolution and Formation of Vo and Io



- Oxygen atoms have the tendency to diffuse into Si sub and MG
- Formation Oxygen vacancy (V_o^+) or Oxygen interstitial (I_o^-) in hi-K layer
- Formation of SiOx IL (below hi-K) and MOx IL layer (above hi-K)
- Electron redistribution across IL's results in uncontrollable dipoles

Trends and Solutions for 2x nm

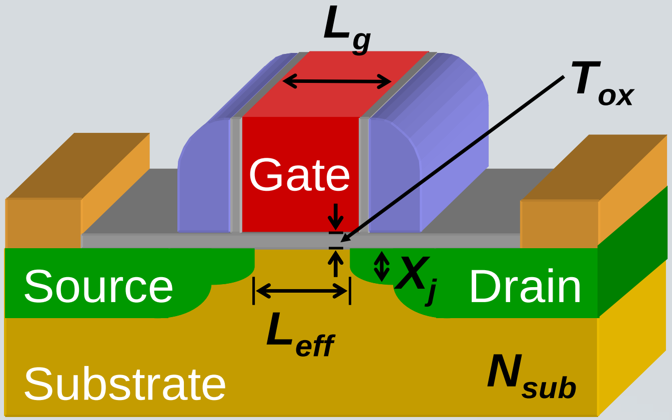
- Base Oxide
  - Use of SiON for aggressive EOT scaling in HP application
  - Utilize densified base Ox to prevent trace element penetration into channel

- Hi-k
  - Use of optimal ALD seq and temp for complete & secure in-film bonding
  - Post deposition anneal to suppress Vo formation (ie; NH3 PDA)
  - Post deposition nitridation for morphology stability and Vo reduction

- Capping Layer
  - Possible alternatives for PMOS: MnOx, VOx, TaOx, ZrOx
  - Use of densified base Ox to prevent La or Al penetration to channel
  - Use of uniform deposition technique / process for Vt control

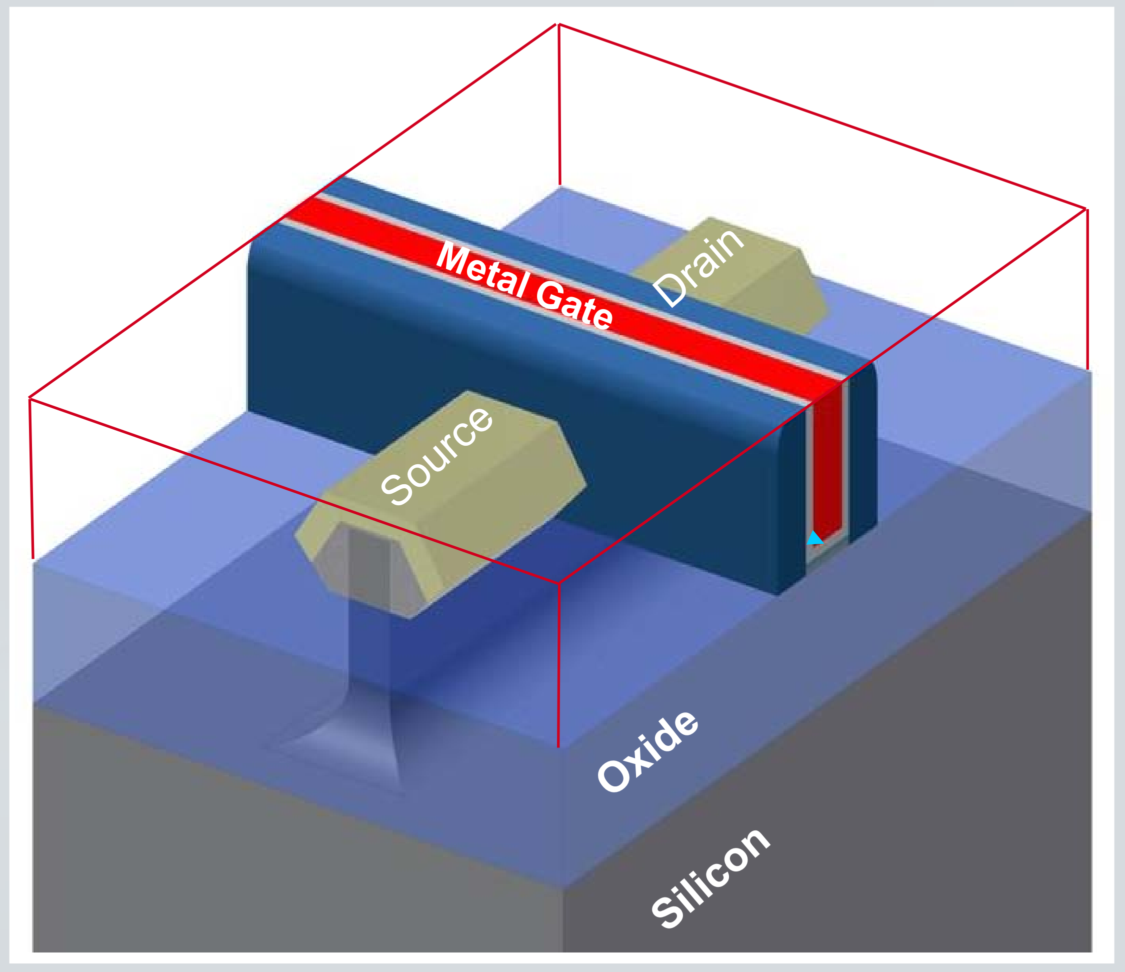
- MG
  - Low damage deposition to prevent Metal or N diffusion into hi-k
  - ALD metal dep for GL or 3D applications

Device Structure Innovation



Enabling Technologies for FinFET Fabrication

- Etch
  - Fin Etch (i.e. STI Etch)
  - STI Oxide Recess Etch
  - Gate Etch
  - Side-Wall-Spacer Etch
- Front-End Processing
  - Base Oxide and Nitridation
  - High-k Deposition and Nitridation
  - Doping
  - RTP and Laser Anneal
  - EPI (Si, SiC, and SiGe)
- Metal Deposition
  - Dielectric Capping Film
  - Work Function Film
  - Barrier Film
  - Bulk Metal Fill
- CMP
  - STI CMP
  - Polysilicon Planarization
  - Polysilicon Opening Polish
  - Metal Gate Polish
- Dielectric Deposition
  - Dielectric Film as Doping Source
  - Low-k Side-Wall-Spacer Film
  - Low Temp Oxide Liner/Spacer
  - PMD Film
  - Patterning Film



- Inspection and Metrology
  - Fin sidewall angle control
  - Detection and review of defects on fin sidewall
  - Gate cd control across fin height

Enabling Technologies for FinFET Fabrication

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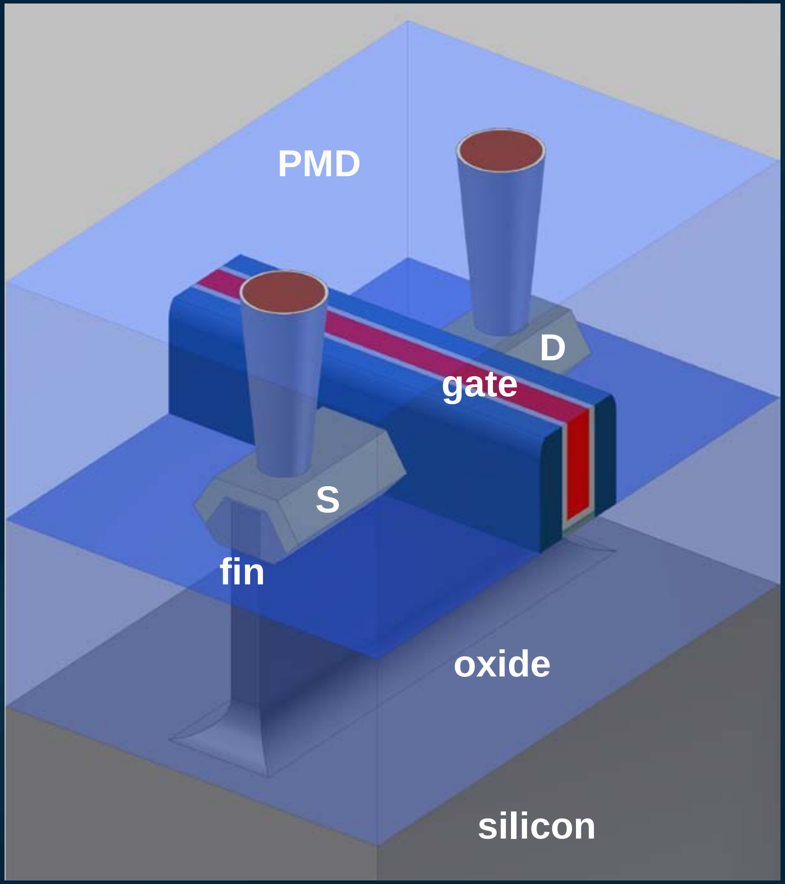

- Inspection and Metrology
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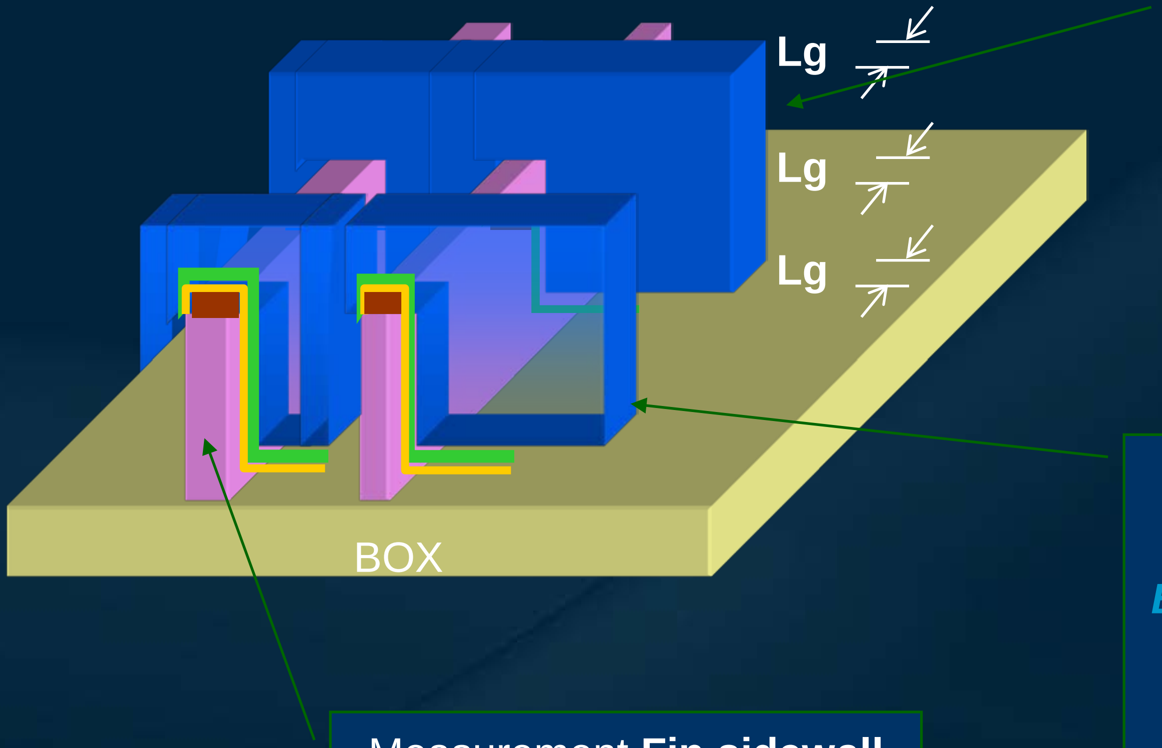
FinFET – M&I Challenges and Applications



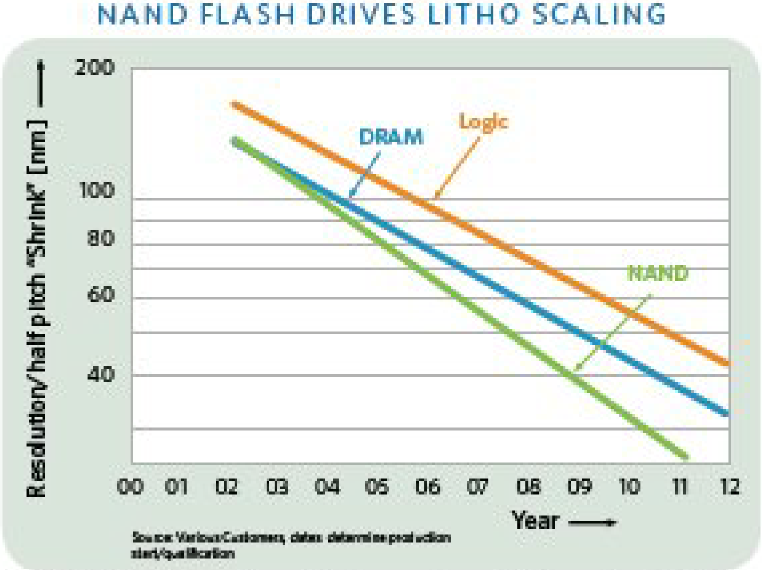
Measurement of **gate CD** across the Fin height
CD SEM Metrology

Detection of **defects on Fin sidewalls** after gate etch
Brightfield Wafer Inspection

Tilted review of the detected **defects on the fin sidewall**
SEM Defect Review

Measurement **Fin sidewall angle** to control the **3D transistor width**
CD SEM Metrology

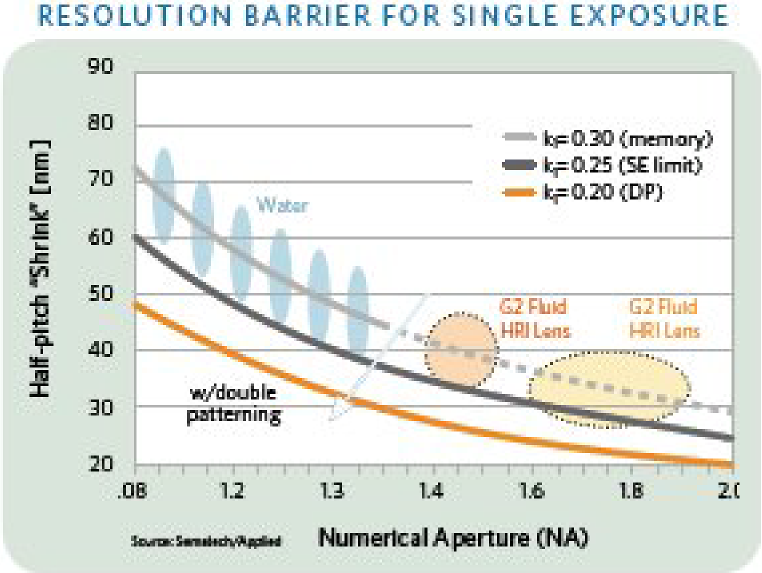
Next Generation Lithography



NAND FLASH DRIVES LITHO SCALING

Source: Various Customers, dates determine production start/qualification

NAND Flash is driving the resolution requirements below 45nm by 2008. DRAM will follow one to two years later.



RESOLUTION BARRIER FOR SINGLE EXPOSURE

Source: Sematech/Applied

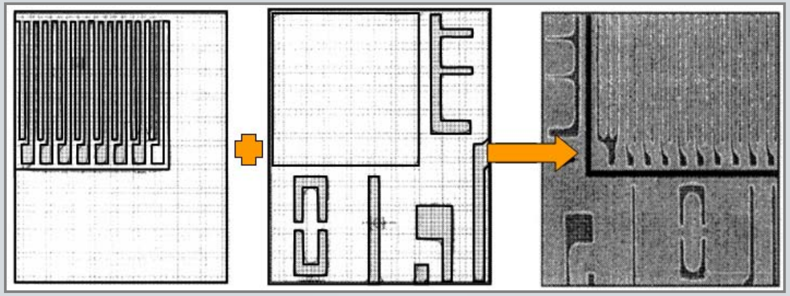
With 193nm exposure wavelength and current NA, double patterning is the only way to reach the required half-pitch for 32nm.

- Flash - aggressive half pitch needs
- Immersion lithography – resolution limitations
- Double patterning is the present scheme to reach the required half pitch

The Many Forms of Double Patterning

Double exposure illumination splitting

Dipole Conventional



Line + cut, and / or printed assist features + removal

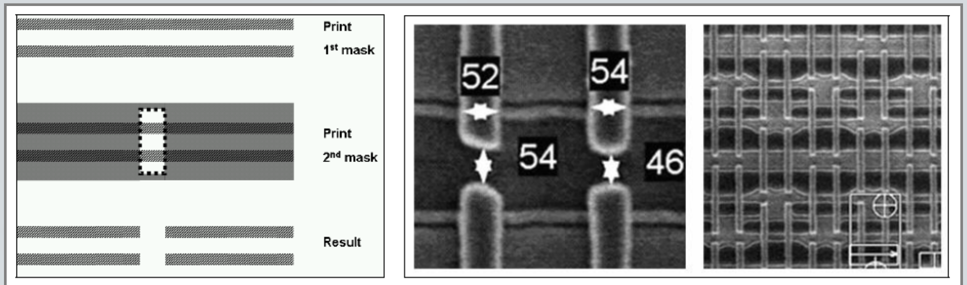
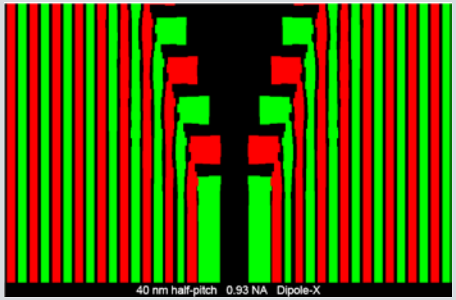


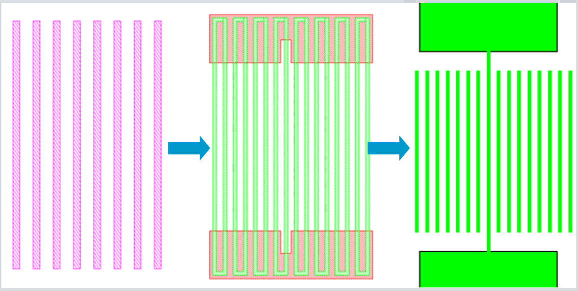
Figure 2: Line cutting double patterning scheme and experimental results post final etch using 193nm dry lithography with a NA of 0.93 for SRAM poly-conductor level (from Zhuang *et al.* [2]).

Pitch fragmentation

Double Patterning (litho etch litho etch)



Sidewall Spacer Double Patterning

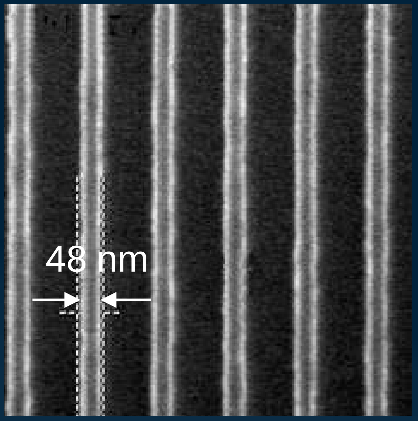


External Use

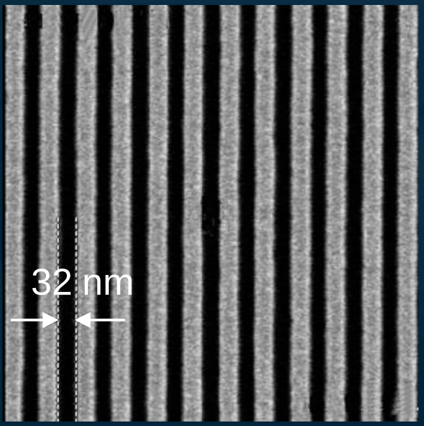
Double Patterning Metrology Challenges

Line Edge Roughness (LER)

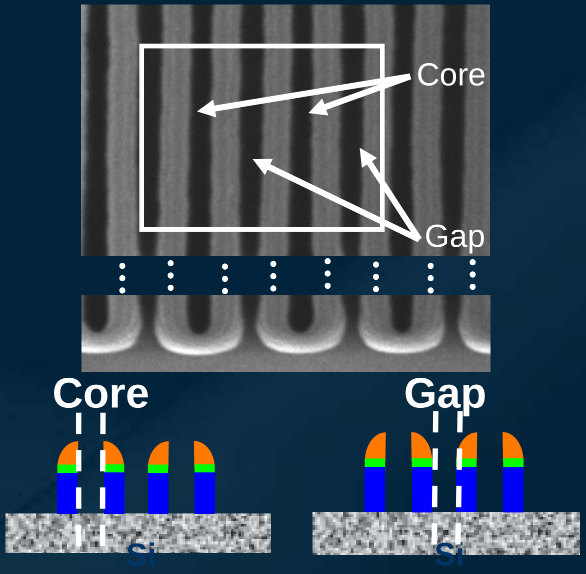
Photoresist Before Trim



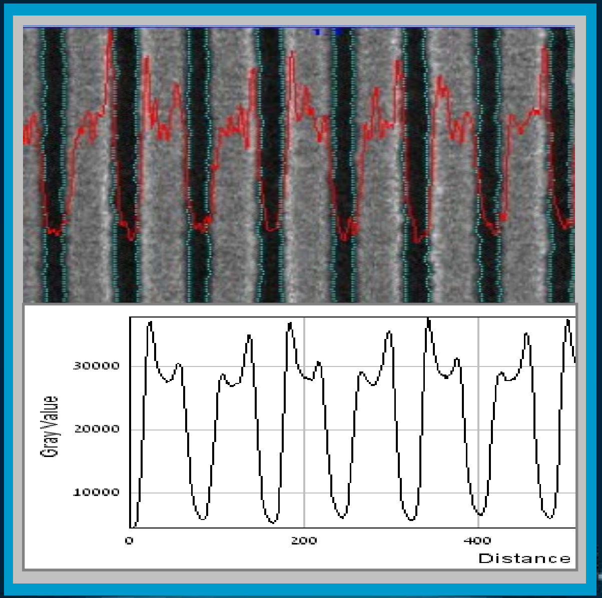
LER: 3.1nm



LER: 1.5nm



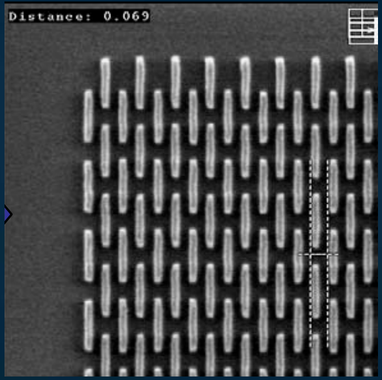
Core/Gap Etch Trim Control



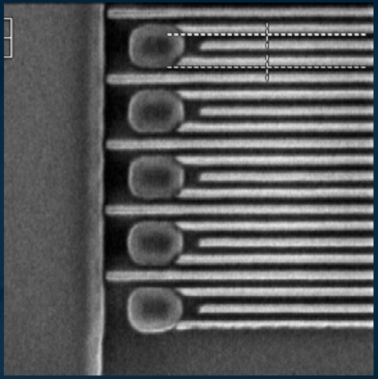
Growing Double Patterning Use

Migration to DRAM

Shallow Trench Isolation

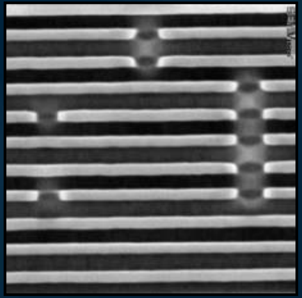


Bit Line, Word Line

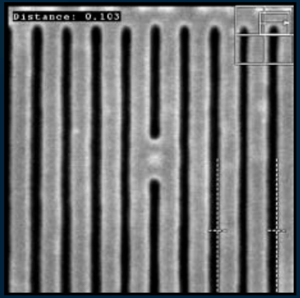


Gridded Design Rules
Logic to 16nm Node

Poly GDR

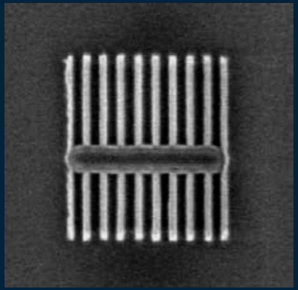


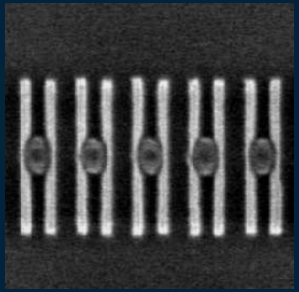
Metal 1&2 GDR



2-D Logic on the Way

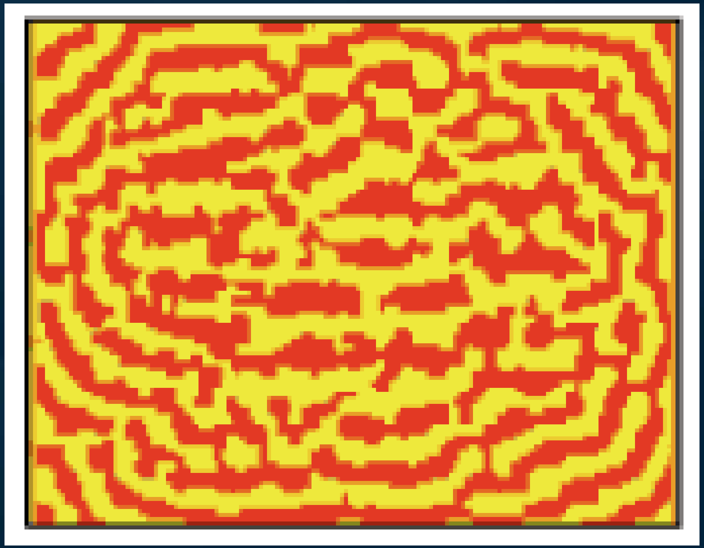
3-Mask EDA Tools Verified



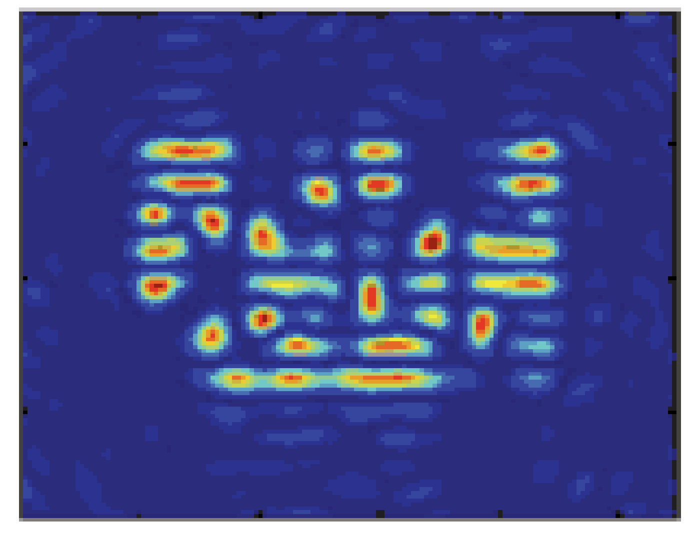


Printing Challenges at 2xnm

- Double patterning
  - k1 is relaxed, but requirement on defect signal to noise continues to increase
  - Tight CDU requirements - Overlay of 2 masks contributes to wafer CD error
- Source mask optimization
  - Mask patterns become more complex
  - Printability connection between mask and wafer even looser



Mask pattern



Aerial image

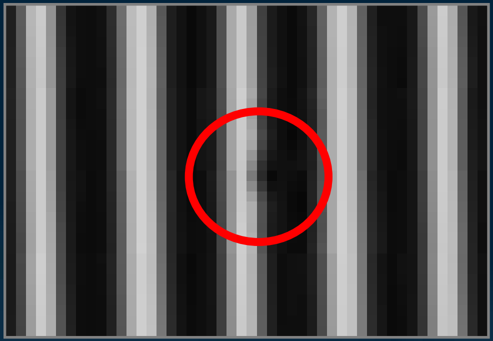
Prediction of Printing Defects

Low k_1 Mask

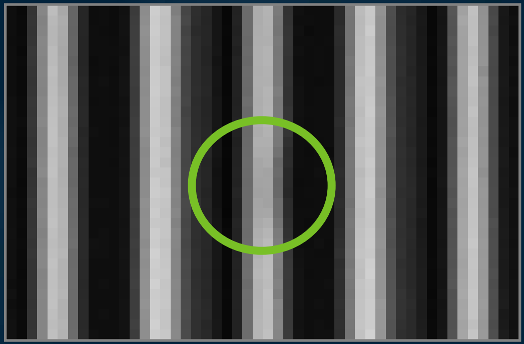
Standard Inspection Image
"What the mask looks like"

Aerial Image
"What the wafer looks like"

Non-printing defect

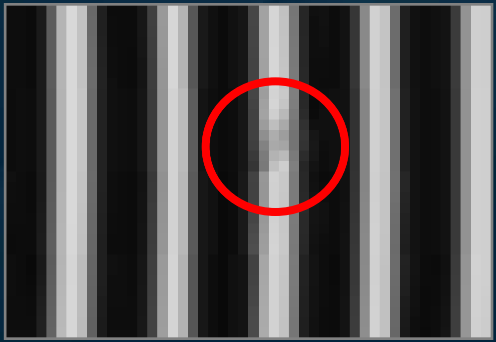


Defect

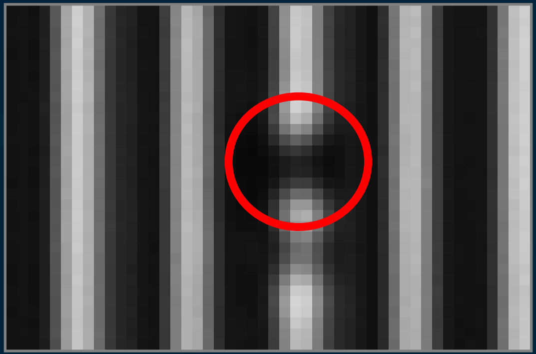


Non-printing Defect

Printing defect



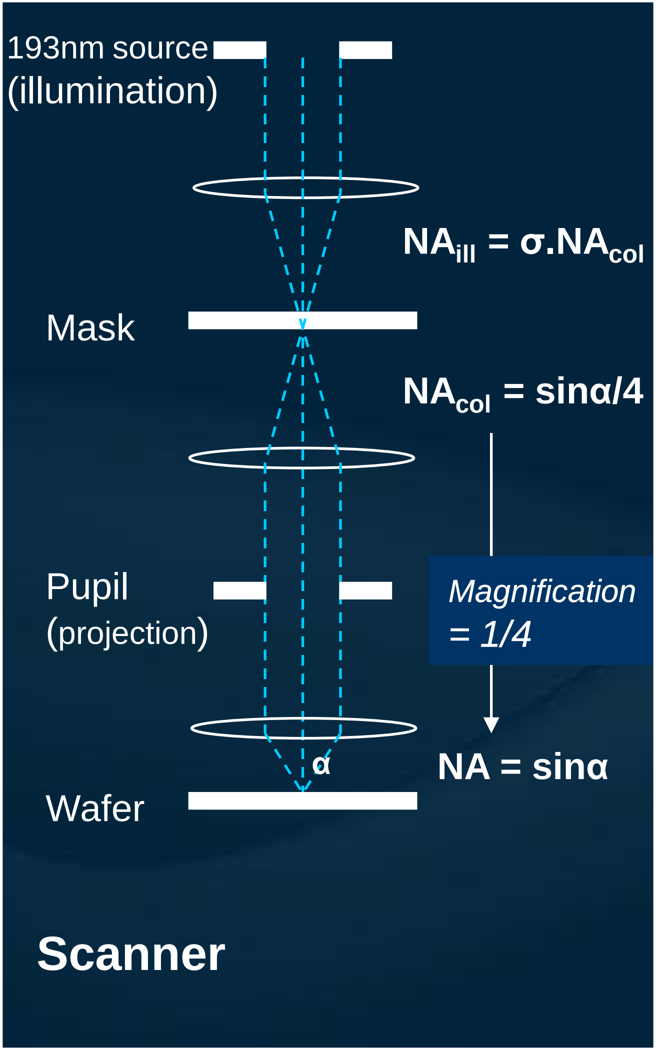
Defect



Printing Defect

Aerial Imaging Technology

Same pupil shape, NA, and σ as the scanner



193nm source (illumination)

$NA_{ill} = \sigma.NA_{col}$

Mask

$NA_{col} = \sin\alpha/4$

Pupil (projection)

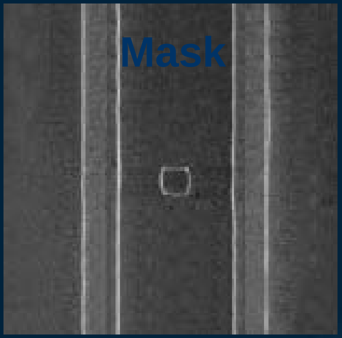
Magnification = 1/4

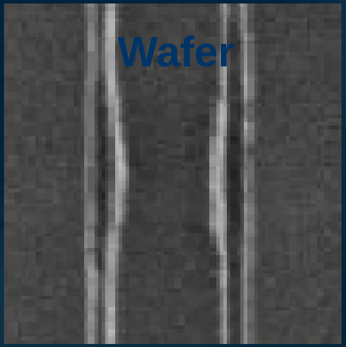
α

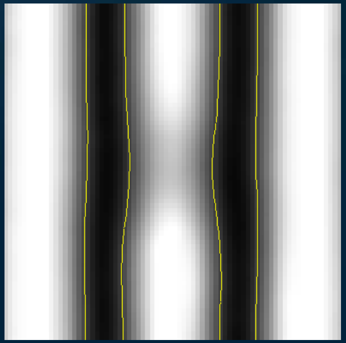
$NA = \sin\alpha$

Wafer

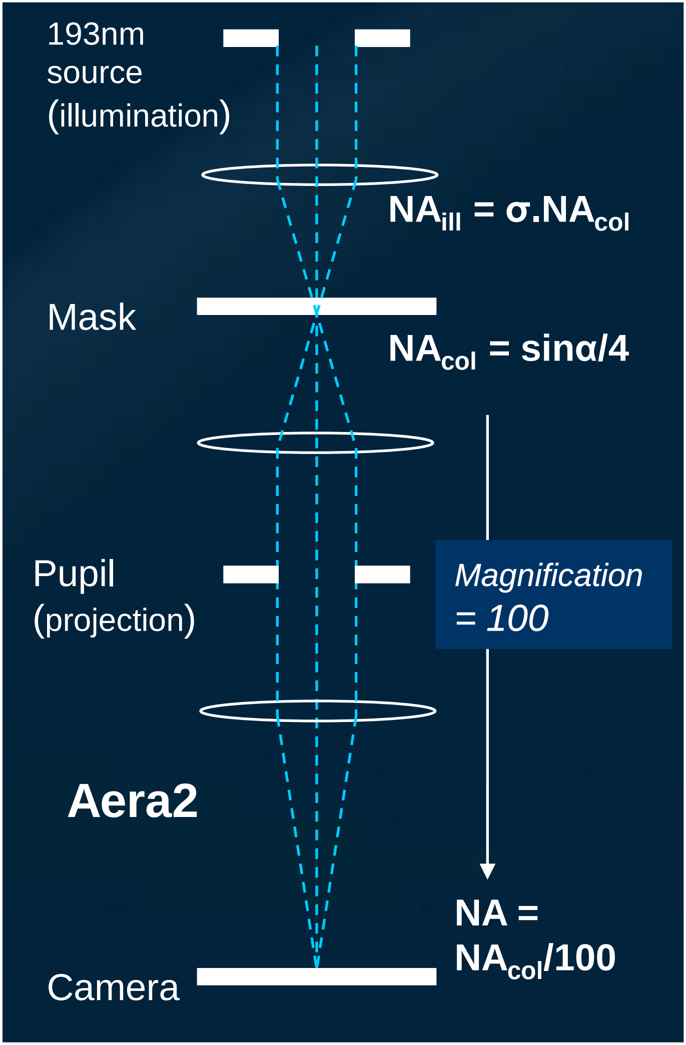
Scanner







Aerial Image



193nm source (illumination)

$NA_{ill} = \sigma.NA_{col}$

Mask

$NA_{col} = \sin\alpha/4$

Pupil (projection)

Magnification = 100

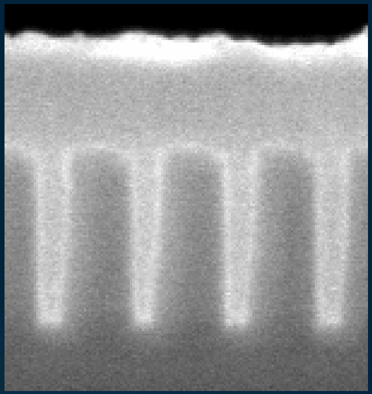
Aera2

$NA = NA_{col}/100$

Camera

Back-end Processing Challenges

Cu Interconnect



Effective scaling – controlling R (metal) and C (dielectric)
  - Cu gapfill and resistivity control
  - Lower K dielectric materials with good Hardness, modulus, Stress

Maintaining interface integrity

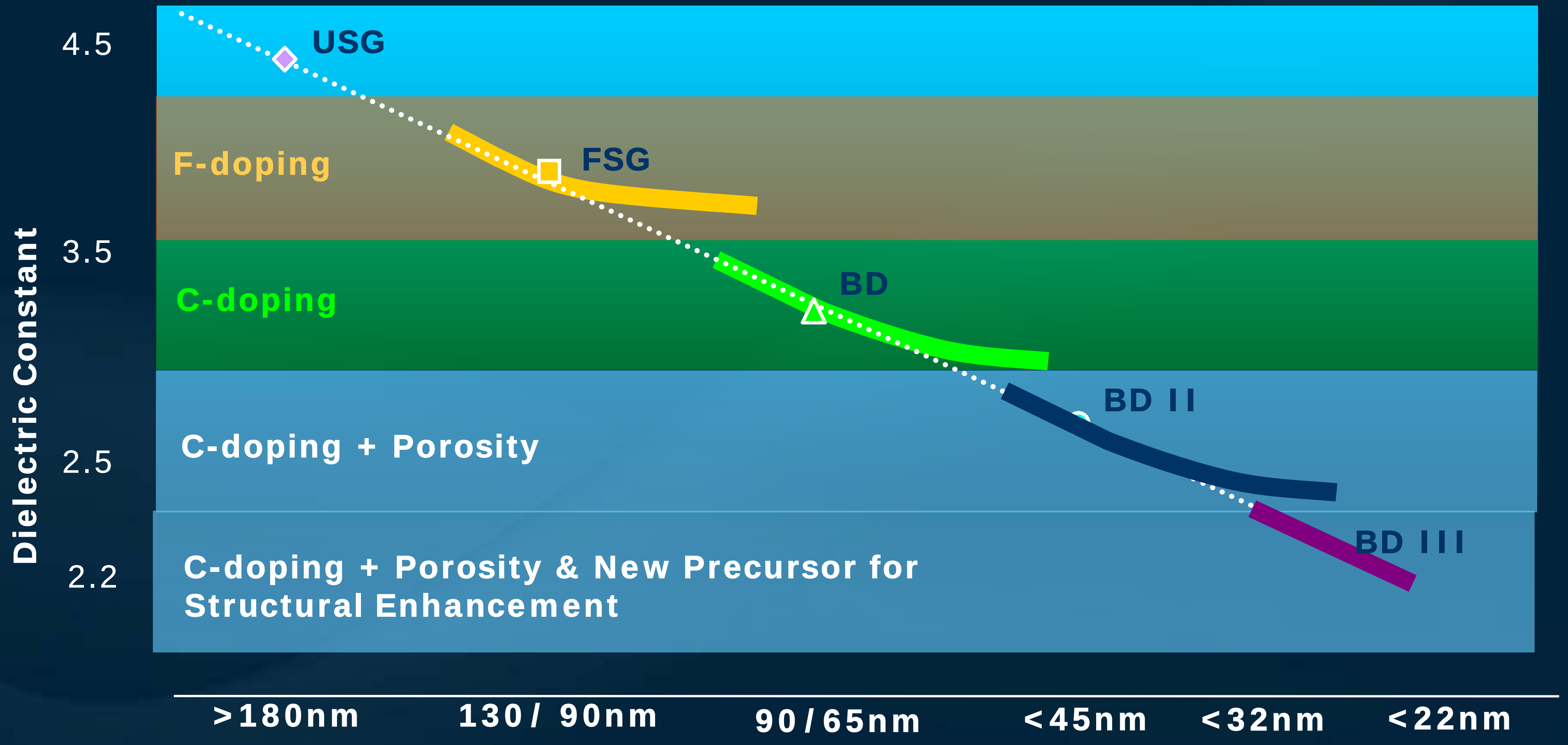
Profile and damage control

Wafer Level Packaging

High productivity, low cost processes

Via profile control

Applied Materials Low k IMD Roadmap

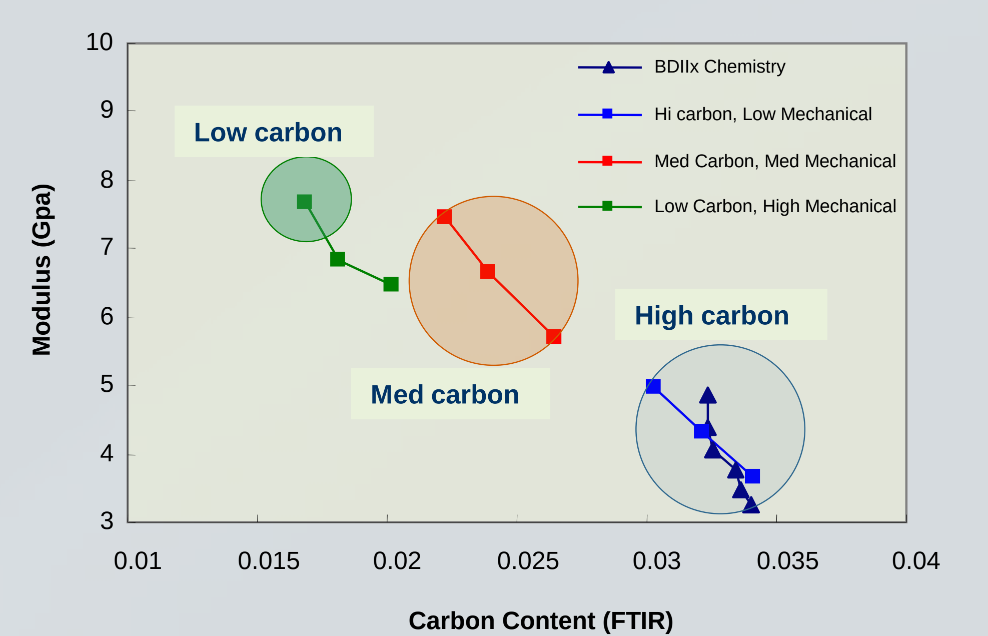


New precursor chemistry being evaluated for k ~ 2.2

Low K Development Activities for 22nm

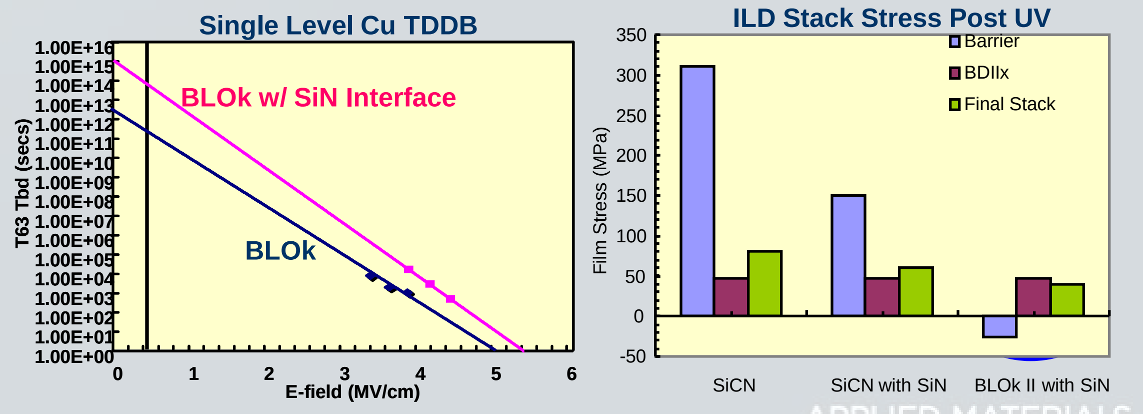
Black Diamond III

- Targeting higher modulus with sufficient carbon content to improve integration performance
- Same methyl content due to various process can yield to different modulus

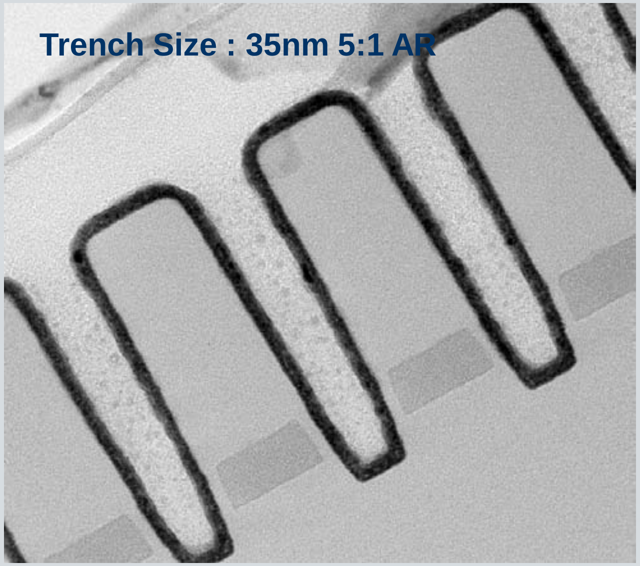


BLOk II

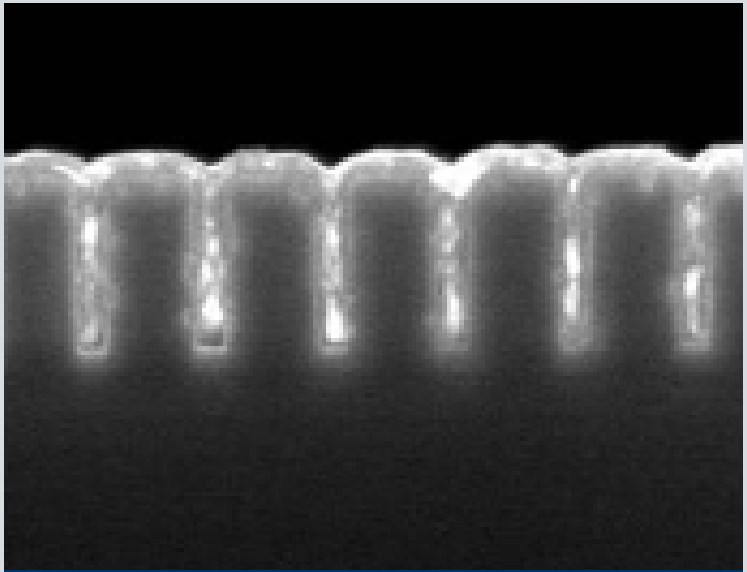
- Enhanced Nitride Interface
  - Improves adhesion and TDDB
  - Provides stress management to improve UV compatibility



Next Generation Cu Interconnect: Direct Plating



CVD Metal on PVD TaN

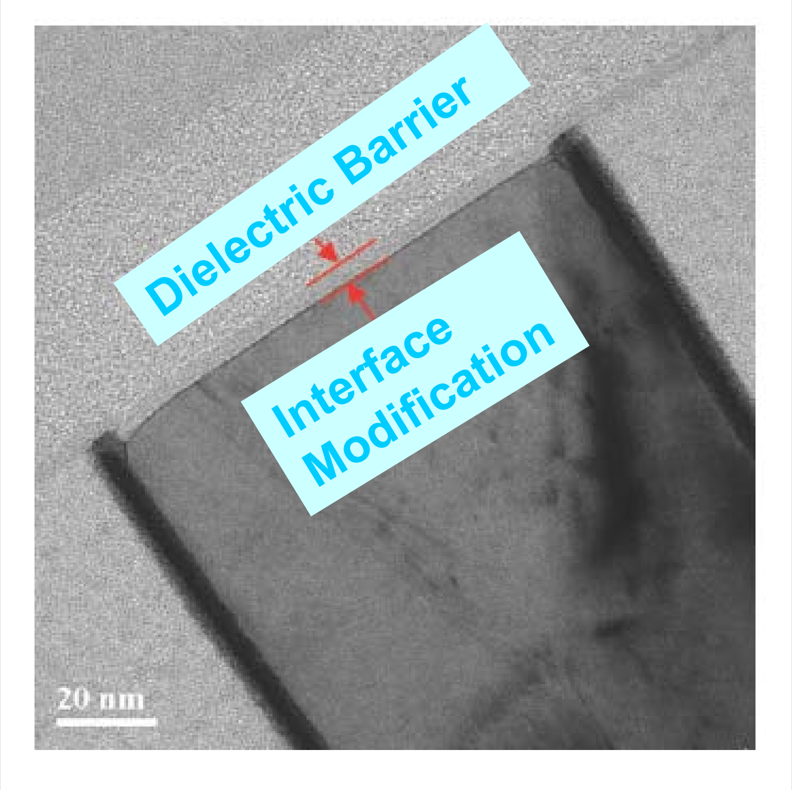


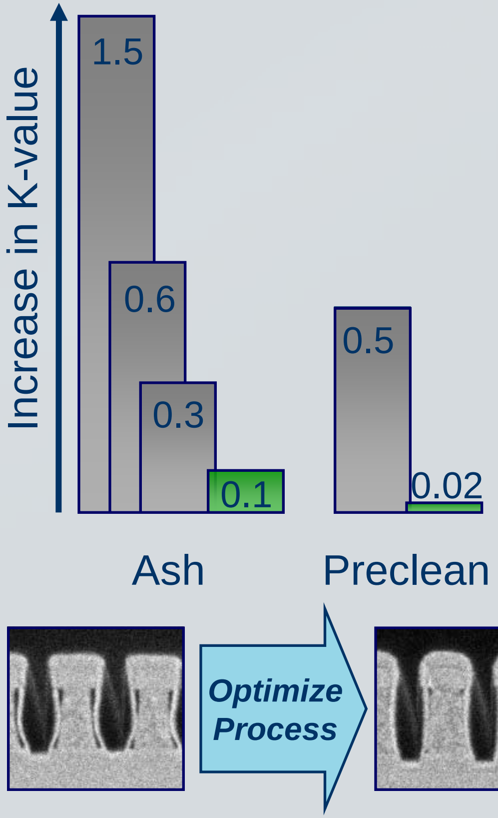
Post ECP fill with Semitool ECP

- Step coverage >90%, prevent overhang
- Continuous, smooth film

- Conformal seed coverage
- Full fill

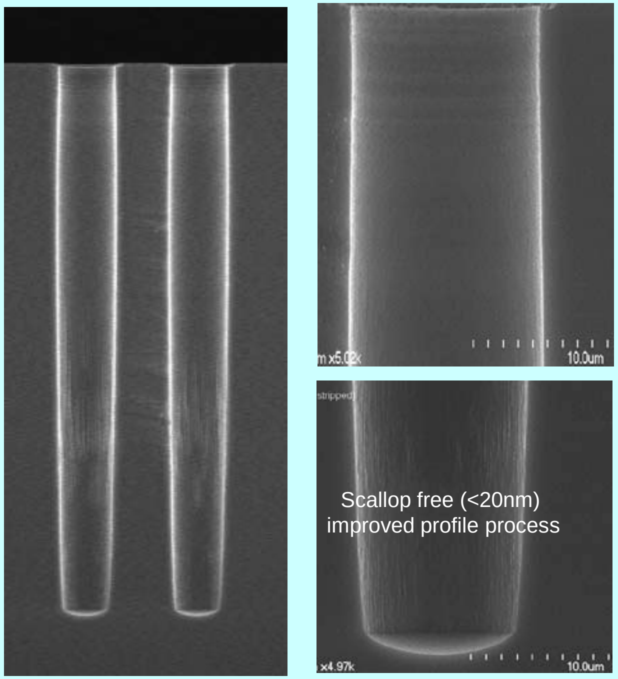
Logic Challenge: Low k Integration





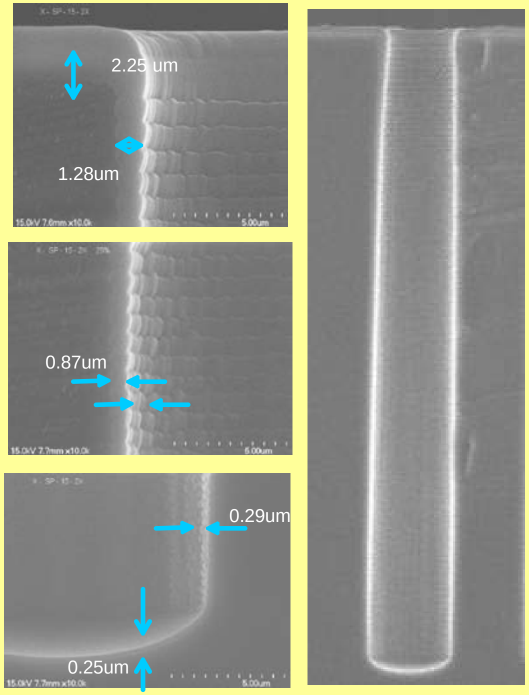
- Low k interface integrity
  - Adhesion
  - EM performance
- Profile control via ash and preclean damage minimization

Technologies for TSV

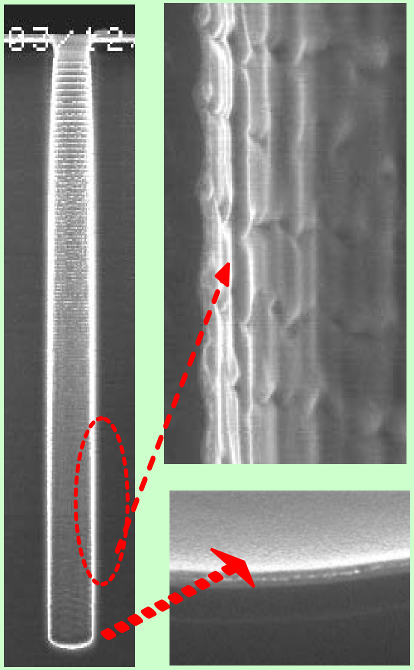


Scallop free (<20nm) improved profile process

TSV Etch
Scallop, Etch Depth, Selectivity, Throughput



Dielectric Oxide Liner
Step Coverage, Thermal Budget



Barrier-Seed
Scallop, Seed Coverage and Fill

Key solution elements have been successfully demonstrated as extensions of CMOS processing

TSV Via Fill

25µm X 80µm

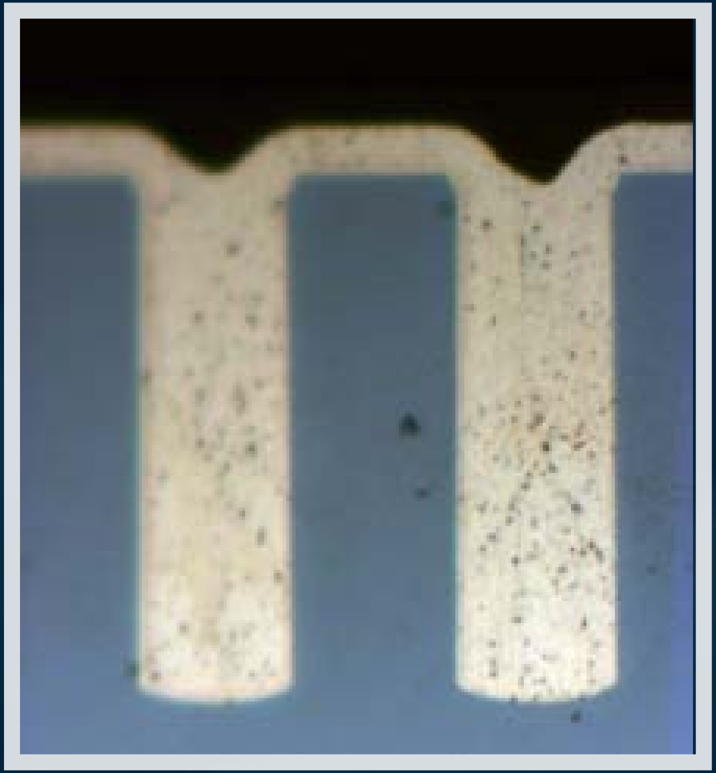
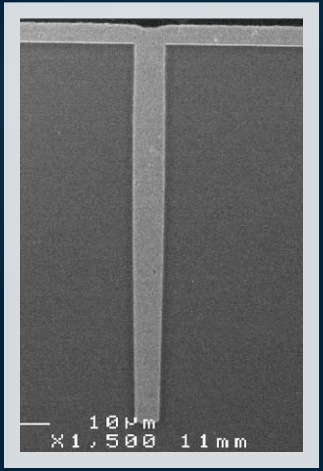


Image Sensor

10µm X 100µm

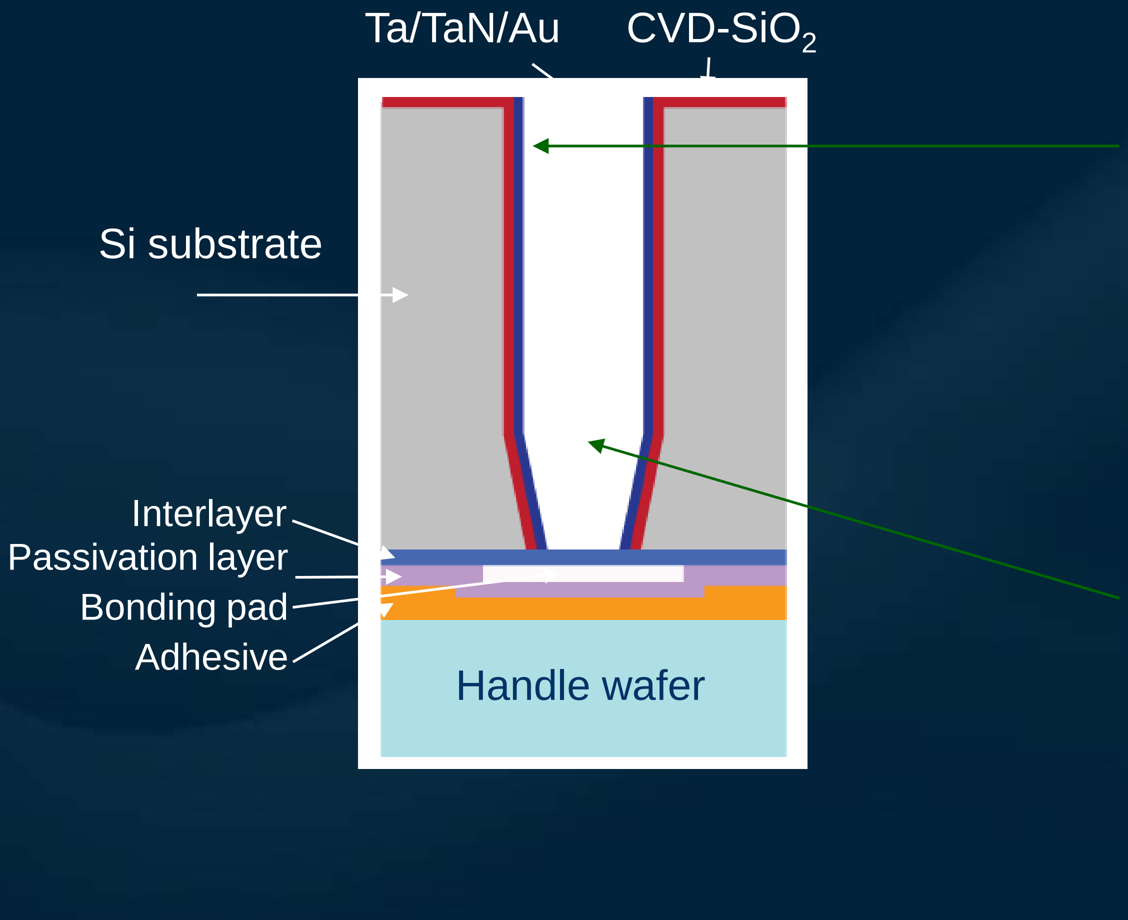
DRAM

5µm X 50µm



Logic

TSV – M&I Challenges and Applications



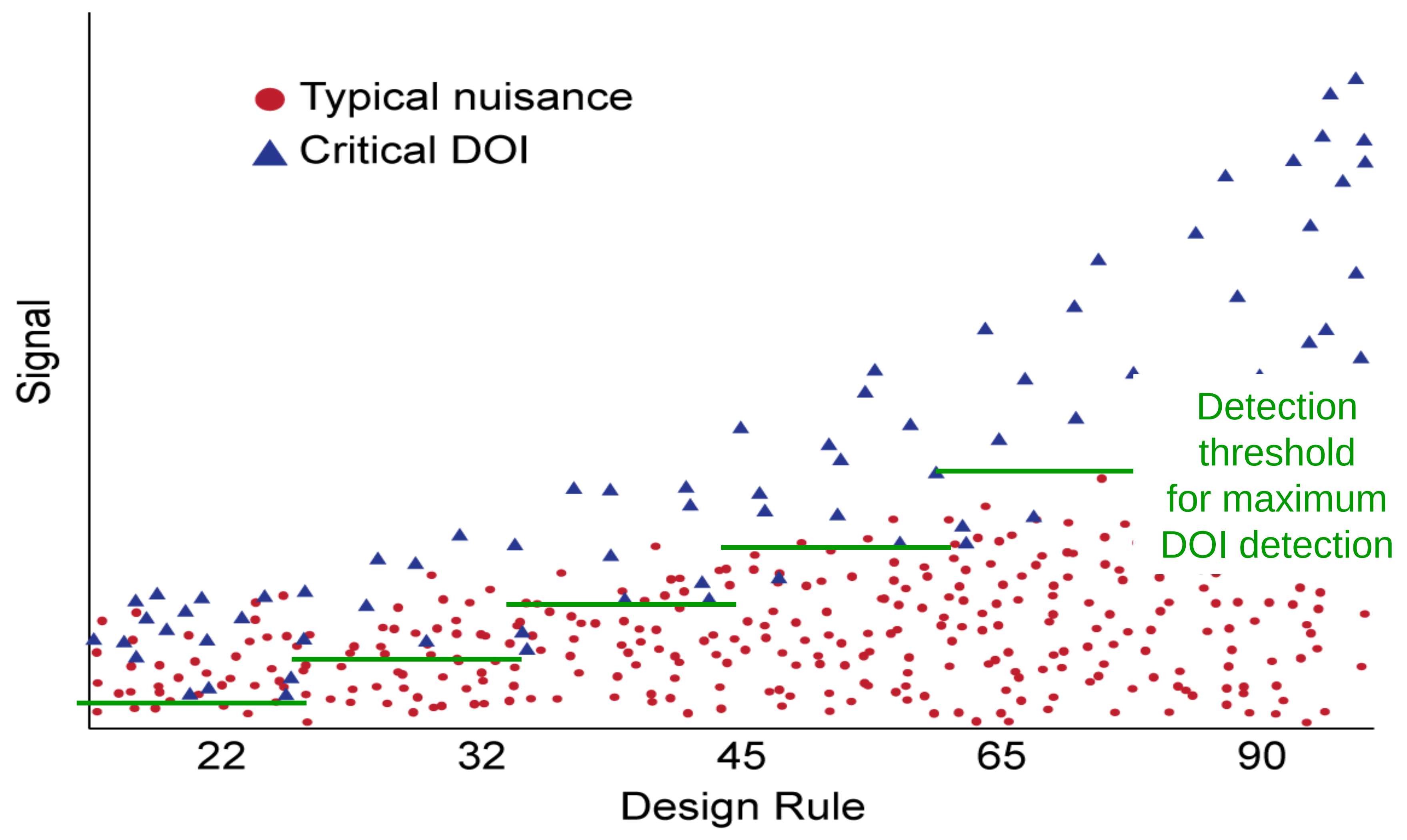
Wafer inspection for **surface defects on TSV sidewalls**

Darkfield Wafer Inspection

HAR SEM-based defect review for **sidewall and bottom defects**

SEM Defect Review and Analysis

Design rules shrink, defects hide in the noise



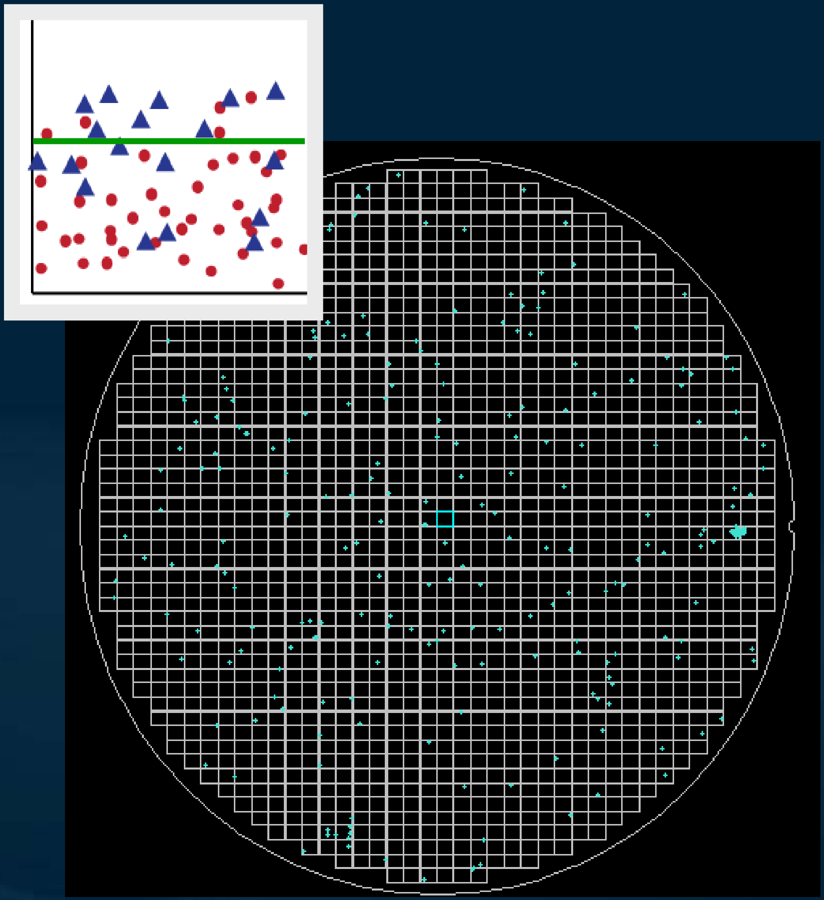
APPLIED MATERIALS.

SILICON SYSTEMS GROUP

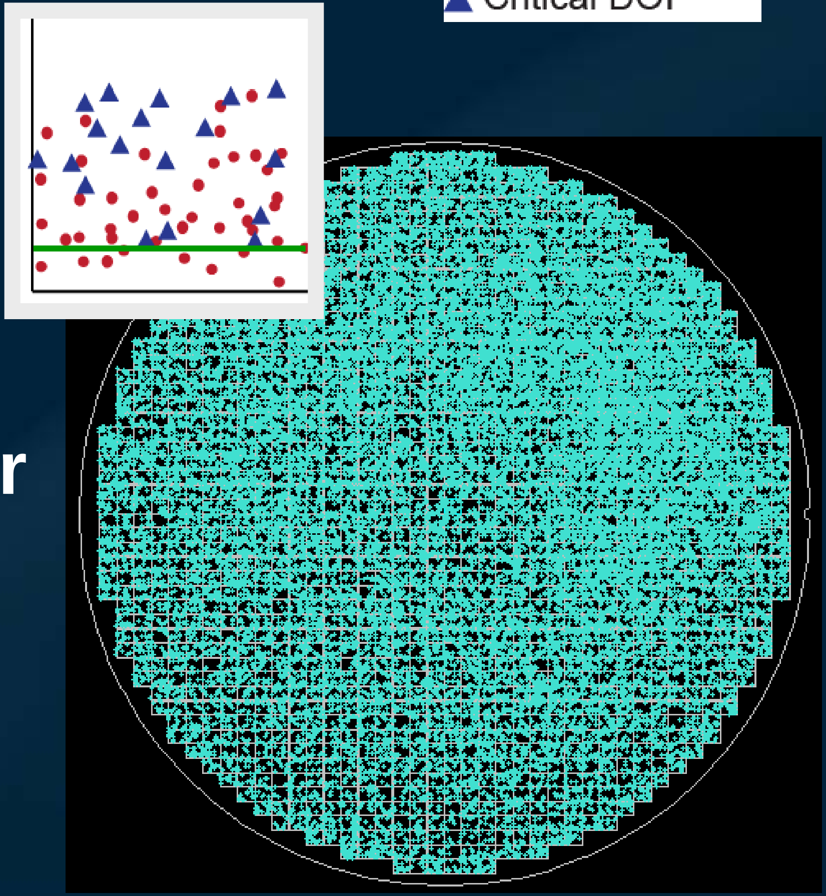
External Use

Inspection Options

● Typical nuisance
▲ Critical DOI



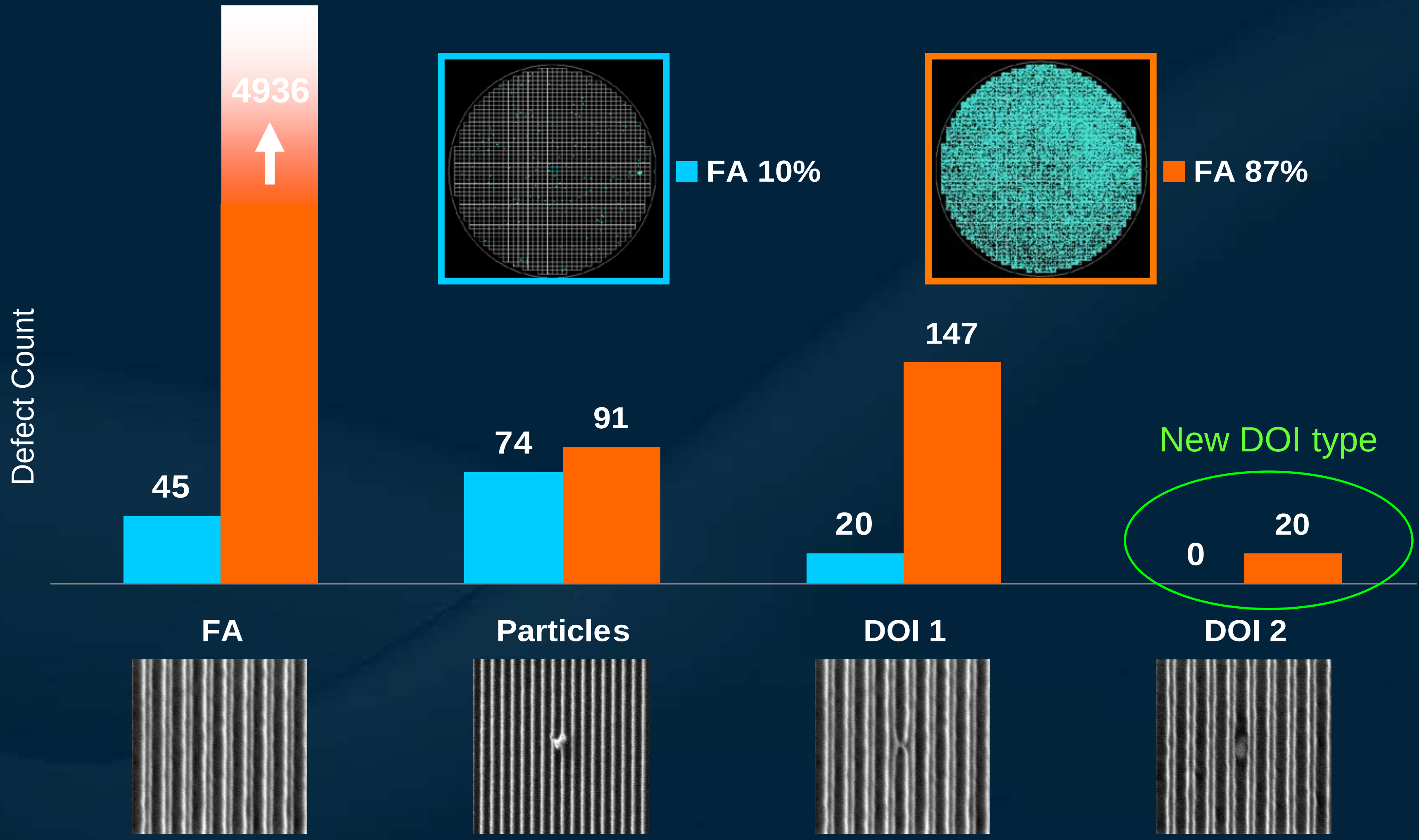
or



- ✗ Don't find all DOI's
- ✓ Manageable data

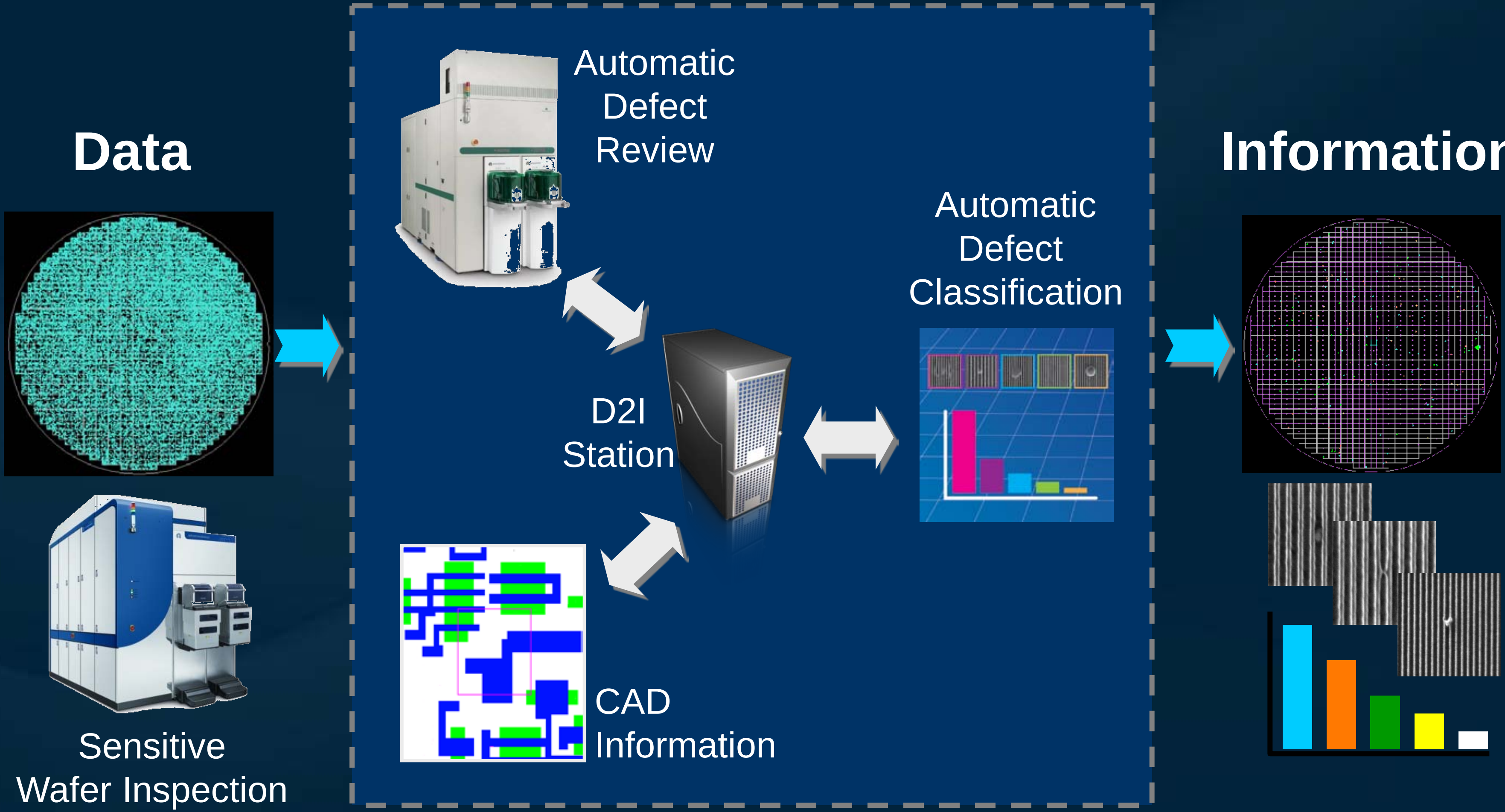
- ✓ Find all DOI's
- ✗ Vast amount of nuisance

A Painful Tradeoff – Sensitivity or Practicality



Increasing sensitivity detects new DOI but creates unmanageable amounts of data

Data to Information Flow – Basic Architecture



D2I Flow

Data

Sensitive
Wafer Inspection

Automatic
Defect
Review

D2I
Station

CAD
Information

Automatic
Defect
Classification

Information

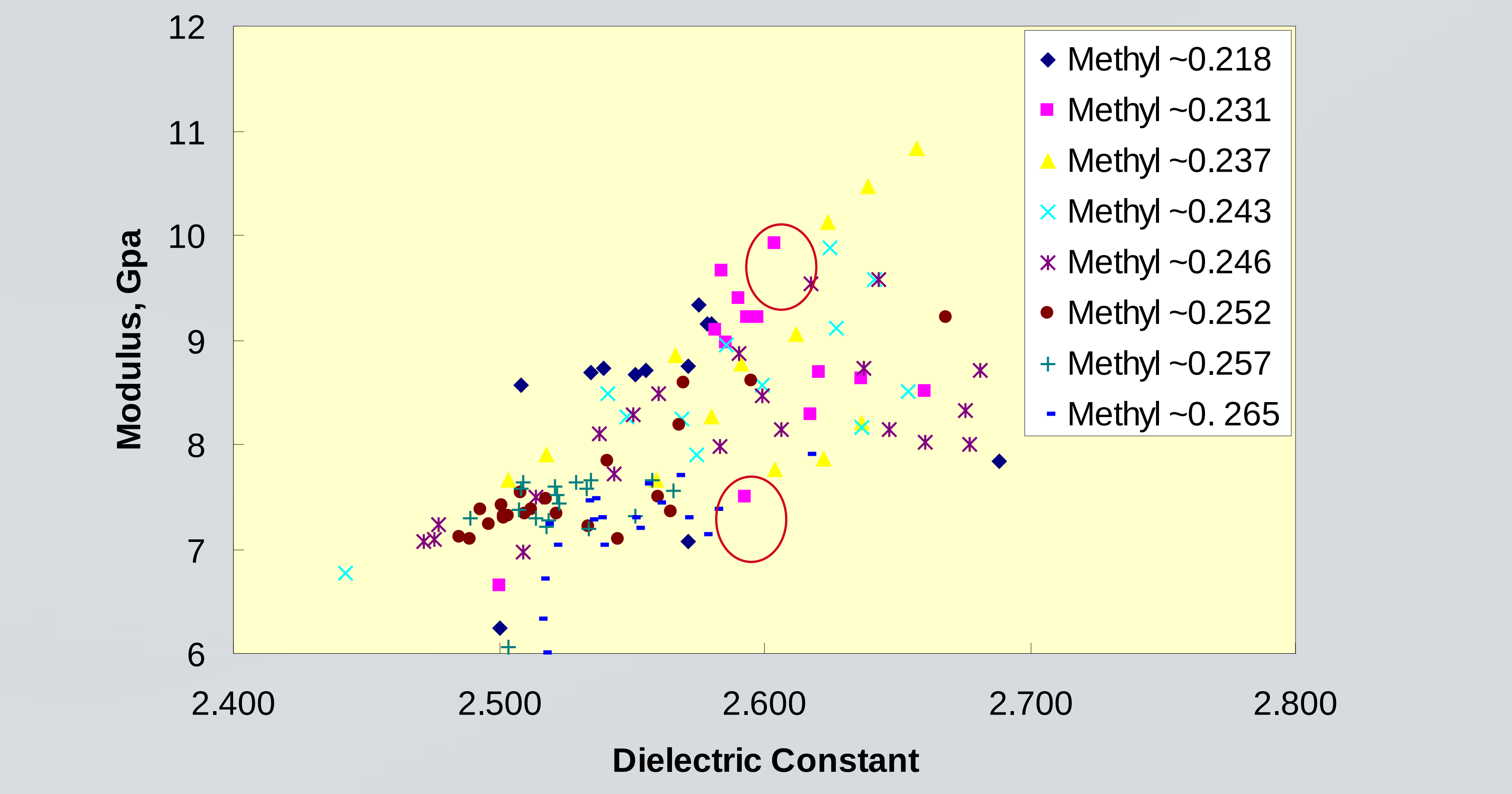
Summary

- Atomic level understanding of interfaces is essential for continued progress in high-k and low-k dielectric applications
- Patterning control and metrology exponentially more complex with ultra low-k1 and double patterning
- Separating data from noise needs a priori knowledge of design for effective filtering and information generation

APPLIED MATERIALS®

Material Complexity: Low K Film Modulus vs. K

At Constant Methyl Content (Film Composition)



Same Methyl content but various modulus due to process