Metrology’s Value in the semiconductor industry

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Metrology

*is a modern engineer’s eyes*

- Sees and measures at nanometer scale dimensions
- Without measurement it is impossible to adjust complex processes
- The result: computers and chips become capable of solving ever more complex problems
  - More cost effectively
  - While using less power
Metrology is Enabling

• Metrology:
  – Empowers engineers with the information needed to make transistors smaller
  – while systematically eliminating
    • The causes of yield losses
    • Performance sapping variability at the transistor level

• At the semiconductor and electronics levels
  – Metrology creates demand using Moore’s Law to lower the cost of chips and computers
  – The macroeconomic result is greater productivity, lower inflation, and job creation
The Power of Inspection & Metrology

300 mm wafer

10 nm

Scatter 100 coins

Find in 1 hour

Optical Inspection

Samples all ~17 trillion pixels in this area and finds the coins in about an hour

Source: KLA Tencor
Value is created through these mechanisms:

- Koomey’s Law
- Moore’s Law
- Dennard’s scaling rules
Koomey’s Law

- Computer power efficiency grows at a 54% CAGR
- Thus power-per-computation is declining at a 35% annual rate
Moore’s Law

Component density doubles every two years due to geometry shrinks for roughly the same areal cost

Gordon Moore - 1975

Source: Intel
Dennard’s scaling rules

Transistor **shrinks** result in **proportional power** and/or **performance gains**.

*Robert Dennard - 1974*
The Value of Metrology is delivered in many forms

- Return on Investment
- Increased Revenues
- Faster Time to Money
- Greater Profits
- Loss Prevention
- Business Continuity
  – Brand value
Metrology ROI

Steady increase for last 10 years
Chip Makers’ Return

• In 2002:
  – Each dollar spent on metrology generated
    • $11 in IC sales

• In 2012:
  – Each dollar spent on metrology generated
    • $22 in IC sales
Value of Yield

1%↑ = 8%↑ = $40B↑

Yield → Profit → Industry Share Holder Value
Faster Time to Money

Defect Density Learning Rates
(Typical App Processor SOCs)

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Delay in Yield Ramp Denies Profits

Preventing investment in R&D and future nodes

Cumulative Revenue
Effect of a Yield Ramp Delay

Cumulative Net Margin
Effect of a Yield Ramp Delay

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Cost of Delay

Over the life cycle of the node

- One quarter delay costs $3B
- Two quarters $6B
- And full year $11B
- Time to money has also been driving the manufacturing consolidation
Increased Revenues

Revenue Based on Defect Density Learning Rates

(Typical App Processor SOCs in annual rates, $M per Fab)

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1 Quarter Delay is Worth Half a Fab

Cumulative Revenue
Effect of a Yield Ramp Delay

Revenue ($B)

- $25
- $20
- $15
- $10
- $5
- $

Normal | 1Q Delay | 2Q Delay | 4Q Delay

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Faster Learning = Greater Profits

Cumulative Net Margin
Effect of a Yield Ramp Delay

Normal  1Q Delay  2Q Delay  4Q Delay

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Value of Yield Improvement

Shareholders are the greatest beneficiaries

• For a 1% yield improvement from a $1B metrology investment
  – The result is 4000% return for shareholders

Or opposite….

• When metrology budgets are reduced by $1B costing 1% in yield
  – Risking yield loss resulting -3000% shareholder return though profitability reduction

• Metrology becomes the best insurance available
Thank You

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ChipHistory.org
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