The R&D Crisis
By G. Dan Hutcheson
Equipment makers will spend less on RD&E than chip makers for the first time in three decades.
A flat equipment market is forcing equipment makers to cap R&D spending. ROI for equipment makers has become too low to justify the spending. This pushes R&D burden back on the chip makers.
Chip sales have been growing at around 6% a year since 1995. But R&D is growing at a 12% CAGR. By 2020, RD&E spending rate would reach 40%. Clearly, this is unaffordable.
RD&E Spending per Node

(WW in $M. Includes both Chip and Equipment Spending)

Node in nm & Year

Annual Change in RD&E Spending per Node
(CAGR per Node)

Pre-Consortia Era Average CAGR per Node = 33%

New Generation Litho Introductions

Consortia Era Average CAGR per Node = 12%

Node in nm & Year


127000 76200 50800 25400 16000 10000 8000 5000 4000 3000 2000 1500 1250 1000 800 600 350 250 180 130 90 65

0% 10% 20% 30% 40% 50% 60% 70% 80%

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• If the R&D spending rate must slow, then
  – Either the clock rate of Moore’s Law must slow.
  – Or the industry must become more efficient in R&D.
The R&D Crisis

• Slowing Moore’s Law would mean:
  – A substantial reduction in the growth of both the semiconductors and electronics market.
  – Then we will have to slow RD&E spending growth more.
    • which will extend the clocking rate further.
    • and lower the market potential to an even lower level.
  – It is a downward spiral that no one would want to initiate.
Conclusions:

• As an industry, we have a choice. We can let R&D slow and see what happens OR…
  – Find new ways to make R&D more efficient. Doing this means learning to work together better.
  – Get prepared for the introduction of new lithography generations so that costs do not spike.
  – Figure out what is broken in the equipment model and fix it.
  – Find out what it is about SEMATECH that made it so good and then make it better
Thank you

This presentation is available as a white paper at: