New Materials and Structures Based on Spin, Charge and Wavefunction Phase Control

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• Nanoscale Charge-based Transistors
• Nanoparticle Gate Flash Memory
• Spintronics
• Phasetronics

Acknowledgments: NRI-SWAN, DARPA-MARCO, NSF, SRC
III-V and Ge CMOS

- **TaN**
- **HfO₂**
- **N⁺**
- **GaAs or III-V**
- **N⁺**
- **P⁺**
- **Ge or Ge₁₋ₓCₓ**

**Si Substrate**

- **TaN**
- **HfO₂**
- **Si**
- **Ge**
- **n-type GaAs**

**Capacitance [µF-cm⁻²]**

- **Voltage [volts]**
  - -1.5 -1.0 -0.5 0.0 0.5 1.0 1.5 2.0
  - **Capacitance**
    - 0.0
    - 0.2
    - 0.4
    - 0.6
    - 0.8
    - 1.0
    - 1.2
    - 1.4
    - 1.6

- **No in situ anneal**
- **in situ annealed**

- **RTA anneal only** (5 sec. at 700°C)

**Band Gap (eV)**

- **Wavelength (Gm)**
- at the band gap energy

- **InAs**
- **GaAs**
- **InP**
- **AIP**
- **AlAs**
- **GaSb**

- **Si₀.₈₀Ge₀.₂₀**
- **Si₀.₇₅Ge₀.₂₅**
- **Si₀.₆₀Ge₀.₄₀**

- **Post-growth in situ anneal** in the MBE growth chamber (5 min. at 500°C)
Relaxed Si \quad \text{Strained} \quad \text{Si}_{1-x} \text{Ge}_x

\Delta 6 \quad \Delta E_c \quad \Delta 4

HH & LH \quad \Delta E_v

\text{Type-I (Compressive)}
Subthreshold and mobility-field characteristics for 180nm Si$_{0.8}$Ge$_{0.2}$-HfO$_2$ PHFETs and control Si PMOSFET.

Recovery of mobility degradation for high-k gate dielectrics with enhanced-mobility channels: (Onsongo,.., Banerjee)

Carbon Strain Compensation of Ge

- Carbon has a smaller lattice constant than Si, Ge
  - Strain compensation of SiGe (~8:1 Ge-C ratio)
- Need low T for metastable C incorporation: low solubility (5x10^{17} cm^{-3})
- C has different impact on strain than on bandstructure

XTEM Comparison of $\text{Ge}_{1-x}\text{C}_x$ on Si with pure Ge on Si

- Pure Ge grown at low temperature directly on Si shows large number of threading dislocations
- Not present in $\text{Ge}_{1-x}\text{C}_x$ layer
- RMS Roughness $> 3$ Å
Ge$_{1-x}$C$_x$ pMOSFET Devices

We have already demonstrated enhanced performance in high-k/metal gate pMOSFETs using Ge$_{1-x}$C$_x$ layers deposited directly on Si:

- Kelly, et al., IEDM 2005
Carbon Incorporation (Yacaman)

SIMS

- SIMS measured using standard prepared by ion implantation
- Higher C level at interface

EFTEM

- Brighter regions correspond to higher C concentration
- Higher C incorporation has been observed at interface
Nanoparticle Gate Flash Memory

Conventional Flash Memory
A defect totally discharges the floating gate

- Thick tunnel oxide
- High voltage/ power
- Low reliability/ speed

Nano-floating Gate Memory
A defect discharges only one dot

- High-k tunnel oxide
- Speed/ power/ density better
- Reliability improved
- New phenomena- self-assembly, Coulomb blockade, multi-level cells

SiGe Nanocrystals on High-K Dielectrics

AFM scans (1 micron x 1 micron) showing SiGe dots grown at ~ 500°C for 90 s with 0.75 gas ratio of GeH₄ to Si₂H₆.

Band diagram of HfO$_2$ and SiO$_2$ dielectric at low program voltage
Program & Erase Transient Characteristics

Kim DW, Kim T, Banerjee SK, ELECTRON DEV 50 (9): 1823-1829 SEP 2003
Coulomb Blockade in SiGe dot on SiO$_2$ and HfO$_2$

- Limits programming by direct tunneling at low voltages
- Multiple electron storage reduces lifetime in nanocrystals
  
  \[ dE = \frac{e^2}{C} \]
  
  For small capacitor \((C \sim 10^{-18} \text{ F})\), \(dE\) can be > thermal energy, \(kT\)

- Low \(T\): Given a Write voltage, fixed no. of electrons in nanocrystal
- For nanocrystals < 5nm, this effect is significant at room temperature
Approach: Protein Assembly- FN P/E

Chaperonin proteins to template CdSe nanocrystal assembly- 2005

Trapping of Co, CdSe, PbSe nanocrystal on protein templates: w/o and with chaperonins $\sim 10^{12}$ cm$^{-2}$

Cobalt is ferromagnetic

7nm tunnel oxide, 35nm control oxide, w/ and w/o protein-mediated CdSe nanocrystals (size: 7nm)

Problems with memory window closure after several write/erase cycles.
Endurance & Retention

**Large NC**

![Threshold Voltage vs Cycles Graph for Large NC](image1)

Pulse = +/-12V 50ms

**Small NC**

![Threshold Voltage vs Cycles Graph for Small NC](image2)

Pulse = +/-10V 100ms

**Temperature = 85°C**

10V ± 200ms
erase/program
SWAN - Novel Transistors Based on Electron Spin, Phase, Charge

**MOTIVATION:**
Finding New Logic Switch

**SPIN**
- Spin Hall Effect
- Pseudospintronics
- Dilute Magnetic Semiconductors
- Quantum Point Contacts
- Quantum Wires
- Quantum Wire Transistors
- Magnetic Nanoparticles
- Thin Film / FIB Characterization
- Nanophotonic Waveguides
- Nanomagnets

**PHASE**
- Non-Dissipative Response
- Dramatic Change in Current Voltage Relationship
- Spin-Momentum Transfer
- Exchange Interactions for Logic
- Spin Manipulation for Computation and Logic
- New Characterization Techniques for Devices
- Device-Device Interaction for Quantum Logic Gates
- Reduced Interactions for Near Ballistic Response
- Interaction Induced Switching
- Tunneling Enhanced Switching

**CHARGE**
- Task 1: Novel Devices
- Task 2: Novel Materials
- Task 3: Novel Transfer
- Task 4: Novel Interconnect
- Task 5: Novel Metrology

**GOAL:**
Fundamentally New Device Concepts, Implementations, and Tools
Tasks 1-3: ITRS 2005, Emerging Research Devices

- Spin (e-, n, photon); MQCA
- Novel charge-based
- Phase, quantum state
- Non-equilibrium devices
- Molecular state, deformation, dipole orientation

Figure 51 A Taxonomy for Nano Information Processing
Nanomagnet-Based Logic- MQCA
Wolfgang Porod and Gary Bernstein, Univ. Notre Dame

Binary wire

Inverter

Majority gate

Programmable 2-input AND or OR gate.
DILUTED MAGNETIC SEMICONDUCTORS (DMS)
Novel materials that coalesce ferromagnetism and semiconducting properties

Datta-Das Spintronic transistor – magnetoresistance controlled by gate voltage by Rashba effect

Mn - (~1-10%)
Mn has spin 5/2
and acts as acceptors:
Hole mediated FM

(Ga,Mn)As - excellent DMS except for record FM $T_c \sim -100$ °C

Jungwirth, Mašek, Sinova, MacDonald, Rev. Mod. Phys. in press
Phasetronics: Nanowire Bundle FETs- Quantum Interference Devices?

Ge nanowire with SFLS, Korgel

Metal contact

p-type nanowire cable

n-type nanowire cable

Metal contact
Green’s Function Quantum Transport for “phasetronic” Devices

Register, Gilbert, Banerjee

- Foundation of existing first-principles semiclassical and quantum transport simulation tools (SEMC)
- Addition of novel device physics, e.g., spin & spin precession, spin scattering/relaxation mechanisms
- Interplay of multiple complex physical effects in possible novel switching devices
  - momentum, energy and spin scattering
  - full band-structure
  - strain
  - quantum confinement

Self-consistent electron transport through quantum wire transistor subject to acoustic and optical intravalley and intervalley phonon scattering
Nearly Ballistic Behavior

SR Induced degradation

- 0.20 V
- 0.07 V
0.07 V
0.20 V
0.33 V
0.47 V
0.60 V

Severe Degradation
Normally-off Aharonov-Bohm Device

Normally-off Aharonov-Bohm Device + gate voltage

(Velocity dependent) relative phase precession relative to lower leg

\[ e \rightarrow \]
Spin (and spin precession about a magnetic field or due to the spin-Rashba effect)

\[ \hat{H}_{\text{Rashba}} \approx \frac{\alpha_y}{\hbar} (\hat{\sigma} \times \hat{p})_y \]

\[ \hat{H}_{\text{Zeeman}} \approx \frac{\mu_B g_s}{\hbar} (\mathbf{B} \cdot \hat{\sigma}) \]
EX OR Gates

A=0, B=0  C=0
A=0, B=1  C=1
A=1, B=0  C=1
A=1, B=1  C=0
Continuing Need for High Performance Integrated Circuits
- Tomorrow’s computing applications demand greater performance: processor speed, memory, low power, smaller size and portability
- Technology scaling required to meet demands

Nanoscale Integration Challenges
- Interaction between different physical domains: Analog, Digital, Photonic, and Spintronic Devices and interconnect
- Complex due to increasing number of devices per chip
- Need to capture complex phenomena at the nanoscale level
- Need efficient modeling to facilitate solutions for nanoscale ICs

Scaling of Copper Interconnect Intractable for Future ICs
- Increase of delay and crosstalk
- Power consumption and electromigration

Nanoscale On-Chip Communication Solutions

Nanoscale Modeling Solutions
- Nanoscale electronics will require new modeling paradigm
- Efficient Modeling Techniques (Fast and Accurate)
- Integrated Modeling Platform to efficiently characterize complex systems (analytical methods + fast computational techniques)
- Automate the design process to generate OPTIMUM and ROBUST designs
- Paradigm has already proven effective in traditional designs

Task 4: Novel Interconnects- Plasmonics
(Massoud, Halas, Nordlander, Rice University, TX)
Ballistic transport through one single conduction channel

\[ G_0 = \frac{2e^2}{h} = (12.9 \, \text{K}\Omega)^{-1} \]
What is needed in the new switch?

**CMOS ca 2020**

- Energy \( \sim 10 \text{ aJ/op}; \) power \( \sim 10^7 \text{ W/cm}^2 \)
- Speed \( \sim 0.1 \text{ ps/op} \) \((10 \text{ THz } f_T; 100 \text{ GHz circuit})\)
- Size \( \sim L_g 5 \text{ nm}; \) cell \( \sim 100 \text{ nm}, I_{DN} \sim 3 \text{ mA/\mu m} \)
- Density \( \sim 10^{10} \text{ cm}^{-2}; \) BIT \( \sim 100 \text{ GBit/ns/cm}^2 \)
- Cost \( \sim 10^{-12} \$/\text{gate} \)

**Speed** = \( CV/I \)

**Active Power** = \( CV^2f \)

**Stand-by Power** = \( \text{Sub-}V_T, \text{ gate leakage} \)

**Desirable Attributes**

- Energy efficiency
- Speed (performance, noise)
- Room T operation (non-equilibrium devices?)
- Size (device/ wafer): capacitance, fan-out
- Gain; uni-directional signal flow (I/O isolation)
- Reliability, manufacturability, cost
- CMOS compatibility (process, topology)