

Metrology for 3D IC Integration

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ABSTRACT

Performance and functionality of microelectronic devices have increased continuously by increasing transistor integration densities (“More Moore”) over more than four decades. However, today it has become questionable if this development alone will be able to overcome the predicted performance and cost issues as well as time to market for new product generations. The ITRS roadmap predicts 3D integration as a key technology to overcome this so-called “wiring crisis”. The corresponding solution will most probably be based on through silicon via (TSV) technology. Many companies and research organizations are working currently in the area of 3D integration. A large percentage of this process flows are usually feasible but are still not commercially viable. Others are already part of products based on TSV technologies and actually present in the market. There are 3 ways to use TSVs to electrically connect multiple chips in a single package: die-to-die, die-to-wafer or wafer-to-wafer. This paper covers several process and materials approaches as well as analytical techniques for process and quality control.

At the same time that research in 3D stacking technology is advancing quickly, new requirements to microscopy techniques are coming up, and the analytical techniques have to be developed further. Void inspection after copper plating, defect detection and overlay measurements after wafer bonding are challenging. Microscopy techniques for which silicon is opaque such as scanning acoustic microscopy (SAM) and confocal infrared microscope (IR) are capable of inspecting the interface between bonded wafer pairs, while high-resolution X-Ray microscopy is used to detect voids in TSVs. This paper discusses the current status of SAM, IR microscopy and X-ray tomography, complemented by Focused Ion Beam analysis, in terms of their application to process metrology and failure analysis for 3D IC integration.