Metrology Challenges for the Ultra-thin SOI

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ABSTRACT

Silicon on insulator (SOI) wafers have become today one of the standard substrate choices for high-end CMOS applications. Current quality of SOI wafers is approaching to the quality of high end bulk Si products. The manufacturing process requires monitoring of tens of parameters, both on-line during wafer processing and off-line on the finished product. Among those parameters the most important require SOI specific metrology. Recent development of technology based on planar fully depleted MOSFET architecture drives thickness of Si and buried oxide layer (BOX) of SOI wafers in sub 10nm range [1]. This new transistor design reduces significantly Vt variation due to random doping fluctuation but imposes additional tight requirements on Si thickness uniformity. It becomes the critical parameter for fully depleted MOSFETs and has to be controlled in the wide range of spatial frequencies, covering frequencies from wafer scale to tens of nanometers. Traditional spectroscopic ellipsometry has to be expanded into submicron lateral resolution domain and complemented by surface roughness techniques. Difficulties of correlation and calibration of multiple techniques will be highlighted.

Big challenge of particle measurements on SOI wafers is the inspection limitations of conventional LPD measurement tools [2]. Introduction of SP2 scanner allowed significantly decrease threshold of LPD inspection on SOI wafers together with quantitative measurement of surface roughness. Limitations and possible extensions of this technique for thin (10 – 20nm) SOI layers will be discussed.

Another specific feature of SOI wafers is reduced tolerance to metal contamination and structural defects in top Si layer as compared with standard bulk Si technology. Oxygen precipitates or agglomerations of Si vacancies with size superior to the top Si layer thickness will result in killer defects due to underetching of the BOX during wet cleaning steps used in CMOS processing. Interesting application of well known HF etching technique became possible due to very high quality of modern SOI process. HF defect densities in standard SOI wafers typically fall below 0.05 defects per cm$^2$. It allows mapping of the HF defects by LPD inspection tools. Combination of these techniques with non-preferential chemical thinning of top Si layer is a powerful method which allows quantitative measurements of density and size of oxygen precipitates in incoming Si wafers used as donor wafers for SOI production. Detection limits of < 10nm in precipitate size and < 10$^5$cm$^{-3}$ in precipitate density are demonstrated, which are superior to those of conventional techniques, such as LST. It will be shown that this technique also is very sensitive to traces of metal contamination in the 10$^8$cm$^{-2}$ levels.

Quality of BOX/Si interface is a result of BOX formation method as well as SOI manufacturing steps. Various techniques assessing quality of the interfacial layer can be used for statistical process control. One of the techniques is electrical characterization of the interface using pseudo-MOS method. Examples of sensitivity of this technique to metal contamination and interface defectivity will be shown. Overview of different variations of the technique will be presented and challenges associated with decreasing of the thickness of the layers are discussed.

REFERENCES