

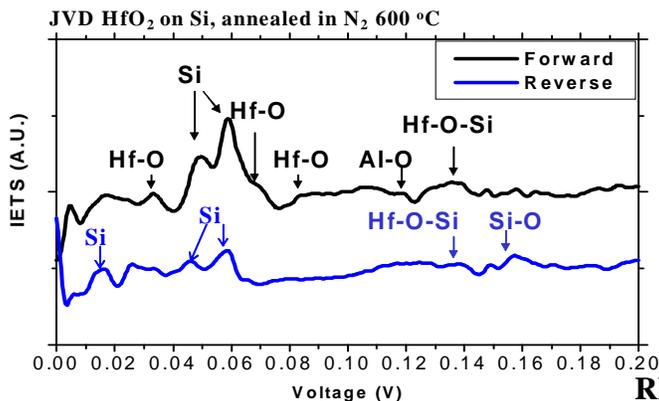
# Inelastic Electron Tunneling Spectroscopy for Measuring Microscopic Bonding Structures, Impurities, and Traps

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## ABSTRACT

As the thickness (EOT) of the gate dielectric in a CMOS transistor continues to shrink in each new generation of integrated circuits in order to meet the targeted gains in performance and circuit density, it becomes increasingly difficult for some conventional dielectric characterization tools, such as infrared spectroscopy, Raman spectroscopy, neutron scattering, and Rutherford scattering, to reveal their structural and compositional information. In contrast, the Inelastic Electron Tunneling Spectroscopy (IETS) technique, which relies on tunneling current to probe the ultra-thin gate dielectric in a metal-insulator-semiconductor (MIS) sandwich [1-5], becomes more sensitive when the tunneling current increases, which is in the direction of the CMOS scaling trend. It has been shown that a wealth of information about an MIS sample may be obtained by IETS, with excellent sensitivity and resolution [1-5]. An IETS spectrum is essentially a  $d^2I/dV^2$  vs  $V$  plot, where  $V$  is the applied voltage, which equals the Fermi level separation between the two electrodes. Thus, the voltage at which a feature appears in the IETS spectrum corresponds to the characteristic energy (in eV) of a specific inelastic interaction, such as energy loss to phonons, bonding vibrations, impurity bonds, and traps, where the intensity of the interaction is also reflected in the feature size. Figure 1 shows an example of IETS spectra, measured in both polarities, for an Al/HfO<sub>2</sub>/SiO<sub>x</sub>/Si MOS capacitor structure, where the data for the positive polarity (i.e., reverse bias) preferentially probes the interactions near the gate/dielectric interface while the data for the negative polarity (i.e., forward bias) preferentially probes those near the dielectric/Si interface. Traps have been shown to exhibit distinctly different IETS features [4,5], and have been measured and analyzed in numerous gate stacks. Trap energies and spatial locations can be extracted from IETS spectra [4,5]. Many examples will be shown in the presentation to illustrate the capabilities and limitations of the IETS technique.



**FIGURE 1.** Reverse-bias (gate negative) IETS spectrum reveals information near Si/HfO<sub>2</sub> interface, while forward-bias (gate positive) IETS reveals information near gate/HfO<sub>2</sub> interface.

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