

Metrology and Characterization Challenges for Emerging Research Materials and Devices¹

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ABSTRACT

The ITRS Emerging Research Materials (ERM) and Emerging Research Devices (ERD) Technology Workgroups have identified materials and devices that could enable continued increases in the density and performance of future integrated circuit(IC) technologies and the challenges that must be overcome; however, this will require significant advances in metrology and characterization to enable progress. New memory devices and beyond CMOS logic devices operate with new state variables (e.g. spin, redox state, etc.) and metrology and characterization techniques are needed to verify their switching mechanisms and scalability, and enable improvement of operation of these devices. Similarly, new materials and processes are needed to enable these new devices. Additionally, characterization is needed to verify that the materials and their interfaces have been fabricated with required quality and performance.

New materials and processes are also needed to extend lithography, interconnects, and assembly and packaging, and metrology is needed to verify and improve functional performance. While directed self assembly is a candidate for extending lithography, metrology is needed to characterize defect densities of these thin polymers over large areas to determine whether it will be possible to achieve ITRS defect densities of $<0.01\text{cm}^{-2}$. For extending copper interconnects, metrology is needed to evaluate the effectiveness of ultrathin diffusion barriers to 1nm in thickness. For more advanced concepts, such as carbon nanotubes or graphene for interconnects and vias, metrology is needed to evaluate the contact resistance and quality of materials deposited into vias and interconnects. For carbon nanotubes(CNTs), metrology is needed to determine their density and determine whether growth factors will limit this density. Furthermore, as graphene or CNTs are deposited on other materials, it is important to determine whether their performance has been degraded by interfacing to these materials.

In assembly and packaging, materials are needed to enable a thermal hierarchy of assembly temperatures, low stress on the integrated circuits, and spreading of heat generated between the ICs. The challenge for assembly materials is to be able to simultaneously satisfy required thermal conductivity, modulus, hardness, adhesion, electrical resistivity, moisture resistance, and other functional properties. Nanosolders offer the possibility of establishing a thermal hierarchy for assembly, but the resulting structure and reliability of these solders must be verified when they are connecting multiple ICs.

The critical challenge is to develop characterization techniques that can determine whether it is possible for the emerging materials and devices to achieve their most important performance limitations and be viable candidates for progressing to process or circuit development.

REFERENCES

1. Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2009 Edition. International SEMATECH:Austin, TX, 2009.