

Nanocharacterization Challenges in a Changing Microelectronics Landscape

Michel Brillouët

CEA/Leti

Minatec Campus – 17, rue des Martyrs 38054 Grenoble Cedex 9 - France
Phone: +33 (4) 38 78 43 02; Fax: +33 (4) 38 78 26 26
e-mail:michel.brillouet@cea.fr

ABSTRACT

As the microelectronics industry enters the “nano”-era new challenges emerge. Traditional scaling of the MOS transistor faces major obstacles in fulfilling “Moore’s law”. New features like strain and new materials (e.g. high k – metal gate stack) are introduced in order to sustain the performance increase. For a better electrostatic control devices use the 3rd dimension e.g. in gate-all-around nanowire structures. In this low dimensional regime a single atom can have a major impact in the performance and variability of the logic circuit: advanced measurement techniques are required to address this concern. Memories are probably the components where scaling is the most aggressively pursued. A slight shift in a row of atoms or the built-up of a nm-sized filament induces the bistability of the memory cell. In this paper we will show some examples of 2D and 3D characterization techniques at the nm-level which combine resolution, sensitivity and potentially throughput and in-line operation.

Due to the escalating cost and complexity of sub-28nm technologies fewer industrial players can afford the development and production of advanced CMOS processes. From a European perspective value in products can also be obtained in using more diversified non-digital technologies in the packaged devices (the so-called “More-than-Moore” domain, see Figure 1). Here also innovative measurement techniques are needed to characterize devices as diverse as image sensors, NEMS or biochips which will be eventually integrated with the logic chips through advanced packaging techniques including 3D integration and TSVs.

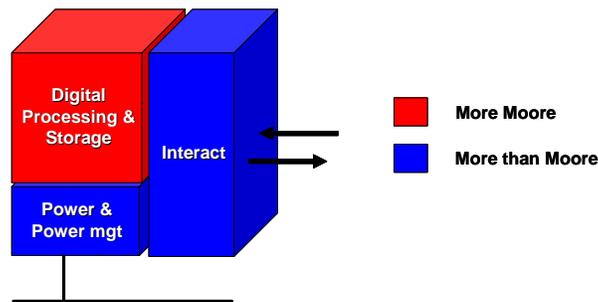


FIGURE 1. “More-than-Moore” devices complement the “More Moore” digital processing and storage elements in allowing the interaction of the packaged system with the outside world and in powering it. From [1]

Keywords: More Moore, More-than-Moore, heterogeneous integration, 3D integration, nanocharacterization

REFERENCES

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On-line at http://www.itrs.net/Links/2010ITRS/IRC-ITRS-MtM-v2_3.pdf