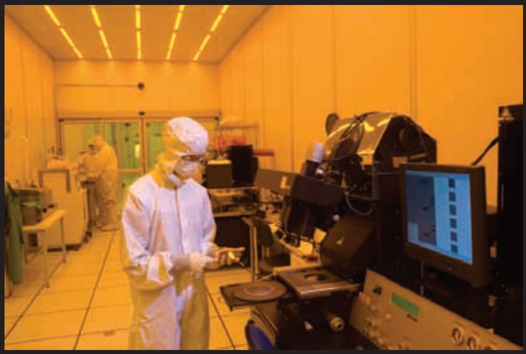
Reliability Metrologies for Advanced Electronic Interconnects

Objective

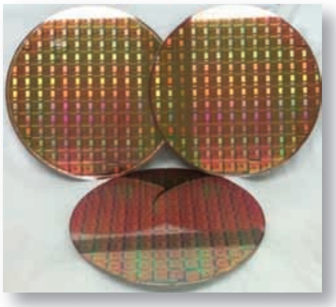
Our goal is to develop methods to measure the long term performance of state of the art (copper-based) and future (carbon-based) electronic interconnects in their as-manufactured states, under stressing by heat, electric current, and mechanical loading. The project addresses a growing challenge faced by the semiconductor industry – since reliability of interconnects is strongly dependent on properties of the surrounding materials as well as physical dimensions, fundamental reliability limits must be identified in this context.



SEMICONDUCTORS

Impact and Customers

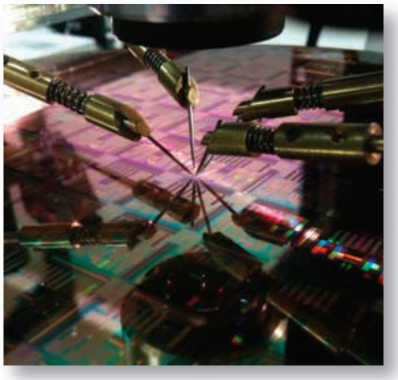
- Semiconductor products represent a global market of over $250 billion per year. As semiconductor devices become ultra miniaturized, reliability testing becomes increasingly challenging since direct access to specific materials is extremely difficult.



- Testing *in situ* is highly desirable as materials in real devices are subjected to stresses vastly different from those generated in idealized test specimens. Providing data in near-real-world conditions will enable product designers to better balance performance and reliability.
- We are working directly with industry to measure and improve electromigration and stress voiding performance of state of the art copper-dielectric systems for the near term. We are also developing new metrologies to evaluate thermal and electrical performance of carbon nanotube interconnects, to assess their viability as a potential long-term replacement for copper technology.

Approach

Basic thin film mechanical properties are often measured by microtensile or nanoindentation testing. For situations where such tests are inapplicable, for example, because a structure is too small or inaccessible, we have developed an approach to determine the properties of these materials without the need for special specimens. Our electrical methods can evaluate extremely narrow lines, including those buried beneath other materials. The test applies controlled joule heating via a 4-point probe system. Conditions are controlled so electromigration does not necessarily take place; rather, heat is generated and dissipated in each power cycle. Cyclic thermal strain is induced, allowing for determination of properties such as fatigue lifetime and strength. We can correlate these data with electrical properties and electromigration performance – key qualifiers for the semiconductor industry. The approach was validated in recent years on aluminum, gold, and damascene copper lines and vias. We are now using it to develop a new accelerated test for stress voiding, a method for tailoring electromigration-resistant microstructures, and new methods for determining reliability foundations in carbon nanotube interconnects.

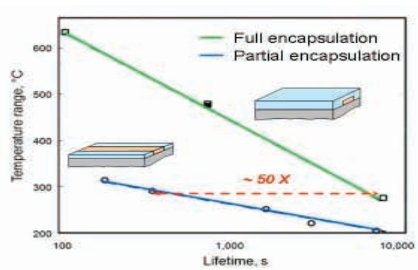


Accomplishments

We have made recent advances in three key areas of interconnect reliability: (i) application of electrical test methods to lifetime measurements of buried structures, (ii) discernment of competing damage mechanisms during thermal stressing of damascene copper, and (iii) preliminary measurements of the electrical response of carbon nanotubes (CNTs).

Testing of Buried Structures

State of the art metal interconnects in functional solid state devices are typically encapsulated in rigid dielectrics such as silicon dioxide. Maintaining structural integrity during thermal cycling of these materials is an important aspect of product qualification. We performed a series of cyclic thermal tests on damascene copper encapsulated in silicon dioxide, using low frequency (~ 100 Hz), high current density (~ 10 MA/cm2) AC. We found that the cyclic thermal lifetimes of fully encapsulated lines exceeded by more than a factor of ten the lifetimes of lines with their top surfaces left uncovered, as shown in the figure.

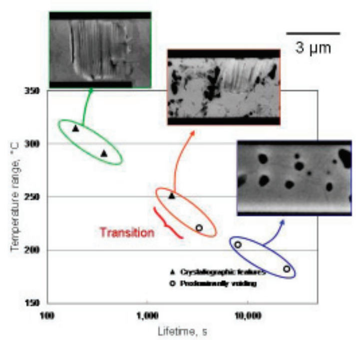


Effect of Encapsulation on Cyclic Thermal Lifetime of Damascene Copper

The difference in temperature-lifetime behavior was replicated in finite element simulations, which showed that a given applied temperature range produces less strain in fully encapsulated copper. These measurements convincingly demonstrated the applicability of our electrical testing approach to state of the art buried interconnects.

Damage Mechanisms in Damascene Copper

Real structures that make up microelectronic devices can see a variety of different damage modes, any of which has the potential to lead to catastrophic failure. As examples, crystallographic defects (dislocations) can damage material interfaces as well as cause cracking or changes to internal geometries; void formation can locally reduce conductor cross sections, leading to localized hot spots or open circuits. By varying applied cyclic temperature ranges, we induced both types of damage in partially encapsulated damascene copper, as shown in the figure.

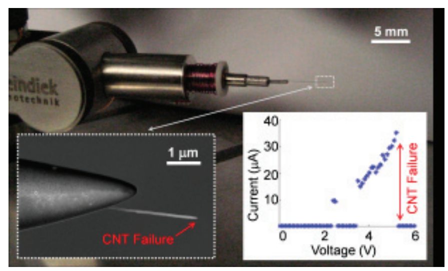


Damage Modes Induced by AC Electrical Stressing of Damascene Copper

The different forms of damage seen above correspond to traversing different regions of the deformation mechanism map of applied stress versus temperature for fine-grained copper. This result is especially exciting in that it may open door to the development of new accelerated tests for void formation.

Electrical Response of CNTs

The long term future of electronic interconnects likely lies in non-metallic conductors such as CNTs or graphene. These materials can provide extraordinary physical properties, including, potentially, near-ballistic electron transport. While the research community is actively working to explore new design concepts with these materials, the foundations for the reliability physics remain untouched. We are developing new metrologies to establish these foundations, based on what we have learned from our work on metallic interconnects. Critical to the attainment of reliable, high performing carbon-based interconnects is treatment of the material system, including substrate and surrounding dielectric materials, and the ability to handle extremely fine scale structures. The figure shows a failed CNT conductor attached to the probe of a nanomanipulator. Prior to testing, the other end of this multiwalled CNT was attached to a Pt/Ir wire and carried a ramping current up to 35 μA before it failed at its midpoint; this corresponds to a current density in the range of several mega-amps per square centimeter, depending on the tube wall thickness. This setup forms the basis for additional thermal and electrical reliability studies on more complex CNT systems, to be conducted in an electron microscope.



Carbon Nanotube Conductor Failed by Ramping Current and Corresponding Electrical Response

Learn More

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Publications

Read DT, Geiss RH, Barbosa III N, *Constraint Effect in Deformation of Copper Interconnect Lines Subjected to Cyclic Joule Heating*, Journal of Strain Analysis for Engineering Design 44: 543 (2009)

Read DT, Geiss RH, *Micrometer-width Damascene Copper Conductors at > 10 MA/cm²*, Proceedings of the 5th IEEE Vehicle Power and Propulsion Conference, Dearborn (2009)

Read DT, Geiss RH, *Thermal Cycling of 300 nm Buried Damascene Copper Interconnect Lines by Joule Heating*, Proceedings of the 2008 NSTI Nanotechnology Conference, Boston (2008)

Keller RR, Barbosa III N, Geiss RH, Read DT, *An Electrical Method for Measuring Fatigue and Tensile Properties of Thin Films on Substrates*, Key Engineering Materials 345-346: 1115 (2007)