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Scanning Probe Microscopes for Subsurface Imaging

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Scanning probe microscopes (SPMs) have some ability to image sub-surface structures. This paper describes the theoretical and practical basis for imaging metal lines buried beneath insulating layers and for imaging insulating regions or voids within metal with SPMs. Three techniques are discussed: scanning Kelvin force microscopy (SKFM) to image the potential of buried metal lines, scanning microwave microscopy (SMM) to image the capacitance of buried metal lines, and SMM to image voids in metals through the frequency dependence of the skin depth. A test chip, designed at NIST, and that contains buried structures to precisely produce electric potential and magnetic field variations at the surface to test the presumptions is described, along with some preliminary results.

Introduction

Scanning probe microscopes (SPMs) have remarkable sensitivity to the surface. The scanning tunneling microscope, for example, can achieve atomic resolution of the local density of states (LDOS) of the surface. STM accomplishes this superlative result because the tunneling current depends exponentially on the tip-to-sample distance so that the image is dominated by the tunneling between the last atom of the tip and the first atomic layer of the surface. The atomic force microscope (AFM) images surface topography utilizing the van der Waals force, which has an inverse seventh-power tip-to-sample distance dependence, again resulting in high spatial resolution images.

However, SPMs that measure surface potential (scanning Kelvin force microscopy, SKFM), magnetic field (magnetic force microscopy, MFM), or capacitance (scanning capacitance microscopy, SCM) form their images from the electromagnetic field that varies with the inverse square of the tip-to-sample distance. In practice, this means that the signal imaged by these electrical SPMs have components due not only to the interaction of the tip apex and the sample, but also the tip sidewall, the cantilever, and any part of the high side of the microscope that is not shielded from the surface. In simple implementations, these electrical SPMs could have very poor spatial resolution and measure a signal that is not dominated by the region directly under the tip. (Sophisticated data acquisition techniques can improve spatial resolution considerably.) The ability of electrical SPMs to gather information from a large volume, while a weakness in absolute spatial resolution, opens up the possibility of extending the range of SPMs into the subsurface of materials and to produce three-dimensional images of the structure beneath the sample surface.

While basic subsurface imaging has been easy to demonstrate, it has not been optimized. Sophisticated electronic measurement instrumentation, developed to measure very small electrical signals for communications, is rapidly increasing in sensitivity and precision. Especially promising are the cases where an external bias can be applied to the subsurface structure at a known ac-frequency, allowing lock-in and difference frequency techniques to be employed.

We have been developing the subsurface imaging capabilities of various SPMs for a few significant applications to integrated circuit and nano-electronics metrology. The so called back end of the line (BEOL) integrated circuit processes cover the parts of the integrated circuit from the transistor contact upwards, including all the levels of interconnect metallization, separating dielectric layers, and the various contact pads and bump structures. For BEOL, subsurface imaging may be useful for the verification of buried metal line dimensions, determination of the frequency spectrum of interaction between lines, and for the identification of shorts and opens for failure analysis. Another important emerging technology where SPM based subsurface metrology may make a contribution are three-dimensional integrated circuits (3D-ICs). 3D-ICs stack multiple thinned chips of various functionalities to produce a circuit with increased overall integration density. An important technology for 3D-ICs is through silicon vias (TSVs) which provide the electrical interconnections between stacked chips. Here we seek an easy method to identify voids or other subsurface defects within the metal TSV. Another potential application will be imaging of filament formation in resistive random access memory.

This paper will discuss the practicalities of using scanning Kelvin force microscopy (SKFM) to image the potential of buried metal lines, scanning microwave microscopy (SMM) to image the capacitance of buried metal lines, and SMM to image voids in metals through the frequency dependence of the skin depth. A test chip, designed at NIST, and that contains buried structures to precisely produce electric potential and magnetic field variations at the surface to test the presumptions is described, along with detailed COMSOL simulations of the structures and some preliminary imaging results.

NIST Potential and Magnetic Field Test Chip

Test Structure Layouts

A key tool in developing and improving the subsurface imaging capabilities of SPMs is a target test chip that contains buried structures that can produce precisely calculatable electric field and magnetic field distributions at the surface. Towards this end we have produced two test chips. One containing isolated metal lines and squares of Cr, Al, or Au (1) and a second containing metal interconnect lines buried within an insulator at four discrete depths. The test structure with the isolated metal lines and squares with different work functions, while relatively large, is helping us determine the ability of SKFM to detect the subsurface structure of nano-composites of conducting particles within an insulating matrix. The second test chip, discussed in depth here consists of buried metal lines which can be biased to produce various patterns of electric or magnetic field that be imaged at the surface with the appropriate SPM. The test chip has been designed so that the bonding pads are to one side, leaving clearance for the active regions to be probed with a cantilevered SPM probe. By having a known potential distribution we can evaluate

the performance of different image modes. Characterization of the magnetic field test structures will be discussed in future publications. The test chip was fabricated by MOSIS using a 0.35 µm CMOS process from TSMC which includes four levels of metallization[1]. Insulator and metal thicknesses were determined from imaging a polished cross-section in a scanning electron microscope.

The test chip contains eight variations of test patterns, some of which can be operated in both a potential and magnetic field mode. All structures contain variations of line width and combinations of metal 1 through metal 4. Test structures are connected between two 40-µm wide metal bus lines, separated by 80-µm, employing all four level of metal to produce a low resistance bus with very low loss along the bus. This ensures that structures along the bus all see essentially the same potential drop. Several representative test structures are shown in Figure 1 below.

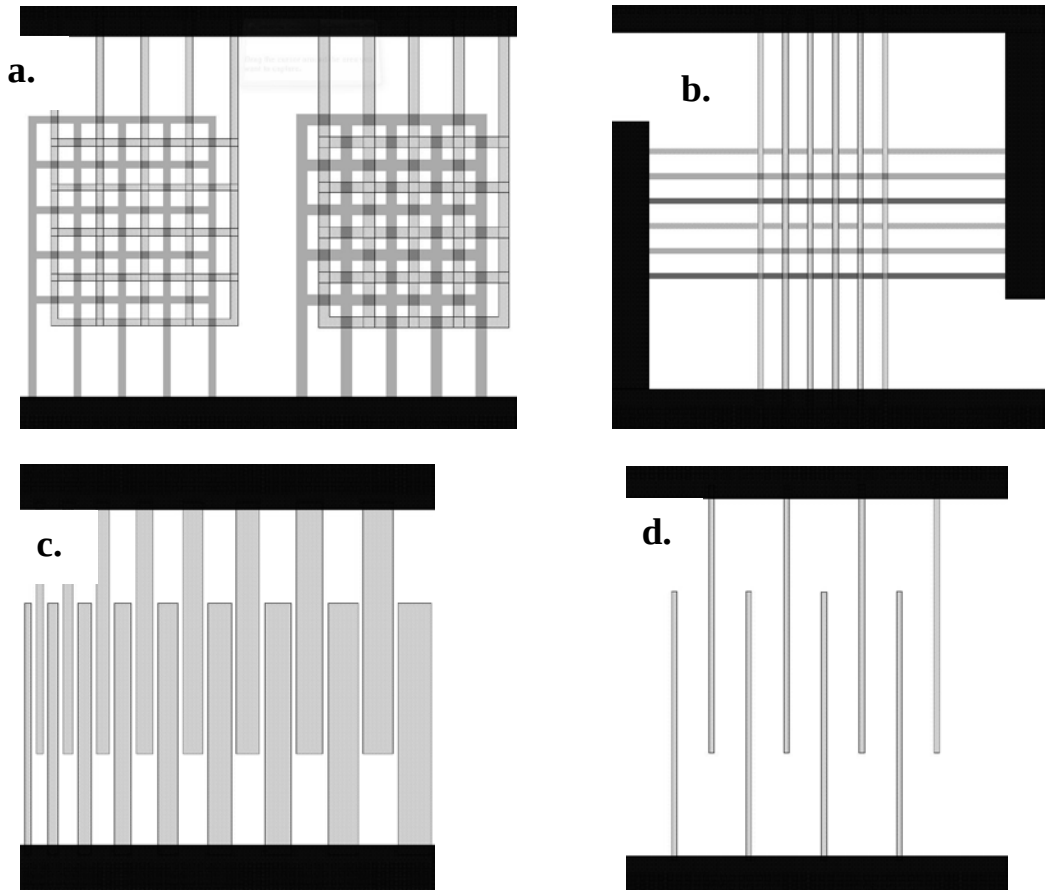

Figure 1: Representative potential and magnetic field test structures. a) Waffle pattern, provides parallel and perpendicular lines at two or more different depths; each waffle can be biased at a different potential; b) Perpendicular lines at various combinations of depth; pattern can be held at a contact potential or a constant current; c) and d) Interdigitated fingers: Alternating lines can be at different potentials, increasing image contrast.

[1]Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the materials or equipment used are necessarily the best available for the purpose.

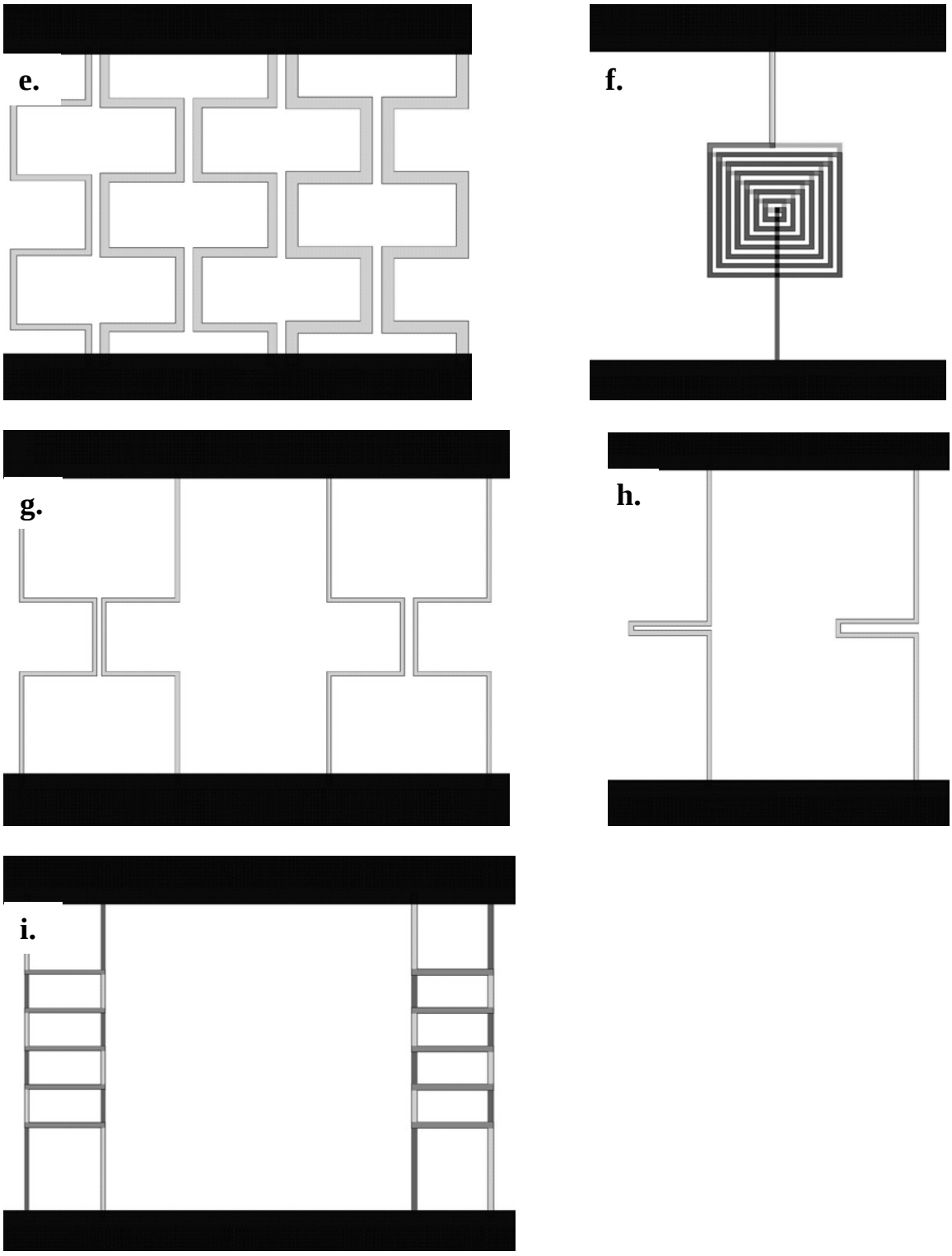

Figure 1: e) Brick style zig zag; provides parallel and perpendicular current carrying lines; f) Micro-coils: intended to generate strong surface magnetic fields, but may also function as magnetic field sensors; g and h) perpendicular and parallel lines: can be used to generate complex magnetic field patterns; i) Dual lines at multiple depths. Spacing between the upper and lower bus lines is 80μm for all structures.

COMSOL Simulations

The electric field and surface potential distributions generated by various test structures from this chip have been simulated with a simple analytical model and with the COMSOL Multiphysics software. Basic simulation geometry consists of three metal lines, 1.2-μm in width, separated by 1.2 μm. The lines are also separated and buried beneath an insulating layer (dielectric constant of 3.9) of varying thickness. COMSOL was utilized to simulate the potential at the surface of the insulator. This potential should be measurable with the scanning Kelvin force microscope. While quite sharp transitions in the surface potential are observed with an infinitely small test electrode, insertion of a probe with the shape of a real SKFM probe into the simulation substantially dampens the spatial resolution. The simulated conical tip has a 20 nm flat and a 15 degree cone angle. This result emphasizes the need for high aspect probes and advanced Kelvin force imaging to adequately resolve buried conductors within an insulating matrix (2-3). In Fig. 2a below, the surface potential of these three metal lines on a plannarized dielectric surface is shown. The potential quickly reaches the applied value over the lines and the full 2 volts between lines is seen. In Fig. 2b, the lines are beneath an insulator of 3.2 μm thickness; the potential is smeared out relative to the no insulator case and the maximum difference in potential is 200 mV. Fig. 2c and 2d, show the potential measured with a tip as the second electrode for lines at the surface and for lines buried beneath 3.2 μm of oxide, respectively. Here the measured potential differences are 75 mV for Fig. 2c and 2.5 mV for Fig. 2d.

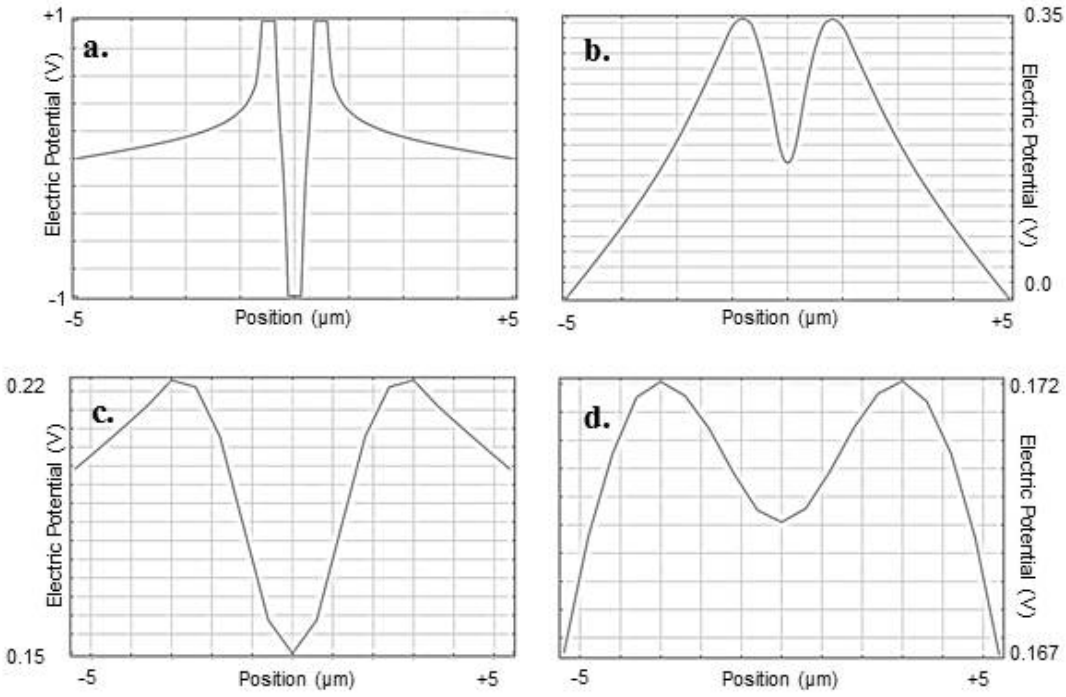

Figure 2: COMSOL simulation of the potential at the surface due to three metal lines, 1.2-μm in width, separated by 1.2 μm, and covered by an insulating layer thick. The outer two lines are biased at +1 V and the inner line is biased at -1 V. a) Surface potential of metal lines with no insulating layer; b) Surface potential with lines at a depth of 3.2 μm beneath an insulator; c) Tip potential, lines with no insulator layer; d) Tip potential, lines at a depth of 3.2 μm beneath an insulator.

The other test structure used in this work consists of isolated metal lines and squares with different work functions. While relatively large, these structures are helping us determine the ability of SKFM to detect the subsurface structure of nano-composites of conducting particle within an insulating matrix.

Methods to Image Buried Conductors within Insulators

Scanning Kelvin Force Microscopy

SKFM is an AFM based technique which uses an applied AC potential to induce oscillations of the cantilevered tip through capacitive forces. A feedback loop is employed to null the oscillations and thereby provide a measure of tip-to-sample contact potential difference. If the work function of the tip is known, the work function or surface potential of the surface under examination can be deduced via Eqn. 1. Various SKFM data acquisition modes exist, including double pass amplitude modulation (AM), single pass AM, and frequency modulation. For a complete overview of SKFM techniques and data acquisition limitations see (4).

$$V_{CPD} = \varphi_{surface} - \varphi_{tip} \quad [1]$$

SKFM should be able to produce subsurface images of biased buried metal lines from the potential at the surface of the insulator. COMSOL simulations show that lines buried beneath as much of 5 μm of silicon dioxide should still produce a surface potential of 5 mV when biased at 1 V, about the detection limit of amplitude-modulated SKFM. SKFM is commonly operated with a tip lift height of a few nm above the surface. Introduction of the insulating layer effectively increases this lift height with a corresponding loss of spatial resolution. One possible way to recover the spatial resolution would be to use highly shielded co-axial tips or tips with very high aspect ratios. Application of an opposite sign back bias could also improve resolution for samples with applicable geometries. Various data acquisition improvements to spatial resolution may also be possible, for example the addition of an AC electrical bias to the line under examination at the cantilever's second harmonic frequency may allow enhanced spatial resolution imaging at the difference frequency.

Scanning Microwave Microscopy

A new implementation of scanning microwave microscopy (SMM) has recently been introduced by Agilent. SMM measures the magnitude and phase of the S_{11} reflected high frequency signal (incident signal minus signal transmitted through the tip into the sample) through use of a vector network analyzer (VNA). Shielding and coupling of the tip to the sample is essential to functional SMM. The input to the VNA is a transmission line terminated by the tip-to-sample impedance. The terminal impedance will be some combination of frequency dependent resistances and capacitances. With additional electronics the SMM can also measure the dC/dV signal between the tip and sample, allowing it to function in SCM mode for semiconductor dopant profiling. Additional details of the mechanism of SMM are available elsewhere (5). Through the capacitive coupling of the tip to conductive structures in an insulating matrix it should be possible to

measure the dimensions and integrity of metallization within low-k dielectrics for back end of the line (BEOL) metrology.

A simple model of the SMM, considers the cable connecting the tip and VNA as a transmission line with the tip and the underlying structure of the sample as the terminal impedance. A transmission line terminated by its characteristic impedance (50 Ω) will transmit the entire incoming signal (no reflection); while an open will reflect all the signal in-phase, and a short will reflect all the signal 180^{o} out of phase. Simply, an insulating substrate would be seen as a high terminal resistance, while a metallic substrate would be seen as a low resistance. Buried metallic structures, whether grounded or floating will contribute a capacitive component. Our buried test structures will produce a complex set of reflection parameters as a function of frequency, but we expect our buried metallic structures to increase the capacitance of the transmission line termination and thus be detectable in the phase of the signal reflected back to the VNA (relative to regions with no buried metal). In contrast to SKFM, no bias will be necessary to see buried metal lines with SMM. A simple test of this supposition is shown as Figure 3, where we plot the phase of the reflected signal as the tip is scanned across buried lines at a depth of a) ~1 μm and b) ~2 μm. The SMM image was acquired at 7.3 GHz, a frequency where a peak was observed in the reflected signal. This is the first demonstration of subsurface imaging with SMM; we expect to improve our signal to noise and spatial resolution as we optimize the imaging and data acquisition conditions. Additional results and discussion are available in (6).

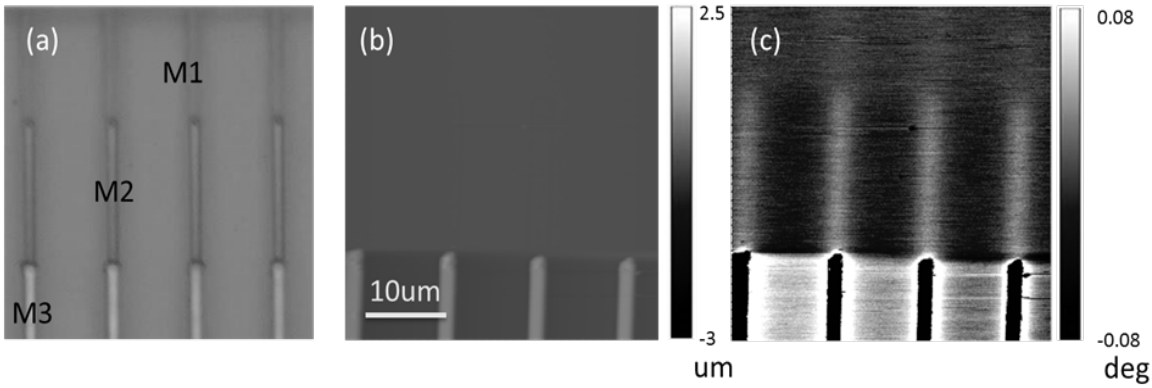

Figure 3 a) Optical microscopy image; metal M3 is on the surface, while M2 is buried beneath ~ 1 μm of low-k dielectric and M1 is buried beneath ~ 2 μm of low-k dielectric; b) AFM topography image shows that M2 and M1 are totally buried within oxide and that there is no topography change above them. (c) VNA phase images shows contrast from both the buried lines.

SMM to Image Buried Insulators or Voids within Conductors

A second distinct subsurface imaging mechanism for SMM utilizes the skin depth as a function of frequency. Here images are acquired at different frequencies, with the primary component of the signal arising from a depth within the sample determined by the skin depth at that frequency. This technique has been demonstrated for defect detection in simple metal-metal structures in (7). The skin effect is the affinity of an alternating electric current (AC) to flow mainly at the surface of wires with decreasing density closer to the center of the conductor. The electric current flows mainly at the "skin" of the conductor, between the surface and a level called the skin depth. A simple

equation characterizes the skin depth as a function of the resistivity of the conductor, ρ, the angular frequency of the current, ω = 2π × frequency, and the absolute magnetic permeability of the conductor, μ:

$$\delta = [(2\rho)/(\omega\mu)]^{1/2} \quad [2]$$

The skin depth for copper as a function of frequency is shown as Figure 3 below. At 60 Hz, the skin depth of copper is about 8.5 mm, at 1 MHz about 65 μm, and at 40 GHz about 1 μm. The very near surface of a sample will be accessible with the highest frequencies available with the VNA and SMM. The maximum depth that could be probed will be limited by the lowest frequency where a good S_{11} can be measured, probably on the order of 50 μm.

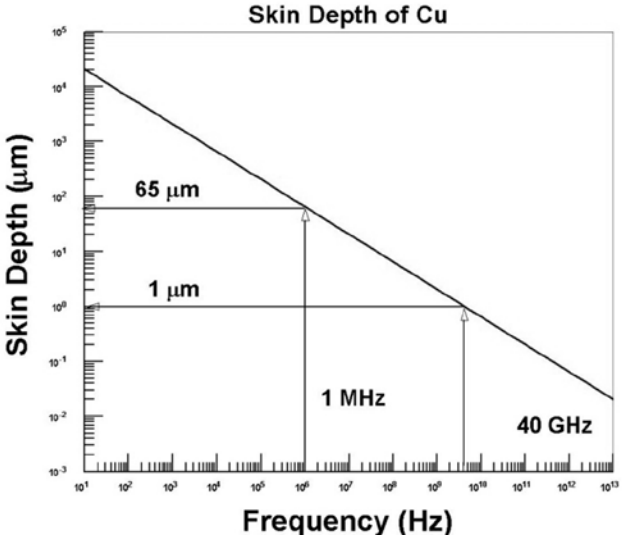

Figure 4: Calculated skin depth for a copper conductor. The limits accessible with SMM are shown at the 1 MHz and 40 GHz points.

This imaging technique may be useful to characterize defects and voids within (metallic) through silicon vias (TSVs). We are in the process of producing test structures consisting of buried insulators sandwiched between two metallic layers to further investigate skin depth profiling with SMM. Some preliminary results are shown in (6).

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