Fabrication and characterization of nanostructured III-V thermoelectric materials

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ABSTRACT

Approximately two thirds of all fossil fuel used is lost as heat. Thermoelectric materials, which convert heat into electrical energy, may provide a solution to partially recover some of this lost energy. To date, most commercial thermoelectric materials are too inefficient to be a viable option for most waste heat applications. This research proposes to investigate the fabrication and characterization of nanostructured III-V semiconductor thermoelectric materials with the goal of increasing the performance of existing technology.

In order to improve thermoelectric material efficiency, either the lattice thermal conductivity must be lowered or the thermoelectric power factor must be increased. This research will focus on the latter by modifying the density of states of the semiconductor material and studying the effect of quantum confinement on the material's thermoelectric properties. Using focused ion beam milling, nanostructured cantilevers are fabricated from single crystal wafers. An allaround gate dielectric and electrode are deposited to create a depletion region along the outer core of the cantilever, thus creating an inner conductive core. The Seebeck coefficient can then be measured as a function of confinement by varying the gate voltage. This technique can be applied to various material systems to investigate the effects of confinement on their thermoelectric properties.

Keywords: Thermoelectrics, nanofabrication, focused ion beam, nanostructures, semiconductor

1. INTRODUCTION

The average global efficiency of all fossil-fueled power generation for the past few decades has increased modestly and is now roughly 40 percent.¹ Thus, about two-thirds of all fuel used is lost as heat. Thermoelectric materials, which convert heat into electrical energy, provide an alternative energy solution to recover some of this lost energy and reduce our dependence on fossil fuels as well as reduce greenhouse gas emissions. Thermoelectric applications range from waste heat recovery in automobiles and factories to space applications such as satellites and space probes.

To date, most commercial thermoelectric materials are too inefficient to be a viable option for most waste heat recovery applications. The potential for these applications is determined partly by the material's figure of merit, *ZT*:

$$ZT = \frac{S^2 \sigma T}{\kappa} \tag{1}$$

where *S* is the Seebeck coefficient (or thermoelectric power), σ is the electrical conductivity, and κ is the total thermal conductivity ($\kappa = \kappa_e + \kappa_L$, the electrical and lattice contributions, respectively). The Seebeck coefficient is defined as the ratio of the change in induced thermoelectric voltage to the temperature difference across the material: $S = -(\Delta V/\Delta T)$. The total efficiency, η , of a thermoelectric material is a function of both *ZT* and the Carnot efficiency (thermodynamic maximum efficiency):

$$\eta = \eta_C \frac{\sqrt{1 + ZT} - 1}{\sqrt{1 + ZT} + \frac{T_C}{T_H}}$$
(2)

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where the Carnot efficiency is $\eta_c = (T_H - T_C)/T_H$, dependent upon the cold and hot side temperatures, T_C and T_H , respectively. It can be seen that in order to achieve a high Carnot efficiency, a large temperature difference across the thermoelectric material is needed. However, most thermoelectric materials only have a small temperature range in which their *ZT* is also large. Possible solutions include segmented or graded material compositions in order to efficiently cover the large temperature range required to obtain a high Carnot efficiency. For decades, most thermoelectric material systems displayed a *ZT* value of 1 or less. At a minimum $ZT\approx 2$ to 3, the conversion efficiency at the materials level approaches 15 % for waste heat recovery applications, a level at which the technology may be economically viable. Recently, advances in nanomaterials have led to *ZT* values around 1.5, with an experimentally achieved *ZT* of 2.2 by taking a panoscopic approach to the scattering of heat carrying phonons across integrated length scales.²

2. METHODOLOGY

2.1 Theory

There are two pathways to increase the figure of merit, ZT: (1) decrease the thermal conductivity by reducing the lattice contribution, or (2) increase the power factor, $S^2 \sigma$. The lattice thermal conductivity is given by:

$$\kappa_L \approx \frac{1}{3} \left(v_s C L_{ph} \right) \tag{3}$$

where v_s is the velocity of sound in the material, *C* is the heat capacity, and L_{ph} is the phonon mean free path. For high temperatures ($T > \sim 300$ K), the heat capacity and sound velocity are basically temperature independent. Thus, there is a minimum thermal conductivity that is set by the mean free phonon path. Typical thermal conductivity values for good thermoelectric materials are less than 2 W/(m·K), with the best materials less than 1 W/(m·K). Analysis shows the minimum achievable thermal conductivity is about 0.25-0.5 W/(m·K).^{3,4} Due to the electronic contribution to thermal conductivity, it is likely that reductions in lattice thermal conductivity alone will yield only modest improvement in *ZT*.

This research proposes to investigate power factor enhancement of thermoelectric materials by modifying the density of states of the semiconductor material and studying the effect of quantum confinement on the material's thermoelectric properties. The goal is to not only address existing unknowns in thermoelectric research, but also to develop materials suitable for practical applications that could result in significant fuel savings and a reduction in carbon emissions.

Theoretical studies by Dresselhaus and co-workers predicted that confined structures, such as quantum wells and nanowires, would lead to enhanced thermoelectric properties due to changes in the electronic band structure.^{5,6} For example, Dresselhaus predicted that a Bi₂Te₃ nanowire of square cross section and width 0.5 nm could reach a maximum ZT of 14 compared to its bulk value of $ZT \le 1$. Initial experimental studies have also shown that nanowires have an enhanced Seebeck coefficient,^{7,8} yet none show the predicted large improvement in ZT.^{9,10} The Seebeck coefficient is given by the Mott relation for systems with density of states (DOS), g(E):

$$S = \frac{\pi^2}{3} \frac{k_B}{q} k_B T \left\{ \frac{d \left[\ln \sigma(E) \right]}{dE} \right\}_{E=E_F}$$

$$S = \frac{\pi^2}{3} \frac{k_B}{q} k_B T \left\{ \frac{1}{n} \frac{dn(E)}{dE} + \frac{1}{\mu} \frac{d\mu(E)}{dE} \right\}_{E=E_F}$$
(4)

where the energy-dependent conductivity $\sigma(E) = n(E)q\mu(E)$ is taken at the Fermi energy, E_F , with mobility, μ , and carrier density n(E)=g(E)f(E), where f(E) is the Fermi function. As the quantum confinement increases from bulk to 1D, sharp increases of the DOS occur due to electronic confinement. Therefore, by creating a localized increase of the DOS near the Fermi level, the Seebeck coefficient can be increased.

2.2 Proposed Research

One of the key questions this research sets out to answer is what type of ZT and Seebeck coefficient enhancement, if any, can be observed experimentally for nanowires of various confinement conditions. This research will follow a top down approach to create test structures for this experiment that will provide clear, definitive results. Precise experimental techniques such as focused ion beam (FIB) milling and atomic layer deposition (ALD) will be utilized to fabricate these unique test structures.

	InSb	InAs	InP	GaAs	GaP	
E _g (eV)	0.17	0.35	1.34	1.42	2.26	
T _{melt} (°C)	527	942	1060	1240	1457	
μ_e (cm ² /Vs)	≤77,000	≤40,000	≤5,400	≤8,500	≤250	
μ_h (cm ² /Vs)	≤850	≤500	≤200	≤400	≤150	
3	16.8	15.2	12.5	12.9	11.1	
m _e * (m _o)	0.014	0.023	0.089	0.063	0.82	
m _h * (m _o)	0.43	0.41	0.60	0.51	0.60	

Table 1. Material properties of III-V semiconductors.¹¹

The proposed experiment will focus initially on III-V semiconductors, though the fabrication process is not limited to this specific material set. Some of their material properties are given in Table 1. The basis of the experiment is to mill a 1D cantilever (CL) nanostructure from a III-V wafer, coat the nanostructure with a dielectric and then a gate electrode that completely surrounds the nanostructure, and finally observe the induced voltage between the two ends of the nanostructure as a constant temperature gradient is applied across the material. As the gate voltage increases, the nanostructure becomes more and more depleted and the carriers become more confined to the central core. Thus, the thermoelectric properties of the material can be observed as a function of quantum confinement via the depletion of the nanostructure by the gate voltage. Previous experimental studies¹² were unable to decouple surface effects and carrier concentration from their results when attempting to observe this field-effect modulation of the Seebeck coefficient. While theoretical studies of a radial electric field effect on thermoelectric transport properties of nanowires have been conducted,¹³ experimental measurements of a completely radial gate electrode have not been performed to date. Using the proposed fabrication process, nanostructures of various materials, doping levels, and crystal orientations can be studied and the effect of quantum confinement on their thermoelectric properties can be clearly deduced. The results will provide insight into how quantum confinement affects thermoelectric material performance, which is extremely useful for the nanoengineering of materials for waste heat recovery applications.

Another question this research raises is how the transition from bulk material to 1D material affects the depletion region that is created by the gate electrode. Quantum confinement causes a change in the material's band structure, which in turn affects the density of states, g(E), and thus the effective density of states of the conduction and valence band, N_c and N_v , respectively, of the semiconductor:

$$g_{3D}(E) = \frac{1}{2\pi^2} \left(\frac{2m^*}{\hbar}\right)^{\frac{3}{2}} \sqrt{E - E_C} \qquad g_{1D}(E) = \left(\frac{m^*}{\pi\hbar^2}\right) \sqrt{\frac{m^*}{2(E - E_C)}} \\ N_{C,3D} = 2 \left(\frac{2\pi m_e^* kT}{\hbar^2}\right)^{\frac{3}{2}} \qquad N_{C,1D} = \sqrt{\frac{2\pi m_e^* kT}{\hbar^2}}$$
(5)

When a voltage, V_G , is applied to a metal-oxide-semiconductor structure (for example, a p-type semiconductor), a depletion region of width, $X_d(V_G)$, of charges is created near the surface:

$$X_{D}(V_{G}) = t_{ox} \frac{\varepsilon_{s}}{\varepsilon_{ox}} \left[\sqrt{1 + \frac{2\left(\frac{\varepsilon_{ox}}{t_{ox}}\right)^{2} \left(V_{G} - V_{FB}\right)}{q\varepsilon_{s}N_{A}}} - 1} \right]$$

$$where \quad V_{FB} = -\frac{kT}{q} \ln\left(\frac{N_{A}}{n_{i}}\right) \qquad n_{i} = \sqrt{N_{C}N_{V}} e^{-\frac{E_{s}}{2kT}}$$
(6)

Thus the depletion region width is dependent upon the dielectric oxide thickness and dielectric, t_{ox} and ε_{ox} respectively, the gate voltage V_G , the substrate doping N_A , the bandgap E_g , the semiconductor dielectric constant ε_s , and the effective density of states of the valence and conduction band that change with increase confinement. Assuming a 50 nm Al₂O₃ oxide layer, the values for the maximum depletion width for a 1D and 3D system are calculated and shown in Table 2. In this table, values listed for E_g are from literature,¹¹ values for N_c , N_v , and n_i are calculated from the values from Table 1, and values for N_d are based on the doping concentrations of purchased wafers. Thus, the nanostructures will be fabricated such that the cross section is no more than twice the maximum 3D depletion width, so that the entire structure can be depleted if desired without creating an inversion layer at the surface. This research will thus look to answer the question of how the transition from a 3D system to a 1D system occurs and its effect on the depletion region.

	Tabl	le 2.	Maximum	depletion	width for	3D	and 1D	v systems
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<u>3D</u>	InSb	InSb	InAs	InP	GaAs	GaP	<u>1D</u>	InSb	InSb	InAs	InP	GaAs	GaP
E _g (eV)	0.17	0.17	0.35	1.34	1.42	2.26	E _g (eV)	0.17	0.17	0.35	1.34	1.42	2.26
N _c (cm ⁻³)	4.16E+16	5.41E+15	8.76E+16	5.68E+17	3.97E+17	1.86E+19	N _c (cm⁻³)	2.75E+01	1.39E+01	3.52E+01	6.57E+01	5.83E+01	2.07E+02
N _v (cm⁻³)	7.12E+18	9.26E+17	6.70E+18	1.23E+19	9.73E+18	1.17E+19	N _v (cm⁻³)	1.53E+02	7.74E+01	1.50E+02	1.83E+02	1.69E+02	2.12E+02
n _i (cm ⁻³)	2.03E+16	1.93E+11	7.25E+14	1.47E+07	2.15E+06	1.53E+00	n _i (cm ⁻³)	2.42E+00	8.97E-05	6.87E-02	6.09E-10	1.09E-10	2.17E-17
N _d (cm⁻³)	2.00E+14	2.00E+14	2.70E+16	4.40E+15	5.50E+16	5.00E+16	N _d (cm⁻³)	2.00E+14	2.00E+14	2.70E+16	4.40E+15	5.50E+16	5.00E+16
T _{experiment} (K)	300	77	300	300	300	300	T _{experiment} (K)	300	77	300	300	300	300
X _{d,max} (nm)	-	925	108	562	179	220	X _{d,max} (nm)	3922	2282	360	964	287	312

3. EXPERIMENTAL RESEARCH

3.1 Nanostructure Fabrication

The top down fabrication approach for these CLs is accomplished using a dual beam (field emission scanning electron microscope column and focused ion beam column) system. For the first structures, an undoped InP wafer with carrier concentration $4.4 \cdot 10^{15}$ cm⁻³ and etch pit density <5000/cm² was used. The process detailed here can, however, be transferred to other wafers. The InP wafer was diced into samples of approximate size 1 cm x 1 cm.

The nanostructure fabrication process can be broken down into five steps. First, the length of the CL is defined by the initial cuts into the top of the wafer using the FIB, with the sample tilted to 52° such that the sample is perpendicular to the ion beam. The first samples for testing have a length between 100 and 150 μ m, however CLs of lengths up to 500 μ m have been fabricated using the same process. Figure 1 is an example of a 150 μ m CL cut. Four CLs are fabricated on each sample, and are numbered as CL01-CL04 and delineated by box cuts near the CL, as seen in Figure 1.

The next step is to begin the liftout process by performing undercuts. These are done at a 0° tilt so that the FIB is at an angle to the sample. Once the undercuts are complete, the sides of the CL are trimmed down to define the width of the final CL. The fourth step is to liftout the CL from the substrate. This is accomplished by attaching a nanomanipulator to

the CL, cutting the CL away from the substrate, and then lifting out the CL. Figure 2 shows the moment the CL is being lifted out of the substrate using the nanomanipulator. Once removed, the CL is then attached to the edge of the substrate for further processing, as seen in Figure 3.



Figure 1. CL length cut of 150 $\mu m.$ Here CL03 is shown.



Figure 2. Liftout of CL from the InP substrate using the nanomanipulator.



Figure 3. Attachment of the CL to the edge of the InP substrate.

The final FIB fabrication process involves the trimming of the CL to finalize the cross section. Here the goal is to achieve a CL cross section less than 1 μ m x 1 μ m. As seen in Figure 4, the ends of the structure are not trimmed to allow for a nanomanipulator landing site. Here, approximately 130 μ m of the structure is trimmed down to give the resultant CL.



Figure 4. Final trimming of the CL structure.

Once the CL is fabricated, the gate dielectric and electrode are deposited onto the CL. The substrate is placed into an ALD system to be coated with a dielectric (in this case, 50 nm of Al_2O_3). Because ALD deposition occurs in a sequential, self-limiting fashion, the conformal thin films can be deposited very accurately and reproducibly so that the gate oxide thickness can be a known and controlled variable. Next, the structure is then placed back into the FIB for gate electrode deposition. It is important to have a metal coating around the entire structure so that confinement can occur in all directions. This is accomplished by depositing Pt in the FIB onto the desired locations. The FIB allows for complete rotation of the CL to ensure a full wrap around gate electrode.

3.2 Measurement Structure Fabrication

In order to carry out measurements on these fabricated nanostructures, a measurement chip had to be designed and fabricated. The goal was to create a measurement substrate that could perform both four point probe measurements as well as Seebeck coefficient measurements. The final design is shown in Figure 5. The ends of the CL have two connections each, allowing for a four point probe measurement. Here, the gate dielectric is removed via FIB milling such that the Pt connections are directly deposited to the underlying InP nanostructure. The center connections in Figure 5 are deposited onto the gate electrode to allow for field modulation experiments. The "S-structure" at the top of Figure 5 is a nickel heater to allow for heating of the CL during Seebeck coefficient measurements. Two sets of experiments are currently being conducted on these structures: (1) resistivity modulation via field effect (four point probe measurement with various applied gate voltages); (2) Seebeck coefficient modulation via field effect (end point voltage measurements as a function of applied temperature and gate voltage).



Figure 5. CL attached to measurement substrate.

4. CONCLUSIONS

Theoretically, there are no limits to the possible value of the thermoelectric figure of merit, ZT. The research proposed here looks to investigate how nanomaterials and quantum confinement can lead to improved values of ZT compared to present day thermoelectric materials. With the increasing demand for more efficient energy use, alternative energy research such as novel thermoelectric material development will be a necessary solution to meet this demand.

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